GigaDevice Semiconductor Inc.

Device limitations of GD32E501

Errata Sheet

Revision 1.1

(Jun. 2025)

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1. Introduction

This document applies to GD32E501 product series, as shown in ***Table 1-1. Applicable products***. It provides the technical details that need to be paid attention to in the process of using GD32 MCU, as well as solutions to related problems.

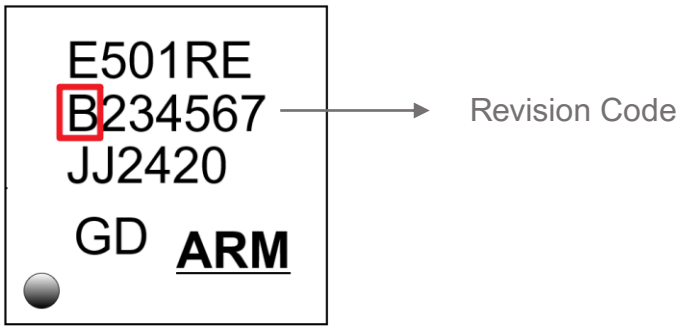
Table 1-1. Applicable products

Type	Part Numbers
MCU	GD32E501xx series

1.1. Revision identification

The device revision can be determined by the mark on the top of the package. The 1st code on the line 2 of the mark represents product revision code. As the picture shown in ***Figure 1-1. Device revision code of GD32E501***.

Figure 1-1. Device revision code of GD32E501



1.2. Summary of device limitations

The device limitations of GD32E501 are shown in ***Table 1-2. Device limitations***, please refer to section 2 for more details.

Table 1-2. Device limitations

Module	Limitations	Workaround	
		Rev. Code A	Rev. Code B
PMU	*Standby mode cannot be waked up due to frequent wakeup signals before or after entering standby mode*	N	N
RCU	*MCU cannot be waked up after entering deep-sleep mode when DSLP_HOLD bit is set*	Y	Y
	The LXTALSTB bit cannot be cleared by disabling LXTAL when LXTAL stops unexpectedly	Y	Y
DAC	*In the DAC noise mode, when the value (DH+DWBW) is configured more than 4095, the DAC output voltage will have an abnormal break point*	Y	Y
	The DAC reset hold function fails	Y	Y
TIMER	*Data lost when using timer capture / compare event to trigger DMA transfer and enabling the output compare shadow function*	Y	Y
I2C	*When I2C works in 7/10 address slave mode, receiving an abnormal timing will cause the SDA line to stuck*	Y	Y
SPI	*When the SPI CRC function is enabled, switching from receive-only mode to transmit-only mode will cause the CRCERR to be set*	N	N

Note:

Y = Limitation present, workaround available

N = Limitation present, no workaround available

'--' = Limitation fixed

2. Descriptions of device limitations

2.1. PMU

2.1.1. Standby mode cannot be waked up due to frequent wakeup signals before or after entering standby mode

Description & impact

When reset the internal signal STBY_CTL to enter to standby mode, if the Tglitch is smaller than 100ns, which will cause the mcu cannot be waked up. The narrow glitch will result in incorrect Vcore voltage.

Note: The T_{glitch} is the time between STBY_CTL low level and the wakeup signal (PA0 high level).

Workarounds

Not available.

2.2. RCU

2.2.1. MCU cannot be waked up after entering deep-sleep mode when DSLP_HOLD bit is set

Description & impact

When DSLP_HOLD bit is set and debug the mcu in deep-sleep mode, the mcu will not be waked up.

Workarounds

When the DSLP_HOLD bit is set to enable low power debugging, the application program needs to switch the system clock to IRC8M before entering the deep-sleep mode.

2.2.2. The LXTALSTB bit cannot be cleared by disabling LXTAL when LXTAL stops unexpectedly

Description & impact

When LXTAL stops unexpectedly, the LXTALSTB bit cannot be cleared by disabling the LXTAL, which prevents the LXTAL from restarting.

Workarounds

By repeatedly setting and resetting the LXTALBPS more than ten times to clear the LXTALSTB bit, and then reconfiguring the LXTAL. The reference code for clearing LXTALSTB bits is as follows:

```
void lxtal_stb_clear(void)
{
    volatile    uint32_t i = 0U;
    /* close LXTAL clock */
    rcu_osci_off(RCU_LXTAL);
    for(i = 0; i < 10; i++) {
        /* enable the LXTAL bypass mode */
        rcu_osci_bypass_mode_enable(RCU_LXTAL);
        /* disable the LXTAL bypass mode */
        rcu_osci_bypass_mode_disable(RCU_LXTAL);
    }
}
```

2.3. DAC

2.3.1. In the DAC noise mode, when the value (DH+DWBW) is configured more than 4095, the DAC output voltage will have an abnormal break point

Description & impact

When the DAC is configured in noise mode and the DAC output value is set to a large value, the superimposed value (DH+DWBW) will exceed the maximum value of 4095, resulting in an abnormal break point of zero voltage in the DAC output signal.

Workarounds

When the DAC output value and the noise wave peak value are configured, avoid the superimposed value (DH+DWBW) overflow.

2.3.2. The DAC reset hold function fails

Description & impact

When VREF is enabled (VREF_EN = 1), and only the channel of DAC2 or DAC3 is configured, and the reset hold function for the corresponding channel is enabled (DRSTMD0 = 1 or DRSTMD1 = 1), any reset signal will cause the output of the DAC channel to be unable to be held, resulting in the failure of the reset hold function.

Note: DAC0 / DAC1 reset hold function is normal.

Workarounds

In design, ensure that at least one of the DAC0 / DAC1 channels is used and its reset hold function is enabled.

2.4. TIMER

2.4.1. Data lost when using timer capture / compare event to trigger DMA transfer and enabling the output compare shadow function

Description & impact

When using timer capture / compare event to trigger DMA transfer and enabling the output compare shadow function, DMA transfers data 0x00 to TIMERx_CHyCV register which will result in the second data lost after data 0x00.

Workarounds

Use one of the following methods:

1) Do not use data 0x00 in DMA transfer buffer.
2) Transfer the second data after the 0x00 twice.
3) Use the timer update event to trigger DMA transfer.

2.5. I2C

2.5.1. When I2C works in 7/10 address slave mode, receiving an abnormal timing will cause the SDA line to stuck

Description & impact

When the I2C is operating as a slave device in 7-bit address mode and the I2C master simulates I2C communication via IO. If the master sends the following sequence, the I2C slave will enter an error state, causing it to malfunction and the SDA line to remain low:

Start + 10-bit Match Head Address + Start + 7-bit Address Read + Wait ACK + Start

When the I2C is operating as a slave device in 10-bit address mode and the I2C master simulates I2C communication via IO. If the master sends the following sequence, the I2C slave will enter an error state, causing it to malfunction and the SDA line to remain low:

Start + 10-bit Mismatch Head Address + Start
or
Start + 10-bit Match Head Address + Wait ACK + 10-bit Mismatch 8-bit Address + Start

Workarounds

Software periodically checks the status of the SDA line. If SDA is detected to be stuck low, reinitialize the I2C module.

2.6. SPI

2.6.1. When the SPI CRC function is enabled, switching from receive-only mode to transmit-only mode will cause the CRCERR to be set

Description & impact

When the SPI CRC function is enabled and the SPI firstly operates in receive-only mode, the CRC calculates continuously. Then, when the operating mode is switched to transmit-only mode, the internal Rx CRC value used for comparison is cleared to zero, while the RCRC value in the SPI_RCRC register remains. This ultimately causes the CRCERR flag to be set.

Workarounds

Ignore this CRC error or avoid this usage.

3. Revision history

Table 3-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Aug.22 2024
1.1	Update the description of I2C limitation, refer to ***When I2C works in 7/10 address slave mode, receiving an abnormal timing will cause the SDA line to stuck***	Jun.20 2024

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