GigaDevice Semiconductor Inc.

Device limitations of GD32E232

Errata Sheet

Revision 1.1

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1. Introduction

This document applies to GD32E232 product series, as shown in ***Table 1-1. Applicable products***. It provides the technical details that need to be paid attention to in the process of using GD32 MCU, as well as solutions to related problems.

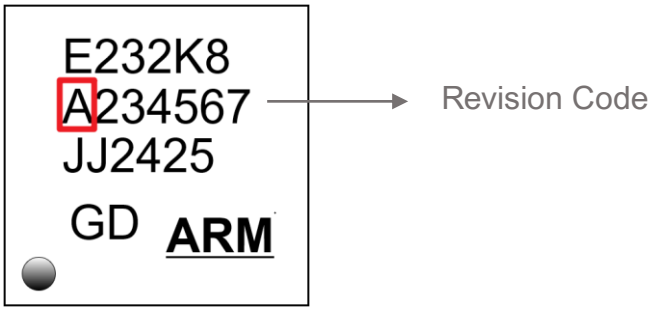
Table 1-1. Applicable products

Type	Part Numbers
MCU	GD32E232xx series

1.1. Revision identification

The device revision can be determined by the mark on the top of the package. The 1st code on the line 2 of the mark represents product revision code. As the picture shown in ***Figure 1-1. Device revision code of GD32E232***.

Figure 1-1. Device revision code of GD32E232



1.2. Summary of device limitations

The device limitations of GD32E232 are shown in ***Table 1-2. Device limitations***, please refer to section 2 for more details.

Table 1-2. Device limitations

Module	Limitations	Workaround
		Rev. Code A
System	***DMA transmission is blocked when the CPU performs flash memory erase / program operations in the flash***	Y
FMC	***When performing double-word programming, if one of the words at the programming address is 0xFFFFFFFF, then executing the double-word programming operation at that address will not cause the PGERR bit to be set***	Y
PMU	***Standby mode cannot be waked up due to frequent wakeup***	N

	signals before or after entering standby mode	
RCU	***MCU cannot be waked up after entering deep-sleep mode when DSLP_HOLD bit is set***	Y
ADC	***ADC data acquisition error occurs when the ADC clock is much slower than the PCLK clock***	Y
DAC	***In the DAC noise mode, when the DH value is configured too high, the DAC output voltage will have an abnormal break point***	Y
	When the DAC is disabled and the DAC channel pin is connected to a high voltage level, there will be a leakage current of about 20uA	Y
TIMER	***Data lost when using timer capture / compare event to trigger DMA transfer and enabling the output compare shadow function***	Y
I2C	***Read one more data because the BTC flag was not cleared***	Y
	The 90ms timeout interrupt cannot be entered in SAM_V mode	Y
	Switching I2CEN from the disabled state to the enabled state may cause the I2C to send a start signal	N
	In the communication process of I2C as a slave, if SCL and SDA are pulled down at the same time, the bus will mistakenly enter the extended state	Y
	When SCL is pulled low, the timeout period for the first transaction is 25ms, and for all subsequent transactions, the timeout period is 130ms	Y
CLA	***The CLA reset hold function fails***	N
VREF	***When VREF is disabled and VREFP is connected to VDD or VDDA, there will be a leakage current***	N

Note:

Y = Limitation present, workaround available

N = Limitation present, no workaround available

'--' = Limitation fixed

2. Descriptions of device limitations

2.1. System

2.1.1. DMA transmission is blocked when the CPU performs flash memory erase / program operations in the flash

Description & impact

When the CPU performs flash memory erase / program operations in the flash, DMA transmission is blocked due to bus being locked by flash operation.

Workarounds

During project linking, scatter load the the interrupt vector table, all interrupt service routines, and flash erase / program operation function to SRAM. This means the interrupt handlers and programs related to flash erase / program will be executed in SRAM.

2.2. FMC

2.2.1. When performing double-word programming, if one of the words at the programming address is 0xFFFFFFFF, then executing the double-word programming operation at that address will not cause the PGERR bit to be set

Description & impact

When performing double-word programming, if one of the words at the programming address is 0xFFFFFFFF, then executing the double-word programming operation at that address will not cause the PGERR bit to be set, but the programmed data will be incorrect.For example, if the value at address 0x08001000 is 0xFFFFFFFF A55AA55A, then performing a double-word programming operation at 0x08001000 next time will not cause the PGERR bit to be set.

Workarounds

Ensure that the data at the address is empty before programming. Before programming the same address, programme need to perform an erase operation on that address area.

2.3. PMU

2.3.1. Standby mode cannot be waked up due to frequent wakeup signals before or after entering standby mode

Description & impact

When reset the internal signal STBY_CTL to enter to standby mode, if the Tglitch is smaller than 100ns, which will cause the mcu cannot be waked up. The narrow glitch will result in incorrect Vcore voltage.

Note: The T_{glitch} is the time between STBY_CTL low level and the wakeup signal (PA0 high level).

Workarounds

Not available.

2.4. RCU

2.4.1. MCU cannot be waked up after entering deep-sleep mode when DSLP_HOLD bit is set

Description & impact

When DSLP_HOLD bit is set and debug the mcu in deep-sleep mode, the mcu will not be waked up.

Workarounds

When the DSLP_HOLD bit is set to enable low power debugging, the application programme need switch the system clock to IRC8M before entering the deep-sleep mode.

2.5. ADC

2.5.1. ADC data acquisition error occurs when the ADC clock is much slower than the PCLK clock

Description & impact

When the ADC clock is much slower than the PCLK clock,the ADC_RDATA register is read immediately after the EOC is set and a data acquisition error occurs.

Workarounds

When the delay between reading EOC flag and reading ADC_RDATA is no more than two ADC clocks, after the EOC flag is set, software need to delay two ADC clocks before reading the ADC_RDATA register.

2.6. DAC

2.6.1. In the DAC noise mode, when the DH value is configured too high, the DAC output voltage will have an abnormal break point

Description & impact

When the DAC is configured in noise mode and the DAC output value is set to a large value, the superimposed value (DH+DWBW) will exceed the maximum value of 4095, resulting in an abnormal break point of zero voltage in the DAC output signal.

Workarounds

When the DAC output value and the noise wave peak value are configured, avoid the superimposed value (DH+DWBW) overflow.

2.6.2. When the DAC is disabled and the DAC channel pin is connected to a high voltage level, there will be a leakage current of about 20uA

Description & impact

When the DAC is disabled and the DAC channel pin (PA4 / PA5 / PA6 / PA7) is connected to a high level, due to the internal pull-down path from the DAC pin to VSS within the chip, and the pull-down impedance is about 160K. Improper design will affect the power consumption and pin input identification.

Workarounds

When DAC channel pins (PA4 / PA5 / PA6 / PA7) do not use DAC mode, avoid internal and external pull-up mode application scenarios.

2.7. TIMER

2.7.1. Data lost when using timer capture / compare event to trigger DMA transfer and enabling the output compare shadow function

Description & impact

When using timer capture / compare event to trigger DMA transfer and enabling the output compare shadow function, DMA transfers data 0x00 to TIMERx_CHyCV register which will result in the second data lost after data 0x00.

Workarounds

Use one of the following methods:

1) Do not use data 0x00 in DMA transfer buffer.
2) Transfer the second data after the 0x00 twice.
3) Use the timer update event to trigger DMA transfer.

2.8. I2C

2.8.1. Read one more data because the BTC flag was not cleared

Description & impact

If an interrupt occurs before reading I2C_DATA register when RBNE flag is set and BTC flag is reset, I2C will read an additional data if BTC flag is set during the interrupt processing because the read data operation cannot clear the BTC flag.

Workarounds

Use one of the following solutions:

1) Using interrupt method to read the I2C_DATA register (need higher interrupt priority).
2) Using DMA method to read the I2C_DATA register (recommend).

2.8.2. The 90ms timeout interrupt cannot be entered in SAM_V mode

Description & impact

When the SAM_V interface timeout detection function is enabled, the 90ms timeout interrupt cannot be triggered.

Workarounds

Enable the SMBus host mode by setting SMBSEL and SMBEN, and disable STOEN.

2.8.3. Switching I2CEN from the disabled state to the enabled state may cause the I2C to send a start signal

Description & impact

Switching I2CEN from the disabled state to the enabled state may cause the I2C to send a start signal.

Workarounds

Not available.

2.8.4. In the communication process of I2C as a slave, if SCL and SDA are pulled down at the same time, the bus will mistakenly enter the extended state

Description & impact

In the communication process of I2C as a slave, if the time interval between SCL and SDA is less than or equal to 2 PCLK clock cycles, the chip will mistakenly enter the extended state.

Workarounds

1) If the I2C mode is used, the application code should be used to monitor whether the SCL is in the extended state, and if so, the I2C module should be re-initialized;
2) If SMBUS mode is used, the mode has 25ms timeout detection function, and the bus will be released automatically if the delay time exceeds 25ms, and the interrupt processing flag is required.

2.8.5. When SCL is pulled low, the timeout period for the first transaction is 25ms, and for all subsequent transactions, the timeout period is 130ms

Description & impact

In I2C mode, if TOEN function is enabled or in SMBUS mode, when SCL is continuously pulled down, the timeout period is 25ms for the first timeout and 130ms for subsequent timeouts.

Workarounds

Not available.

2.9. CLA

2.9.1. The CLA reset hold function fails

Description & impact

When the PIN_RSTMD bit is set, the CLA output cannot be held after any reset occurs.

Workarounds

Not available.

2.10. VREF

2.10.1. When VREF is disabled and VREFP is connected to VDD or VDDA, there will be a leakage current

Description & impact

When VREF is disabled (VREF_EN = 0) and VREFP is connected to VDD or VDDA, the internal pull-down path from the VREFP pin to VSS within the chip will cause a leakage current of approximately 120uA, affecting the system's power consumption.

Workarounds

Not available.For applications with power consumption requirements, it is not recommended to connect VREFP directly to VDD / VDDA.

3. Revision history

Table 3-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Aug.22 2024
1.1	1. Delete RCU limitation, ***The LXTALSTB bit cannot be cleared by disabling LXTAL when LXTAL stops unexpectedly*** 2. Delete I2C limitation, ***The I2C master cannot initiate a new access when arbitration is lost*** 3. Update the description and workarounds of DAC limitation, refer to ***When the DAC is disabled and the DAC channel pin is connected to a high voltage level, there will be a leakage current of about 20uA*** 4. Update the workarounds of I2C limitation, refer to ***When SCL is pulled low, the timeout period for the first transaction is 25ms, and for all subsequent transactions, the timeout period is 130ms*** 5. Add I2C limitation, refer to ***In the communication process of I2C as a slave, if SCL and SDA are pulled down at the same time, the bus will mistakenly enter the extended state***	Jun.11 2025

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