GigaDevice Semiconductor Inc.

GD32H77Dxx
Arm® Cortex®-M7 32-bit MCU

Datasheet

Revision 0.9RC1

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1. General description

The GD32H77Dxx device belongs to the high performance line of GD32 MCU family. It is a new 32-bit general-purpose microcontroller based on the Arm® Cortex®-M7 core with best cost-performance ratio in terms of enhanced processing capacity, reduced power consumption and peripheral set. The Arm® Cortex®-M7 processor is a highly efficient high-performance, embedded processor that features low interrupt latency, low-cost debug, and has backwards compatibility with existing Cortex-M profile processors. The processor has an in-order super-scalar pipeline that means many instructions can be dual-issued, including load/load and load/store instruction pairs because of multiple memory interfaces. The Cortex-M7 is a high-performance processor, which features a 6-stage superscalar pipeline with branch prediction and an optional FPU capable of single-precision and optionally double-precision operations. The instruction and data buses have been enlarged to 64-bit wide over the previous 32-bit buses. It also provides a Memory Protection Unit (MPU) and powerful trace technology for enhanced application security and advanced debug support.

The GD32H77Dxx device incorporates the Arm® Cortex®-M7 32-bit processor core operating at 600 MHz frequency with NVM security protection to prevent illegal code/data access. It provides up to 2048KB code non-volatile memory (CNVM) and up to 7680KB extended code non-volatile memory (ECNVM), 1152KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to four APB buses. The devices offer up to two 14-bit ADCs, a 12-bit ADC, a 12-bit DAC, up to twelve general 16-bit timers, two 16-bit PWM advanced timers, four 32-bit general timers, two 64-bit basic timers and two 32-bit basic timers, as well as standard and advanced communication interfaces: up to six SPIs, two OSPIs, four I2Cs, four USARTs and four UARTs, four I2Ss, three CAN-FDs, two USBHSs, two ENETs, two SDIOs and two CMPs. Additional peripherals as cyclic redundancy checks management unit (CRC), true random number generator (TRNG), cryptographic acceleration unit (CAU), hash acceleration unit (HAU), public key cryptographic acceleration unit (PKCAU), real-time decryption (RTDEC), digital camera interface (DCI), DSI host controller (DSI), general parallel slave interface(GPSI), EXMC interface with SDRAM extension support, TFT-LCD Interface (TLI), image processing accelerator (IPA), serial audio Interface (SAI), receiver of Sony/Philips digital interface (RSPDIF), trigonometric math unit (TMU), fast fourier transform (FFT), filter arithmetic accelerator (FAC), management data input / output (MDIO), encoder Divided-Output controller (EDOUT), encoder interface module (EDIM), resolver-to-digital module (RDCM), low power digital temperature sensor (LPDTS), Hardware semaphore (HWSEM), and high performance digital filter module (HPDF) are included.

The device operates from a 1.71V to 3.6V power supply and available in -40 to +105 °C temperature range for grade 7 devices. Three power saving modes provide the flexibility for maximum optimization of power consumption, an especially important consideration in low power applications.

The above features make GD32H77Dxx devices suitable for a wide range of interconnection and advanced applications, especially in areas such as industrial control, consumer and handheld equipment, embedded modules, human machine interface, security and alarm

systems, energy storage system, graphic display, audio player, automotive navigation, drone, IoT and so on.



2. Device overview

2.1. Device information

Table 2-1. GD32H77Dxx devices features and peripheral list

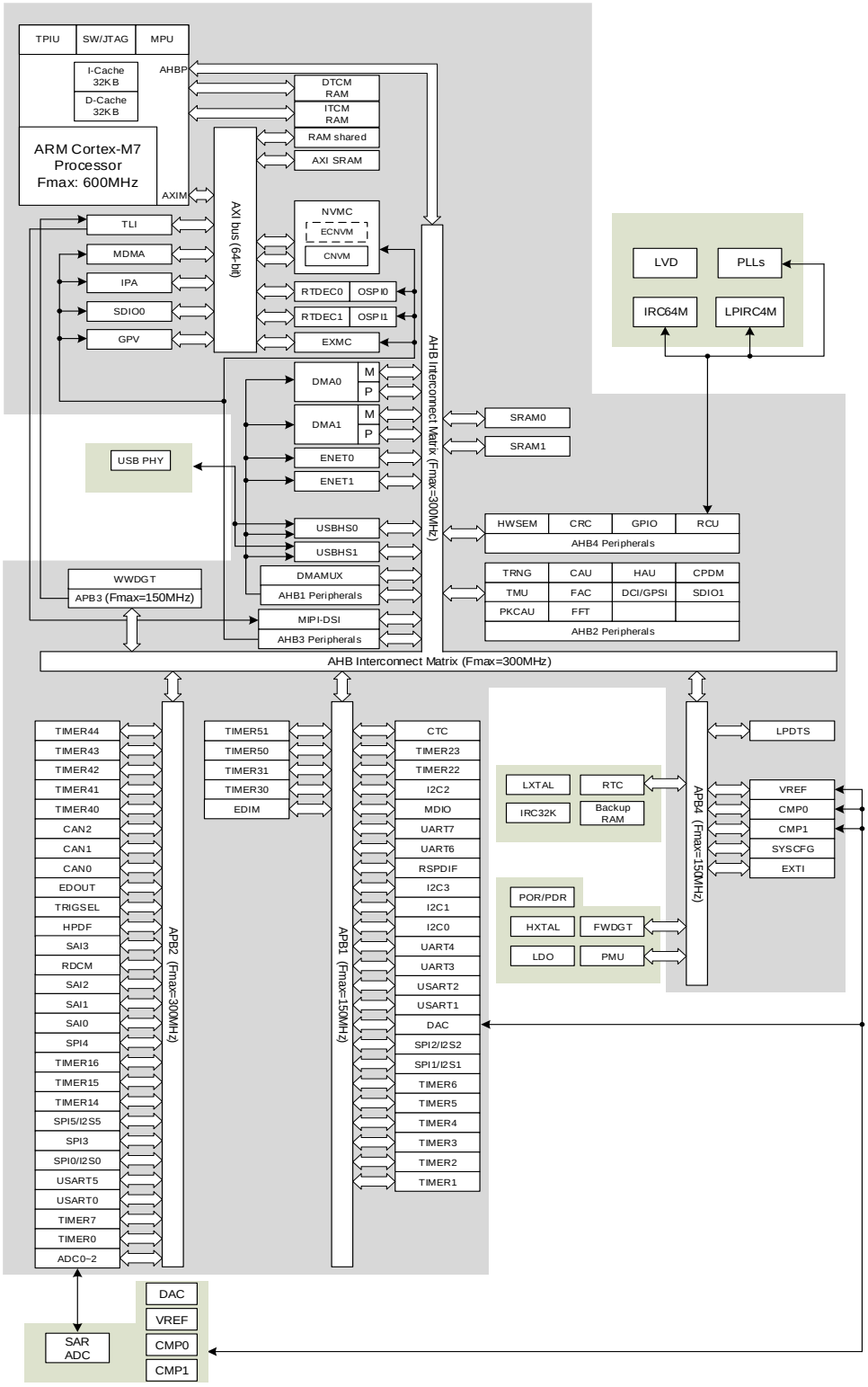
Part Number		GD32H77D		
		IWK7	IPK7	IIK7
NVM	CNVM (KB)	2048	2048	1664
	ECNVM (KB)	7680	3584	0
	Total(KB)	9728	5632	1664
SRAM	SRAM (KB)	512	512	512
	TCM SRAM(KB)	640	640	640
	Total(KB)	1152	1152	1152
Timers	General timer (16-bit)	12 (2-3,14-16,30-31,40-44)	12 (2-3,14-16,30-31,40-44)	12 (2-3,14-16,30-31,40-44)
	General timer (32-bit)	4 (1,4,22-23)	4 (1,4,22-23)	4 (1,4,22-23)
	Advanced timer(16-bit)	2 (0,7)	2 (0,7)	2 (0,7)
	Basic timer (32-bit)	2 (5,6)	2 (5,6)	2 (5,6)
	Basic timer (64-bit)	2 (50,51)	2 (50,51)	2 (50,51)
	SysTick	1	1	1
	Watchdog	2	2	2
	RTC	1	1	1
Connectivity	USART	4 (0-2,5)	4 (0-2,5)	4 (0-2,5)
	UART	4 (3,4,6,7)	4 (3,4,6,7)	4 (3,4,6,7)
	I2C	4 (0-3)	4 (0-3)	4 (0-3)
	SPI/I2S	6/4 (0-5)/(0-2,5)	6/4 (0-5)/(0-2,5)	6/4 (0-5)/(0-2,5)
	OSPI	2	2	2
	SDIO	2	2	2

Part Number		GD32H77D		
		IWK7	IPK7	IIK7
	MDIO	1	1	1
	CAN	3xFD	3xFD	3xFD
	USBHS	2	2	2
	ENET	2	2	2
CRC		1	1	1
TRNG		1	1	1
CAU		1	1	1
HAU		1	1	1
PKCAU		1	1	1
RTDEC		2	2	2
TLI		1	1	1
DCI		1	1	1
MIPI-DSI		1	1	1
RSPDIF		1	1	1
SAI		4	4	4
HPDF		1	1	1
LPDTS		1	1	1
EXMC/SDRAM		1/1	1/1	1/1
GPSI		1	1	1
IPA		1	1	1
EDOUT		1	1	1
CPDM		4	4	4
HWSEM		1	1	1
TMU		1	1	1
FFT		1	1	1
FAC		1	1	1
EDIM		1	1	1
RDCM		1	1	1

Part Number		GD32H77D		
		IWK7	IPK7	IIK7
14bit ADC	Units	2	2	2
	Channels	22	22	22
12bit ADC	Units	1	1	1
	Channels	17	17	17
DAC	Units	1	1	1
	Channels	2	2	2
CMP		2	2	2
GPIO		116	116	116
Package		BGA176	BGA176	BGA176

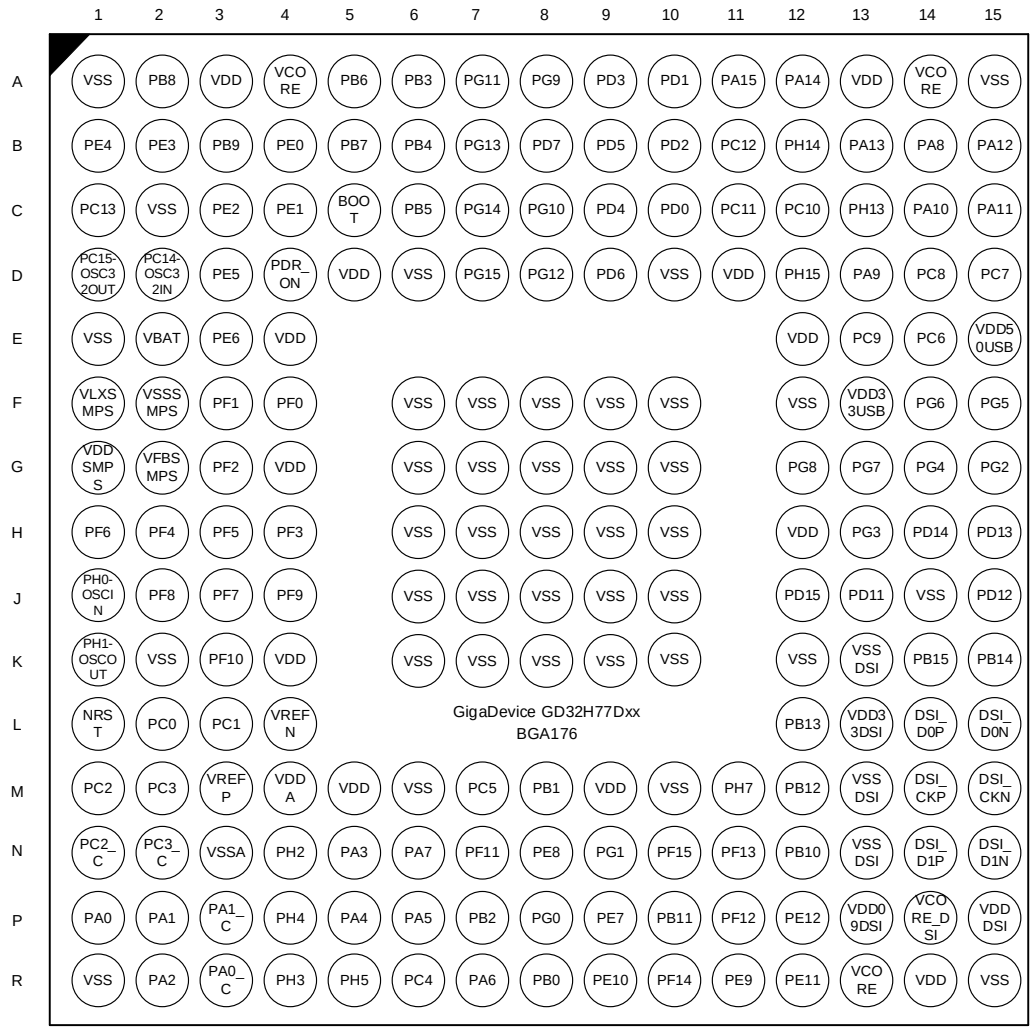
2.2. Block diagram

Figure 2-1. GD32H77Dxx block diagram



2.3. Pinouts and pin assignment

Figure 2-2. GD32H77Dxx BGA176 pinouts(1)



Note:

(1) The above figure shows the package top view.

(2) The pin count of the BGA176 package is 176+25 (with an additional 25 VSS pins).

2.4. Memory map

Table 2-2. Memory map of GD32H77Dxx devices

Pre-defined Regions	Bus	Address	Peripherals
External RAM		0xD000 0000 - 0xDFFF FFFF	EXMC - SDRAM device 1
		0xC000 0000 - 0xCFFF FFFF	EXMC - SDRAM device 0 (EXMC Bank 0 Region 0-3)
		0xA000 1000 - 0xBFFF FFFF	Reserved

Pre-defined Regions	Bus	Address	Peripherals
		0xA000 0000 - 0xA000 0FFF	Reserved
		0x9000 0000 - 0x9FFF FFFF	OSPI0
		0x8000 0000 - 0x8FFF FFFF	EXMC - NAND
		0x7000 0000 - 0x7FFF FFFF	OSPI1
		0x6000 0000 - 0x6FFF FFFF	EXMC - NOR/PSRAM/SRAM
		0x5F00 4000 - 0x5FFF FFFF	Reserved
		0x5F00 0000 - 0x5F00 3FFF	Reserved
Peripheral	AHB4	0x5802 6800 - 0x5EFF FFFF	Reserved
		0x5802 6400 - 0x5802 67FF	HWSEM
		0x5802 6000 - 0x5802 63FF	Reserved
		0x5802 5000 - 0x5802 5FFF	Reserved
		0x5802 4C00 - 0x5802 4FFF	CRC
		0x5802 4800 - 0x5802 4BFF	Reserved
		0x5802 4400 - 0x5802 47FF	RCU
		0x5802 2C00 - 0x5802 43FF	Reserved
		0x5802 2800 - 0x5802 2BFF	GPIOK
		0x5802 2400 - 0x5802 27FF	GPIOJ
		0x5802 2000 - 0x5802 23FF	Reserved
		0x5802 1C00 - 0x5802 1FFF	GPIOH
		0x5802 1800 - 0x5802 1BFF	GPIOG
		0x5802 1400 - 0x5802 17FF	GPIOF
		0x5802 1000 - 0x5802 13FF	GPIOE
		0x5802 0C00 - 0x5802 0FFF	GPIOD
		0x5802 0800 - 0x5802 0BFF	GPIOC
		0x5802 0400 - 0x5802 07FF	GPIOB
		0x5802 0000 - 0x5802 03FF	GPIOA
		0x5801 0000 - 0x5801 FFFF	Reserved
	APB4	0x5800 7400 - 0x5800 FFFF	Reserved
		0x5800 7000 - 0x5800 73FF	Reserved
		0x5800 6C00 - 0x5800 6FFF	Reserved
		0x5800 6800 - 0x5800 6BFF	LPDTS
		0x5800 5C00 - 0x5800 67FF	Reserved
		0x5800 5800 - 0x5800 5BFF	PMU
		0x5800 5400 - 0x5800 57FF	Reserved
		0x5800 4C00 - 0x5800 53FF	Reserved
		0x5800 4800 - 0x5800 4BFF	FWDGT
		0x5800 4100 - 0x5800 43FF	Reserved
		0x5800 4000 - 0x5800 40FF	RTC
		0x5800 3C00 - 0x5800 3FFF	VREF
		0x5800 3800 - 0x5800 3BFF	CMP0 - CMP1
		0x5800 3400 - 0x5800 37FF	Reserved

Pre-defined Regions	Bus	Address	Peripherals
		0x5800 3000 - 0x5800 33FF	Reserved
		0x5800 2C00 - 0x5800 2FFF	Reserved
		0x5800 2800 - 0x5800 2BFF	Reserved
		0x5800 2400 - 0x5800 27FF	Reserved
		0x5800 2000 - 0x5800 23FF	Reserved
		0x5800 1C00 - 0x5800 1FFF	Reserved
		0x5800 1400 - 0x5800 17FF	Reserved
		0x5800 0800 - 0x5800 13FF	Reserved
		0x5800 0400 - 0x5800 07FF	SYSCFG
		0x5800 0000 - 0x5800 03FF	EXTI
	AHB3	0x5200 C000 - 0x57FF FFFF	Reserved
		0x5200 BC00 - 0x5200 BFFF	RTDEC1
		0x5200 B800 - 0x5200 BBFF	RTDEC0
		0x5200 B400 - 0x5200 B7FF	OSPIM
		0x5200 B000 - 0x5200 B3FF	CPDM(OSPI1)
		0x5200 A000 - 0x5200 AFFF	OSPI1
		0x5200 9400 - 0x5200 9FFF	Reserved
		0x5200 9100 - 0x5200 93FF	Reserved
		0x5200 9000 - 0x5200 90FF	RAMECCMU Region 0
		0x5200 8400 - 0x5200 8FFF	Reserved
		0x5200 8000 - 0x5200 83FF	CPDM(SDIO0)
		0x5200 7400 - 0x5200 7FFF	Reserved
		0x5200 7000 - 0x5200 73FF	SDIO0
		0x5200 6400 - 0x5200 6FFF	Reserved
		0x5200 6000 - 0x5200 63FF	CPDM(OSPI0)
		0x5200 5000 - 0x5200 5FFF	OSPI0
		0x5200 4000 - 0x5200 4FFF	EXMC
		0x5200 3000 - 0x5200 3FFF	MIPI-DSI
		0x5200 2400 - 0x5200 2FFF	Reserved
		0x5200 2000 - 0x5200 23FF	NVMC
		0x5200 1000 - 0x5200 1FFF	IPA
		0x5200 0800 - 0x5200 0FFF	Reserved
		0x5200 0000 - 0x5200 07FF	MDMA
		0x5110 0000 - 0x51FF FFFF	Reserved
		0x5100 0000 - 0x510F FFFF	AXI interconnect matrix
		0x5001 1000 - 0x50FF FFFF	Reserved
		0x5001 0000 - 0x5001 0FFF	Reserved
	APB3	0x5000 4000 - 0x5000 FFFF	Reserved
		0x5000 3400 - 0x5000 3FFF	Reserved
		0x5000 3000 - 0x5000 33FF	WWDGT
		0x5000 2000 - 0x5000 2FFF	Reserved

Pre-defined Regions	Bus	Address	Peripherals
		0x5000 1400 - 0x5000 1FFF	Reserved
		0x5000 1000 - 0x5000 13FF	TLI
		0x5000 0000 - 0x5000 0FFF	Reserved
	AHB2	0x4802 5800 - 0x4FFF FFFF	Reserved(AHB2)
		0x4802 5000 - 0x4802 57FF	Reserved
		0x4802 4800 - 0x4802 4FFF	FAC
		0x4802 4400 - 0x4802 47FF	TMU
		0x4802 4000 - 0x4802 43FF	FFT
		0x4802 3100 - 0x4802 3FFF	Reserved
		0x4802 3000 - 0x4802 30FF	RAMECCMU Region 1
		0x4802 2C00 - 0x4802 2FFF	Reserved(AHB2)
		0x4802 2800 - 0x4802 2BFF	CPDM(SDIO1)
		0x4802 2400 - 0x4802 27FF	SDIO1
		0x4802 1C00 - 0x4802 23FF	Reserved(AHB2)
		0x4802 1800 - 0x4802 1BFF	TRNG
		0x4802 1400 - 0x4802 17FF	HAU
		0x4802 1000 - 0x4802 13FF	CAU
		0x4802 0400 - 0x4802 0FFF	Reserved(AHB2)
		0x4802 0000 - 0x4802 03FF	DCI/GPSI
		0x4800 2000 - 0x4801 FFFF	Reserved(AHB2)
		0x4800 0000 - 0x4800 1FFF	PKCAU
	AHB1	0x400C 0000 - 0x47FF FFFF	Reserved(AHB1)
		0x4008 0000 - 0x400B FFFF	USBHS1
		0x4004 0000 - 0x4007 FFFF	USBHS0
		0x4003 8C00 - 0x4003 FFFF	Reserved
		0x4003 8400 - 0x4003 8BFF	Reserved
		0x4003 8000 - 0x4003 83FF	Reserved
		0x4003 3000 - 0x4003 7FFF	Reserved
		0x4003 0000 - 0x4003 2FFF	Reserved
		0x4002 C000 - 0x4002 FFFF	Reserved
		0x4002 BC00 - 0x4002 BFFF	ENET1
		0x4002 B000 - 0x4002 BBFF	
		0x4002 A000 - 0x4002 AFFF	
		0x4002 8000 - 0x4002 9FFF	ENET0
		0x4002 6800 - 0x4002 7FFF	Reserved
		0x4002 6400 - 0x4002 67FF	Reserved
		0x4002 6000 - 0x4002 63FF	Reserved
		0x4002 5000 - 0x4002 5FFF	Reserved
		0x4002 4000 - 0x4002 4FFF	Reserved
		0x4002 3C00 - 0x4002 3FFF	Reserved
		0x4002 3800 - 0x4002 3BFF	Reserved

Pre-defined Regions	Bus	Address	Peripherals
		0x4002 3400 - 0x4002 37FF	Reserved
		0x4002 3000 - 0x4002 33FF	Reserved
		0x4002 2C00 - 0x4002 2FFF	Reserved
		0x4002 2800 - 0x4002 2BFF	Reserved
		0x4002 2400 - 0x4002 27FF	Reserved
		0x4002 2000 - 0x4002 23FF	Reserved
		0x4002 1C00 - 0x4002 1FFF	Reserved
		0x4002 1800 - 0x4002 1BFF	Reserved
		0x4002 1400 - 0x4002 17FF	Reserved
		0x4002 1000 - 0x4002 13FF	Reserved
		0x4002 0C00 - 0x4002 0FFF	Reserved
		0x4002 0800 - 0x4002 0BFF	DMAMUX
		0x4002 0400 - 0x4002 07FF	DMA1
		0x4002 0000 - 0x4002 03FF	DMA0
	APB2	0x4001 F400 - 0x4001 FFFF	Reserved
		0x4001 F000 - 0x4001 F3FF	TIMER44
		0x4001 E000–0x4001 EFFF	Reserved
		0x4001 DC00 - 0x4001 DFFF	TIMER43
		0x4001 D800 - 0x4001 DBFF	TIMER42
		0x4001 D400 - 0x4001 D7FF	TIMER41
		0x4001 D000 - 0x4001 D3FF	TIMER40
		0x4001 C000 - 0x4001 CFFF	CAN2(4KB)
		0x4001 B000 - 0x4001 BFFF	CAN1(4KB)
		0x4001 A000 - 0x4001 AFFF	CAN0(4KB)
		0x4001 8C00 - 0x4001 9FFF	Reserved
		0x4001 8900 - 0x4001 8BFF	Reserved
		0x4001 8800 - 0x4001 88FF	EDOUT
		0x4001 8400 - 0x4001 87FF	TRIGSEL
		0x4001 8000 - 0x4001 83FF	Reserved(APB2)
		0x4001 7C00 - 0x4001 7FFF	Reserved
		0x4001 7800 - 0x4001 7BFF	Reserved
		0x4001 7400 - 0x4001 77FF	Reserved
		0x4001 7000 - 0x4001 73FF	HPDF
		0x4001 6C00 - 0x4001 6FFF	Reserved
		0x4001 6800 - 0x4001 6BFF	SAI3
		0x4001 6400 - 0x4001 67FF	RDCM
		0x4001 6000 - 0x4001 63FF	SAI2
		0x4001 5C00 - 0x4001 5FFF	SAI1
		0x4001 5800 - 0x4001 5BFF	SAI0
		0x4001 5400 - 0x4001 57FF	Reserved
		0x4001 5000 - 0x4001 53FF	SPI4

Pre-defined Regions	Bus	Address	Peripherals
		0x4001 4C00 - 0x4001 4FFF	Reserved
		0x4001 4800 - 0x4001 4BFF	TIMER16
		0x4001 4400 - 0x4001 47FF	TIMER15
		0x4001 4000 - 0x4001 43FF	TIMER14
		0x4001 3C00 - 0x4001 3FFF	Reserved
		0x4001 3800 - 0x4001 3BFF	SPI5/I2S5
		0x4001 3400 - 0x4001 37FF	SPI3
		0x4001 3000 - 0x4001 33FF	SPI0/I2S0
		0x4001 2C00 - 0x4001 2FFF	ADC2
		0x4001 2800 - 0x4001 2BFF	ADC1
		0x4001 2400 - 0x4001 27FF	ADC0
		0x4001 2000 - 0x4001 23FF	Reserved
		0x4001 1C00 - 0x4001 1FFF	Reserved
		0x4001 1800 - 0x4001 1BFF	Reserved
		0x4001 1400 - 0x4001 17FF	USART5
		0x4001 1000 - 0x4001 13FF	USART0
		0x4001 0C00 - 0x4001 0FFF	Reserved
		0x4001 0800 - 0x4001 0BFF	Reserved
		0x4001 0400 - 0x4001 07FF	TIMER7
		0x4001 0000 - 0x4001 03FF	TIMER0
	APB1	0x4000 F800 - 0x4000 FFFF	Reserved
		0x4000 F400 - 0x4000 F7FF	TIMER51
		0x4000 F000 - 0x4000 F3FF	TIMER50
		0x4000 EC00 - 0x4000 EFFF	TIMER31
		0x4000 E800 - 0x4000 EBFF	TIMER30
		0x4000 E400 - 0x4000 E7FF	TIMER23
		0x4000 E000 - 0x4000 E3FF	TIMER22
		0x4000 DC00 - 0x4000 DFFF	Reserved
		0x4000 C400 - 0x4000 DBFF	EDIM
		0x4000 C000 - 0x4000 C3FF	I2C2
		0x4000 9800 - 0x4000 BFFF	Reserved
		0x4000 9400 - 0x4000 97FF	MDIO
		0x4000 8800 - 0x4000 93FF	Reserved
		0x4000 8400 - 0x4000 87FF	CTC
		0x4000 8000 - 0x4000 83FF	Reserved
		0x4000 7C00 - 0x4000 7FFF	UART7
		0x4000 7800 - 0x4000 7BFF	UART6
		0x4000 7400 - 0x4000 77FF	DAC0
		0x4000 7000 - 0x4000 73FF	Reserved
		0x4000 6C00 - 0x4000 6FFF	Reserved
		0x4000 6800 - 0x4000 6BFF	Reserved

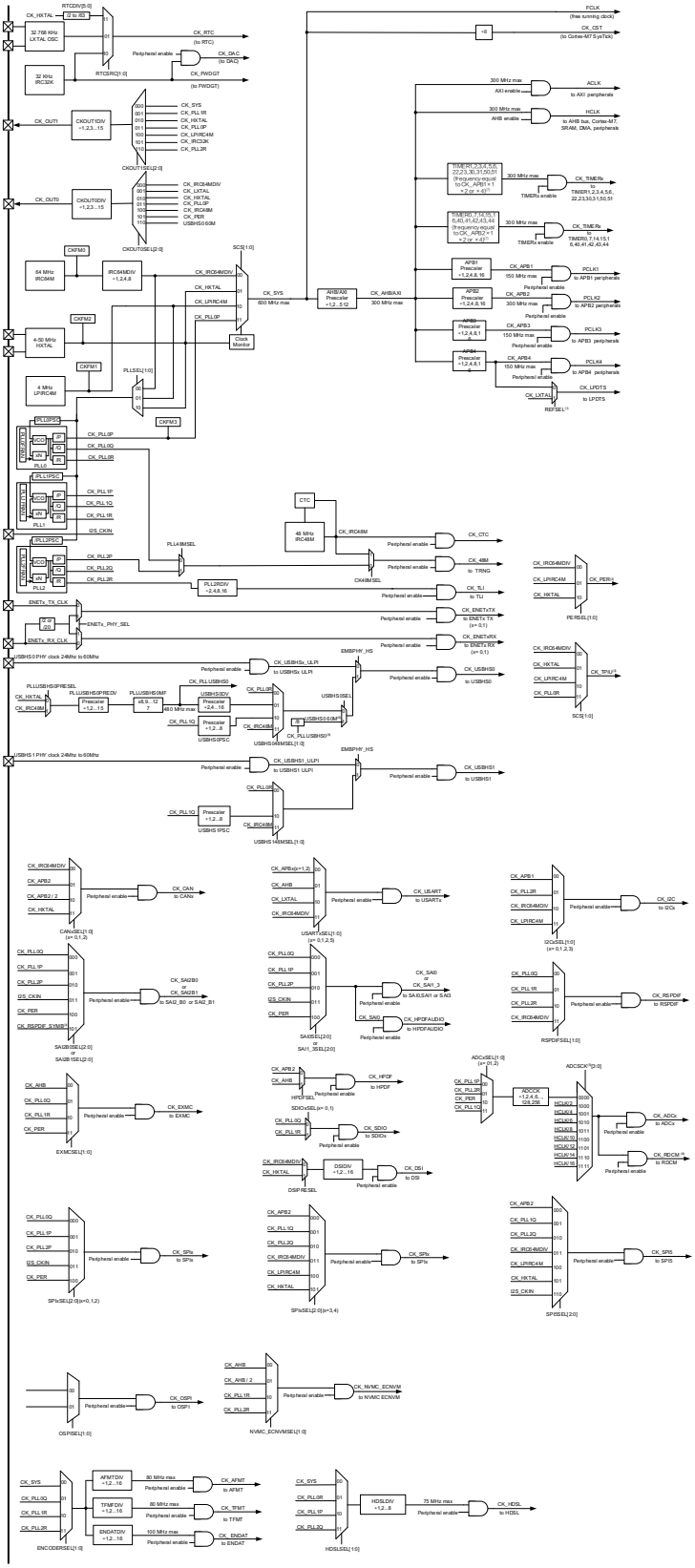
Pre-defined Regions	Bus	Address	Peripherals
		0x4000 6400 - 0x4000 67FF	Reserved
		0x4000 6000 - 0x4000 63FF	Reserved
		0x4000 5C00 - 0x4000 5FFF	I2C3
		0x4000 5800 - 0x4000 5BFF	I2C1
		0x4000 5400 - 0x4000 57FF	I2C0
		0x4000 5000 - 0x4000 53FF	UART4
		0x4000 4C00 - 0x4000 4FFF	UART3
		0x4000 4800 - 0x4000 4BFF	USART2
		0x4000 4400 - 0x4000 47FF	USART1
		0x4000 4000 - 0x4000 43FF	RSPDIF
		0x4000 3C00 - 0x4000 3FFF	SPI2/I2S2
		0x4000 3800 - 0x4000 3BFF	SPI1/I2S1
		0x4000 3400 - 0x4000 37FF	Reserved
		0x4000 3000 - 0x4000 33FF	Reserved
		0x4000 2C00 - 0x4000 2FFF	Reserved
		0x4000 2800 - 0x4000 2BFF	Reserved
		0x4000 2400 - 0x4000 27FF	Reserved
		0x4000 2000 - 0x4000 23FF	Reserved
		0x4000 1C00 - 0x4000 1FFF	Reserved
		0x4000 1800 - 0x4000 1BFF	Reserved
		0x4000 1400 - 0x4000 17FF	TIMER6
		0x4000 1000 - 0x4000 13FF	TIMER5
		0x4000 0C00 - 0x4000 0FFF	TIMER4
		0x4000 0800 - 0x4000 0BFF	TIMER3
		0x4000 0400 - 0x4000 07FF	TIMER2
		0x4000 0000 - 0x4000 03FF	TIMER1
SRAM		0x3880 1000 - 0x3FFF FFFF	Reserved
		0x3880 0000 - 0x3880 0FFF	Backup SRAM
		0x3000 E000 - 0x387F FFFF	Reserved
		0x3000 C000 - 0x3000 DFFF	SRAM shared with FFT(8KB)
		0x3000 A000 - 0x3000 BFFF	SRAM shared with USBHS RAM(8KB)
		0x3000 9000 - 0x3000 9FFF	SRAM shared with ENET1 RAM(4KB)
		0x3000 8000 - 0x3000 8FFF	SRAM shared with ENET0 RAM(4KB)
		0x3000 4000 - 0x3000 7FFF	SRAM1(16KB)
		0x3000 0000 - 0x3000 3FFF	SRAM0(16KB)
		0x2410 0000 - 0x2FFF FFFF	Reserved
		0x240C 0000 - 0x240F FFFF	Reserved

Pre-defined Regions	Bus	Address	Peripherals
		0x2408 0000 - 0x240B FFFF	RAM(256KB) shared (ITCM/AXI)
		0x2400 0000 - 0x2407 FFFF	AXI SRAM(512KB)
		0x2008 0000 - 0x23FF FFFF	Reserved
		0x2007 0000 - 0x2007 FFFF	Reserved
		0x2006 0000 - 0x2006 FFFF	Reserved
		0x2005 0000 - 0x2005 FFFF	Reserved
		0x2004 0000 - 0x2004 FFFF	Reserved
		0x2001 C000 - 0x2003 FFFF	DTCM RAM(from ITCM/DTCM)
		0x2001 8000 - 0x2001 BFFF	
		0x2001 0000 - 0x2001 7FFF	
		0x2000 D000 - 0x2000 FFFF	
		0x2000 C000 - 0x2000 CFFF	
		0x2000 8000 - 0x2000 BFFF	
		0x2000 5000 - 0x2000 7FFF	
		0x2000 2000 - 0x2000 4FFF	
		0x2000 1000 - 0x2000 1FFF	
		0x2000 0000 - 0x2000 0FFF	
Code		0x1FFF FC10 - 0x1FFF FFFF	Reserved
		0x1FFF FC00 - 0x1FFF FC0F	Reserved
		0x1FFF F818 - 0x1FFF FBFF	Reserved
		0x1FFF F800 - 0x1FFF F817	Reserved
		0x1FFF F000 - 0x1FFF F7FF	Reserved
		0x1FFF EC00 - 0x1FFF EFFF	Reserved
		0x1FFF C010 - 0x1FFF EBFF	Reserved
		0x1FFF C000 - 0x1FFF C00F	Reserved
		0x1FFF B000 - 0x1FFF BFFF	Reserved
		0x1FFF 8000 - 0x1FFF AFFF	Reserved
		0x1FFF 7A10 - 0x1FFF 7FFF	Reserved
		0x1FFF 7800 - 0x1FFF 7A0F	Reserved
		0x1FFF 7400 - 0x1FFF 77FF	Reserved
		0x1FFF 7000 - 0x1FFF 73FF	Reserved
		0x1FFF 1A00 -0x1FFF 6FFF	Reserved
		0x1FFF 0000 - 0x1FFF 19FF	OTP
		0x1FEF 0000 - 0x1FFE FFFF	System Memory
		0x1002 0000 - 0x1FEE FFFF	Reserved
		0x1001 0000 - 0x1001 FFFF	Reserved
		0x1000 0000 - 0x1000 FFFF	Reserved
		0x0A00 D000 - 0x0FFF FFFF	Reserved
		0x0A00 C000 - 0x0A00 CFFF	Reserved
		0x0A00 8000 - 0x0A00 BFFF	Reserved

Pre-defined Regions	Bus	Address	Peripherals	
		0x0A00 0000 - 0x0A00 7FFF	Reserved	
		0x08C0 1000 - 0x09FF FFFF	Reserved	
		0x08C0 0000 - 0x08C0 0FFF	Reserved	
		0x0898 0000 - 0x08BF FFFF	Reserved	
		0x0880 0000 - 0x0897 FFFF	ECNVM	
		0x0840 0000 - 0x087F FFFF		
		0x083C 0000 - 0x083F FFFF		
		0x0830 0000 - 0x083B FFFF		
		0x0820 0000 - 0x082F FFFF		
		0x0810 0000 - 0x081F FFFF	CNVM	
		0x0808 0000 - 0x080F FFFF		
		0x0806 0000 - 0x0807 FFFF		
		0x0802 0000 - 0x0805 FFFF		
		0x0801 0000 - 0x0801 FFFF		
		0x0800 0000 - 0x0800 FFFF		
		0x0030 0000 - 0x07FF FFFF	Reserved	
		0x0010 0000 - 0x002F FFFF	Reserved	
		0x000A 0000 - 0x000F FFFF	Reserved	
		0x0006 0000 - 0x0009 FFFF	ITCM RAM	RAM shared
		0x0002 0000 - 0x0005 FFFF		
		0x0001 0000 - 0x0001 FFFF		Dedicated
		0x0000 0000 - 0x0000 FFFF		

2.5. Clock tree

Figure 2-3. GD32H77Dxx clock tree



Legend:

HXTAL: High speed crystal oscillator
LXTAL: Low speed crystal oscillator
LPIRC4M: Low Power Internal 4M RC oscillator
IRC32K: Internal 32K RC oscillator
IRC48M: Internal 48M RC oscillators
IRC64M: Internal 64M RC oscillators

2.6. Pin definitions

2.6.1. GD32H77Dxx BGA176 pin definitions

Table 2-3. GD32H77Dxx BGA176 pin definitions(4)

BGA176(4)				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PE4	B1	I/O		Default: PE4 Alternate: TRACED1, TIMER0_BRKIN1, SAI0_DAT1, HPDF_DATAIN3, TIMER14_MCH0, SPI3_NSS, SAI0_FS0, HDSL_CLK2, SAI2_FS0, SAI2_DAT1, EXMC_A4, EXMC_A20, DCI_D4, TLI_B0, EVENTOUT, SAI3_FS0, SAI3_DAT1, HDSL_LINK
PE5	D3	I/O		Default: PE5 Alternate: TRACED2, TIMER40_BRKIN0, SAI0_CLK1, HPDF_CKIN3, TIMER14_CH0, SPI3_MISO, SAI0_SCK0, HDSL_MISO1, SAI2_SCK0, SAI2_CLK1, EXMC_A5, EXMC_A21, DCI_D6, TLI_G0, EVENTOUT, SAI3_SCK0, SAI3_CLK1, HDSL_SMPL
PE6	E3	I/O		Default: PE6 Alternate: TRACED3, TIMER0_BRKIN2, SAI0_DAT0, TIMER14_CH1, SPI3_MOSI, SAI0_SD0, HDSL_MOSI1, SAI2_SD0, SAI2_DAT0, SAI1_MCLK1, CMP_MUX_OUT3, EXMC_A22, DCI_D7, TLI_G1, EVENTOUT, SAI3_SD0, SAI3_DAT0
VSS	A1	P	-	Default: VSS
VDD	E4	P	-	Default: VDD
VBAT	E2	P	-	Default: VBAT
PC13	C1	I/O		Default: PC13 Alternate: EVENTOUT Additional:RTC_TAMP0, RTC_TS, WKUP3, RTC_OUT, COREPOROFFOUT
PC14-OSC32IN	D2	I/O		Default: PC14 Alternate: EVENTOUT Additional:OSC32IN
PC15-OSC32OUT	D1	I/O		Default: PC15 Alternate: EVENTOUT Additional:OSC32OUT

BGA176[4]				
Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
VSS	C2	P	-	Default: VSS
VSSSMPS	F2	P	-	Default: VSSSMPS
VLXSMPS	F1	P	-	Default: VLXSMPS
VDDSMPS	G1	P	-	Default: VDDSMPS
VFBSMPS	G2	P	-	Default: VFBSMPS
PF0	F4	I/O		Default: PF0 Alternate: SPI3_MISO, I2C1_SDA, USBHS0_ULPI_D4, TIMER41_CH0, HDSL_SEL2, OSPIM_P1_IO0, SAI1_SD0, EXMC_A0, TIMER22_CH0, EVENTOUT
PF1	F3	I/O		Default: PF1 Alternate: SPI3_MOSI, I2C1_SCL, USBHS0_ULPI_D5, TIMER41_MCH0, HDSL_MISO2, OSPIM_P1_IO1, SAI2_SCK0, EXMC_A1, TIMER22_CH1, EVENTOUT
PF2	G3	I/O		Default: PF2 Alternate: ENET0_MDIO, I2C1_SMBA, USBHS0_ULPI_D6, HDSL_MOSI2, OSPIM_P1_IO2, SPI0_NSS, I2S0_WS, EXMC_D23, EXMC_A2, TIMER22_CH2, EVENTOUT, ENET1_MDIO
PF3	H4	I/O		Default: PF3 Alternate: ENET0_MDC, USART0_RX, OSPIM_P1_IO3, EXMC_D22, EXMC_A3, TIMER22_CH3, EVENTOUT, ENET1_MDC Additional:ADC2_IN5
PF4	H2	I/O		Default: PF4 Alternate: TIMER0_MCH1, TIMER7_MCH1, USART0_TX, OSPIM_P1_nSCK, HPDF_DATAIN2, USART2_RTS, USART2_DE, UART3_RTS, UART3_DE, OSPIM_P1_SCK, SDIO1_D0, EXMC_D21, EXMC_A4, TRIGSEL_OUT1, TLI_PIXCLK, EVENTOUT Additional:ADC2_IN9
PF5	H3	I/O		Default: PF5 Alternate: TIMER0_MCH2, TIMER7_MCH2, USART0_RX, HPDF_CKIN2, UART3_CTS, OSPIM_P1_nSCK, SDIO1_D1, EXMC_A5, TRIGSEL_OUT5, TLI_G7, EVENTOUT Additional:ADC2_IN4
VSS	E1	P	-	Default: VSS
VDD	G4	P	-	Default: VDD
PF6	H1	I/O		Default: PF6 Alternate: TIMER15_CH0, CAN2_RX, SAI3_SD1, SPI4_NSS, SAI0_SD1, UART6_RX, SAI2_SD1, OSPIM_P0_IO3, EXMC_D24, TIMER22_CH0, EXMC_A6, EVENTOUT Additional:ADC2_IN8
PF7	J3	I/O		Default: PF7 Alternate: TIMER16_CH0, CAN2_TX, OSPIM_P1_IO0,

BGA176[4]				
Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
				SPI4_SCK, SAI0_MCLK1, UART6_TX, SAI2_MCLK1, SAI3_MCLK1, OSPIM_P0_IO2, EXMC_A4, EXMC_D25, TIMER22_CH1, EVENTOUT Additional:ADC2_IN3
PF8	J2	I/O		Default: PF8 Alternate: TIMER15_MCH0, OSPIM_P1_IO1, SPI4_MISO, SAI0_SCK1, UART6_RTS, UART6_DE, SAI2_SCK1, SAI3_SCK1, OSPIM_P0_IO0, EXMC_D26, TIMER22_CH2, EVENTOUT Additional:ADC2_IN7
PF9	J4	I/O		Default: PF9 Alternate: TIMER16_MCH0, SPI4_MOSI, SAI0_FS1, UART6_CTS, SAI2_FS1, SAI3_FS1, OSPIM_P0_IO1, EXMC_D27, TIMER22_CH3, EVENTOUT, ENET0_PPS_OUT Additional:ADC2_IN2
PF10	K3	I/O		Default: PF10 Alternate: TIMER15_BRKIN0, SAI0_DAT2, DCI_D15, SAI3_SD0, OSPIM_P0_nSCK, OSPIM_P0_SCK, SAI2_DAT2, SAI3_DAT2, DCI_D11, TLI_DE, EVENTOUT, ENET1_PPS_OUT Additional:ADC2_IN6
PH0-OSCIN	J1	I/O		Default: PH0 Alternate: EVENTOUT Additional:OSCIN
PH1-OSCOUT	K1	I/O		Default: PH1 Alternate: EVENTOUT Additional:OSCOUT
NRST	L1	-	-	Default: NRST
PC0	L2	I/O		Default: PC0 Alternate: EXMC_D12, HPDF_CKIN0, TIMER7_CH2BRKIN, HPDF_DATAIN4, TIMER40_CH0, SAI1_FS1, EXMC_A25, USBHS0_ULPI_STP, TLI_G2, EXMC_SDNWE, TRIGSEL_IN8, TLI_R5, EVENTOUT Additional:ADC012_IN10
PC1	L3	I/O		Default: PC1 Alternate: TRACED0, SAI2_DAT0, SAI0_DAT0, HPDF_DATAIN0, HPDF_CKIN4, SPI1_MOSI, I2S1_SD, SAI0_SD0, TIMER40_MCH0, SAI2_SD0, SDIO1_CK, OSPIM_P0_IO4, ENET0_MDC, MDIO_MDC, TRIGSEL_IN9, TLI_G5, EVENTOUT, SAI3_SD0, SAI3_DAT0 Additional:ADC012_IN11, RTC_TAMP1, WKUP5
PC2	M1	I/O		Default: PC2 Alternate: PMU_DEEPSLEEP, HPDF_CKIN1, OSPIM_P0_IO5, SPI1_MISO, HPDF_CKOUT, EXMC_D9, OSPIM_P0_IO2, USBHS0_ULPI_DIR, ENET0_MII_TXD2,

BGA176[4]				
Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
				EXMC_SDNE0, TRIGSEL_IN2, EVENTOUT Additional:ADC012_IN12
PC2_C	N1	I/O		Default: PC2_C Alternate: PMU_DEEPSLEEP, HPDF_CKIN1, OSPIM_P0_IO5, SPI1_MISO, HPDF_CKOUT, EXMC_D9, OSPIM_P0_IO2, USBHS0_ULPI_DIR, ENET0_MII_TXD2, EXMC_SDNE0, TRIGSEL_IN2, EVENTOUT Additional:ADC2_IN0
PC3	M2	I/O		Default: PC3 Alternate: PMU_SLEEP, EXMC_D18, HPDF_DATAIN1, OSPIM_P0_IO6, SPI1_MOSI, I2S1_SD, SPI1_SCK, I2S1_CK, OSPIM_P0_IO0, USBHS0_ULPI_NXT, ENET0_MII_TX_CLK, EXMC_SDCKE0, EVENTOUT Additional:ADC01_IN13
PC3_C	N2	I/O		Default: PC3_C Alternate: PMU_SLEEP, EXMC_D18, HPDF_DATAIN1, OSPIM_P0_IO6, SPI1_MOSI, I2S1_SD, SPI1_SCK, I2S1_CK, OSPIM_P0_IO0, USBHS0_ULPI_NXT, ENET0_MII_TX_CLK, EXMC_SDCKE0, EVENTOUT Additional:ADC2_IN1
VDD	K4	P	-	Default: VDD
VSS	K2	P	-	Default: VSS
VSSA	N3	P	-	Default: VSSA
VREFN	L4	P	-	Default: VREFN
VREFP	M3	P	-	Default: VREFP
VDDA	M4	P	-	Default: VDDA
PA0	P1	I/O		Default: PA0 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER4_CH0, TIMER7_ETI, TIMER14_BRKIN0, SPI5_NSS, I2S5_WS, OSPIM_P0_IO6, USART1_CTS, UART3_TX, SDIO1_CMD, SAI1_SD1, ENET0_MII_CRS, EXMC_A19, TRIGSEL_IN0, EVENTOUT Additional:ADC0_IN16, WKUP0
PA0_C	R3	I/O		Default: PA0_C Alternate: TIMER1_CH0, TIMER1_ETI, TIMER4_CH0, TIMER7_ETI, TIMER14_BRKIN0, SPI5_NSS, I2S5_WS, OSPIM_P0_IO6, USART1_CTS, UART3_TX, SDIO1_CMD, SAI1_SD1, ENET0_MII_CRS, EXMC_A19, TRIGSEL_IN0, EVENTOUT Additional:ADC01_IN0
PA1	P2	I/O		Default: PA1 Alternate: TIMER1_CH1, TIMER4_CH1, TIMER14_MCH0, EXMC_NWAIT, USART1_RTS, USART1_DE, UART3_RX, OSPIM_P0_IO3, SAI1_MCLK1, ENET0_MII_RX_CLK, ENET0_RMII_REF_CLK, OSPIM_P0_DQS, TRIGSEL_IN1,

BGA176[4]				
Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
				TLI_R2, EVENTOUT Additional:ADC0_IN17
PA1_C	P3	I/O		Default: PA1_C Alternate: TIMER1_CH1, TIMER4_CH1, TIMER14_MCH0, EXMC_NWAIT, USART1_RTS, USART1_DE, UART3_RX, OSPIM_P0_IO3, SAI1_MCLK1, ENET0_MII_RX_CLK, ENET0_RMII_REF_CLK, OSPIM_P0_DQS, TRIGSEL_IN1, TLI_R2, EVENTOUT Additional:ADC01_IN1
PA2	R2	I/O		Default: PA2 Alternate: TIMER1_CH2, TIMER4_CH2, TIMER14_CH0, OSPIM_P0_IO0, USART1_TX, SAI1_SCK1, EXMC_A7, ENET0_MDIO, MDIO_MDIO, TRIGSEL_IN7, TLI_R1, EVENTOUT Additional:ADC01_IN14, WKUP1
PH2	N4	I/O		Default: PH2 Alternate: USART2_TX, TIMER40_CH0, USBHS1_ULPI_STP, OSPIM_P0_IO4, SAI1_SCK1, ENET0_MII_CRS, EXMC_SDCKE0, TLI_R0, EVENTOUT Additional:ADC2_IN13
VSS	R1	P	-	Default: VSS
PH3	R4	I/O		Default: PH3 Alternate: EXMC_SDCLK, TIMER40_MCH0, USBHS1_ULPI_DIR, OSPIM_P0_IO5, SAI1_MCLK1, ENET0_MII_COL, EXMC_SDNE0, TLI_G3, TLI_R1, EVENTOUT Additional:ADC2_IN14
PH4	P4	I/O		Default: PH4 Alternate: USART2_RX, I2C1_SCL, TIMER40_BRKIN0, USBHS1_ULPI_NXT, TLI_G5, USBHS0_ULPI_NXT, EXMC_NBL3, TLI_G4, EVENTOUT Additional:ADC2_IN15
PH5	R5	I/O		Default: PH5 Alternate: I2C1_SDA, SPI4_NSS, TIMER41_CH0, USBHS1_ULPI_CK, USBHS0_ULPI_D0, EXMC_SDNWE, EVENTOUT Additional:ADC2_IN16
PA3	N5	I/O		Default: PA3 Alternate: TIMER1_CH3, TIMER4_CH3, OSPIM_P0_nSCK, TIMER14_CH1, I2S5_MCK, OSPIM_P0_IO2, USART1_RX, EXMC_A8, TLI_B2, USBHS0_ULPI_D0, ENET0_MII_COL, OSPIM_P0_SCK, TRIGSEL_IN4, TLI_B5, EVENTOUT Additional:ADC01_IN15
VSS	M6	P	-	Default: VSS

BGA176[4]				
Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
VDD	M5	P	-	Default: VDD
PA4	P5	I/O		Default: PA4 Alternate: TIMER4_ETI, EXMC_D13, SPI0_NSS, I2S0_WS, SPI2_NSS, I2S2_WS, USART1_CK, SPI5_NSS, I2S5_WS, OSPIM_P0_IO7, USBHS0_ULPI_D0, EXMC_D8, DCI_HSYNC, TLI_VSYNC, EVENTOUT Additional:ADC01_IN18, DAC0_OUT0
PA5	P6	I/O		Default: PA5 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER7_MCH0, EXMC_D14, SPI0_SCK, I2S0_CK, SPI5_SCK, I2S5_CK, USBHS0_ULPI_CK, MDIO_A0, EXMC_D9, DCI_D14, TLI_R4, EVENTOUT Additional:ADC01_IN19, DAC0_OUT1
PA6	R7	I/O		Default: PA6 Alternate: TIMER0_BRKIN0, TIMER2_CH0, TIMER7_BRKIN0, EXMC_D15, SPI0_MISO, OSPIM_P0_IO3, SPI5_MISO, EXMC_D4, CMP_MUX_OUT0, MDIO_MDC, DCI_PIXCLK, TLI_G2, EVENTOUT Additional:ADC01_IN3
PA7	N6	I/O		Default: PA7 Alternate: TIMER0_MCH0, TIMER2_CH1, TIMER7_MCH0, SPI0_MOSI, I2S0_SD, SPI5_MOSI, I2S5_SD, OSPIM_P0_IO2, ENET0_MII_RX_DV, ENET0_RMII_CRS_DV, EXMC_SDNWE, TRIGSEL_IN5, TLI_VSYNC, EVENTOUT Additional:ADC01_IN7
PC4	R6	I/O		Default: PC4 Alternate: PMU_DEEPSLEEP, EXMC_A22, HPDF_CKIN2, I2S0_MCK, TIMER41_CH0, RSPDIF_CH2, SDIO1_CKIN, ENET0_MII_RXD0, ENET0_RMII_RXD0, EXMC_SDNE0, DCI_D15, TLI_R7, EVENTOUT Additional:ADC01_IN4, CMP0_IM7
PC5	M7	I/O		Default: PC5 Alternate: PMU_SLEEP, SAI2_DAT2, SAI0_DAT2, HPDF_DATAIN2, SAI3_DAT2, TIMER41_MCH0, EXMC_D27, RSPDIF_CH3, OSPIM_P0_DQS, ENET0_MII_RXD1, ENET0_RMII_RXD1, EXMC_SDCKE0, CMP0_OUT, TLI_DE, EVENTOUT Additional:ADC01_IN8
PB0	R8	I/O		Default: PB0 Alternate: EXMC_D19, TIMER0_MCH1, TIMER2_CH2, TIMER7_MCH1, OSPIM_P0_IO1, EXMC_A0, HPDF_CKOUT, UART3_CTS, TLI_R3, USBHS0_ULPI_D1, ENET0_MII_RXD2, MDIO_A1, TRIGSEL_OUT3, TLI_G1, EVENTOUT

BGA176[4]				
Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
				Additional:ADC01_IN9, CMP0_IP0
PB1	M8	I/O		Default: PB1 Alternate: EXMC_D20, TIMER0_MCH2, TIMER2_CH3, TIMER7_MCH2, OSPIM_P0_IO0, EXMC_A1, HPDF_DATAIN1, TLI_R6, USBHS0_ULPI_D2, ENET0_MII_RXD3, MDIO_A2, TRIGSEL_OUT4, TLI_G0, EVENTOUT Additional:ADC01_IN5, CMP0_IM6
PB2	P7	I/O		Default: PB2 Alternate: RTC_OUT, SAI2_DAT0, SAI0_DAT0, EXMC_D10, HPDF_CKIN1, SAI3_SD0, SAI0_SD0, SPI2_MOSI, I2S2_SD, SAI2_SD0, OSPIM_P0_SCK, OSPIM_P0_DQS, EXMC_NCE, MDIO_A3, TIMER22_ETI, OSPIM_P0_nSCK, EVENTOUT, SAI3_DAT0 Additional: CMP0_IP1
PF11	N7	I/O		Default: PF11 Alternate: ENET0_MII_TXD0, ENET0_RMII_TXD0, SPI4_MOSI, OSPIM_P0_nSCK, SAI1_SD1, EXMC_SDNRAS, DCI_D12, TIMER23_CH0, EVENTOUT Additional:ADC0_IN2
PF12	P11	I/O		Default: PF12 Alternate: ENET0_MII_TXD1, ENET0_RMII_TXD1, SAI3_SD1, OSPIM_P1_DQS, EXMC_D24, EXMC_A6, TIMER23_CH1, EVENTOUT Additional:ADC0_IN6
PF13	N11	I/O		Default: PF13 Alternate: ENET0_MII_TXD2, HPDF_DATAIN6, I2C3_SMBA, EXMC_A7, TIMER23_CH2, EVENTOUT Additional:ADC1_IN2
PF14	R10	I/O		Default: PF14 Alternate: ENET0_MII_TXD3, HPDF_CKIN6, I2C3_SCL, SPI4_IO2, TIMER31_CH2, EXMC_A8, TIMER23_CH3, EVENTOUT Additional:ADC1_IN6
PF15	N10	I/O		Default: PF15 Alternate: ENET0_MII_TX_CLK, I2C3_SDA, SPI4_IO3, TIMER31_CH3, EXMC_A9, EVENTOUT
PG0	P8	I/O		Default: PG0 Alternate: TIMER0_CH2, TIMER31_CH0, OSPIM_P1_IO4, EXMC_A10, EVENTOUT, ENET1_MII_COL
VSS	M10	P	-	Default: VSS
VDD	M9	P	-	Default: VDD
PG1	N9	I/O		Default: PG1 Alternate: TIMER0_MCH2, TIMER31_CH1, USBHS1_ULPI_D3, OSPIM_P1_IO5, TLI_G2, EXMC_A11,

BGA176[4]				
Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
				EVENTOUT, ENET1_MII_CRS
PE7	P9	I/O	5VT	Default: PE7 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER0_ETI, TIMER4_CH0, HPDF_DATAIN2, TIMER7_ETI, SPI4_MOSI, TIMER14_BRKIN0, UART6_RX, USBHS1_ULPI_STP, OSPIM_P0_IO4, EDIM_DO_GROUP0, EXMC_D4, EVENTOUT Additional: CMP1_IM7
PE8	N8	I/O	5VT	Default: PE8 Alternate: TIMER1_CH1, TIMER0_MCH0, TIMER4_CH1, HPDF_CKIN2, TIMER14_MCH0, UART6_TX, USBHS1_ULPI_NXT, OSPIM_P0_IO5, EDIM_DI_GROUP0, EXMC_D5, CMP1_OUT, EVENTOUT, ENET0_MII_RXD0/ENET0_RMII_RXD0
PE9	R11	I/O		Default: PE9 Alternate: TIMER1_CH2, TIMER0_CH0, TIMER4_CH2, HPDF_CKOUT, SPI3_IO2, TIMER14_CH0, UART6_RTS, UART6_DE, OSPIM_P0_IO6, EXMC_D6, EVENTOUT, ENET0_MII_RXD1/ENET0_RMII_RXD1 Additional: CMP1_IP0
PE10	R9	I/O		Default: PE10 Alternate: TIMER1_CH3, TIMER0_MCH1, TIMER4_CH3, HPDF_DATAIN4, SPI3_IO3, TIMER14_CH1, UART6_CTS, OSPIM_P0_IO7, EXMC_D7, EVENTOUT, ENET0_MII_RXD2 Additional: CMP1_IM6
PE11	R12	I/O		Default: PE11 Alternate: TIMER0_CH1, TIMER4_ETI, HPDF_CKIN4, SPI3_NSS, SAI1_SD1, OSPIM_P0_CSN, EXMC_D8, TLI_G3, EVENTOUT, ENET0_MII_RXD3 Additional: CMP1_IP1
PE12	P12	I/O		Default: PE12 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER0_MCH2, HPDF_DATAIN5, TIMER7_MCH0, SPI3_SCK, SAI1_SCK1, EXMC_D9, CMP0_OUT, TLI_B4, EVENTOUT, ENET0_MII_RX_CLK/ENET0_RMII_REF_CLK
PB10	N12	I/O		Default: PB10 Alternate: EXMC_SDNWE, TIMER1_CH2, TIMER7_MCH1, I2C1_SCL, SPI1_SCK, I2S1_CK, HPDF_DATAIN7, USART2_TX, SAI1_CLK0, OSPIM_P0_CSN, USBHS0_ULPI_D3, ENET0_MII_RX_ER, EXMC_NBL3, TRIGSEL_OUT2, TLI_G4, EVENTOUT
PB11	P10	I/O		Default: PB11 Alternate: TIMER1_CH3, TIMER7_MCH2, I2C1_SDA, DSI_TE, HPDF_CKIN7, USART2_RX, SAI1_CLK1, I2S1_MCK, USBHS0_ULPI_D4, ENET0_MII_TX_EN, ENET0_RMII_TX_EN, USBHS1_SOF, EXMC_NBL2, TLI_G5,

BGA176[4]				
Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
				EVENTOUT
VCORE	R13	P	-	Default: VCORE
VSS	R15	P	-	Default: VSS
VDD	R14	P	-	Default: VDD
PH7	M11	I/O		Default: PH7 Alternate: TIMER0_MCH0, EDOUT_A, I2C2_SCL, SPI4_MISO, ENET1_MII_RXD3, TIMER41_BRKIN0, USBHS1_ULPI_D1, ENET0_MII_RXD3, EXMC_SDCKE1, DCI_D9, EXMC_NBL1, EVENTOUT
PB12	M12	I/O	5VT	Default: PB12 Alternate: TIMER0_BRKIN0, EXMC_D25, OSPIM_P0_nSCK, I2C1_SMBA, SPI1_NSS, I2S1_WS, HPDF_DATAIN1, USART2_CK, CAN1_RX, USBHS0_ULPI_D5, ENET0_MII_TXD0, ENET0_RMII_TXD0, OSPIM_P0_IO0, CMP_MUX_OUT2, UART4_RX, EVENTOUT, SDIO1_D1, RDCM_ISIGN
PB13	L12	I/O	5VT	Default: PB13 Alternate: RTC_REFIN, TIMER0_MCH0, OSPIM_P0_IO2, SPI1_SCK, I2S1_CK, HPDF_CKIN1, USART2_CTS, CAN1_TX, USBHS0_ULPI_D6, ENET0_MII_TXD1, ENET0_RMII_TXD1, SDIO0_D0, DCI_D2, UART4_TX, EVENTOUT, SDIO1_D2, RDCM_QSIGN
PB14	K15	I/O		Default: PB14 Alternate: TIMER0_MCH1, TIMER7_MCH1, USART0_TX, SPI1_MISO, HPDF_DATAIN2, USART2_RTS, USART2_DE , UART3_RTS, UART3_DE, SDIO1_D0, EXMC_A2, EXMC_D10, TRIGSEL_OUT1, TLI_PIXCLK, EVENTOUT, OSPIM_P0_CSN Additional: USBHS1_DM
PB15	K14	I/O		Default: PB15 Alternate: RTC_REFIN, TIMER0_MCH2, TIMER7_MCH2, USART0_RX, SPI1_MOSI, I2S1_SD, HPDF_CKIN2, UART3_CTS, SDIO1_D1, EXMC_A11, EXMC_D11, TRIGSEL_OUT5, TLI_G7, EVENTOUT Additional: USBHS1_DP
PD11	J13	I/O		Default: PD11 Alternate: TIMER40_CH1, TIMER7_MCH3, I2C3_SMBA, SAI0_FS0, ENET0_MII_TX_CLK, USART2_CTS, SAI1_DAT2, OSPIM_P0_IO0, SAI1_SD0, EXMC_A16, EXMC_CLE, ENET0_MII_TXD2, EXMC_A9, EVENTOUT
PD12	J15	I/O		Default: PD12 Alternate: TIMER41_CH1, TIMER14_MCH0, TIMER3_CH0, HDSL_CLK2, I2C3_SCL, CAN2_RX, EDOUT_A, USART2_RTS, USART2_DE, USBHS1_ULPI_DIR, OSPIM_P0_IO1, SAI1_FS0, EXMC_A17, EXMC_ALE, DCI_D12, EXMC_A10, EVENTOUT

BGA176[4]				
Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
PD13	H15	I/O		Default: PD13 Alternate: TIMER42_CH1, TIMER14_CH0, TIMER3_CH1, I2C3_SDA, CAN2_TX, EDOUT_B, USBHS1_ULPI_CK, OSPIM_P0_IO3, SAI1_SCK0, EXMC_A18, DCI_D13, EXMC_A11, EVENTOUT
VSS	K12	P	-	Default: VSS
PD14	H14	I/O		Default: PD14 Alternate: TIMER43_CH1, TIMER3_CH2, SAI1_SD0, SPI3_IO2, EDOUT_Z, UART7_CTS, USBHS1_ULPI_D0, EXMC_D0, EVENTOUT
PD15	J12	I/O		Default: PD15 Alternate: TIMER44_CH1, TIMER3_CH3, SAI2_SCK0, DSI_TE, SPI3_IO3, UART7_RTS, UART7_DE, USBHS1_ULPI_D1, EXMC_D1, EVENTOUT
VSS	J14	P	-	Default: VSS
PG2	G15	I/O		Default: PG2 Alternate: EXMC_D6, TIMER0_BRKIN1, TIMER7_BRKIN0, TIMER31_CH2, SPI1_MISO, USBHS1_ULPI_D4, TLI_G3, CMP_MUX_OUT5, EXMC_A12, TIMER23_ETI, EVENTOUT, ENET1_MII_TX_EN/ENET1_RMII_TX_EN
PG3	H13	I/O		Default: PG3 Alternate: EXMC_D7, TIMER7_BRKIN2, TIMER31_CH3, SPI1_MOSI, I2S1_SD, USBHS1_ULPI_D5, CMP_MUX_OUT6, EXMC_A13, TIMER22_ETI, EVENTOUT, ENET1_MII_TXD0/ENET1_RMII_TXD0
VSSDSI	N13	P	-	Default: VSSDSI
VDD33DSI	L13	P	-	Default: VDD33DSI
VSSDSI	M13	P	-	Default: VSSDSI
DSI_D0P	L14	I/O		Default: DSI_D0P
DSI_D0N	L15	I/O		Default: DSI_D0N
DSI_CKP	M14	I/O		Default: DSI_CKP
DSI_CKN	M15	I/O		Default: DSI_CKN
VSSDSI	K13	P	-	Default: VSSDSI
DSI_D1P	N14	I/O		Default: DSI_D1P
DSI_D1N	N15	I/O		Default: DSI_D1N
VDD09DSI	P13	P	-	Default: VDD09DSI
VCORE_DSI	P14	P	-	Default: VCORE_DSI
VDDDSI	P15	P	-	Default: VDDDSI
VSS	F12	P	-	Default: VSS
VDD	H12	P	-	Default: VDD
PG4	G14	I/O		Default: PG4 Alternate: EXMC_D8, TIMER0_BRKIN2, TIMER42_BRKIN0, TIMER7_BRKIN1, TIMER31_ETI, SPI1_SCK, I2S1_CK, USBHS1_ULPI_D6, CMP_MUX_OUT7, EXMC_A14,

BGA176[4]				
Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
				EVENTOUT, ENET1_MII_TXD1/ENET1_RMII_TXD1
PG5	F15	I/O		Default: PG5 Alternate: EXMC_D9, TIMER0_ETI, TIMER42_MCH0, TIMER30_CH0, SPI1_NSS, I2S1_WS, USBHS1_ULPI_D7, EXMC_A15, EVENTOUT, ENET1_MII_TXD2
PG6	F14	I/O		Default: PG6 Alternate: TIMER16_BRKIN0, TIMER42_CH0, TIMER30_CH1, HPDF_DATAIN0, ENET1_MDC, USBHS1_ULPI_D4, OSPIM_P0_CSN, TLI_G4, EXMC_NE2, DCI_D12, TLI_R7, EVENTOUT, ENET1_MII_TXD3
PG7	G13	I/O		Default: PG7 Alternate: EXMC_D28, TIMER43_MCH0, TIMER30_CH2, HPDF_CKIN0, SAI0_MCLK0, USART5_CK, USBHS1_ULPI_D5, OSPIM_P1_DQS, EXMC_D2, EXMC_INT, DCI_D13, TLI_PIXCLK, EVENTOUT
PG8	G12	I/O	5VT	Default: PG8 Alternate: EDIM_TCLK_GROUP0, TIMER43_CH0, TIMER7_ETI, TIMER30_CH3, SPI5_NSS, I2S5_WS, ENET1_PPS_OUT, USART5_RTS, USART5_DE, RSPDIF_CH2, USBHS1_ULPI_D2, ENET0_PPS_OUT, EXMC_SDCLK, EXMC_D3, TLI_G7, EVENTOUT
VDD50USB	E15	P	-	Default: VDD50USB
VDD33USB	F13	P	-	Default: VDD33USB
PC6	E14	I/O		Default: PC6 Alternate: TIMER0_BRKIN1, TIMER2_CH0, TIMER7_CH0, HPDF_CKIN3, I2S1_MCK, ENET1_MDIO, USART5_TX, SDIO0_DAT0DIR, EXMC_NWAIT, SDIO1_D6, HDSL_LINK, SDIO0_D6, DCI_D0, TLI_HSYNC, EVENTOUT
PC7	D15	I/O		Default: PC7 Alternate: ENET1_MII_TX_EN, ENET1_RMII_TX_EN, TIMER0_CH3, TIMER2_CH1, TIMER7_CH1, HPDF_DATAIN3, I2S2_MCK, USART5_RX, SDIO0_DAT123DIR, EXMC_NE0, EXMC_NCE, SDIO1_D7, HDSL_MISO1, SDIO0_D7, DCI_D1, TLI_G6, EVENTOUT Additional: COREPOROFFOUT
PC8	D14	I/O		Default: PC8 Alternate: TRACED1, TIMER2_CH2, TIMER7_CH2, EXMC_D17, ENET1_MII_TX_CLK, USART5_CK, UART4_RTS, UART4_DE, EXMC_NE1, EXMC_INT, HDSL_MOSI1, SDIO0_D0, DCI_D2, EVENTOUT
PC9	E13	I/O		Default: PC9 Alternate: CK_OUT1, TIMER0_MCH3, TIMER2_CH3, TIMER7_CH3, I2C2_SDA, I2S_CKIN, ENET1_MII_TXD3, UART4_CTS, OSPIM_P0_IO0, TLI_G3, HDSL_SMPL,

BGA176[4]				
Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
				SDIO0_D1, DCI_D3, TLI_B2, EVENTOUT
VDD	E12	P	-	Default: VDD
PA8	B14	I/O		Default: PA8 Alternate: CK_OUT0, TIMER0_CH0, TIMER22_CH3, TIMER7_BRKIN2, I2C2_SCL, ENET1_MII_TXD2, USART0_CK, HDSL_SEL1, EXMC_D16, USBHS0_SOF, UART6_RX, CMP_MUX_OUT1, TLI_B3, TLI_R6, EVENTOUT
PA9	D13	I/O	5VT	Default: PA9 Alternate: TIMER0_CH1, TIMER23_CH2, ENET1_MII_TXD1, ENET1_RMII_TXD1, I2C2_SMBA, SPI1_SCK, I2S1_CK, USART0_TX, HDSL_CLK1, TRIGSEL_IN13, EXMC_D17, DCI_D0, TLI_R5, EVENTOUT, EDIM_DE_GROUP1 Additional:USBHS0_VBUS
PA10	C14	I/O	5VT	Default: PA10 Alternate: TIMER0_CH2, TIMER23_CH3, ENET1_MII_TXD0, ENET1_RMII_TXD0, TIMER7_CH3BRKIN, EXMC_D18, USART0_RX, HDSL_CLK2, TRIGSEL_IN12, USBHS0_ID, MDIO_MDIO, TLI_B4, DCI_D1, TLI_B1, EVENTOUT, EDIM_TCLK_GROUP1
PA11	C15	I/O		Default: PA11 Alternate: TIMER0_CH3, RDCM_PWM_P, SPI1_NSS, I2S1_WS, UART3_RX, USART0_CTS, CAN0_RX, MDIO_A1, EXMC_A19, TRIGSEL_IN13, TLI_R4, EVENTOUT, EDIM_DI_GROUP1 Additional:USBHS0_DM
PA12	B15	I/O		Default: PA12 Alternate: TIMER0_ETI, RDCM_PWM_N, SPI1_SCK, I2S1_CK, UART3_TX, USART0_RTS, USART0_DE, SAI1_FS1, CAN0_TX, EXMC_D15, MDIO_A2, TIMER0_BRKIN2, TRIGSEL_IN12, TLI_R5, EVENTOUT, EDIM_DO_GROUP1 Additional: USBHS0_DP
PA13	B13	I/O		Default: JTMS, SWDIO, PA13 Alternate: TIMER0_BRKIN1, TIMER7_BRKIN1, SPI1_NSS, I2S1_WS, UART3_RX, USART0_CTS, CAN0_RX, HDSL_SEL2, MDIO_A3, EXMC_INT, TRIGSEL_IN10, TLI_R4, EVENTOUT
VCORE	A14	P	-	Default: VCORE
VSS	A15	P	-	Default: VSS
VDD	A13	P	-	Default: VDD
PH13	C13	I/O		Default: PH13 Alternate: TIMER7_MCH0, ENET1_MII_COL, TIMER43_BRKIN0, UART3_TX, CAN0_TX, USBHS0_ULPI_D0, EXMC_D21, TLI_G2, EVENTOUT

BGA176[4]				
Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
PH14	B12	I/O		Default: PH14 Alternate: TIMER7_MCH1, ENET1_MDIO, UART3_RX, CAN0_RX, EXMC_D22, DCI_D4, TLI_G3, EVENTOUT
PH15	D12	I/O		Default: PH15 Alternate: TIMER7_MCH2, DCI_HSYNC, ENET1_MII_CRS, EXMC_D23, DCI_D11, TLI_G4, EVENTOUT
PA14	A12	I/O		Default: JTCK, SWCLK, PA14 Alternate: TLI_G7, SPI1_SCK, I2S1_CK, UART3_TX, USART0_RTS, USART0_DE, SAI1_FS1, CAN0_TX, HDSL_MISO2, MDIO_A4, TIMER0_BRKIN2, TRIGSEL_IN11, TLI_R5, EVENTOUT
PA15	A11	I/O		Default: JTDI, PA15 Alternate: TIMER1_CH0, TIMER1_ETI, ENET1_MII_COL, DSI_TE, SPI0_NSS, I2S0_WS, SPI2_NSS, I2S2_WS, SPI5_NSS, I2S5_WS, UART3_RTS, UART3_DE, TLI_R3, HDSL_MOSI2, UART6_TX, MDIO_A0, TRIGSEL_OUT0, TLI_B6, EVENTOUT
PC11	C11	I/O	5VT	Default: PC11 Alternate: TIMER0_ETI, TIMER2_CH3, HPDF_DATAIN5, EDIM_DE_GROUP0, EXMC_NE0, EXMC_NCE, SPI2_MISO, USART2_RX, UART3_RX, OSPIM_P0_CSN, EXMC_NBL2, MDIO_A2, SDIO0_D3, DCI_D4, TLI_B4, EVENTOUT
PC10	C12	I/O		Default: PC10 Alternate: TIMER7_MCH0, TIMER0_CH3, ENET1_MII_CRS, HPDF_CKIN5, EXMC_CLK, SPI2_SCK, I2S2_CK, USART2_TX, UART3_TX, OSPIM_P0_IO1, TLI_B1, MDIO_A1, SDIO0_D2, DCI_D8, TLI_R2, EVENTOUT
PD0	C10	I/O		Default: PD0 Alternate: TIMER15_MCH0, TIMER7_CH2, HPDF_CKIN6, TIMER41_CH0, UART3_RX, CAN0_RX, TIMER0_CH1BRKIN, EXMC_D2, TRIGSEL_IN3, TLI_B1, EVENTOUT, ENET0_MII_COL
PC12	B11	I/O	5VT	Default: PC12 Alternate: TRACED3, EXMC_D6, TIMER14_CH0, ENET1_MII_RX_CLK, ENET1_RMII_REF_CLK, SPI5_SCK, I2S5_CK, SPI2_MOSI, I2S2_SD, USART2_CK, UART4_TX, EDIM_TCLK_GROUP0, TIMER0_CH0BRKIN, SDIO0_CK, DCI_D9, TLI_R6, EVENTOUT
PD2	B10	I/O	5VT	Default: PD2 Alternate: TRACED2, EXMC_D7, TIMER2_ETI, TIMER4_CH1, TIMER14_BRKIN0, ENET1_MII_RX_DV, ENET1_RMII_CRS_DV, TLI_B4, UART4_RX, TLI_B7, EDIM_DI_GROUP0, TIMER0_CH3BRKIN, SDIO0_CMD, DCI_D11, TLI_B2, EVENTOUT
PD1	A10	I/O		Default: PD1 Alternate: TIMER16_MCH0, TIMER4_CH0, HPDF_DATAIN6,

BGA176[4]				
Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
				TIMER41_MCH0, UART3_TX, CAN0_TX, TIMER0_CH2BRKIN, EXMC_D3, TRIGSEL_IN6, EVENTOUT, ENET0_MII_CRS
PD3	A9	I/O		Default: PD3 Alternate: SAI3_FS0, TIMER4_CH2, HPDF_CKOUT, SPI1_SCK, I2S1_CK, ENET1_MII_RX_ER, USART1_CTS, OSPIM_P0_IO3, EXMC_A6, EXMC_CLK, DCI_D5, TLI_G7, EVENTOUT
PD4	C9	I/O		Default: PD4 Alternate: SAI3_MCLK0, TIMER7_MCH3, USART1_RTS, USART1_DE, ENET1_MII_RXD0, ENET1_RMII_RXD0, OSPIM_P0_IO4, EXMC_NOE, TLI_R3, EVENTOUT
PD5	B9	I/O		Default: PD5 Alternate: SAI3_SCK0, TIMER7_CH3, USART1_TX, ENET1_MII_RXD1, ENET1_RMII_RXD1, OSPIM_P0_IO5, EXMC_NWE, EVENTOUT
VSS	D10	P	-	Default: VSS
VDD	D11	P	-	Default: VDD
PD6	D9	I/O		Default: PD6 Alternate: SAI1_DAT0, SAI0_DAT0, HPDF_CKIN4, HPDF_DATAIN1, SPI2_MOSI, I2S2_SD, SAI0_SD0, USART1_RX, SAI2_SD0, ENET1_MII_RXD2, OSPIM_P0_IO6, SDIO1_CK, EXMC_NWAIT, DCI_D10, TLI_B2, EVENTOUT, SAI3_DAT0, SAI3_SD0
PD7	B8	I/O		Default: PD7 Alternate: SAI3_SD1, TIMER4_CH3, HPDF_DATAIN4, SPI0_MOSI, I2S0_SD, HPDF_CKIN1, USART1_CK, ENET1_MII_RXD3, RSPDIF_CH0, OSPIM_P0_IO7, SDIO1_CMD, EXMC_NE0, EXMC_NCE, TLI_R4, EVENTOUT
PG9	A8	I/O		Default: PG9 Alternate: EXMC_D30, CAN2_TX, TIMER7_BRKIN1, TIMER30_ETI, SPI0_MISO, ENET1_MII_TX_CLK, USART5_RX, RSPDIF_CH3, OSPIM_P0_IO6, SAI1_FS1, SDIO1_D0, EXMC_NE1, DCI_VSYNC, EVENTOUT
PG10	C8	I/O		Default: PG10 Alternate: EXMC_D31, CAN2_RX, OSPIM_P1_IO6, SPI0_NSS, I2S0_WS, TLI_G3, SAI1_SD1, SDIO1_D1, EXMC_NE2, DCI_D2, TLI_B2, EVENTOUT
PG11	A7	I/O		Default: PG11 Alternate: EXMC_D29, SPI0_SCK, I2S0_CK, ENET1_MII_TX_EN, ENET1_RMII_TX_EN, RSPDIF_CH0, OSPIM_P1_IO7, SDIO1_D2, ENET0_MII_TX_EN, ENET0_RMII_TX_EN, DCI_D3, TLI_B3, EVENTOUT
PG12	D8	I/O		Default: PG12

BGA176[4]				
Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
				Alternate: TLI_G5, ENET0_MII_TXD2, OSPIM_P1_CSN, SPI5_MISO, ENET1_MII_TXD2, USART5_RTS, USART5_DE, RSPDIF_CH1, TLI_B4, SDIO1_D3, ENET0_MII_TXD1, ENET0_RMII_TXD1, EXMC_NE3, TIMER22_CH0, TLI_B1, EVENTOUT
PG13	B7	I/O		Default: PG13 Alternate: TRACED0, SPI5_SCK, I2S5_CK, ENET1_MII_TXD0, ENET1_RMII_TXD0, USART5_CTS, TIMER44_CH0, SDIO1_D6, ENET0_MII_TXD0, ENET0_RMII_TXD0, EXMC_A24, TIMER22_CH1, TLI_R0, EVENTOUT
PG14	C7	I/O		Default: PG14 Alternate: TRACED1, SPI5_MOSI, I2S5_SD, ENET1_MII_TXD1, ENET1_RMII_TXD1, USART5_TX, TIMER44_MCH0, OSPIM_P0_IO7, SDIO1_D7, ENET0_MII_TXD1, ENET0_RMII_TXD1, EXMC_A25, TIMER22_CH2, TLI_B0, EVENTOUT
PG15	D7	I/O		Default: PG15 Alternate: SPI0_NSS, I2S0_WS, ENET1_MII_TXD3, USART5_CTS, TIMER44_BRKIN0, OSPIM_P1_DQS, EXMC_NE3, EXMC_SDNCAS, DCI_D13, EVENTOUT
PB3	A6	I/O	5VT	Default: JTDO, TRACESWO, PB3 Alternate: TIMER1_CH1, TLI_PIXCLK, ENET1_MII_TX_CLK, SPI0_SCK, I2S0_CK, SPI2_SCK, I2S2_CK, EXMC_A12, SPI5_SCK, I2S5_CK, SDIO1_D2, CTC_SYNC, UART6_RX, MDIO_A4, TRIGSEL_OUT7, TIMER23_ETI, EVENTOUT, EDIM_TCLK_GROUP0
PB4	B6	I/O		Default: NJTRST, PB4 Alternate: TIMER15_BRKIN0, TIMER2_CH0, CAN1_TX, SPI0_MISO, SPI2_MISO, SPI1_NSS, I2S1_WS, SPI5_MISO, SDIO1_D3, ENET1_MII_TXD3, UART6_TX, EXMC_A13, TRIGSEL_OUT6, EXMC_SDCKE0, EVENTOUT, EXMC_SDNE0, EXMC_D5
PB5	C6	I/O		Default: PB5 Alternate: TIMER16_BRKIN0, TIMER2_CH1, TLI_B5, I2C0_SMBA, SPI0_MOSI, I2S0_SD, I2C3_SMBA, SPI2_MOSI, I2S2_SD, SPI5_MOSI, I2S5_SD, CAN1_RX, USBHS0_ULPI_D7, ENET0_PPS_OUT, EXMC_SDCKE1, DCI_D10, UART4_RX, EVENTOUT, EXMC_A9
PB6	A5	I/O		Default: PB6 Alternate: TIMER0_MCH1, TIMER15_MCH0, TIMER3_CH0, EXMC_D11, I2C0_SCL, I2C3_SCL, USART0_TX, ENET1_MII_TX_EN, ENET1_RMII_TX_EN, CAN1_TX, OSPIM_P0_CSN, HPDF_DATAIN5, EXMC_SDNE1, DCI_D5, UART4_TX, EVENTOUT, EXMC_NE0, EXMC_NCE, I2S2_MCK

BGA176[4]				
Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
PB7	B5	I/O		Default: PB7 Alternate: TIMER0_MCH2, TIMER16_MCH0, TIMER3_CH1, TIMER7_CH1BRKIN, I2C0_SDA, I2C3_SDA, USART0_RX, EXMC_SDNE0, HPDF_CKIN5, EXMC_NL, EXMC_NADV, DCI_VSYNC, EVENTOUT
BOOT	C5	I/O		Default: BOOT
PB8	A2	I/O		Default: PB8 Alternate: TIMER40_MCH0, TIMER15_CH0, TIMER3_CH2, HPDF_CKIN7, I2C0_SCL, I2C3_SCL, SDIO0_CKIN, UART3_RX, CAN0_RX, SDIO1_D4, ENET0_MII_TXD3, SDIO0_D4, DCI_D6, TLI_B6, EVENTOUT, EXMC_A10, EXMC_D26
PB9	B3	I/O		Default: PB9 Alternate: TIMER40_CH0, TIMER16_CH0, TIMER3_CH3, HPDF_DATAIN7, I2C0_SDA, SPI1_NSS, I2S1_WS, I2C3_SDA, SDIO0_CMDDIR, UART3_TX, CAN0_TX, SDIO1_D5, I2C3_SMBA, SDIO0_D5, DCI_D7, TLI_B7, EVENTOUT,
PE0	B4	I/O		Default: PE0 Alternate: SPI4_NSS, TIMER3_ETI, HDSL_LINK, UART7_RX, SAI1_MCLK0, EXMC_NOE, EXMC_NBL0, DCI_D2, TLI_R0, EVENTOUT
VCORE	A4	P	-	Default: VCORE
PE1	C4	I/O		Default: PE1 Alternate: SPI4_SCK, HDSL_SMPL, UART7_TX, EXMC_NWE, EXMC_NBL1, DCI_D3, TLI_R6, EVENTOUT
VSS	D6	P	-	Default: VSS
VDD	A3	P	-	Default: VDD
PDR_ON(3)	D4	P	-	Default: PDR_ON
VDD	D5	P	-	Default: VDD
PE2	C3	I/O		Default: PE2 Alternate: TRACECK, TIMER23_CH0, SAI0_CLK0, EXMC_A2, SPI3_SCK, SAI0_MCLK0, HDSL_SEL1, SAI2_MCLK0, OSPIM_P0_IO2, SAI2_CLK0, ENET0_MII_TXD3, EXMC_A23, TIMER7_CH0BRKIN, SAI3_CLK0, EVENTOUT, SAI3_MCLK0
PE3	B2	I/O		Default: PE3 Alternate: TRACED0, TIMER23_CH1, SPI4_MISO, TIMER14_BRKIN0, SPI3_SCK, SAI0_SD1, HDSL_CLK1, SAI2_SD1, EXMC_NBL3, EXMC_A3, EXMC_A19, DCI_PIXCLK, SAI3_SD1, EVENTOUT

BGA176[4]				
Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
VSS	F6	P	-	Default: VSS(4)
VSS	F7	P	-	Default: VSS(4)
VSS	F8	P	-	Default: VSS(4)
VSS	F9	P	-	Default: VSS(4)
VSS	F10	P	-	Default: VSS(4)
VSS	G6	P	-	Default: VSS(4)
VSS	G7	P	-	Default: VSS(4)
VSS	G8	P	-	Default: VSS(4)
VSS	G9	P	-	Default: VSS(4)
VSS	G10	P	-	Default: VSS(4)
VSS	H6	P	-	Default: VSS(4)
VSS	H7	P	-	Default: VSS(4)
VSS	H8	P	-	Default: VSS(4)
VSS	H9	P	-	Default: VSS(4)
VSS	H10	P	-	Default: VSS(4)
VSS	J6	P	-	Default: VSS(4)
VSS	J7	P	-	Default: VSS(4)
VSS	J8	P	-	Default: VSS(4)
VSS	J9	P	-	Default: VSS(4)
VSS	J10	P	-	Default: VSS(4)
VSS	K6	P	-	Default: VSS(4)
VSS	K7	P	-	Default: VSS(4)
VSS	K8	P	-	Default: VSS(4)
VSS	K9	P	-	Default: VSS(4)
VSS	K10	P	-	Default: VSS(4)

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) PDR_ON pin should be pulled up to VDD, refer to *Figure 4-4. Recommended PDR_ON*

pin circuit(1).

(4) The pin count of the BGA176 package is 176+25 (with an additional 25 VSS pins).

2.6.2. GD32H77Dxx pin alternate functions

Table 2-4. Port A alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0		TIMER1_CH0/TIMER1_ETI	TIMER4_CH0	TIMER7_ETI	TIMER14_BRKIN0	SPI5_NSS/I2S5_WS	OSPIM_P0_IO6	USART1_CTS	UART3_TX	SDIO1_CMD	SAI1_SD1	ENET0_MII_CRS	EXMC_A19	TRIGSEL_IN0		EVENTOUT
PA0_C[2]		TIMER1_CH0/TIMER1_ETI	TIMER4_CH0	TIMER7_ETI	TIMER14_BRKIN0	SPI5_NSS/I2S5_WS	OSPIM_P0_IO6	USART1_CTS	UART3_TX	SDIO1_CMD	SAI1_SD1	ENET0_MII_CRS	EXMC_A19	TRIGSEL_IN0		EVENTOUT
PA1		TIMER1_CH1	TIMER4_CH1		TIMER14_MCH0	EXMC_NWAIT		USART1_RTS/USART1_DE	UART3_RX	OSPIM_P0_IO3	SAI1_MCLK1	ENET0_MII_RX_CLK/ENET0_RMII_REF_CLK	OSPIM_P0_DQS	TRIGSEL_IN1	TLI_R2	EVENTOUT
PA1_C[2]		TIMER1_CH1	TIMER4_CH1		TIMER14_MCH0	EXMC_NWAIT		USART1_RTS/USART1_DE	UART3_RX	OSPIM_P0_IO3	SAI1_MCLK1	ENET0_MII_RX_CLK/ENET0_RMII_REF_CLK	OSPIM_P0_DQS	TRIGSEL_IN1	TLI_R2	EVENTOUT
PA2		TIMER1_CH2	TIMER4_CH2		TIMER14_CH0		OSPIM_P0_IO0	USART1_TX	SAI1_SCK1	EXMC_A7		ENET0_MDIO	MDIO_MDIO	TRIGSEL_IN7	TLI_R1	EVENTOUT
PA3		TIMER1_CH3	TIMER4_CH3	OSPIM_P0_nSCK	TIMER14_CH1	I2S5_MCK	OSPIM_P0_IO2	USART1_RX	EXMC_A8	TLI_B2	USBHS0_ULPI_D0	ENET0_MII_COL	OSPIM_P0_SCK	TRIGSEL_IN4	TLI_B5	EVENTOUT
PA4			TIMER4_ETI		EXMC_D13	SPI0_NSS/I2S0_WS	SPI2_NSS/I2S2_WS	USART1_CK	SPI5_NSS/I2S5_WS	OSPIM_P0_IO7	USBHS0_ULPI_D0		EXMC_D8	DCI_HSYNC	TLI_VSYNC	EVENTOUT
PA5		TIMER1_CH0/TIMER1_ETI		TIMER7_MCH0	EXMC_D14	SPI0_SCK/I2S0_CK			SPI5_SCK/I2S5_CK		USBHS0_ULPI_CK	MDIO_A0	EXMC_D9	DCI_D14	TLI_R4	EVENTOUT
PA6		TIMER0_BRKIN0	TIMER2_CH0	TIMER7_BRKIN0	EXMC_D15	SPI0_MISO	OSPIM_P0_IO3		SPI5_MISO	EXMC_D4	CMP_MUX_OUT0	MDIO_MDC		DCI_PIXCLK	TLI_G2	EVENTOUT
PA7		TIMER0_MCH0	TIMER2_CH1	TIMER7_MCH0		SPI0_MOSI/I2S0_SD			SPI5_MOSI/I2S5_SD		OSPIM_P0_IO2	ENET0_MII_RX_DV/ENET0_RMII_CRS_DV	EXMC_SDNWE	TRIGSEL_IN5	TLI_VSYNC	EVENTOUT
PA8	CK_OUT0	TIMER0_CH0	TIMER22_CH3	TIMER7_BRKIN2	I2C2_SCL	ENET1_MII_TXD2		USART0_CK	HDSL_SEL1	EXMC_D16	USBHS0_SOF	UART6_RX	CMP_MUX_OUT1	TLI_B3	TLI_R6	EVENTOUT
PA9	EDIM_DE_GROUP1	TIMER0_CH1	TIMER23_CH2	ENET1_MII_TXD1/ENET1_RMII_	I2C2_SMBA	SPI1_SCK/I2S1_CK		USART0_TX	HDSL_CLK1	TRIGSEL_IN13			EXMC_D17	DCI_D0	TLI_R5	EVENTOUT

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
				TXD1												
PA10	EDIM_TCLK_GROUP1	TIMER0_CH2	TIMER23_CH3	ENET1_MII_TXD0/ENET1_RMII_TXD0	TIMER7_CH3BRKIN	EXMC_D18		USART0_RX	HDSL_CLK2	TRIGSEL_IN12	USBHS0_ID	MDIO_MDIO	TLI_B4	DCI_D1	TLI_B1	EVENTOUT
PA11	EDIM_DI_GROUP1	TIMER0_CH3			RDCM_PWM_P	SPI1_NSS/I2S1_WS	UART3_RX	USART0_CTS		CAN0_RX		MDIO_A1	EXMC_A19	TRIGSEL_IN13	TLI_R4	EVENTOUT
PA12	EDIM_DO_GROUP1	TIMER0_ETI			RDCM_PWM_N	SPI1_SCK/I2S1_CK	UART3_TX	USART0_RTS/USART0_DE	SAI1_FS1	CAN0_TX	EXMC_D15	MDIO_A2	TIMER0_BRKIN2	TRIGSEL_IN12	TLI_R5	EVENTOUT
PA13	JTMS/SWDIO	TIMER0_BRKIN1		TIMER7_BRKIN1		SPI1_NSS/I2S1_WS	UART3_RX	USART0_CTS		CAN0_RX	HDSL_SEL2	MDIO_A3	EXMC_INT	TRIGSEL_IN10	TLI_R4	EVENTOUT
PA14	JTCK/SWCLK				TLI_G7	SPI1_SCK/I2S1_CK	UART3_TX	USART0_RTS/USART0_DE	SAI1_FS1	CAN0_TX	HDSL_MISO2	MDIO_A4	TIMER0_BRKIN2	TRIGSEL_IN11	TLI_R5	EVENTOUT
PA15	JTDI	TIMER1_CH0/TIMER1_ETI		ENET1_MII_COL	DSI_TE	SPI0_NSS/I2S0_WS	SPI2_NSS/I2S2_WS	SPI5_NSS/I2S5_WS	UART3_RTS/UART3_DE	TLI_R3	HDSL_MOSI2	UART6_TX	MDIO_A0	TRIGSEL_OUT0	TLI_B6	EVENTOUT

Table 2-5. Port B alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15	AF16	AF17	AF18
PB0	EXMC_D19	TIMER0_MCH1	TIMER2_CH2	TIMER7_MCH1	OSPIM_P0_IO1	EXMC_A0	HPDF_CKOUT		UART3_CTS	TLI_R3	USBHS0_ULPI_D1	ENET0_MII_RXD2	MDIO_A1	TRIGSEL_OUT3	TLI_G1	EVENTOUT			
PB1	EXMC_D20	TIMER0_MCH2	TIMER2_CH3	TIMER7_MCH2	OSPIM_P0_IO0	EXMC_A1	HPDF_DATAIN1			TLI_R6	USBHS0_ULPI_D2	ENET0_MII_RXD3	MDIO_A2	TRIGSEL_OUT4	TLI_G0	EVENTOUT			
PB2	RTC_OUT	SAI2_DAT0	SAI0_DAT0	EXMC_D10	HPDF_CKIN1	SAI3_SD0	SAI0_SD0	SPI2_MOSI/I2S2_SD	SAI2_SD0	OSPIM_P0_SCK	OSPIM_P0_DQS	EXMC_NCE	MDIO_A3	TIMER22_ETI	OSPIM_P0_nSCK	EVENTOUT			SAI3_DAT0
PB3	JTDO/TRACESWO	TIMER1_CH1	TLI_PIXCLK		ENET1_MII_TX_CLK	SPI0_SCK/I2S0_CK	SPI2_SCK/I2S2_CK	EXMC_A12	SPI5_SCK/I2S5_CK	SDIO1_D2	CTC_SYNC	UART6_RX	MDIO_A4	TRIGSEL_OUT7	TIMER23_ETI	EVENTOUT	EDIM_TCLK_GROUP0		
PB4	NJTRST	TIMER15_BRKIN0	TIMER2_CH0		CAN1_TX	SPI0_MISO	SPI2_MISO	SPI1_NSS/I2S1_WS	SPI5_MISO	SDIO1_D3	ENET1_MII_TXD3	UART6_TX	EXMC_A13	TRIGSEL_OUT6	EXMC_SDCKE0	EVENTOUT	EXMC_SDNE0	EXMC_D5	
PB5		TIMER16_BRKIN0	TIMER2_CH1	TLI_B5	I2C0_SMBA	SPI0_MOSI/I2S0_SD	I2C3_SMBA	SPI2_MOSI/I2S2_SD	SPI5_MOSI/I2S5_SD	CAN1_RX	USBHS0_ULPI_D7	ENET0_PPS_OUT	EXMC_SDCKE1	DCI_D10	UART4_RX	EVENTOUT	EXMC_A9		

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15	AF16	AF17	AF18
PB6	TIMER0_MCH1	TIMER15_MCH0	TIMER3_CH0	EXMC_D11	I2C0_SCL		I2C3_SCL	USART0_TX	ENET1_MII_TX_EN/ENET1_RMII_TX_EN	CAN1_TX	OSPIM_P0_CSN	HPDF_DATAIN5	EXMC_SDNE1	DCI_D5	UART4_TX	EVENTOUT	EXMC_NE0/EXMC_NCE	I2S2_MCK	
PB7	TIMER0_MCH2	TIMER16_MCH0	TIMER3_CH1	TIMER7_CH1BRKIN	I2C0_SDA		I2C3_SDA	USART0_RX			EXMC_SDNE0	HPDF_CKIN5	EXMC_NL/EXMC_NADV	DCI_VSYNC		EVENTOUT			
PB8	TIMER40_MCH0	TIMER15_CH0	TIMER3_CH2	HPDF_CKIN7	I2C0_SCL		I2C3_SCL	SDIO0_CKIN	UART3_RX	CAN0_RX	SDIO1_D4	ENET0_MII_TXD3	SDIO0_D4	DCI_D6	TLI_B6	EVENTOUT	EXMC_A10	EXMC_D26	
PB9	TIMER40_CH0	TIMER16_CH0	TIMER3_CH3	HPDF_DATAIN7	I2C0_SDA	SPI1_NSS/I2S1_WS	I2C3_SDA	SDIO0_CMDDIR	UART3_TX	CAN0_TX	SDIO1_D5	I2C3_SMBA	SDIO0_D5	DCI_D7	TLI_B7	EVENTOUT			
PB10	EXMC_SDNWE	TIMER1_CH2		TIMER7_MCH1	I2C1_SCL	SPI1_SCK/I2S1_CK	HPDF_DATAIN7	USART2_TX	SAI1_CLK0	OSPIM_P0_CSN	USBHS0_ULPI_D3	ENET0_MII_RX_ER	EXMC_NBL3	TRIGSEL_OUT2	TLI_G4	EVENTOUT			
PB11		TIMER1_CH3		TIMER7_MCH2	I2C1_SDA	DSI_TE	HPDF_CKIN7	USART2_RX	SAI1_CLK1	I2S1_MCK	USBHS0_ULPI_D4	ENET0_MII_TX_EN/ENET0_RMII_TX_EN	USBHS1_SOF	EXMC_NBL2	TLI_G5	EVENTOUT			
PB12		TIMER0_BRKIN0	EXMC_D25	OSPIM_P0_nSCK	I2C1_SMBA	SPI1_NSS/I2S1_WS	HPDF_DATAIN1	USART2_CK		CAN1_RX	USBHS0_ULPI_D5	ENET0_MII_TXD0/ENET0_RMII_TXD0	OSPIM_P0_IO0	CMP_MUX_OUT2	UART4_RX	EVENTOUT	SDIO1_D1	RDCM_ISIGN	
PB13	RTC_REFIN	TIMER0_MCH0			OSPIM_P0_IO2	SPI1_SCK/I2S1_CK	HPDF_CKIN1	USART2_CTS		CAN1_TX	USBHS0_ULPI_D6	ENET0_MII_TXD1/ENET0_RMII_TXD1	SDIO0_D0	DCI_D2	UART4_TX	EVENTOUT	SDIO1_D2	RDCM_QSIGN	
PB14		TIMER0_MCH1		TIMER7_MCH1	USART0_TX	SPI1_MISO	HPDF_DATAIN2	USART2_RTS/USART2_DE	UART3_RTS/UART3_DE	SDIO1_D0		EXMC_A2	EXMC_D10	TRIGSEL_OUT1	TLI_PIXCLK	EVENTOUT	OSPIM_P0_CSN		
PB15	RTC_REFIN	TIMER0_MCH2		TIMER7_MCH2	USART0_RX	SPI1_MOSI/I2S1_SD	HPDF_CKIN2		UART3_CTS	SDIO1_D1		EXMC_A11	EXMC_D11	TRIGSEL_OUT5	TLI_G7	EVENTOUT			

Table 2-6. Port C alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15	AF16	AF17	AF18
PC0		EXMC_D12		HPDF_CKIN0	TIMER7_CH2BRKIN		HPDF_DATAIN4	TIMER40_CH0	SAI1_FS1	EXMC_A25	USBHS0_ULPI_STP	TLI_G2	EXMC_SDNWE	TRIGSEL_IN8	TLI_R5	EVENTOUT			
PC1	TRACED0	SAI2_DAT0	SAI0_DAT0	HPDF_DATAIN0	HPDF_CKIN4	SPI1_MOSI/I2S1_SD	SAI0_SD0	TIMER40_MCH0	SAI2_SD0	SDIO1_CK	OSPIM_P0_IO4	ENET0_MDC	MDIO_MDC	TRIGSEL_IN9	TLI_G5	EVENTOUT	SAI3_SD0	SAI3_DAT0	
PC2	PMU_DEEPSLEEP			HPDF_CKIN1	OSPIM_P0_IO5	SPI1_MISO	HPDF_CKOUT		EXMC_D9	OSPIM_P0_IO2	USBHS0_ULPI_DIR	ENET0_MII_TXD2	EXMC_SDNE0	TRIGSEL_IN2		EVENTOUT			
PC2_C[2)]	PMU_DEEPSLEEP			HPDF_CKIN1	OSPIM_P0_IO5	SPI1_MISO	HPDF_CKOUT		EXMC_D9	OSPIM_P0_IO2	USBHS0_ULPI_DIR	ENET0_MII_TXD2	EXMC_SDNE0	TRIGSEL_IN2		EVENTOUT			
PC3	PMU_SLEEP	EXMC_D18		HPDF_DATAIN1	OSPIM_P0_IO6	SPI1_MOSI/I2S1_SD	SPI1_SCK/I2S1_CK			OSPIM_P0_IO0	USBHS0_ULPI_NXT	ENET0_MII_TX_CLK	EXMC_SDCKE0			EVENTOUT			
PC3_C[2)]	PMU_SLEEP	EXMC_D18		HPDF_DATAIN1	OSPIM_P0_IO6	SPI1_MOSI/I2S1_SD	SPI1_SCK/I2S1_CK			OSPIM_P0_IO0	USBHS0_ULPI_NXT	ENET0_MII_TX_CLK	EXMC_SDCKE0			EVENTOUT			
PC4	PMU_DEEPSLEEP	EXMC_A22		HPDF_CKIN2		I2S0_MCK		TIMER41_CH0		RSPDIF_CH2	SDIO1_CKIN	ENET0_MII_RXD0/ENET0_RMII_RXD0	EXMC_SDNE0	DCI_D15	TLI_R7	EVENTOUT			
PC5	PMU_SLEEP	SAI2_DAT2	SAI0_DAT2	HPDF_DATAIN2	SAI3_DAT2			TIMER41_MCH0	EXMC_D27	RSPDIF_CH3	OSPIM_P0_DQS	ENET0_MII_RXD1/ENET0_RMII_RXD1	EXMC_SDCKE0	CMP0_OUT	TLI_DE	EVENTOUT			
PC6		TIMER0_BRKIN1	TIMER2_CH0	TIMER7_CH0	HPDF_CKIN3	I2S1_MCK	ENET1_MDIO	USART5_TX	SDIO0_DAT0DIR	EXMC_NWAIT	SDIO1_D6	HDSL_LINK	SDIO0_D6	DCI_D0	TLI_HSYNC	EVENTOUT			
PC7	ENET1_MII_TX_EN/ENET1_RMII_TX_EN	TIMER0_CH3	TIMER2_CH1	TIMER7_CH1	HPDF_DATAIN3		I2S2_MCK	USART5_RX	SDIO0_DAT123DIR	EXMC_NE0/EXMC_NCE	SDIO1_D7	HDSL_MISO1	SDIO0_D7	DCI_D1	TLI_G6	EVENTOUT			
PC8	TRACED1		TIMER2_CH2	TIMER7_CH2	EXMC_D17		ENET1_MII_TX_CLK	USART5_CK	UART4_RTS/UART4_DE	EXMC_NE1	EXMC_INT	HDSL_MOSI1	SDIO0_D0	DCI_D2		EVENTOUT			
PC9	CK_OUT1	TIMER0_MCH3	TIMER2_CH3	TIMER7_CH3	I2C2_SDA	I2S_CKIN		ENET1_MII_TXD	UART4_CTS	OSPIM_P0_IO0	TLI_G3	HDSL_SMPL	SDIO0_D1	DCI_D3	TLI_B2	EVENTOUT			

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15	AF16	AF17	AF18
								3											
PC10	TIMER7_MCH0	TIMER0_CH3	ENET1_MII_CRS	HPDF_CKIN5		EXMC_CLK	SPI2_SCK/I2S2_CK	USART2_TX	UART3_TX	OSPIM_P0_IO1	TLI_B1	MDIO_A1	SDIO0_D2	DCI_D8	TLI_R2	EVENTOUT			
PC11		TIMER0_ETI	TIMER2_CH3	HPDF_DATAIN5	EDIM_DE_GROUP0	EXMC_NE0/EXMC_NCE	SPI2_MISO	USART2_RX	UART3_RX	OSPIM_P0_CSN	EXMC_NBL2	MDIO_A2	SDIO0_D3	DCI_D4	TLI_B4	EVENTOUT			
PC12	TRACED3	EXMC_D6	TIMER14_CH0	ENET1_MII_RX_CLK/ENET1_RMII_REF_CLK		SPI5_SCK/I2S5_CK	SPI2_MOSI/I2S2_SD	USART2_CK	UART4_TX		EDIM_TCLK_GROUP0	TIMER0_CH0BRKIN	SDIO0_CK	DCI_D9	TLI_R6	EVENTOUT			
PC13																EVENTOUT			
PC14-OSC32IN																EVENTOUT			
PC15-OSC32OUT																EVENTOUT			

Table 2-7. Port D alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15	AF16	AF17	AF18
PD0		TIMER15_MCH0	TIMER7_CH2	HPDF_CKIN6	TIMER41_CH0				UART3_RX	CAN0_RX	ENET0_MII_COL	TIMER0_CH1BRKIN	EXMC_D2	TRIGSEL_IN3	TLI_B1	EVENTOUT			
PD1		TIMER16_MCH0	TIMER4_CH0	HPDF_DATAIN6	TIMER41_MCH0				UART3_TX	CAN0_TX	ENET0_MII_CRS	TIMER0_CH2BRKIN	EXMC_D3	TRIGSEL_IN6		EVENTOUT			
PD2	TRACED2	EXMC_D7	TIMER2_ETI	TIMER4_CH1	TIMER14_BRKIN0		ENET1_MII_RX_DV/ENET1_RMII_CRS_DV	TLI_B4	UART4_RX	TLI_B7	EDIM_DI_GROUP0	TIMER0_CH3BRKIN	SDIO0_CMD	DCI_D11	TLI_B2	EVENTOUT			
PD3		SAI3_FS0	TIMER4_CH2	HPDF_CKOUT		SPI1_SCK/I2S1_CK	ENET1_MII_RX_ER	USART1_CTS	OSPIM_P0_IO3			EXMC_A6	EXMC_CLK	DCI_D5	TLI_G7	EVENTOUT			

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15	AF16	AF17	AF18
PD4		SAI3_MCLK0		TIMER7_MCH3				USART1_RTS/USART1_DE		ENET1_MII_RXD0/ENET1_RMII_RXD0	OSPIM_P0_IO4		EXMC_NOE	TLI_R3		EVENTOUT			
PD5		SAI3_SCK0		TIMER7_CH3				USART1_TX		ENET1_MII_RXD1/ENET1_RMII_RXD1	OSPIM_P0_IO5		EXMC_NWE			EVENTOUT			
PD6		SAI1_DAT0	SAI0_DAT0	HPDF_CKIN4	HPDF_DATAIN1	SPI2_MOSI/I2S2_SD	SAI0_SD0	USART1_RX	SAI2_SD0	ENET1_MII_RXD2	OSPIM_P0_IO6	SDIO1_CK	EXMC_NWAIT	DCI_D10	TLI_B2	EVENTOUT	SAI3_DAT0	SAI3_SD0	
PD7		SAI3_SD1	TIMER4_CH3	HPDF_DATAIN4		SPI0_MOSI/I2S0_SD	HPDF_CKIN1	USART1_CK	ENET1_MII_RXD3	RSPDIF_CH0	OSPIM_P0_IO7	SDIO1_CMD	EXMC_NE0/EXMC_NCE		TLI_R4	EVENTOUT			
PD11	TIMER40_CH1			TIMER7_MCH3	I2C3_SMBA	SAI0_FS0	ENET0_MII_TX_CLK	USART2_CTS	SAI1_DAT2	OSPIM_P0_IO0	SAI1_SD0		EXMC_A16/EXMC_CLE	ENET0_MII_TXD2	EXMC_A9	EVENTOUT			
PD12	TIMER41_CH1	TIMER14_MCH0	TIMER3_CH0	HDSL_CLK2	I2C3_SCL	CAN2_RX	EDOUT_A	USART2_RTS/USART2_DE	USBHS1_ULPI_DIR	OSPIM_P0_IO1	SAI1_FS0		EXMC_A17/EXMC_ALE	DCI_D12	EXMC_A10	EVENTOUT			
PD13	TIMER42_CH1	TIMER14_CH0	TIMER3_CH1		I2C3_SDA	CAN2_TX	EDOUT_B		USBHS1_ULPI_CK	OSPIM_P0_IO3	SAI1_SCK0		EXMC_A18	DCI_D13	EXMC_A11	EVENTOUT			
PD14	TIMER43_CH1		TIMER3_CH2	SAI1_SD0		SPI3_IO2	EDOUT_Z		UART7_CTS	USBHS1_ULPI_D0			EXMC_D0			EVENTOUT			
PD15	TIMER44_CH1		TIMER3_CH3	SAI2_SCK0	DSI_TE	SPI3_IO3			UART7_RTS/UART7_DE	USBHS1_ULPI_D1			EXMC_D1			EVENTOUT			

Table 2-8. Port E alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15	AF16	AF17	AF18
PE0		SPI4_NSS	TIMER3_ETI					HDSL_LINK	UART7_RX		SAI1_MCLK0	EXMC_NOE	EXMC_NBL0	DCI_D2	TLI_R0	EVENTOUT			
PE1		SPI4_SCK						HDSL_SMPL	UART7_TX			EXMC_NWE	EXMC_NBL1	DCI_D3	TLI_R6	EVENTOUT			

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15	AF16	AF17	AF18
PE2	TRACECK	TIMER23_CH0	SAI0_CLK0		EXMC_A2	SPI3_SCK	SAI0_MCLK0	HDSL_SEL1	SAI2_MCLK0	OSPIM_P0_IO2	SAI2_CLK0	ENET0_MII_TXD3	EXMC_A23	TIMER7_CH0BRKIN	SAI3_CLK0	EVENTOUT	SAI3_MCLK0		
PE3	TRACED0	TIMER23_CH1	SPI4_MISO		TIMER14_BRKIN0	SPI3_SCK	SAI0_SD1	HDSL_CLK1	SAI2_SD1		EXMC_NBL3	EXMC_A3	EXMC_A19	DCI_PIXCLK	SAI3_SD1	EVENTOUT			
PE4	TRACED1	TIMER0_BRKIN1	SAI0_DAT1	HPDF_DATAIN3	TIMER14_MCH0	SPI3_NSS	SAI0_FS0	HDSL_CLK2	SAI2_FS0		SAI2_DAT1	EXMC_A4	EXMC_A20	DCI_D4	TLI_B0	EVENTOUT	SAI3_FS0	SAI3_DAT1	HDSL_LINK
PE5	TRACED2	TIMER40_BRKIN0	SAI0_CLK1	HPDF_CKIN3	TIMER14_CH0	SPI3_MISO	SAI0_SCK0	HDSL_MISO1	SAI2_SCK0		SAI2_CLK1	EXMC_A5	EXMC_A21	DCI_D6	TLI_G0	EVENTOUT	SAI3_SCK0	SAI3_CLK1	HDSL_SMPL
PE6	TRACED3	TIMER0_BRKIN2	SAI0_DAT0		TIMER14_CH1	SPI3_MOSI	SAI0_SD0	HDSL_MOSI1	SAI2_SD0	SAI2_DAT0	SAI1_MCLK1	CMP_MUX_OUT3	EXMC_A22	DCI_D7	TLI_G1	EVENTOUT	SAI3_SD0	SAI3_DAT0	
PE7	TIMER1_CH0/TIMER1_ETI	TIMER0_ETI	TIMER4_CH0	HPDF_DATAIN2	TIMER7_ETI	SPI4_MOSI	TIMER14_BRKIN0	UART6_RX	USBHS1_ULPI_STP		OSPIM_P0_IO4	EDIM_DO_GROUP0	EXMC_D4			EVENTOUT			
PE8	TIMER1_CH1	TIMER0_MCH0	TIMER4_CH1	HPDF_CKIN2			TIMER14_MCH0	UART6_TX	USBHS1_ULPI_NXT		OSPIM_P0_IO5	EDIM_DI_GROUP0	EXMC_D5	CMP1_OUT		EVENTOUT		ENET0_MII_RXD0/ENET0_RMII_RXD0	
PE9	TIMER1_CH2	TIMER0_CH0	TIMER4_CH2	HPDF_CKOUT		SPI3_IO2	TIMER14_CH0	UART6_RTS/UART6_DE			OSPIM_P0_IO6		EXMC_D6			EVENTOUT		ENET0_MII_RXD1/ENET0_RMII_RXD1	
PE10	TIMER1_CH3	TIMER0_MCH1	TIMER4_CH3	HPDF_DATAIN4		SPI3_IO3	TIMER14_CH1	UART6_CTS			OSPIM_P0_IO7		EXMC_D7			EVENTOUT		ENET0_MII_RXD2	
PE11		TIMER0_CH1	TIMER4_ETI	HPDF_CKIN4		SPI3_NSS					SAI1_SD1	OSPIM_P0_CSN	EXMC_D8		TLI_G3	EVENTOUT		ENET0_MII_RXD3	
PE12	TIMER1_CH0/TIMER1_ETI	TIMER0_MCH2		HPDF_DATAIN5	TIMER7_MCH0	SPI3_SCK					SAI1_SCK1		EXMC_D9	CMP0_OUT	TLI_B4	EVENTOUT		ENET0_MII_RX_CLK/ENET0_RMII_REF_CLK	

Table 2-9. Port F alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PF0		SPI3_MISO			I2C1_SDA	USBHS0_ULPI_D4	TIMER41_CH0	HDSL_SEL2		OSPIM_P1_IO0	SAI1_SD0		EXMC_A0	TIMER22_CH0		EVENTOUT
PF1		SPI3_MOSI			I2C1_SCL	USBHS0_ULPI_D5	TIMER41_MCH0	HDSL_MISO2		OSPIM_P1_IO1	SAI2_SCK0		EXMC_A1	TIMER22_CH1		EVENTOUT
PF2				ENET0_MDIO	I2C1_SMBA	USBHS0_ULPI_D6		HDSL_MOSI2		OSPIM_P1_IO2	SPI0_NSS/I2S0_WS	EXMC_D23	EXMC_A2	TIMER22_CH2	ENET1_MDIO	EVENTOUT
PF3				ENET0_MDC	USART0_RX					OSPIM_P1_IO3		EXMC_D22	EXMC_A3	TIMER22_CH3	ENET1_MDC	EVENTOUT
PF4		TIMER0_MCH1		TIMER7_MCH1	USART0_TX	OSPIM_P1_nSCK	HPDF_DATAIN2	USART2_RTS/USART2_DE	UART3_RTS/UART3_DE	OSPIM_P1_SCK	SDIO1_D0	EXMC_D21	EXMC_A4	TRIGSEL_OUT1	TLI_PIXCLK	EVENTOUT
PF5		TIMER0_MCH2		TIMER7_MCH2	USART0_RX		HPDF_CKIN2		UART3_CTS	OSPIM_P1_nSCK	SDIO1_D1		EXMC_A5	TRIGSEL_OUT5	TLI_G7	EVENTOUT
PF6		TIMER15_CH0	CAN2_RX		SAI3_SD1	SPI4_NSS	SAI0_SD1	UART6_RX	SAI2_SD1		OSPIM_P0_IO3		EXMC_D24	TIMER22_CH0	EXMC_A6	EVENTOUT
PF7		TIMER16_CH0	CAN2_TX		OSPIM_P1_IO0	SPI4_SCK	SAI0_MCLK1	UART6_TX	SAI2_MCLK1	SAI3_MCLK1	OSPIM_P0_IO2	EXMC_A4	EXMC_D25	TIMER22_CH1		EVENTOUT
PF8		TIMER15_MCH0			OSPIM_P1_IO1	SPI4_MISO	SAI0_SCK1	UART6_RTS/UART6_DE	SAI2_SCK1	SAI3_SCK1	OSPIM_P0_IO0		EXMC_D26	TIMER22_CH2		EVENTOUT
PF9	ENET0_PPS_OUT	TIMER16_MCH0				SPI4_MOSI	SAI0_FS1	UART6_CTS	SAI2_FS1	SAI3_FS1	OSPIM_P0_IO1		EXMC_D27	TIMER22_CH3		EVENTOUT
PF10	ENET1_PPS_OUT	TIMER15_BRKIN0	SAI0_DAT2		DCI_D15			SAI3_SD0	OSPIM_P0_nSCK	OSPIM_P0_SCK	SAI2_DAT2	SAI3_DAT2		DCI_D11	TLI_DE	EVENTOUT
PF11		ENET0_MII_TXD0/ENET0_RMII_TXD0				SPI4_MOSI				OSPIM_P0_nSCK	SAI1_SD1		EXMC_SDNRAS	DCI_D12	TIMER23_CH0	EVENTOUT
PF12		ENET0_MII_TXD1/ENET0_RMII_TXD1						SAI3_SD1		OSPIM_P1_DQS		EXMC_D24	EXMC_A6		TIMER23_CH1	EVENTOUT
PF13		ENET0_MII_TXD2		HPDF_DATAIN6	I2C3_SMBA								EXMC_A7		TIMER23_CH2	EVENTOUT
PF14		ENET0_MII_TXD3		HPDF_CKIN6	I2C3_SCL	SPI4_IO2	TIMER31_CH2						EXMC_A8		TIMER23_CH3	EVENTOUT

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PF15		ENET0_MII_TX_CLK			I2C3_SDA	SPI4_IO3	TIMER31_CH3						EXMC_A9			EVENTOUT

Table 2-10. Port G alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PG0				TIMER0_CH2	TIMER31_CH0					OSPIM_P1_IO4			EXMC_A10		ENET1_MII_COL	EVENTOUT
PG1				TIMER0_MCH2	TIMER31_CH1				USBHS1_ULPI_D3	OSPIM_P1_IO5	TLI_G2		EXMC_A11		ENET1_MII_CRS	EVENTOUT
PG2	EXMC_D6	TIMER0_BRKIN1		TIMER7_BRKIN0	TIMER31_CH2	SPI1_MISO			USBHS1_ULPI_D4	ENET1_MII_TX_EN/ENET1_RMII_TX_EN	TLI_G3	CMP_MUX_OUT5	EXMC_A12		TIMER23_ETI	EVENTOUT
PG3	EXMC_D7			TIMER7_BRKIN2	TIMER31_CH3	SPI1_MOSI/I2S1_SD			USBHS1_ULPI_D5	ENET1_MII_TXD0/ENET1_RMII_TXD0		CMP_MUX_OUT6	EXMC_A13	TIMER22_ETI		EVENTOUT
PG4	EXMC_D8	TIMER0_BRKIN2	TIMER42_BRKIN0	TIMER7_BRKIN1	TIMER31_ETI	SPI1_SCK/I2S1_CK			USBHS1_ULPI_D6	ENET1_MII_TXD1/ENET1_RMII_TXD1		CMP_MUX_OUT7	EXMC_A14			EVENTOUT
PG5	EXMC_D9	TIMER0_ETI	TIMER42_MCH0		TIMER30_CH0	SPI1_NSS/I2S1_WS			USBHS1_ULPI_D7	ENET1_MII_TXD2			EXMC_A15			EVENTOUT
PG6		TIMER16_BRKIN0	TIMER42_CH0		TIMER30_CH1	HPDF_DATAIN0	ENET1_MDC		USBHS1_ULPI_D4	ENET1_MII_TXD3	OSPIM_P0_CSN	TLI_G4	EXMC_NE2	DCI_D12	TLI_R7	EVENTOUT
PG7		EXMC_D28	TIMER43_MCH0		TIMER30_CH2	HPDF_CKIN0	SAI0_MCLK0	USART5_CK	USBHS1_ULPI_D5	OSPIM_P1_DQS		EXMC_D2	EXMC_INT	DCI_D13	TLI_PIXCLK	EVENTOUT
PG8		EDIM_TCLK_GROUP0	TIMER43_CH0	TIMER7_ETI	TIMER30_CH3	SPI5_NSS/I2S5_WS	ENET1_PPS_OUT	USART5_RTS/USART5_DE	RSPDIF_CH2		USBHS1_ULPI_D2	ENET0_PPS_OUT	EXMC_SDCLK	EXMC_D3	TLI_G7	EVENTOUT
PG9		EXMC_D30	CAN2_TX	TIMER7_BRKIN1	TIMER30_ETI	SPI0_MISO	ENET1_MII_TX_CLK	USART5_RX	RSPDIF_CH3	OSPIM_P0_IO6	SAI1_FS1	SDIO1_D0	EXMC_NE1	DCI_VSYNC		EVENTOUT
PG10		EXMC_D31	CAN2_RX	OSPIM_P1_IO6		SPI0_NSS/I2S0_WS				TLI_G3	SAI1_SD1	SDIO1_D1	EXMC_NE2	DCI_D2	TLI_B2	EVENTOUT
PG11			EXMC_D29			SPI0_SCK/I2S0_CK	ENET1_MII_TX_EN/ENET1_RMII_TX_EN		RSPDIF_CH0	OSPIM_P1_IO7	SDIO1_D2	ENET0_MII_TX_EN/ENET0_RMII_TX_EN		DCI_D3	TLI_B3	EVENTOUT

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PG12		TLI_G5	ENET0_MII_TXD2	OSPIM_P1_CSN		SPI5_MISO	ENET1_MII_TXD2	USART5_RTS/USART5_DE	RSPDIF_CH1	TLI_B4	SDIO1_D3	ENET0_MII_TXD1/ENET0_RMII_TXD1	EXMC_NE3	TIMER22_CH0	TLI_B1	EVENTOUT
PG13	TRACED0					SPI5_SCK/I2S5_CK	ENET1_MII_TXD0/ENET1_RMII_TXD0	USART5_CTS	TIMER44_CH0		SDIO1_D6	ENET0_MII_TXD0/ENET0_RMII_TXD0	EXMC_A24	TIMER22_CH1	TLI_R0	EVENTOUT
PG14	TRACED1					SPI5_MOSI/I2S5_SD	ENET1_MII_TXD1/ENET1_RMII_TXD1	USART5_TX	TIMER44_MCH0	OSPIM_P0_IO7	SDIO1_D7	ENET0_MII_TXD1/ENET0_RMII_TXD1	EXMC_A25	TIMER22_CH2	TLI_B0	EVENTOUT
PG15						SPI0_NSS/I2S0_WS	ENET1_MII_TXD3	USART5_CTS	TIMER44_BRKIN0	OSPIM_P1_DQS		EXMC_NE3	EXMC_SDNCAS	DCI_D13		EVENTOUT

Table 2-11. Port H alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PH0-OSCIN																EVENTOUT
PH1-OSCOUT																EVENTOUT
PH2		USART2_TX						TIMER40_CH0	USBHS1_ULPI_STP	OSPIM_P0_IO4	SAI1_SCK1	ENET0_MII_CRS	EXMC_SDCKE0		TLI_R0	EVENTOUT
PH3							EXMC_SDCLK	TIMER40_MCH0	USBHS1_ULPI_DIR	OSPIM_P0_IO5	SAI1_MCLK1	ENET0_MII_COL	EXMC_SDNE0	TLI_G3	TLI_R1	EVENTOUT
PH4		USART2_RX			I2C1_SCL			TIMER40_BRKIN0	USBHS1_ULPI_NXT	TLI_G5	USBHS0_ULPI_NXT		EXMC_NBL3		TLI_G4	EVENTOUT
PH5					I2C1_SDA	SPI4_NSS		TIMER41_CH0	USBHS1_ULPI_CK		USBHS0_ULPI_D0		EXMC_SDNWE			EVENTOUT
PH7		TIMER0_MCH0		EDOUT_A	I2C2_SCL	SPI4_MISO	ENET1_MII_RXD3	TIMER41_BRKIN0	USBHS1_ULPI_D1			ENET0_MII_RXD3	EXMC_SDCKE1	DCI_D9	EXMC_NBL1	EVENTOUT
PH13				TIMER7_MCH0			ENET1_MII_COL	TIMER43_BRKIN0	UART3_TX	CAN0_TX	USBHS0_ULPI_D0		EXMC_D21		TLI_G2	EVENTOUT
PH14				TIMER7_MCH1			ENET1_MDIO		UART3_RX	CAN0_RX			EXMC_D22	DCI_D4	TLI_G3	EVENTOUT

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PH15		DCI_HSYNC(1)		TIMER7_MCH2			ENET1_MII_CRS						EXMC_D23	DCI_D11	TLI_G4	EVENTOUT

Note:

(1) This feature only supports input functionality.

(2) For the usage of PA0_C,PA1_C,PC2_C and PC3_C alternate function, please refer to the user manual General-purpose and alternate-function I/Os chapter.

3. Functional description

3.1. Arm® Cortex®-M7 core

The Arm® Cortex®-M7 processor is a highly efficient high-performance, embedded processor that features low interrupt latency, low-cost debug, and has backwards compatibility with existing Cortex-M profile processors. The processor has an in-order super-scalar pipeline that means many instructions can be dual-issued, including load/load and load/store instruction pairs because of multiple memory interfaces. The Cortex-M7 is a high-performance processor, which features a 6-stage superscalar pipeline with branch prediction and an optional FPU capable of single-precision and optionally double-precision operations. The instruction and data buses have been enlarged to 64-bit wide over the previous 32-bit buses.

The interfaces that the processor supports include:

- 64-bit AXI4 interface.
- 32-bit AHB master interface.
- 32-bit AHB slave interface.
- 64-bit instruction TCM interface.
- 2x32-bit data TCM interfaces.

The processor contains the following external interfaces:

- AHBP interface.
- AHBS interface.
- AHBD interface.
- External Private Peripheral Bus.
- ATB interfaces.
- TCM interface.
- Cross Trigger interface.
- MBIST interface.
- AXIM interface.

The Cortex®-M7 processor is based on the ARMv7-M architecture and supports a powerful and scalable instruction set including general data processing I/O control tasks, advanced data processing bit field manipulations, DSP and floating point instructions. Some system peripherals listed below are also provided by Cortex®-M7:

- Nested Vectored Interrupt Controller (NVIC).
- Flash Patch and Breakpoint (FPB).
- Data Watchpoint and Trace (DWT).
- Instrumentation Trace Macrocell (ITM).
- Embedded Trace Macrocell (ETM).
- JTAG or SWD Debug Port.
- Trace Port Interface Unit (TPIU).
- Memory Protection Unit (MPU).

- Floating Point Unit (FPU), double-precision.
- Load Store Unit (LSU).
- Data Processing Unit (DPU).
- Prefetch Unit (PFU).

3.2. On-chip memory

- Up to 2MB of code non-volatile memory (CNVM).
- Up to 7.5MB of extended code non-volatile memory (ECNVM) for instruction and data.
- Up to 512KB of on-chip SRAM (AXI SRAM).
- Up to 256KB of RAM shared by ITCM or DTCM.
- Up to 256KB of RAM shared by ITCM or AXISRAM.
- Up to 128KB of dedicated ITCM
- 16KB of SRAM0 and 16KB of SRAM1
- 4KB of backup SRAM.
- RAM ECC monitor for each Region.

The GD32H77Dxx main NVM consists of: A code non-volatile memory (CNVM) block of up to 2048 KB, it is divided into 32 sectors; A extended code non-volatile memory (ECNVM) block of up to 7680 KB, it is divided into 120 sectors; An information block of 128 KB; A check information block of 32 KB; A special region dedicated to option byte storage, accessible by the application software only through the AHB slave interface.

The devices of GD32H77Dxx series contain up to 512KB of on-chip SRAM (AXI SRAM), and up to 256KB of RAM shared by ITCM or DTCM, 256KB of RAM shared by ITCM or AXISRAM, 128KB of dedicated ITCM, 16KB of SRAM0 and 16KB of SRAM1, 4KB of backup SRAM. All of AHB SRAM support byte, half-word (16 bits), and word (32 bits) accesses. The on-chip SRAM (AXI SRAM) support byte, half-word (16 bits), word (32 bits) and double words (64 bits) accesses. SRAM0 and SRAM1 can be accessed by almost all AHB masters. The backup SRAM (BKPSRAM) is implemented in the backup domain, which can keep its content even when the VDD power supply is down.

Table 2-2. Memory map of GD32H77Dxx devices shows the memory map of the GD32H77Dxx series of devices, including NVM, SRAM, peripheral, and other pre-defined regions.

3.3. Clock, reset and supply management

- Internal 64 MHz factory-trimmed RC and external 4 to 50 MHz crystal oscillator.
- Internal 48 MHz RC oscillator.
- Low power internal 4 MHz RC oscillator.
- Internal 32 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator.
- Integrated system clock PLL.
- 1.71 to 3.6V application supply and I/Os.

- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD).

The Clock Control Unit (CCTL) provides a range of oscillator and clock functions. These include internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AXI, three AHB and four APB domains. The maximum frequency of the system clock can be up to 600 MHz. The maximum frequency of the three AHB domains are 300 MHz. The maximum frequency of the four APB domains including APB1 = APB3 = APB4 is 150 MHz and APB2 is 300 MHz. See *Figure 2-3. GD32H77Dxx clock tree* for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components except for the SW-DP controller and the Backup domain. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from 1.53V and down to 1.48V. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- V_{DD} range: 1.71V to 3.6V, external power supply for I/Os and the internal regulator, RCs and PLL. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} range: 1.71V to 3.6V, external analog power supplies for ADC, reset blocks. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} range: 1.71V to 3.6V, power supply for RTC, external clock 32 KHz oscillator and backup registers (through power switch) when V_{DD} is not present.

3.4. Boot modes

GD32H77Dxx supports four BOOT modes, including:

- USER BOOT
- SECURITY BOOT
- SYSTEM BOOT
- SRAM BOOT

At startup, the boot memory space is selected by the BOOT pin and BOOT_ADDR0/1 in Boot address, allowing to program any boot memory address from 0x0000 0000 to 0x9000 0000.

The boot loader is located in non-user System memory. It is used to reprogram the NVM by using USART0 (PA9 and PA10), USART1 (PA2 and PA3), USART2 (PB10 and PB11), USBHS0 (PA11 and PA12) and SDIO0 (PC12, PD2, PB13, PC9, PC10 and PC11) in device mode. It also can be used to transfer and update the NVM code, the data and the vector table sections.

To ensure system reliability and stability, it is recommended not to connect peripherals that may generate interference signals (such as sensor outputs, watchdog chips, buttons, etc.) to the above-mentioned pins during the hardware design stage, in order to avoid affecting the

normal function of the Bootloader and causing abnormal outputs to the connected peripherals.

Note: When booting from system memory, the USART RX pins (PA3/PA10/ PB11) are in input level detection mode. Therefore, unused USART RX pins (PA3/PA10/ PB11) need to be kept at a stable logic level to prevent false triggering.

3.5. Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are sleep mode, deep-sleep mode, and standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep mode**
  In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt / event can wake up the system.
- **Deep-sleep mode**
  In deep-sleep mode, all clocks in the V_{CORE} domain are off, and all of LPIRC4M, IRC48M, IRC64M, HXTAL and PLLs are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the 16 external lines, the RTC alarm, RTC tamper and timestamp event, LXTAL clock stuck, the VAVD \ LVD \ VOVD \ VUVD, CMP output, LPDTS wakeup, ENET wakeup, RTC wakeup, CAN wakeup, I2C wakeup, USART wakeup and USBHS wakeup. When exiting the deep-sleep mode, the IRC64M is selected as the system clock.
- **Standby mode**
  In standby mode, the whole V_{CORE} domain is power off, the LDO is shut down, and all of IRC48M, LPIRC4M, IRC64M, HXTAL and PLLs are disabled. The contents of SRAM and registers in V_{CORE} power domain are lost. There are five wakeup sources for the standby mode, including the external reset from NRST pin, the RTC, the FWDGT reset, WKUP pins and LCKMD.

3.6. Trigger selection controller (TRIGSEL)

- Supports different optional trigger inputs.
- Trigger input source could be external input signal or output of peripheral.
- Trigger selection output could be for external output or peripheral.

The trigger selection controller (TRIGSEL) allows software to select the trigger input signal for various peripherals. TRIGSEL provides a flexible mechanism for a peripheral to select different trigger inputs. Every output could select from different trigger input signal.

3.7. General-purpose and alternate-function I/Os (GPIO and AFIO)

- Output push-pull/open drain enable control.
- Analog input/output configuration.
- Alternate function input/output configuration.

Each GPIO port has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt/Event Controller Unit (EXTI). The GPIO ports are pin-shared with other alternative functions (Afs) to obtain maximum flexibility on the package pins.

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), input, peripheral alternate function or analog mode. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current capable except for analog mode.

3.8. CRC calculation unit (CRC)

- Supports 8/16/32 bits data input.
- For 7(8)/16/32 bits input data length, the calculation cycles are 1/2/4 AHB clock cycles.
- User configurable polynomial value and size.
- Free 8-bit register is unrelated to calculation and can be used for any other goals by any other peripheral devices.

A cyclic redundancy check (CRC) is an error-detecting code commonly used in digital networks and storage devices to detect accidental changes to raw data. The CRC calculation unit can be used to calculate 7/8/16/32 bits CRC code within user configurable polynomial.

3.9. True random number generator (TRNG)

- LFSR (Linear Feedback Shift Register) mode and NIST (National Institute of Standards and Technology) mode to generate random number.
- About 40 periods of TRNG_CLK are needed between two consecutive random numbers in LFSR mode.
- 32-bit random numbers are generated each time in LFSR mode.
- TRNG NIST mode follows the NIST SP800-90B.
- Support health tests recommended by the NIST SP800-90B.
- 32-bit*4 or 32-bit*8 random numbers are generated each time in NIST mode.
- TRNG has the functions of startup and health tests, associated with specific error flags.

The true random number generator (TRNG) module can generate a 32-bit random value by using continuous analog noise and it has been pre-certified NIST SP800-90B.

3.10. Cryptographic Acceleration Unit (CAU)

- AES encryption / decryption algorithms are supported.
- Multiple modes are supported respectively in AES, including Electronic codebook (ECB), Cipher block chaining (CBC), Counter mode (CTR), Galois / counter mode (GCM), Galois message authentication code mode (GMAC), Counter with CBC-MAC (CCM) , cipher message authentication code mode (CMAC), Cipher Feedback mode (CFB) and Output Feedback mode(OFB).
- DMA transfer for incoming and outgoing data is supported.

AES

- Supports the ECB, CBC, CTR, GCM, GMAC, CCM, CMAC, CFB and OFB chaining algorithms.
- Supports 128-bit, 192-bit and 256-bit keys.
- Four 32-bit initialization vectors (IV) are used in CBC, CTR, GCM, GMAC, CCM, CMAC, CFB and OFB modes.
- 8*32-bit input and output FIFO.
- Multiple data types are supported, including No swapping, Half-word swapping Byte swapping and Bit swapping.
- Data can be transferred by DMA, CPU during interrupts, or without both of them.
- Support to use initial key from OTP by setting KEY_SEL register.

The cryptographic acceleration unit (CAU) is used to encipher and decipher data with AES (128, 192, or 256) algorithms. AES algorithms with different key sizes are supported to perform data encryption and decryption in the CAU in multiple modes. The CAU is a 32-bit peripheral, DMA transfer is supported and data can be accessed in the input and output FIFO.

3.11. Hash Acceleration Unit (HAU)

- Federal Information Processing Standards Publication 180-4(FIPS PUB 180-4).
- Secure Hash Standard specifications (SHA-1, SHA-224, SHA-256).
- Internet Engineering Task Force Request for Comments number 1321 (IETF RFC 1321) specifications (MD5).
- High performance of computation of hash algorithms.
- Automatic data padding to fill the 512-bit message block for digest computation.
- DMA transfer is supported.
- Hash / HMAC process suspended mode.

The hash acceleration unit (HAU) is used for information security. The secure hash algorithm (SHA-1, SHA-224, SHA-256), the message-digest algorithm (MD5) and the keyed-hash message authentication code (HMAC) algorithm are supported for various applications. The digest will be computed and the length is 160 / 224 / 256 / 128 bits for a message up to (264 - 1) bits computed by SHA-1, SHA-224, SHA-256 and MD5 algorithms respectively. In HMAC algorithm, SHA-1, SHA-224, SHA-256 or MD5 will be called twice as hash functions and

authenticating messages can be produced.

3.12. Public Key Cryptographic Acceleration Unit (PKCAU)

- Support RSA/DH algorithms with up to 3136 bits of operands
- Support ECC algorithm with up to 640 bits of operands
- Embedded RAM of 3584 bytes
- Conversion between the Montgomery domain and the natural domain
- Only 32-bit access is supported

Public key encryption is also called asymmetric encryption, asymmetric encryption algorithms use different keys for encryption and decryption. The Public Key Cryptographic Acceleration Unit (PKCAU) can accelerate RSA (Rivest, Shamir and Adleman), Diffie-Hellmann (DH key exchange) and ECC (elliptic curve cryptography) in GF(p) (Galois domain). These operations are performed in the Montgomery domain to improve computational efficiency.

3.13. Direct memory access controller (DMA)

- Two AHB master interface for transferring data, and one AHB slave interface for programming DMA.
- 16 channels (8 for DMA0 and 8 for DMA1) and each channel are configurable.
- Support independent single, 4, 8, 16-beat incrementing burst memory and peripheral transfer.
- Support independent 8, 16, 32-bit memory and peripheral transfer.

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory.

Two AHB master interfaces and eight four-word depth 32-bit width FIFOs are presented in each DMA controller, which achieves a high DMA transmission performance. There are 16 independent channels in the DMA controller (8 for DMA0 and 8 for DMA1). Each channel is assigned a specific or multiple target peripheral devices for memory access request management. Two arbiters respectively for memory and peripheral are implemented inside to handle the priority among DMA requests.

3.14. Master direct memory access controller (MDMA)

- 16 channels, each channel supports software triggering and requests can be selected among any request source.
- Support independent single, 2, 4, 8, 16, 32, 64, 128-beat incrementing burst source and destination transfer.
- Support three transfer modes:

- Read from memory and write to memory (software triggered).
- Read from peripheral and write to memory (or memory mapped peripherals).
- Read from memory (or memory mapped peripherals) and write to peripheral.

- Automatic pack / unpack of data to optimize bandwidth when the data width of the source and destination are different.
- 34 hardware trigger sources, all channels can be connected to any hardware trigger source.
- Two FIFOs of 16 double word depth to maximize data bandwidth and bus utilization.

The master direct memory access (MDMA) controller provides a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby increasing system performance by off-loading the CPU from copying large amounts of data and avoiding frequent interrupts to serve peripherals needing more data or having available data. MDMA can be used in combination with a DMA controller (DMA0 or DMA1) to provide up to 16 channels. Each channel request can be selected among any request source. The built-in arbiter is used to handle priority among MDMA requests.

3.15. DMA request multiplexer (DMAMUX)

- 16 channels for DMAMUX request multiplexer.
- 8 channels for DMAMUX request generator.
- Support 59 trigger inputs and 51 synchronization inputs.

DMAMUX is a transmission scheduler for DMA requests. The DMAMUX request multiplexer is used for routing a DMA request line between the peripherals / generated DMA request (from the DMAMUX request generator) and the DMA controller. Each DMAMUX request multiplexer channel selects a unique DMA request line, unconditionally or synchronously with events from its DMAMUX synchronization inputs. The DMA request is pending until it is served by the DMA controller which generates a DMA acknowledge signal (the DMA request signal is de-asserted).

3.16. Fast Fourier Transform (FFT)

- Support 1024 / 512 / 256 / 128 / 64 / 32 points FFT.
- Support IFFT mode.
- IEEE-754 single precision float point complex number input and output data.
- DMA master to load and store data.
- Support window function configured in memory.
- Support input down sample.

The Fast Fourier Transform (FFT) is an efficient computation of the Discrete Fourier Transform (DFT). The module supports CPU to offload FFT operations. Compared to a software implementation, it can accelerate calculations and time critical tasks. The module supports 6 configuration FFT point number up to 1024, and input and output data should be IEEE-754 single precision float point complex number.

3.17. Analog to digital converter (ADC)

- High performance.
  - ADC sampling resolution: ADC0 and ADC1, 14-bit,12-bit, 10-bit or 8-bit configurable resolution. ADC2, 12-bit, 10-bit, 8-bit or 6-bit configurable resolution.
  - Programmable sampling time.
  - Data storage mode: the most significant bit and the least significant bit
  - DMA support.
- Analog input channels.
  - 20 external analog inputs in ADC0, 18 external analog inputs in ADC1, 17 external analog inputs in ADC2.
  - Internal temperature sensor (V_{SENSE}).
  - Internal reference voltage (V_{REFINT}).
  - External battery power supply pin (V_{BAT}).
  - Internal high-precision temperature sensor (V_{SENSE2}).
  - Connection to DAC internal channels.
- Start-of-conversion can be initiated.
  - By software.
  - By TRIGSEL.
- Operation modes.
  - Converts a single channel or scans a sequence of channels.
  - Single operation mode converts selected inputs once per trigger.
  - Continuous operation mode converts selected inputs continuously.
  - Discontinuous operation mode.
  - SYNC mode (the device with two ADCs).
- Conversion result threshold monitor function: analog watchdog.
- Interrupt generation.
  - At the end of routine / inserted conversions.
  - Analog watchdog event.
  - Overflow event.
- Oversampler.
  - 32-bit data register in ADC0 and ADC1, 16-bit data register in ADC2.
  - In ADC0 and ADC1, Oversampling ratio arbitrarily adjustable from 2x to 1024x, In ADC2, Oversampling ratio arbitrarily adjustable from 2x to 256x.
  - In ADC0 and ADC1, Programmable data shift up to 11-bit, In ADC2, Programmable data shift up to 8-bit.
- Channel input range: V_{REFN} <=V_{IN} <=V_{REFP}.
- Data can be routed to HPDF for post processing.

A 12 / 14-bit successive approximation analog-to-digital converter module(ADC) is integrated on the MCU chip. ADC0 has 20 external channels, 2 internal channel(DAC0_OUT0 channel, VREFINT inputs channel), ADC1 has 18 external channels, 3 internal channels(the battery voltage, VREFINT inputs channel and DAC0_OUT1 channel), ADC2 has 17 external channels, 3 internal channels(the battery voltage, temperature sensor and high-precision

temperature sensor). After sampling and conversion, the conversion results can be stored in the corresponding data registers according to the least significant bit(LSB) alignment or the most significant(MSB) bit alignment(ADC0 / 1 are 32-bit data register, ADC2 is 16-bit data register). An on-chip hardware oversample scheme improves performances and reduces the computational burden of MCU.

3.18. Digital to analog converter (DAC)

- 8-bit or 12-bit resolution. Left or right data alignment.
- Conversion update synchronously.
- Conversion triggerd by external triggers.
- Input voltage reference, V_{REFP}.
- Output buffer calibration.
- Using sample and keep mode to reduce the power consumption.
- Noise wave generation (LFSR noise mode and Triangle noise mode).
- Two DAC channels in concurrent mode.

The Digital-to-analog converter converts 12-bit digital data to a voltage on the external pins. The digital data can be set to 8-bit or 12-bit mode, left-aligned or right-aligned mode. DMA can be used to update the digital data on external triggers. The output voltage can be optionally buffered for higher drive capability, and DAC output buffer can be calibrated to improve output accuracy. The sample and keep mode can reduce the power consumption of DAC.

3.19. Real time clock (RTC) and backup registers

- Support calendar function, which can support year, month, date, day, hours, minutes, seconds and subseconds (date is the day of week and day is the day of month).
- Daylight saving compensation supported, which is realized through software.
- External high-accurate low frequency (50Hz or 60Hz) clock used to achieve higher calendar accuracy performed by reference clock detection option function.
- Atomic clock adjust (max adjust accuracy is 0.95PPM) for calendar calibration performed by digital calibration function.
- Sub-second adjustment by shift function.

The RTC provides a time which includes hour/minute/second/sub-second and a calendar includes year/month/day/week day. The time and calendar are expressed in BCD code except sub-second. Sub-second is expressed in binary code. Hour adjust for daylight saving time.

The RTC is an independent timer which provides a set of continuously running counters in backup registers to provide a real calendar function, and provides an alarm interrupt or an expected interrupt. It is not reset by a system or power reset, or when the device wakes up from standby mode. A prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 KHz from external crystal oscillator.

3.20. Timers and PWM generation

- Two 16-bit Advanced timer (TIMER0 & TIMER7), four16-bit General-L0 timers (TIMER2, TIMER3, TIMER30, TIMER31), four 32-bit General-L0 timers (TIMER1, TIMER4, TIMER22, TIMER23), six 16-bit General-L3 timers (TIMER14, TIMER40, TIMER41, TIMER42, TIMER43, TIMER44), two16-bit General-L4 timers (TIMER15, TIMER16), two 32-bit Basic timer (TIMER5 & TIMER6) and two 64-bit Basic timer (TIMER50 & TIMER51).
- Up to 70 independent channels of PWM, output compare or input capture for each general timer and external trigger input.
- 16-bit, motor control PWM advanced timer with programmable dead-time generation for output match.
- Encoder interface controller with two inputs using quadrature decoder and decoder mode.
- 24-bit SysTick timer down counter.
- 2 watchdog timers (free watchdog timer and window watchdog timer).

The advanced timer (TIMER0 & TIMER7) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general timer. The 8 independent channels can be used for input capture, output compare, PWM generation (edge-aligned or center-aligned counting modes) and single pulse mode output. If configured as a general 16-bit timer, it has the same functions as the TIMERx timer. It can be synchronized with external signals or to interconnect with other general timers together which have the same architecture and features.

The general level 0 timer, can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TIMER1/4/22/23 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TIMER2/3/30/31 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. The general level 0 timer also supports an encoder interface with two inputs using quadrature decoder mode and decoder mode.

The general level3 timer module (TIMER14/40/41/42/43/44) is a three-channel timer that supports both input capture and output compare. They can generate PWM signals to control motor or be used for power management applications. The general level3 timer has a 16-bit counter that can be used as an unsigned counter.

The general level4 timer module (TIMER15/16) is a two-channel timer that supports both input capture and output compare. They can generate PWM signals to control motor or be used for power management applications. The general level4 timer has a 16-bit counter that can be used as an unsigned counter.

The basic timer module(TIMER5/6/50/51) has a 32-bit or 64-bit counter that can be used as an unsigned counter. The basic timer can be configured to generate a DMA request and a TRGO0 to connect to DAC.

The GD32H77Dxx have two watchdog peripherals, free watchdog timer and window watchdog timer. They offer a combination of high safety level, flexibility of use and timing

accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-bit prescaler. It is clocked from an independent 32 KHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog timer is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wakeup interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter.
- Auto reload capability.
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source.

3.21. Universal synchronous/asynchronous receiver transmitter (USART/UART)

- Programmable baud-rate generator allowing speed up to 37.5 Mbits/s when the clock frequency is 300 MHz and oversampling is by 8.
- Supports both asynchronous and clocked synchronous serial communication modes.
- IrDA SIR encoder and decoder support.
- LIN break generation and detection.
- ISO 7816-3 compliant smart card interface.

The USART (USART0, USART1, USART2, USART5) and UART (UART3, UART4, UART6, UART7) are used to transfer data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART/UART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART/UART transmitter and receiver.

3.22. Inter-integrated circuit (I2C)

- Up to four I2C bus interfaces can support both master and slave mode with a frequency up to 1 MHz (Fast mode plus).
- Provide arbitration function, optional PEC (packet error checking) generation and checking.
- Supports 7-bit and 10-bit addressing mode and general call addressing mode.

- SMBus 3.0 and PMBus 1.3 compatible.
- Wakeup from sleep mode and Deep-sleep mode on I2C address match.

The I2C (inter-integrated circuit) module provides an I2C interface which is an industry standard two-line serial interface for MCU to communicate with external I2C interface. I2C bus uses two serial lines: a serial data line, SDA, and a serial clock line, SCL. The I2C interface implements standard I2C protocol with standard mode (up to 100KHz), fast mode (up to 400KHz) and fast mode plus (up to 1MHz) as well as CRC calculation and checking, SMBus (system management bus), and PMBus (power management bus).

3.23. Serial peripheral interface (SPI)

- Master or slave operation with full-duplex, half-duplex or simplex mode.
- Separate transmit and receive 32-bit FIFO.
- Data frame size can be 4 to 32 bits.
- Hardware CRC calculation, transmission and checking.
- SPI TI mode supported.
- Multi-master or multi-slave mode function.
- Protect configurations and settings.
- Adjustable main device receiver sampling time.
- Configurable FIFO thresholds (data packing).
- Quad-SPI configuration available in master mode (in SPI3 / 4).

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). Both SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking. Quad-SPI master mode is also supported in SPI3 and SPI4.

3.24. Inter-IC sound (I2S)

- Master or slave operation for transmission/reception.
- Four I2S standards supported: Philips, MSB justified, LSB justified and PCM standard.
- Data length can be 16 bits, 24 bits or 32 bits.
- Channel length can be 16 bits or 32 bits.
- Transmission and reception use a 32 bits wide buffer.
- Audio sample frequency can be 8 kHz to 192 kHz using I2S clock divider.
- Programmable idle state clock polarity.
- Separate transmit and receive 32-bit FIFO.

The Inter-IC sound (I2S) bus provides a standard communication interface for digital audio applications by 4-wire serial lines. GD32H77Dxx contain an I2S-bus interface that can be operated with 16/32 bit resolution in master or slave mode The audio sampling frequencies from 8 KHz to 192 KHz is supported.

3.25. OSPI I/O manager(OSPIM)

- Supports two OSPI (single-line, two-lines, four-lines, eight-lines) interfaces.
- Support two ports for pin assignment.
- Fully programmable IO matrix, can assign pins according to function.

OSPIM supports OSPI pin assignment with full matrix.

3.26. Octal-SPI interface(OSPI)

- Three functional modes:
  - indirect mode: all operations are performed depends on OSPI registers.
  - status polling mode: the values of status registers in external memory are periodically read and check.
  - memory-mapped mode: the external memory is mapped to the microcontroller address space(OSPI0: 0x9000 0000 - 0x9FFF FFFF, OSPI1: 0x7000 0000 - 0x7FFF FFFF) and is accessed as an internal memory.
- Support read and write in memory-mapped mode.
- Support single, dual, quad, dual-quad and octal communication.
- Support DQS.
- Fully programmable command format for both indirect and memory-mapped mode.
- Support SDR(signal data rate) and DTR(double transfer rate).
- Support two frame format:
  - the standard frame format.
  - HyperBus™ frame format.
- Support wrap for both standard frame format and HyperBus™ frame format.
- Integrated FIFO for transmission/reception.
- 8, 16 and 32-bits data access.
- MDMA channel for indirect mode.
- Interrupt generation on FIFO threshold, status match, transfer complete and access error.

The OSPI is a specialized interface that communicate with external memories such as serial PSRAMS, serial NAND, serial NOR Flash, HypterRAMTM and HypterFlashTM memories. The interface support single, dual, quad, dual-quad and octal SPI mode.

3.27. Clock phase delay module (CPDM)

- Supports the input clock frequency ranges: 25 MHz ~ 208MHz.
- Supports up to 12 output clock phase selections.

The Clock Phase Delay Module (CPDM) is used to delay the phase of the input clock and then output the clock. When used, the application needs to first program the phase of the output clock, and then use the output clock in other peripherals to receive data.

Phase delay is related to voltage and temperature and may require reconfiguration of the application and redetermination of the phase relationship between the output clock and the received data as parameters change.

3.28. Digital camera interface (DCI)

- Digital video/picture capture.
- 8/10/12/14 data width supported.
- High transfer efficiency with DMA interface.
- Video/picture crop supported.
- Various pixel digital encoding formats supported including YcbCr422 / RGB565 / YUV420 / Bayer.
- Hard/embedded synchronous signals supported.
- Support for CCIR656 video interface as well as traditional sensor interface.

DCI is an 8-bit to 14-bit parallel interface that able to capture video or picture from a camera via Digital Camera Interface. It supports 8/10/12/14 bits data width through DMA operation.

DCI supports various color space such as YUV/RGB, as well as compression format such as JPEG. Support CCIR656 video decoder formats and perform additional processing of the image.

3.29. General parallel slave interface (GPSI)

- Supported 8/16-bit parallel data input or output.
- 32-byte FIFO.
- Supported slave mode.
- Alternate function input of data enable(GPSI_DE).
- Alternate function output of ready(GPSI_RDY).

The GPSI is a general synchronous input/output slave interface for 8/16-bit parallel data. When the data is valid, it sends a data valid signal by the transmitter. If the receiver is ready to sample the data, it will give a flow control signal. The GPSI shared same functions, GPIO and interrupt vector with DCI(Digital camera interface), so two peripherals cannot be used at the same time.

3.30. TFT LCD interface (TLI)

- Supports up to 24 bits data output per pixel
- Supports up to 2048 x 2048 resolution
- Timing parameters is fully programmable
- Built-in DMA engine to handle frame data copy
- 2 separate frame layers with window and blending function
- Support various pixel formats: ARGB8888, RGB888, RGB565, etc

- Support CLUT (Color Look-Up-Table) and Color-Keying format
- Dithering operation to low bits of a pixel
- AXI master interface with burst of 16 double-words
- 2 display layers with dedicated FIFO (64x64-bit)

The TLI (TFT-LCD Interface) module handles the synchronous LCD interface and provides pixel data, clock and timing signals for passive LCD display. It supports a wide variety of displays with fully programmable timing parameters. A built-in DMA engine continuously move data from system memory to TLI and then, output to an external LCD display. Two separate layers are supported in TLI, as well as layer window and blending function.

3.31. DSI host controller (DSI)

DSI controller:

- Compliant with DSI MIPI specification for Display Serial Interface (Version1.3.1).
- Compliant with D-PHY standard MIPI specification (Version1.2).
- Compliant with MIPI Alliance Standard for Display Pixel Interface (DPI-2) Version 2.00.
- Compliance with MIPI Alliance Standard for Display Command Set Version 1.3.
- Supports Display resolutions - QCIF(resolution 176x144 pixels or 144x176 pixels), QVGA(resolution 320x240 pixels or 240x320 pixels), VGA(resolution 640x480 pixels or 480x640 pixels), WVGA(resolution 800x480 pixels or 480x800 pixels), XVGA(1024x768 pixels).
- Can be programmed to support either video mode or command mode in single channel mode.
- Supports generic read and write commands.
- Supports pixel formats of type 16bpp [RGB565], 18bpp [RGB666], 18bpp [Loosely packed RGB666] and 24bpp [RGB888].
- Supports recovery due to contention.
- Supports timers and recovery schemes to come out of mode fault errors.
- Has watchdog timers to monitor D-PHY activity at low power mode, high speed mode and during turn-around.
- Supports interrupt to report protocol errors and expiry of timers.
- Supports programmable device initialization timers.
- Supports programmable maximum return packet size command.
- Supports DPI interface signals with different polarities.
- Supports PHY data lane programmability up-to two.
- Supports DPI interface for pixel stream transfer.
- Supports data lane switching to low power mode during idle time
- Supports tearing effect.
- Supports ultra low power mode switching.
- Supports Bus turn around.
- Supports EOT disabling capacity to suit backward compatible Displays.
- Supports Clock stop enabling feature during idle time.
- Supports burst, non-burst video modes with sync pulse and sync events types.

- Added support for deskew calibration.

DPHY:

- Supports synchronous transfer at high speed mode with a bit rate of 80-1500 Mb/s without deskew calibration and upto 2000 Mb/s with deskew calibration.
- Supports asynchronous transfer at low power mode with a bit rate of 10 Mb/s.
- Spaced one hot encoding for Low power [LP] data.
- Supports one clock lane and two data lanes.
- Supports error detection mechanism for sequence errors and contentions.
- Data lanes support transfer of data in high speed mode.
- Supports ultra-low power mode, high speed mode and control mode.
- Has clock divider unit to generate clock for parallel data reception from the PPI.
- Supports 8-bit data PPI to be interoperable with DSI protocol.
- Optional TxClkEsc divide by 2 support.
- Clock lane supports unidirectional communication.
- On-chip clock generation is configurable for the transmitter.
- PHY can be configured only as a master.
- Core is structured to increase the number of data lanes.
- Supports High speed mode in Forward communication.
- Support for Stuck-At Scan and at speed BIST for Digital and Analog.

The Display Serial Interface (DSI) is a component of a suite of communication protocols established by the MIPI® Alliance. The MIPI® DSI Host Controller is a digital module that encompasses the full range of protocol functionalities as outlined in the MIPI® DSI Specification. This controller facilitates a connection between the system and the MIPI® D-PHY, enabling users to interact with displays that adhere to the DSI standards.

3.32. Receiver of Sony/Philips Digital Interface (RSPDIF)

- Supports audio IEC-60958 and IEC-61937.
- Up to 4 inputs available.
- Supports maximum symbol rate: 12.288 MHz.
- Supports stereo stream from 8 to 192 kHz.
- Supports automatic symbol rate detection.
- Generate symbol clock.
- Check the parity bit of the received data.
- Support multiple data processing methods, which can process audio data and user channel information separately or together.
- Supports using DMA communication to receive audio data and user channel information respectively.

The receiver of Sony/Philips Digital Interface (RSPDIF) module provides the function of receiving and decoding SPDIF audio data streams.

3.33. Serial Audio Interface (SAI)

- Two independent audio sub-blocks.
- Each audio sub-block can be configured as any of the master/slave and transmitter/receiver combination with 8-word FIFO.
- Local clock divider logic to satisfy the various audio sampling rates.
- Flexible audio protocol configuration such as I2S, PCM/DSP, AC'97, LSB or MSB-justified and TDM.
- PDM interface, supporting up to 3 microphone pairs.
- Mono/Stereo audio capability with mute option.
- Frame Synchronization configuration (active level, active length and offset).
- Each audio frame contains up to 16 configurable slots.
- Slot length is flexible, and can be configured as active or inactive.
- Each slot can hold a data of size 8-, 10-, 16-, 20-, 24-, and 32-bits with configurable first bit offset, and configurable LSB or MSB data transfer.
- Two independent DMA interface for each audio sub-block. Support slave mode with a frequency up to 4MHz.

The Serial Audio Interface (SAI) is designed to target a wide range of commonly used audio protocols, both in mono and stereo modes, such as I2S, PCM/DSP, AC'97, LSB or MSB-justified and TDM. SPDIF output is offered when the audio block is configured as a transmitter. The SAI can be configured to any of the master/slave and transmitter/receiver combination, full/half-duplex operating mode depends on synchronous/asynchronous configuration of the audio sub-blocks.

3.34. Image processing accelerator (IPA)

- One AXI master interface for memory access
- One AHB slave interface for IPA configuration with 8-bit, 16-bit, 32-bit
- Three four-doubleword depth 64-bit FIFOs independently for the source and destination images
- Support four pixel-format-convert modes
  - Copy one source image to the destination image
  - Convert one source image to the destination image with specific pixel format
  - Convert and blend two source images to the destination image with specific pixel format
  - Fill up the destination image with a specific color
- Support configurable LUT size independently for two source images
- Support two LUT pixel formats separately for two source images
- Support LUT automatically loading for two source images
- Support transfer hang up and stop
- Support pixel offset per line independently for the source and destination images
- Support pre-defined pixel channel value independently for the source and destination

images

- Support three alpha channel value calculation algorithms separately for two source images
- Support 18 pixel formats for foreground image
- Support 11 pixel formats for background image
- Support 7 pixel formats for the destination image
- Support configurable image size
- Support automatically AXI bandwidth adjustment with an internal timer
- Support one interrupt with six types of event flags
- Support interrupt enable and clear
- Support decimal scaling and bilinear scaling
- Support image rotation (0, 90, 180, 270 degrees)
- Support interlace input for the foreground image

The IPA provides a configurable and flexible image format conversion from one or two source image to the destination image. 18 pixel formats for foreground from 4-bit up to 32-bit per pixel, 11 pixel formats for background from 4-bit up to 32-bit per pixel, and 7 pixel formats from 16-bit up to 32-bit per pixel for the destination image are supported. Two 256*32 bits LUTs (Look-Up Table) separately for the two source images are implemented for the indirect pixel formats.

3.35. Secure digital input and output card interface (SDIO)

- ***e*•MMC:** Support for embedded Multimedia Card System Specification Version 4.51 (and previous versions) Card and five different data bus modes: 1-bit (default), 4-bit (SDR/DDR) and 8-bit(SDR/DDR).
- **SD Card:** Full support for SD Memory Card Specifications Version 3.0.
- **SD I/O:** Full support for SD I/O Card Specification Version 3.0 card and three different data bus modes: 1-bit (default) and 4-bit (SDR/DDR).
- 208MHz data transfer frequency and 8-bit data transfer mode.
- Support DDR and max clock frequency is 50Mhz.

The secure digital input/output interface (SDIO) defines the SD, SD I/O and embedded MultiMediaCard (e•MMC) host interface, which provides command/data transfer between the AHB system bus and SD memory cards, SD I/O cards and e•MMC.

3.36. Management data input/output (MDIO)

- Support slave mode with a frequency up to 4MHz.
- Support CFP/CFP2 MSA Management Interface Specification.

The MDIO interface can receive complete MDIO frames. As long as the data is written to the register before receiving the turnaround bits (TA) of the read or post read increment address frame, the MDIO interface can transmit complete MDIO frames. Interrupts are generated at the end of every complete frame, which can be used or provided at correct time. Interrupts

can also be generated after every valid PHYADR and DEVADD, which allows more complex controls within frames.

3.37. External memory controller (EXMC)

- Supported external memory:
  - SRAM
  - PSRAM
  - ROM
  - NOR Flash
  - 8-bit or 16-bit NAND Flash
  - Synchronous DRAM(SDRAM)
- Protocol translation between the AXI and the multitude of external memory protocol.
- Offering a variety of programmable timing parameters to meet user's specific needs.
- Each bank has its own chip-select signal which can be configured independently.
- Independent read / write timing configuration to a sub-set memory type.
- Embedded ECC hardware for NAND Flash access.
- 8,16, or 32 bits bus width.
- Address and data bus multiplexing mechanism for NOR Flash and PSRAM.
- Write enable and byte select are provided as needed.
- Automatic AXI transaction split when internal and external bus width is not compatible.

The external memory controller EXMC, is used as a translator for CPU to access a variety of external memory, it automatically converts AXI memory access protocol into a specific memory access protocol defined in the configuration register, such as SRAM, ROM, NOR Flash, PSRAM, NAND Flash and SDRAM. The EXMC also can be configured to interface with the most common LCD module of Motorola 6800 and Intel 8080 series and reduce the system cost and complexity.

3.38. VREF

- Stable voltage, and product calibrated.
- Connects to VREFP pin to source off-chip circuits.
- 1.5V, 1.8V, 2.048V or 2.5V configurable reference voltage output.

A precision internal reference circuit is inside. The internal voltage reference unit is used to provide voltage reference for ADC / DAC, or used by off-chip circuit connecting to VREFP pin.

3.39. Low power digital temperature sensor (LPDTS)

- The trigger source of measurement can be set to software or hardware.
- Programmable sampling time.
- Counter synchronized on LXTAL or PCLK.

- The interrupt can be generated when the temperature is below a low threshold or above a high threshold and at the end of measurement.
- The generation of asynchronous wakeup signal indicates that the measurement result is higher or lower than the specified threshold when the LXTAL is selected as reference clock.

Low power digital temperature sensor(LPDTS) is used to transmit square wave, which is converted by temperature and the frequency is proportional to the absolute temperature. The frequency measurement is based on the PCLK or the LXTAL clock.

3.40. Encoder Divided-Output controller (EDOUT)

- Support for changing the activation polarity of B.
- Support configuration of Z-phase output location and pulse width.
- Number of edges per rotation: 16 to 65536 (must be the multiple of four).
- Support for the input of update period event signals from the TRIGSEL.

The encoder divided-output controller (EDOUT) is used to output location information obtained from the encoder in the form of A-phase, B-phase, and Z-phase pulses.

3.41. Controller area network (CAN)

- Supports CAN protocol version 2.0A/B.
- Compliant with the ISO 11898-1:2015 standard.
- Supports CAN FD frame with up to 64 data bytes, baudrate up to 8 Mbit/s.
- Supports CAN classical frame with up to 8 data bytes, baudrate up to 1 Mbit/s.
- Supports time stamp based on 16-bit free running counter.
- Supports transmitter delay compensation for CAN FD frames at faster data rates.
- Maskable interrupts.
- Supports four communication mode: normal mode, Inactive mode, Loopback and silent mode, and Monitor mode.
- Supports two power saving modes: CAN_Deepsleep mode, and CAN_sleep mode.
- Support two wakeup methods for waking up from Pretended Networking mode: wakeup matching event, and wakup timeout event.
- Global network time, synchronized by a specific message.

CAN bus (Controller Area Network) is a bus standard designed to allow microcontrollers and devices to communicate with each other without a host computer. The CAN interface supports the CAN 2.0A/B protocol, ISO 11898-1:2015 and BOSCH CAN FD specification.

The CAN module is a CAN Protocol controller with a very flexible mailbox system for transmitting and receiving CAN frames. The mailbox system consists of a set of mailboxes that store configuration and control data, timestamp, message ID, and data. The space of up to 32 mailboxes can also be configured as Rx FIFO with ID filtering against up to 104 extended IDs or 208 standard IDs or 416 partial 8-bit IDs, and configure receive FIFO/mailbox private

filter register for up to 32 ID filter table elements.

3.42. Ethernet (ENET)

- IEEE 802.3 compliant media access controller (MAC) for Ethernet LAN.
- 10/100 Mbit/s rates with dedicated DMA controller and SRAM.
- Support hardware precision time protocol (PTP) with conformity to IEEE 1588.

The Ethernet media access controller (MAC) conforms to IEEE 802.3 specifications and fully supports IEEE 1588 standards. The embedded MAC provides the interface to the required external network physical interface (PHY) for LAN bus connection via an internal media independent interface (MII) or a reduced media independent interface (RMII). The function of 32-bit CRC checking is also available.

3.43. Comparator (CMP)

- Rail-to-rail comparators.
- Configurable hysteresis.
- Configurable speed and consumption.
- Configurable analog input source.
  - DAC output.
  - Multiplexed I / O pins.
  - The whole or sub-multiple values of internal reference voltage.
- Outputs with blanking source.
- Window comparator.
- Outputs to I / O.
- Outputs to timers for triggering.
- Digital filter.
- Outputs to EXTI.
- Outputs to NVIC.
- Outputs to TRIGSEL.

The general purpose CMP can work either standalone (all terminal are available on I/Os) or together with the timers.

It can be used to wake up the MCU from low-power mode by an analog signal, provide a trigger source when an analog signal is in a certain condition, achieve some current control by working together with a PWM output of a timer and the DAC.

3.44. High-Performance Digital Filter (HPDF)

- 8 multiplex digital serial input channels.
  - configurable SPI and Manchester interfaces.
- 8 internal digital parallel input channels.

  - input with up to 16-bit resolution.
  - internal source: ADC data or memory (CPU/DMA write) data stream.
- Configurable Sinc filter and integrator.
  - the order and oversampling rate (decimation rate) of Sinc filter can be configured.
  - sampling rate of configurable integrator.
- Threshold monitor function.
  - independent Sinc filter, configurable order and oversampling rate (decimation rate).
  - configurable data input source: serial channel input data or HPDF output data.
- Malfunction monitor function.
  - A counter with 8 bits is used to monitor the continuous 0 or 1 in the serial channel input data stream.
- Extreme monitor function.
  - store minimum and maximum values of output data values of HPDF.
- Up to 24-bit output data resolution.
- Clock signal can be provided to external sigma delta modulator.
  - provide configurable clock signal by the CKOUT pin.
- HPDF output data is in signed format.
- The third-phase data is obtained by adding the two phases of filtered data and taking the inverse, and it supports threshold monitoring
- The number of break signals can be configured
  - The TIMER is triggered after the break signal occurs the configured number of times

A high performance digital filter module (HPDF) for external sigma delta (Σ-Δ) modulator is integrated in GD32H77Dxx. HPDF supports SPI interface and Manchester-coded single-wire interface. The external sigma delta modulator can be connected with MCU by the serial interface, and the serial data stream output by sigma delta modulator can be filtered. In addition, HPDF also supports the parallel data stream input, which can be selected from internal ADC peripherals or from MCU memory.

3.45. Real-time decryption (RTDEC)

- Software configurable encrypted areas up to 4.
- Granularity is 4096 bytes in RTDEC programmed areas.
- Every area can be configured the independent 128-bits key, 16-bits area firmware version, and 64-bits application-defined nonce.
- Confidentiality and completeness protection for encryption keys.
  - 128-bits key registers are write-only, with software locking mechanism.
  - 8-bits CRC is calculated automatically by hardware, and it's used as the public key information.
- The real-time decryption when OSPI memory-mapped read operations.
  - Use of AES-128 in CTR mode.
  - Support key stream FIFO with depth 4.
  - Support various read size.
  - Decryption / encryption with physical address of the reads.

- Support for GD32 OSPI pre-fetching mechanism.

The real-time decryption (RTDEC) allows to decrypt in real-time according to information of the read request address. RTDEC can configure four independent and different encrypted areas. And each area has the option of execute-only or execute-never enforcement to choose.

3.46. Filter arithmetic accelerator (FAC)

- Fixed or float multiplier and accumulator.
- 256 x 32-bit local memory.
- 16-bit fixed-point or 32-bit float point input and output.
- Up to three buffers, two input buffers and one output buffer.
- Buffer can be circular.
- FIR and IIR can be realized.
- Vector functions support convolution, Dot product, correlation functions.
- Data can be read and written through DMA.

The filter arithmetic accelerator unit consist of multiplier, accumulator and address generation logic, so as to index vector elements stored in local memory. Circular buffering is valid for both input and output, which allows to realize finite impulse response (FIR) filters and infinite impulse response (IIR) filters. The unit support CPU to be free from frequent or lengthy filtering operations, compared with software implementation, it can accelerate calculations and the processing speed of time critical tasks.

3.47. Trigonometric Math Unit (TMU)

- 10 kinds of functions.
- Interrupt and DMA requests.
- The fixed point q1.31 / q1.15 format or IEEE754 32-bit single precision floating-point format is configurable.
- Programmable precision.
- CORDIC-algorithm core: circular system and hyperbolic system, rotation pattern and vectoring pattern.

The Trigonometric Math Unit (TMU) is a fully configurable block that execute common trigonometric and arithmetic operations. It can be used to calculate total 10 kinds of functions. The input / output data meet q1.31 or q1.15 fixed point format or IEEE754 32-bit single precision floating-point format.

3.48. Hardware semaphore (HWSEM)

- 32 semaphores.
- An interrupt is generated when a semaphore is unlocked.
- Semaphore is unlocked only when MID[3:0] and PID[7:0] are matched.

Hardware semaphore (HWSEM) provides a non-blocking mechanism to ensure the synchronous of processes. HWSEM realizes 32 semaphores in an atomic way, supporting semaphore write lock and read lock, and semaphore can only be unlocked when bus master and process are matched.

3.49. Universal serial bus high-speed interface (USBHS)

- Supports USB 2.0 Host mode at High-Speed(480Mb/s), Full-Speed(12Mb/s) or Low-Speed(1.5Mb/s).
- Supports USB 2.0 device mode at High-Speed(480Mb/s) or Full-Speed(12Mb/s).
- Supports OTG protocol with HNP (Host Negotiation Protocol) and SRP (Session Request Protocol).

USB High-Speed (USBHS) controller provides a USB-connection solution for portable devices. USBHS supports both host and device modes, as well as OTG mode with HNP (Host Negotiation Protocol) and SRP (Session Request Protocol). USBHS contains an embedded USB PHY internal which can be configured as High-Speed or Full-Speed. USBHS supports all the four types of transfer (control, bulk, Interrupt and isochronous) defined in USB 2.0 protocol. There is also a DMA engine operating as an AHB bus master in USBHS to speed up the data transfer between USBHS and system. For Full-Speed operation, battery charging detection (BCD), attach detection protocol (ADP), and link power management (LPM) are also supported.

Note: USBHS1 can not support OTG mode, and it contains an embedded PHY internal which can be configured as Full-Speed only. It also can not support BCD and ADP.

3.50. Encoder Interface Module (EDIM)

The EDIM module includes 5 protocols: A-format encoder protocol, T-format encoder protocol, EnDat 2.2 encoder protocol, BiSS-C encoder protocol, and HIPERFACE DSL encoder protocol.

3.50.1. AFMT

- Support the A-format version 2.0 protocol.
- Up to 8 encoders.
- Software trigger and external trigger.
- Monitor the status of the communication.
  - Communication completion
  - Timeout detection
  - Transmission busy
- Interrupt generation.
- Support DMA mode.
- Multi configurable baud rates of 2.5 Mbits/s, 4 Mbits/s, 6.67 Mbits/s, 8 Mbits/s, and 16

Mbits/s

The A-format encoder interface module (AFMT) serves as a master to communicate with encoders that support the A-format.

3.50.2. TFMT

- Support communication with Tamagawa smart-abs encoder.
- Monitor the status of the communication.
  - Encoder error
  - Timeout detection
  - Transmission/receive busy
  - Communication completion
  - Received frame error
- Interrupt generation.
- Support DMA mode.
- Baud rate: 2.5 Mbits/s.

The T-format encoder interface module (TFMT) serves as a master to communicate with encoders that support the Tamagawa format.

3.50.3. ENDAT

- Support communication with encoder supporting EnDat 2.2 and EnDat 2.1.
- Transimission clock generator.
- Continuous clock mode.
- Configurable received data length.
- Cable propagation delay time compensation.
- Recovery time II / III.
- Support software trigger, internal timer trigger and external trigger.
- Reset selected additional information of encoder.
- Configurable digital filter for data input to avoid spike.
- Monitor the status of the communication.
  - Encoder error
  - TYPE I / II / III error
  - CRC
  - Timeout detection
- Interrupt generation.
- Support DMA mode

The EnDat 2.2 encoder interface module (ENDAT) serves as a master to communicate with encoders that support the EnDat 2.2 interface.

3.50.4. BISS

- Support BiSS-C communication with up to 8 slaves.
  - Each slave process data up to 64 bits.

- CRC checks with up to 16 bits for data verification.
- Process data transfer and register communication simultaneously.
- Compensating for line delays and conversion times automatically.
- The independent memory banks enable the controller to access data freely while BiSS sensor data is being transferred.
- The memory for bidirectional register communication is 64 bytes.
- A parallel interface with a 32-bit data/address bus.
- Support point-to-point connection.
- Interrupt generation.
- Support DMA mode.

The BiSS-C encoder interface module (BISS) serves as a master to communicate with encoders that support the BiSS-C interface.

3.50.5. HDSL

- Support communication with encoder supporting HIPERFACE DSL.
- Support HIPERFACE DSL safety function.
- Drive interface and safe channel 1 interface can be configured for access either from the internal bus or through SPI interface 1.
- Safe channel 2 interface can be configured for access either from the internal bus or through SPI interface 2.
- System diagnostics function
- Fast position function
  - Estimator
  - Free running mode
  - SYNC mode
- Monitor the status and error messages
  - Event register
  - Online status
  - Status summary of the motor feedback system
  - Motor feedback system error messages
- Communication status error interrupt.
- Supports baud rate up to 9.375 MHz

The HIPERFACE DSL encoder interface module (HDSL) serves as a master to communicate with encoders that support the HIPERFACE DSL.

3.51. Resolver-to-digital module (RDCM)

- Complete monolithic resolver-to-digital converter
- High tracking rate
- Up to 14-bit resolution
- Programmable On-chip excitor
  - Analog sinusoidal waveform

  - Digital PWM waveform
- Calculation support for ADC data or simulation data
- Configuable gain adjustment for I/Q signals
- Configurable high-pass filter for I/Q signals
- Configurable Synthetic Reference Signal for I/Q Rectification
  - Manual mode, phase error adjustment range is 0 to 2pi
  - Calibration mode (on-chip excitor reference), phase error extraction range is 0 to 2pi
  - Calibration mode (external reference sign signal), phase error extraction and adjustment range is 0 to 2pi
  - Auto mode, phase error extraction and adjustment range is φ to φ + pi (φ is configurable)
  - Moving average function for carrier phase extraction
- Demodulator (concatenated hardware filter stages)
  - Configurable CIC3 filter with decimation rates of 4 to 512
  - FIR0 filter with 8 coefficients (10-bit) with decimation rate 2
  - FIR1 filter with 28 coefficients (10-bit) with decimation rate 1 or 2
- Nonorthogonal phase mismatch compensation
- Configurable tracking loop for different resolution (default 14bit) and tracking rate
- Absolute position and velocity detection
- Smooth filter function for velocity extraction
- System fault detection support
  - I channel envelope signal threshold match function
  - Q channel envelope signal threshold match function
  - Monitor signal threshold match function
  - Track error signal threshold match function
- Programmable fault detection thresholds
- Interrupt generation
- Support DMA mode
- Support timestamp
- Support result gate
- Support result data FIFO

The RDCM is a complete 14-bit tracking resolver-to-digital converter, integrating an on-chip programmable sinusoidal oscillator that provides sine wave excitor for resolvers.

The excitation signal frequency range output by the RDCM is 2 kHz to 100 kHz (DAC buffer on). The input I/Q signals utilize a Type II tracking loop to track the input signals and convert the input sine and cosine information into a digital representation of the input angle and velocity.

3.52. Debug mode

- JTAG and SWD Debug Port.

The GD32H77Dxx series provide a large variety of debug, trace and test features. They are implemented with a standard configuration of the Arm® CoreSight™ module together with a daisy chained standard TAP controller. Debug and trace functions are integrated into the ARM® Cortex®-M7. The debug system supports serial wire debug (SWD) and trace functions in addition to standard JTAG debug.

3.53. Package and operation temperature

- BGA176.
- Operation temperature range: -40°C to +105°C.

4. Electrical characteristics

4.1. Parameter introduction

- Parameter conditions: Unless otherwise specified, all values given for V_{DD} = V_{DDA} = 3.3 V, T_J = 25°C, and all voltages are referenced to Vss.
- Values guaranteed by design, characterization, sample are indicated in the table footnotes, and are not 100% tested in production. If not specially indicated, it means the values guaranteed by 100% tested in production.
- Value guaranteed by design, not 100% tested in production indicates that the value is derived from design or simulation and / or process characteristics.
- Value guaranteed by characterization, not 100% tested in production indicates that the value is derived from comprehensive evaluation after random test. And the minimum and maximum values represent the mean value plus or minus three times the standard deviation (mean +/-3σ).
- Value guaranteed by sample, not 100% tested in production indicates that the value is derived from testing parameters with a small sample size.

See the following table for some abbreviation terms and their descriptions in this chapter.

Table 4-1. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
CAN	Controller Area Network
CMP	Comparator
CPDM	Clock phase delay module
DAC	Digital-to-Analog Converter
DCI	Digital camera interface
DSI	Display serial interface
DMA	Direct Memory Access
EDIM	Encoder Interface Module
AFMT	A-format encoder interface module
TFMT	T-format encoder interface module
ENDAT	EnDat 2.2 encoder interface module
BISS	BiSS-C encoder interface module
HDSL	HIPERFACE DSL encoder interface module
EDOUT	Encoder Divided-Output controller
EXMC	External memory controller
eNVM	Execution non-volatile memory
GPIO	General Purpose Input/Output
GPSI	General parallel slave interface
HPDF	High-Performance Digital Filter
I2C	Inter-integrated circuit interface
JTAG	Joint Test Action Group
MDIO	Management data input / output
OSPI	Octal-SPI interface
OSPIM	OSPI I/O manager
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RDCM	Resolver-to-digital module
RMII	Reduced Media Independent Interface
RSPDIF	Receiver of Sony/Philips Digitial Interface
SAI	Serial Audio Interface
SDIO	Secure digital input/output interface
SPI	Serial Peripheral Interface
TLI	TFT-LCD interface
USBHS	Universal serial bus High-Speed interface
WDGT	Watchdog timer

4.2. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-2. Absolute maximum ratings(1)

Symbol	Description	Min	Max	Unit
V_{DD}	External voltage range(2)	V_{SS} - 0.3	3.6	V
V_{DDA}	External analog supply voltage(3)	V_{SSA} - 0.3	3.6	V
V_{BAT}	External battery supply voltage	V_{SS} - 0.3	3.6	V
$V_{DD50USB}$	$V_{DD50USB}$ supply voltage	V_{SS} - 0.3	V_{SS} + 5.6	V
V_{IN}	Input voltage on 5VT I/O(4)	V_{SS} - 0.3	V_{DD} + 3.6	V
	Input voltage on other I/O	V_{SS} - 0.3	V_{DD}+0.3	
$\|\Delta V_{DDX}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSX}-V_{SS}\|$	Variations between different ground pins	-	50	mV
I_{IO}	Maximum current for GPIO pins	-	20	mA
$\sum I_{IO}$	Maximum current sunk/sourced by all GPIO pin	-	140	
I_{DD}	Maximum current into each V_{DD} pin	-	100	
I_{SS}	Maximum current into each V_{SS} pin	-	100	
T_{STG}	Storage temperature range	-65	150	°C
T_{JMAX}	Maximum junction temperature	-	125	°C

(1) Value guaranteed by design, not 100% tested in production.

(2) All power supply pins must be connected to the correct voltage range.

(3) It is recommended that V_{DD} and V_{DDA} are powered by the same source. The maximum difference between V_{DD} and V_{DDA} does not exceed 300 mV during power-up and operation.

(4) V_{IN} maximum value cannot exceed 5.5 V.

4.3. General operating conditions

Table 4-3. General operating conditions (1)(2)(3)

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Digital supply voltage	-	1.71	3.3	3.6	V
V_{DDA}	Analog supply voltage	Same as V_{DD}	1.71	3.3	3.6	
V_{BAT}	Battery supply voltage	-	1.71	-	3.6	
$V_{DD50USB}$	$V_{DD50USB}$ supply voltage	USB regulator ON	4.0	5.0	5.5	
		USB regulator OFF	-	$V_{DD33USB}$	-	
$V_{DD33USB}$	Standard operating voltage, USB domain	USB used	3.0	-	3.6	
		USB not used	0	-	3.6	
V_{DDSMPS}	Supply voltage for the internal SMPS Step-down converter	V_{DDSMPS} = V_{DD}	1.71	-	3.6	
V_{CORE}	Core logic supply powered by VCORE pin	SMPS mode	0.87	0.9	0.97	
		Bypass mode(4)	0.87	0.9	0.97	
f_{CPU}	core clock frequency	-	-	-	600	MHz
f_{ACLK}	AXI clock frequency	-	-	-	300	
f_{HCLK}	AHB clock frequency	-	-	-	300	
f_{APB1}	APB1 clock frequency	-	-	-	150	
f_{APB2}	APB2 clock frequency	-	-	-	300	
f_{APB3}	APB3 clock frequency	-	-	-	150	
f_{APB4}	APB4 clock frequency	-	-	-	150	
T_J	Junction temperature	-	-40	-	125	°C
P_D	Power dissipation at T_A = 105°C of BGA176	-	-	-	552	mW

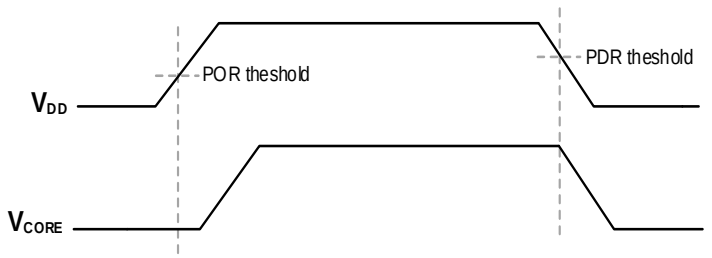
(1) Value guaranteed by design, not 100% tested in production.

(2) It is recommended that VDD and VDDA are powered by the same source. The maximum difference between VDD and VDDA does not exceed 300 mV during power-up and operation.

(3) The device junction temperature must be kept below maximum T_J, otherwise it may cause permanent damage to the device.

(4) The power-up and power-down sequence for the power bypass mode should meet the requirements as illustrated in ***Figure 4-1. Bypass mode power-up and power-down timing diagram*** (1)(2)(3)

Figure 4-1. Bypass mode power-up and power-down timing diagram (1)(2)(3)



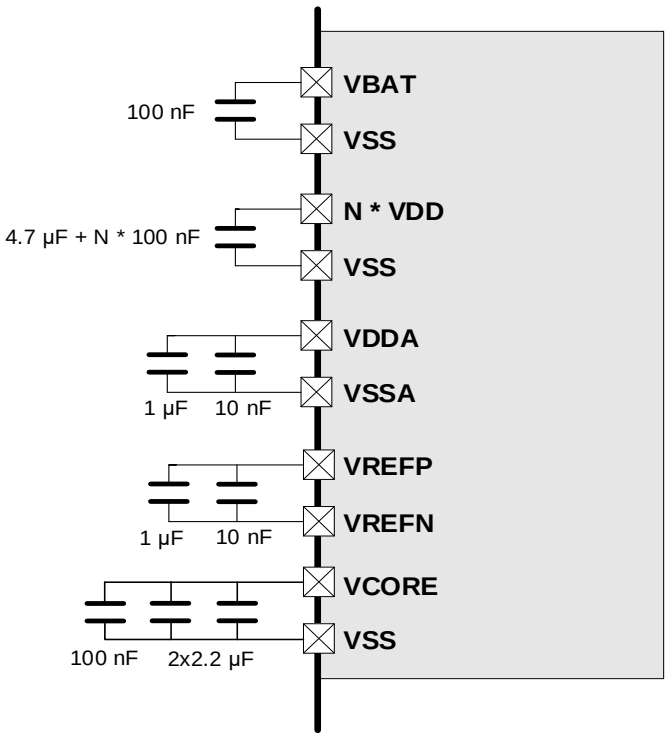
(1) When using Bypass mode power supply, the VCORE domain can be powered after POR. Before the V_{CORE} power supply stabilizes, the VCORE domain remains in reset steady state.

(2) When using Bypass mode power supply, if VCORE PDR is not enabled, the VCORE domain power-down must occur later than PDR. If VCORE PDR is enabled, the VCORE domain power-down can occur earlier

than PDR.

(3) Under any operating condition, ensure that the VDD/VDDA voltage is greater than the VCORE voltage.

Figure 4-2. Recommended power supply decoupling capacitors(1)(2)



(1) It is recommended to configure a 100nF capacitor for each VDD pin.

(2) The V_{REFP} and V_{REFN} pins are only available on certain packages, or else the V_{REFP} and V_{REFN} pins are not available and internally connected to V_{DDA} and V_{SSA} pins.

(3) All decoupling capacitors need to be as close as possible to the pins on the PCB board.

4.4. SMPS step-down converter

Figure 4-3. External components for SMPS step-down converter

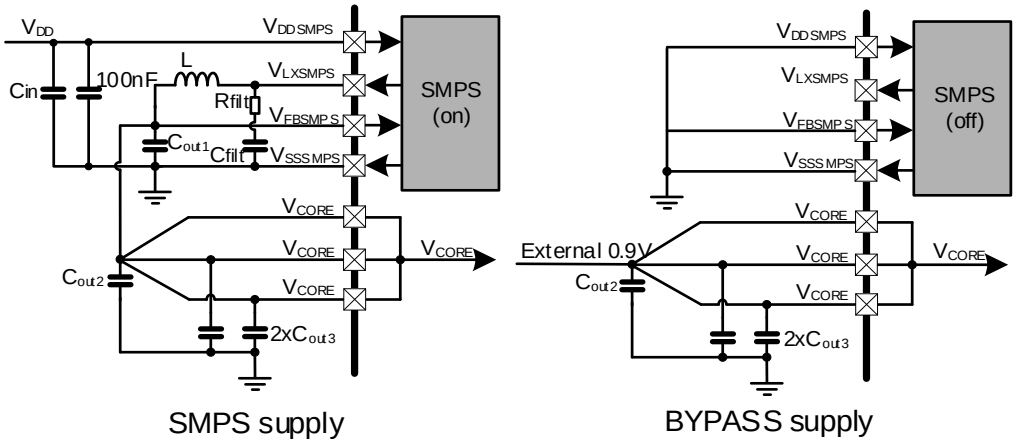


Table 4-4. Characteristics of SMPS step-down converter external components

Symbol	Parameter	Conditions
C_{in}	Capacitance of external capacitor on V_{DDSMPS}	4.7 µF
	ESR of external capacitor	100 mΩ
C_{filt}	Capacitance of external capacitor on V_{LXSMPS} pin	220 pF
R_{filt}	Resistor of external capacitor on V_{LXSMPS} pin	50 Ω
C_{out1}	Capacitance of external capacitor on V_{FBSMPS} pin	10 µF
	ESR of external capacitor	20 mΩ
C_{out2}	Capacitance of external capacitor on V_{CORE} pin	100 nF
C_{out3}	Capacitance of external capacitor on V_{CORE} pin	2.2 µF
	ESR of external capacitor	50 mΩ
L	Inductance of external Inductor on V_{LXSMPS} pin	2.2 µH
	Serial DC resistor	150 mΩ
I_{SAT}	DC current at which the inductance drops 30% from its value without current	1.7 A
I_{RMS}	Average current for a 40 °C rise: rated current for which the temperature of the inductor is raised 40 °C by DC current	1.4 A

Table 4-5. SMPS step-down converter characteristics

Symbol	Conditions	Min	Typ	Max	Unit
V_{DDSMPS}(1)	V_{OUT} = 0.9 V	1.71	-	3.6	V
V_{OUT}(2)	I_{out}=600 mA	-	0.9	-	V
I_{OUT}(3)	-	-	-	600	mA
$R_{DS(ON)}$(3)	-	-	90	-	mΩ
I_{DDSMPS_Q}(3)	Quiescent current	-	400	-	µA
T_{SMPS_START}(3)	V_{OUT} = 0.9V	-	50	-	µS
I_{INRUSH}(3)	V_{OUT} = 0.9, POR, Wake from Standby	-	900	-	mA

(1) The switching frequency is 2 MHz +/- 10%

(2) Including line transient and load transient.

(3) Value guaranteed by design, not 100% tested in production.

4.5. Power supply requirement characteristics

Table 4-6. Power supply requirement characteristics (1)

Symbol	Description	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	μs/V
	V_{DD} fall time rate		100	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	
	V_{DDA} fall time rate		100	∞	
$t_{VDD(USB)}$	$V_{DD(USB)}$ rise time rate	-	0	∞	
	$V_{DD(USB)}$ fall time rate		100	∞	
$t_{VDD(DSI)}$	V_{DD} rise time rate	-	0	∞	
	V_{DD} fall time rate		100	∞	
t_{VCORE}(2)	V_{DD} rise time rate	-	10	500	
	V_{DD} fall time rate		10	500	
$t_{VDD09DSI}$(2)	V_{DD} rise time rate	-	10	500	
	V_{DD} fall time rate		10	500	

(1) Value guaranteed by design, not 100% tested in production.

(2) When using the bypass power supply mode.

4.6. Power supply supervisor characteristics

Table 4-7. Power supply supervisor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LVD}(1)	Low voltage Detector level selection	LVDT<2:0> = 000(rising edge)	-	1.95	-	V
		LVDT<2:0> = 000(falling edge)	-	1.85	-	

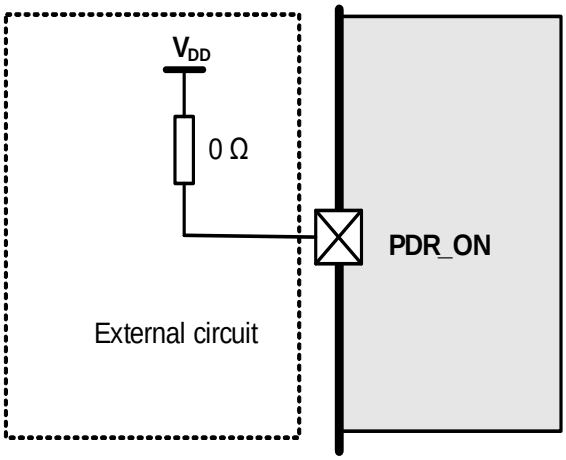
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		LVDT<2:0> = 001(rising edge)	-	2.10	-	
		LVDT<2:0> = 001(falling edge)	-	2	-	
		LVDT<2:0> = 010(rising edge)	-	2.25	-	
		LVDT<2:0> = 010(falling edge)	-	2.15	-	
		LVDT<2:0> = 011(rising edge)	-	2.4	-	
		LVDT<2:0> = 011(falling edge)	-	2.3	-	
		LVDT<2:0> = 100(rising edge)	-	2.55	-	
		LVDT<2:0> = 100(falling edge)	-	2.45	-	
		LVDT<2:0> = 101(rising edge)	-	2.70	-	
		LVDT<2:0> = 101(falling edge)	-	2.60	-	
		LVDT<2:0> = 110(rising edge)	-	2.85	-	
		LVDT<2:0> = 110(falling edge)	-	2.75	-	
$V_{LVDhyst}$(1)	LVD hystersis	-	-	100	-	mV
V_{POR}(1)	Power on reset threshold	-	-	1.53	-	V
V_{PDR}(1)	Power down reset threshold	-	-	1.48	-	V
$V_{HYST(POR_PDR)}$(1)	Hysteresis of POR and PDR	-	-	50	-	mV
V_{BOR3}(1)	Brownout level 3 threshold	Falling edge	-	2.0	-	V
		Rising edge	-	2.1	-	V
V_{BOR2}(1)	Brownout level 2 threshold	Falling edge	-	2.3	-	V
		Rising edge	-	2.4	-	V
V_{BOR1}(1)	Brownout level 1 threshold	Falling edge	-	2.6	-	V
		Rising edge	-	2.7	-	V
$V_{HYST(BOR)}$(1)	BOR hysteresis	-	-	100	-	mV
$t_{RSTTEMPO}$(1)	Reset temporization	-	-	520	-	µs
V_{AVD_0}(1)	Analog voltage detector for V_{DDA} threshold 0	VAVDVC<1:0> = 00(rising edge)	-	1.7	-	V
		VAVDVC<1:0> = 00(falling edge)	-	1.6	-	
V_{AVD_1}(1)	Analog voltage detector for V_{DDA} threshold 1	VAVDVC<1:0> = 01(rising edge)	-	2.1	-	
		VAVDVC<1:0> = 01(falling edge)	-	2	-	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{AVD_2}(1)	Analog voltage detector for V_{DDA} threshold 2	VAVDVC<1:0> = 10(rising edge)	-	2.5	-	
		VAVDVC<1:0> = 10(falling edge)	-	2.4	-	
V_{AVD_3}(1)	Analog voltage detector for V_{DDA} threshold 3	VAVDVC<1:0> = 11(rising edge)	-	2.8	-	
		VAVDVC<1:0> = 11(falling edge)	-	2.7	-	
V_{hyst_AVD}(1)	Hysteresis of V_{DDA} voltage detector	-	-	100	-	mV
V_{OVD_0}(1)	V_{CORE} over voltage detector for threshold 0	VOVDVC<1:0> = 00(rising edge)	-	0.9	-	V
		VOVDVC<1:0> = 00(falling edge)	-	0.875	-	
V_{OVD_1}(1)	V_{CORE} over voltage detector for threshold 1	VOVDVC<1:0> = 01(rising edge)	-	1.0	-	
		VOVDVC<1:0> = 01(falling edge)	-	0.975	-	
V_{OVD_2}(1)	V_{CORE} over voltage detector for threshold 2	VOVDVC<1:0> = 10(rising edge)	-	1.1	-	
		VOVDVC<1:0> = 10(falling edge)	-	1.075	-	
V_{OVD_3}(1)	V_{CORE} over voltage detector for threshold 3	VOVDVC<1:0> = 11(rising edge)	-	1.2	-	
		VOVDVC<1:0> = 11(falling edge)	-	1.175	-	
V_{hyst_OVD}(1)	Hysteresis of V_{OVD} voltage detector	-	-	25	-	mV
V_{UVD_0}(1)	V_{CORE} under voltage detector for threshold 0	VUVDVC<1:0> = 00(rising edge)	-	0.825	-	V
		VUVDVC<1:0> = 00(falling edge)	-	0.8	-	
V_{UVD_1}(1)	V_{CORE} under voltage detector for threshold 1	VUVDVC<1:0> = 01(rising edge)	-	0.725	-	
		VUVDVC<1:0> = 01(falling edge)	-	0.7	-	
V_{UVD_2}(1)	V_{CORE} under voltage detector for threshold 2	VUVDVC<1:0> = 10(rising edge)	-	0.675	-	
		VUVDVC<1:0> = 10(falling edge)	-	0.65	-	
V_{UVD_3}(1)	V_{CORE} under voltage detector for threshold 3	VUVDVC<1:0> = 11(rising edge)	—	0.9	—	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		VUVDVC<1:0> = 11(falling edge)	—	0.875	—	
V_{hyst_UVD}(1)	Hysteresis of V_{UVD} voltage detector	-	-	25	-	mV

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-4. Recommended PDR_ON pin circuit(1)



(1) PDR_ON pin should be pulled up to V_{DD}.

4.7. Start-up timings of Operating conditions

Table 4-8. Start-up timings of Operating conditions(1)(2)(3)(4)

Symbol	Description	Conditions			Min	Typ	Max	Unit
t_{ST}	Start-up time	Clock source from IRC64M	GD32H77xxW	No self-check	-	622	-	μs
				Hardware OTA upgrade within 2M range	-	570	-	ms
			GD32H77xxP	No self-check	-	622	-	μs
			GD32H77xxW / GD32H77xxP	Hardware self-check within 2M range + 1 injected error	-	82	-	ms
				Hardware self-check within 2M range + 100 injected error	-	88	-	
			GD32H77xxI	No self-check	-	2.49	-	ms

(1) Value guaranteed by sample, not 100% tested in production.

(2) After power-up, the start-up time is the time between the rising edge of NRST high and the first I/O instruction conversion in SystemInit function.

(3) PLL is off.
(4) Excluding the time to initialize SRAM during startup.

4.8. Wake-up times from power saving modes

Table 4-9. Wake-up times from power saving modes(1)(2)

Symbol	Description	Conditions	Min	Typ	Max	Unit
t_{Sleep}	Wakeup from Sleep mode	-	-	805	-	ns
$t_{Deep-sleep}$	Wakeup from Deep-sleep mode	SRAM disable	-	1.95	-	μs
		SRAM precharge	-	2.02	-	
		SRAM retetion	-	2.02	-	
$t_{Standby}$	Wakeup from Standby mode	-	-	2.32	-	ms

(1) Value guaranteed sample, not 100% tested in production.
(2) The wakeup time is measured from the wakeup event to the point at which the application code reads the first instruction under the below conditions: V_{DD} = V_{DDA} = 3.3 V, sleep and deep-sleep system clock = HXTAL= 25 MHz, standby mode system clock = IRC64M = 64 MHz, and SMPS supply is used.

4.9. Power consumption

The power consumption is measured as described in ***Figure 4-5. Power consumption measurement diagram*** Except for Backup mode, the SMPS supply current consumption values are obtained from tests powered by V_{DD} = V_{DDA} = V_{DDSMPS}, with the current being I_{SUM}, while the BYPASS supply current consumption values are obtained from tests powered by V_{DD} = V_{DDA} and V_{CORE}. The RTC unit and LXTAL oscillator are powered by the V_{BAT}, while the current is I_{BAT}. Unless otherwise stated, in SMPS supply mode, V_{DD} = V_{DDA} = V_{DDSMPS} =3.3 V, is applied to the supply pins; in BYPASS supply mode, V_{DD} = V_{DDA} = 3.3 V, V_{CORE} = 0.9 V is applied to the supply pins.

The MCU is configured under the following conditions:

- All I/O pins are in analog input mode.
- All peripherals are disabled except when explicitly mentioned.

Figure 4-5. Power consumption measurement diagram

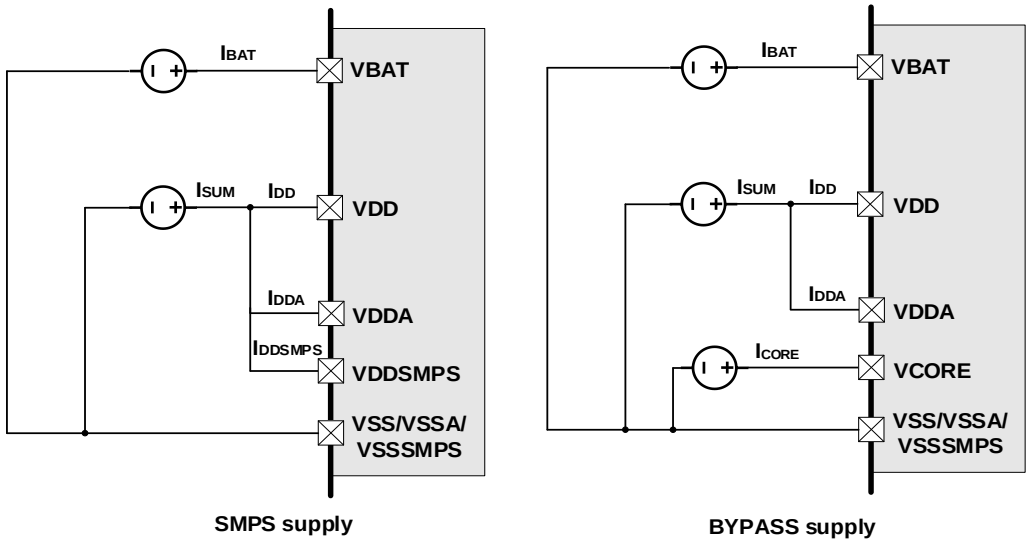


Table 4-10. Power consumption in Run mode(SMPS mode)(1)(2)(3)

Symbol	Description	Conditions			Typ				Unit
		Execute from	Peripherals	f_{CPU}	T_J = -40°C	T_J = 25°C	T_J = 105°C	T_J = 125°C	
I_{SUM}	Sum of supply current from VDD、VDDA、VDDSMPS (Run mode)	ITCM	All disabled	600 MHz	16.1	18.0	49.8	86.3	mA
				400 MHz	11.8	13.8	46.0	83.2	
				64 MHz	5.3	7.1	39.6	77.5	
		CNVM (cache on)	All disabled	600 MHz	23.1	24.8	60.9	93.6	
				400 MHz	17.2	19.0	54.8	89.0	
				64 MHz	5.6	7.8	44.3	74.8	
		CNVM (cache off)	All disabled	600 MHz	21.9	23.6	61.1	94.7	
				400 MHz	16.2	18.1	55.2	86.1	
				64 MHz	5.5	7.7	45.2	74.8	

(1) Value guaranteed by sample, not 100% tested in production.

(2) During power consumption test, GPIO needs to be configure as Analog Input mode.

(3) The memory access time is adjusted with the correctly wait states number.

Table 4-11. Power consumption in Run mode(BYPASS mode)(1)(2)(3)

Symbol	Description	Conditions			Current	Typ				Unit
		Execute from	Peripherals	f_{CPU}		T_J = -40°C	T_J = 25°C	T_J = 105°C	T_J = 125°C	
I_{BYPASS}	Sum of supply current from VDD、VDDA、VCORE (Run mode)	ITCM	All disabled	600 MHz	I_{SUM}	3.6	3.7	4.3	4.6	mA
					I_{CORE}	33.1	40.3	146.8	218.2	
				400 MHz	I_{SUM}	3.0	3.1	3.6	3.99	
					I_{CORE}	23.1	30.1	137.4	209.9	
				64 MHz	I_{SUM}	1.4	1.4	1.8	2.2	
					I_{CORE}	8.8	15.4	115.7	195.5	
		CNVM	All disabled	600 MHz	I_{SUM}	3.6	3.7	4.3	4.7	

Symbol	Description	Conditions			Current	Typ				Unit
		Execute from	Peripherals	f_{CPU}		T_J = -40°C	T_J = 25°C	T_J = 105°C	T_J = 125°C	
		(cache on			I_{CORE}	47.2	54.5	162.3	236.4	
				400 MHz	I_{SUM}	3.0	3.1	3.6	4.0	
					I_{CORE}	32.5	39.6	148.1	222.6	
				64 MHz	I_{SUM}	1.4	1.4	1.8	2.2	
					I_{CORE}	9.4	16.0	117.1	198.9	
		CNVM (cache off)	All disabled	600 MHz	I_{SUM}	3.6	3.7	4.3	4.7	
					I_{CORE}	47.1	54.6	166.3	241.5	
				400 MHz	I_{SUM}	3.0	3.1	3.7	4.0	
					I_{CORE}	32.4	39.6	151.1	226.1	
				64 MHz	I_{SUM}	1.4	1.4	1.8	2.2	
					I_{CORE}	9.3	16.0	119.3	201.4	

(1) Value guaranteed by sample, not 100% tested in production.

(2) During power consumption test, GPIO needs to be configure as Analog Input mode.

(3) The memory access time is adjusted with the correctly wait states number.

Table 4-12. Power consumption in Run mode with different codes(SMPS mode, all peripherals disabled)(1)(2)

Symbol	Description	Conditions			Clock	Typ	Unit	Typ	Unit
		cache	Code (Code+RAM)	Core Mark					
I_{SUM}	Sum of supply current from VDD、VDDA、VDDSMPS (Run mode)	cache on	ITCM + DTCM	2989	HXTAL = 25 MHz, PLL on, System clock = 600 MHz, f_{HCLK} = 300 MHz	32.5	mA	54.17	µA / MHz
			CNVM + AXI SRAM	2918		34.0		56.67	
			CNVM + DTCM	2989		32.7		54.5	
			ECNVM+ DTCM	2989		32.9		54.83	
			AXI SRAM + DTCM	2979		32.0		53.33	
			AXI SRAM + AXI SRAM	2919		33.7		56.17	

Symbol	Description	Conditions			Clock	Typ	Unit	Typ	Unit
		cache	Code (Code+RAM)	Core Mark					
		cache off	ITCM + DTCM	2989		32.5		54.17	
			CNVM + AXI SRAM	740		33.9		56.5	
			CNVM + DTCM	746		30.1		50.17	
			ECNVM + DTCM	67		36.7		61.17	
			AXI SRAM + DTCM	1467		29.1		48.5	
			AXI SRAM + AXI SRAM	735		27.1		45.17	

(1) Value guaranteed by sample, not 100% tested in production.

(2) During power consumption test, GPIO needs to be configure as Analog Input mode.

Table 4-13. Power consumption in Run mode with different codes(BYPASS mode, all peripherals disabled)(1)(2)

Symbol	Description	Conditions				Current	Typ	Unit	Typ	Unit
		Clock	cache	Code (Code+RAM)	CoreMark					
I_{BYPASS}	Sum of supply current from VDD、VDDA、VCORE (Run mode)	HXTAL = 25 MHz, PLL on, System clock = 600 MHz, f_{HCLK} = 300 MHz	cache on	ITCM + DTCM	2989	I_{SUM}	3.6	mA	6.0	µA / MHz
						I_{CORE}	80.3		133.83	
				CNVM + AXI SRAM	2918	I_{SUM}	3.6		6.00	
						I_{CORE}	84.6		141.0	
				CNVM + DTCM	2989	I_{SUM}	4.0		6.67	
						I_{CORE}	80.1		133.5	
				ECNVM + DTCM	2989	I_{SUM}	4.0		6.67	
						I_{CORE}	80.2		133.67	
				AXI SRAM + DTCM	2979	I_{SUM}	3.6		6.0	
						I_{CORE}	79.1		131.83	
				AXI SRAM + AXI SRAM	2919	I_{SUM}	3.6		6.0	
						I_{CORE}	82.8		138.0	

Symbol	Description	Conditions				Current	Typ	Unit	Typ	Unit
		Clock	cache	Code (Code+RAM)	CoreMark					
			cache off	ITCM + DTCM	2989	I_{SUM}	3.6		6.0	
						I_{CORE}	80.6		134.33	
				CNVM + AXI SRAM	740	I_{SUM}	4.5		7.5	
						I_{CORE}	81.2		135.33	
				CNVM + DTCM	746	I_{SUM}	4.5		7.5	
						I_{CORE}	70.9		118.17	
				ECNVM + DTCM	67	I_{SUM}	16.5		27.5	
						I_{CORE}	54.8		91.33	
				AXI SRAM + DTCM	1467	I_{SUM}	3.6		6.0	
						I_{CORE}	70.6		117.67	
				AXI SRAM + AXI SRAM	735	I_{SUM}	3.6		6.0	
						I_{CORE}	64.8		108.0	

(1) Value guaranteed by sample, not 100% tested in production.

(2) During power consumption test, GPIO needs to be configure as Analog Input mode.

Table 4-14. Power consumption in Sleep mode(SMPS mode)(1)(2)(3)

Symbol	Description	Conditions			Typ				Unit
		Execute from	Peripherals	f_{CPU}	T_J = -40°C	T_J = 25°C	T_J = 105°C	T_J = 125°C	
I_{SUM}	Sum of supply current from VDD、VDDA、VDDSMPS (Sleep mode)	CNVM	All disabled	600 MHz	18.4	20.3	58.0	92.3	mA
				400 MHz	13.4	15.5	53.3	83.3	
				64 MHz	5.2	7.5	45.5	74.6	

(1) Value guaranteed by sample, not 100% tested in production.
(2) During power consumption test, GPIO needs to be configure as Analog Input mode.
(3) The memory. Access time is adjusted with the correctly wait states number.

Table 4-15. Power consumption in Sleep mode(BYPASS mode)(1)(2)(3)

Symbol	Description	Conditions				Typ				Unit
		Execute from	Peripherals	f_{CPU}	Current	T_J = -40°C	T_J = 25°C	T_J = 105°C	T_J = 125°C	
I_{BYPASS}	Sum of supply current from VDD、VDDA、VCORE (Sleep mode)	CNVM	All disabled	600 MHz	I_{SUM}	3.6	3.7	4.3	4.7	mA
					I_{CORE}	36.8	44.0	156.5	231.4	
				400 MHz	I_{SUM}	3.0	3.1	3.7	4.0	
					I_{CORE}	25.5	32.6	145.1	219.2	
				64 MHz	I_{SUM}	1.4	1.4	1.9	2.2	
					I_{CORE}	8.8	15.4	119.7	201.3	

(1) Value guaranteed by sample, not 100% tested in production.
(2) During power consumption test, GPIO needs to be configure as Analog Input mode.
(3) The memory access time is adjusted with the correctly wait states number.

Table 4-16. Power consumption in Deep-sleep mode(SMPS mode)(1)(2)

Symbol	Description	Conditions		Typ				Unit
		Execute from	General	T_J = -40°C	T_J = 25°C	T_J = 105°C	T_J = 125°C	
I_{SUM}	Sum of supply current from VDD、VDDA、VDDSMPS (Deep-sleep mode)	CNVM	V_{CORE} = 0.7 V, IRC32K off, RTC off, All GPIOs analog mode	0.8	1.9	22.5	36.7	mA
			V_{CORE} = 0.8 V, IRC32K off, RTC off, All	0.9	2.5	30.3	49.9	

Symbol	Description	Conditions		Typ				Unit
		Execute from	General	T_J = -40°C	T_J = 25°C	T_J = 105°C	T_J = 125°C	
			GPIOs analog mode					
			V_{CORE} = 0.9 V, IRC32K off, RTC off, All GPIOs analog mode	1.1	3.5	40.7	68.0	

(1) Value guaranteed by sample, not 100% tested in production.

(2) During power consumption test, GPIO needs to be configure as Analog Input mode.

Table 4-17. Power consumption in Deep-sleep mode(BYPASS mode)(1)(2)

Symbol	Description	Conditions			Typ				Unit
		Execute from	General	Current	T_J = -40°C	T_J = 25°C	T_J = 105°C	T_J = 125°C	
I_{BYPASS}	Sum of supply current from VDD、VDDA、VCORE (Deep-Sleep mode)	CNVM	V_{CORE} = 0.9 V, IRC32K off, RTC off, All GPIOs analog mode	I_{SUM}	0.3	0.7	1.4	1.7	mA
				I_{CORE}	0.9	7.6	112.1	192.4	

(1) Value guaranteed by sample, not 100% tested in production.

(2) During power consumption test, GPIO needs to be configure as Analog Input mode.

Table 4-18. Power consumption in Standby mode(1)

Symbol	Description	Conditions		Typ				Unit
		General	V_{DD}	T_J = -40°C	T_J = 25°C	T_J = 105°C	T_J = 125°C	
I_{SUM}	Sum of supply current from VDD、VDDA、VDDSMPS (Standby mode)	FWDGT off, Backup SRAM off, RTC and LXTAL off	1.71V	49.3	56.2	78.2	101.1	µA
			2.6V	51.7	59.3	88.8	121.6	
			3.3V	55.7	65.1	116.5	169.5	
			3.6V	62.0	75.8	152.7	221.9	
		FWDGT off, Backup SRAM on, RTC and LXTAL off	1.71V	87.8	109.8	314.8	489.7	
			2.6V	89.2	112.3	326.4	514.4	
			3.3V	92.8	118.0	354.5	565.5	
			3.6V	98.4	128.8	389.8	618.9	
		FWDGT off, Backup SRAM off, RTC and LXTAL on	1.71V	49.8	57.6	79.1	101.7	
			2.6V	52.3	59.7	89.3	122.1	
			3.3V	55.0	65.3	117.1	169.2	
			3.6V	61.2	76.5	151.7	219.8	
		FWDGT off, Backup SRAM on, RTC and LXTAL on	1.71V	87.6	110.2	314.7	490.5	
			2.6V	89.8	112.5	326.7	515.0	
			3.3V	93.4	118.7	354.4	561.6	
			3.6V	99.0	129.4	388.6	620.6	
		FWDGT on, Backup SRAM off, RTC and LXTAL off	1.71V	50.3	57.3	78.4	101.2	
			2.6V	52.1	59.3	89.0	121.8	
			3.3V	54.5	65.3	116.6	169.2	
			3.6V	60.7	76.0	152.4	220.8	
		FWDGT on, Backup SRAM on, RTC and LXTAL off	1.71V	87.6	110.1	315.3	489.8	
			2.6V	89.4	112.5	326.9	515.7	
			3.3V	93.1	118.5	355.2	560.6	
			3.6V	98.7	129.2	390.4	619.3	

Symbol	Description	Conditions		Typ				Unit
		General	V_{DD}	T_J = -40°C	T_J = 25°C	T_J = 105°C	T_J = 125°C	
		FWDGT on, Backup SRAM off, RTC and LXTAL on	1.71V	50.0	57.8	79.2	101.8	
			2.6V	52.7	60.2	89.6	122.6	
			3.3V	55.8	66.0	118.0	170.5	
			3.6V	62.1	77.1	154.0	223.0	
		FWDGT on, Backup SRAM on, RTC and LXTAL on	1.71V	87.9	111.5	315.6	489.7	
			2.6V	90.1	113.3	327.5	515.9	
			3.3V	93.9	119.5	356.6	564.4	
			3.6V	99.8	130.5	393.1	617.5	

(1) Value guaranteed by sample, not 100% tested in production.

Table 4-19. Power consumption in Backup mode(1)

Symbol	Description	Conditions		Typ				Unit
		General	V_{BAT}	T_J = -40°C	T_J = 25°C	T_J = 105°C	T_J = 125°C	
I_{BAT}	LXTAL+RTC current from VBAT	V_{DD} off, V_{DDA} off, Backup SRAM off, RTC and LXTAL off	2.6V	0.01	0.03	0.4	1.2	μA
			3.3V	0.3	0.6	1.9	3.4	
			3.6V	1.2	2.1	5.0	7.1	
		V_{DD} off, V_{DDA} off, Backup SRAM on, RTC and LXTAL off	2.6V	37.6	53.1	238.5	394.0	
			3.3V	37.9	53.8	240.8	396.9	
			3.6V	38.8	55.3	244.0	400.7	
		V_{DD} off, V_{DDA} off, Backup SRAM off, RTC and LXTAL on	2.6V	0.7	0.8	1.2	2.1	
			3.3V	1.1	1.5	2.9	4.4	
			3.6V	2.1	3.1	6.1	8.3	
		V_{DD} off, V_{DDA} off, Backup SRAM on, RTC and LXTAL on	2.6V	38.2	53.8	239.5	395.4	
			3.3V	38.7	54.7	242.0	398.5	
			3.6V	39.6	56.3	245.2	402.4	

(1) Value guaranteed by sample, not 100% tested in production.

The current consumption of the on-chip peripherals is given in the following table. To avoid adding the CPU dynamic power consumption to the peripheral power consumption, the MCU needs to enter sleep mode to stop the CPU operation during current measurement. The MCU is configured under the following conditions:

• All I/O pins are in analog input mode

• The given value is in the table calculated by measuring the difference of the current consumptions:

-- The target peripheral is clocked on and enters sleep mode

-- All peripherals are clocked off and enter sleep mode

• The ambient operating temperature is 25 °C and VDD = VDDA = VDDSMPS = 3.3 V.

• BYPASS mode uses an external LDO, with the input terminal being VDD and the output terminal providing power to the VCORE.

The power consumption of the digital part of the on-chip peripherals is given in the following table. The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

The values in the table are equal to the peripheral current divided by the clock frequency of the corresponding BUS.

Table 4-20. Peripheral current consumption characteristics(1)(2)

Peripherial		Typical consumption		Unit
		SMPS	BYPASS	
AHB1	ENET1	2.775	10.571	μA/MHz
	ENET1TX	-	-	
	ENET1RX	-	-	
	ENET1PTP	-	-	
	USBHS0	2.1	7.349	
	USBHS0ULPI	-	-	
	DMA0	1.151	3.644	
	DMA1	1.099	3.787	
	DMAMUX	0.7	2	
	ENET0	2.916	10.74	
	ENET0TX	-	-	
	ENET0RX	-	-	
	ENET0PTP	-	-	
	USBHS1	2.103	7.345	
	USBHS1ULPI	-	-	
AHB2	DCI/PSSI	0.369	0.824	
	FAC	0.515	1.461	
	SDIO1	1.325	4.928	
	CAU	2.993	11.24	
	HAU	0.49	1.432	
	GPSI	0.96	3.291	
	TRNG	0.947	2.788	
	TMU	0.093	0.322	

Peripherial		Typical consumption		Unit
		SMPS	BYPASS	
	RAMECCMU1	-	-	
	PKCAU	-	-	
	FFT	1.194	4.117	
AHB3	EXMC	1.739	6.167	
	IPA	1.274	4.483	
	SDIO	1.414	4.766	
	MDMA	2.344	8.588	
	OSPIM	-	-	
	OSPI0	1.585	5.716	
	OSPI1	1.766	5.657	
	DSI	TBD	TBD	
	RTDEC0	0.844	1.88	
	RTDEC1	0.726	1.889	
	RAMECCMU0	-	-	
AHB4	GPIOA	0.573	1.517	
	GPIOB	0.633	1.502	
	GPIOC	0.548	1.497	
	GPIOD	0.578	1.598	
	GPIOE	0.554	1.48	
	GPIOF	0.502	1.48	
	GPIOG	0.6	1.519	
	GPIOH	0.509	1.479	
	GPIOJ	0.427	1.06	
	GPIOK	0.432	0.995	
	BKPSRAM	0.269	0.683	
	CRC	0.054	0.158	
	HWSEM	1.08	3.47	
ABP1	TIMER1	2.297	7.041	
	TIMER2	2.199	5.999	
	TIMER3	2.181	5.606	
	TIMER4	2.229	7.055	
	TIMER5	0.275	0.622	
	TIMER6	0.305	0.711	
	TIMER22	2.29	7.075	
	TIMER23	1.966	7.06	
	TIMER30	1.79	5.673	
	TIMER31	1.87	5.569	
	TIMER50	0.54	1.087	
	TIMER51	0.408	1.034	
	RSPDIF	0.871	2.374	
	SPI1	1.04	2.994	

Peripherial		Typical consumption		Unit
		SMPS	BYPASS	
	SPI2	1.061	2.642	
	MDIO	0.083	0.342	
	USRAT1	1.028	3.254	
	USRAT2	1.023	3.169	
	UART3	0.39	1.291	
	UART4	0.485	1.322	
	I2C0	0.803	1.954	
	I2C1	0.704	1.913	
	I2C2	0.742	2.012	
	I2C3	0.845	1.963	
	CTC	0.071	0.19	
	DACHOL	-	-	
	DAC	0.145	0.545	
	UART6	0.648	1.317	
	UART7	0.467	1.338	
ABP2	TIMER0	1.926	7.018	
	TIMER7	1.992	6.975	
	USART0	0.984	3.269	
	USART5	0.91	3.318	
	ADC0	0.285	0.818	
	ADC1	0.275	0.77	
	ADC2	0.254	0.718	
	SPI0	0.669	2.047	
	SPI3	0.661	1.966	
	SAI3	1.212	3.964	
	TIMER14	0.817	2.611	
	TIMER15	0.505	1.453	
	TIMER16	0.514	1.481	
	HPDF	3.925	14.822	
	SPI4	0.639	2.193	
	SPI5	0.643	2.045	
	SAI0	1.185	4.021	
	SAI1	1.349	4.514	
	SAI2	1.302	4.567	
	TIMER40	0.892	2.798	
	TIMER41	0.743	2.645	
	TIMER42	0.786	2.628	
	TIMER43	0.899	2.671	
	TIMER44	0.846	2.659	
	EDOUT	0.158	0.424	
	TRIGSEL	0.151	0.404	

Peripherial		Typical consumption		Unit
		SMPS	BYPASS	
APB3	TLI	1.189	3.657	
	WWDGT	0.047	0.142	
APB4	SYSCFG	0.685	1.624	
	CMP	0.09	0.182	
	VREF	-	-	
	LPDTS	0.214	0.587	
	PMU	0.6	1.705	
ADDAPB2	RDCM	0.878	2.961	
	HDSLE	3.184	11.73	
	BISS	0.477	1.42	
	ENDAT	0.841	2.839	
	TFMTE	0.504	1.515	
	AFMTE	0.714	2.44	
	CAN2	0.739	2.5	
	CAN1	0.681	2.429	
	CAN0	0.702	2.399	

(1) Value guaranteed by sample, not 100% tested in production.

(2) If there is no other description, then HXTAL = 25 MHz, f_{HCLK}= f_{CPU} / 2, f_{APB1} = f_{HCLK} / 2, f_{APB2} = f_{HCLK1}, f_{APB3} = f_{HCLK} / 2, f_{APB4} = f_{HCLK} / 2.

4.10. EMC characteristics

System level ESD (Electrostatic discharge, according to IEC 61000-4-2) and EFT (Electrical Fast Transient/burst, according to IEC 61000-4-4) testing result is given in the ***Table 4-21. System level ESD and EFT characteristics(1)***. System level ESD is for end-customer operation, it includes ESD field events on system level occur in an unprotected area (outside EPA). System level ESD protection necessary to satisfy higher ESD levels.

Table 4-21. System level ESD and EFT characteristics(1)(2)

Symbol	Description	Conditions	Package	Class	Level
V_{ESD}	Contact / Air mode high voltage stressed on few special I/O pins	V_{DD} = 3.3 V, T_A = 25 °C, f_{CK_SYS} = 600 MHz IEC 61000-4-2	BGA176	CD 8KV AD 15KV	4A
V_{EFT}	Fast transient high voltage burst stressed on Power and GND	V_{DD} = 3.3 V, T_A = 25 °C, f_{CK_SYS} = 600 MHz IEC 61000-4-4	BGA176	4KV	4A

(1) Value guaranteed by sample, not 100% tested in production

(2) The explanation of the evaluation methods for system-level ESD and system-level EFT test methods and test levels can be referred to in AN127 and AN128.

EMI (Electromagnetic Interference) emission test result is given in the ***Table 4-22. EMI***

characteristics(1), The electromagnetic field emitted by the device are monitored while an application, executing EEMBC code, is running. The test is compliant with SAE J1752-3 standard which specifies the test board and the pin loading.

Table 4-22. EMI characteristics(1)(2)

Symbol	Parameter	Conditions	Package	Mode	Max vs. [f_{HXTAL} / f_{SYS}] 25 / 600 MHz				Unit
					0.1-30MHz	30-130MHz	130MHz-1GHz	1-3GHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, f_{CPU} = 600 MHz, conforms to SAE J1752-3	BGA176	SMPS supply	5.62	9.11	10.81	6.82	dBµV
				Bypass supply	2.52	1.58	4.23	7.40	

(1) Value guaranteed by sample, not 100% tested in production.

(2) The explanation of the chip-level EMI test methods can be referred to in AN125.

Component level ESD include HBM (Human body model, according to ANSI/ESDA/JEDEC JS-001) and CDM (ANSI/ESDA/JEDEC JS-002), that ESD field events during manufacturing in an ESD protected area, such as PCB assembly/repair, IC assembly/test and Fab environment. The ESD protected area (EPA) has many measures, for instance ESD protective packaging, grounding person wrist strap to ground (or flooring/footwear), grounded work surface and ionizer.

Static latch-up (LU, according to JEDEC78) test is based on the two measurement methods, I/O current injection value (I-test) and power supply over-voltage value.

Table 4-23. Component level ESD and latch-up characteristics(1)(2)

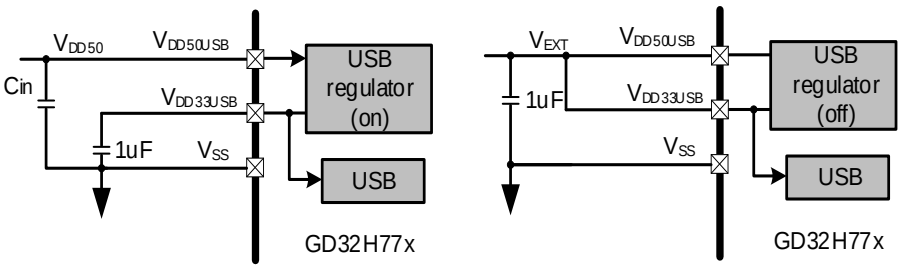
Symbol	Description	Conditions	Package	Max	Unit	Level
V_{HBM}	Human body model electrostatic discharge voltage	T_A = 25 °C, JS-001	BGA176	2000	V	2
V_{CDM}	Charge device model electrostatic discharge voltage (All pins)	T_A = 25 °C, JS-002	BGA176	500	V	C2a
LU	I-test	T_A = 125°C, JESD78	BGA176	200	mA	Class II Level A
	V_{supply} over voltage			5.4	V	

(1) Value guaranteed by sample, not 100% tested in production.

(2) The levels of system-level ESD and chip-level ESD are not related. The differences between the two can be referred to in AN159.

4.11. Embedded USB regulator characteristics

Figure 4-6. External components for USB regulator (1)



(1) When the USB regulator is not used, if VDD33USB is connected to VDD, it is required that 3V <= VDD <= 3.6V.

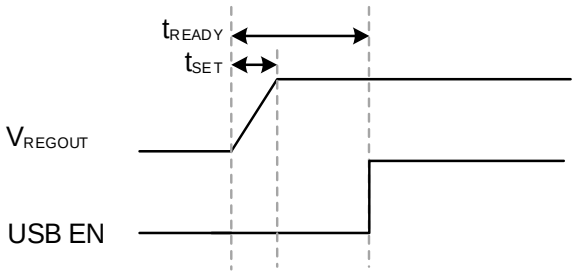
Table 4-24. USB regulator characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD50USB}$	Supply voltage	-	4	5	5.5	V
$I_{DD50USB}$(2)	Current consumption at no load	-	-	28	-	μA
$V_{REGOUT(V3.3V)}$	Regulated output voltage	-	3	3.3	3.6	V
I_{OUT}	Output current load sinked by USB block	-	-	-	40	mA
t_{SET}	V_{REGOUT} setting time	-	-	75	88	μs
t_{READY}	V_{REGOUT} ready time	-	-	400	791	μs

(1) Value guaranteed by design, not 100% tested in production.

(2) Input current of USB regulator at no load.

Figure 4-7. USB regulator power-up timing diagram



4.12. Embedded DSI regulator characteristics

Figure 4-8. External components for DSI regulator

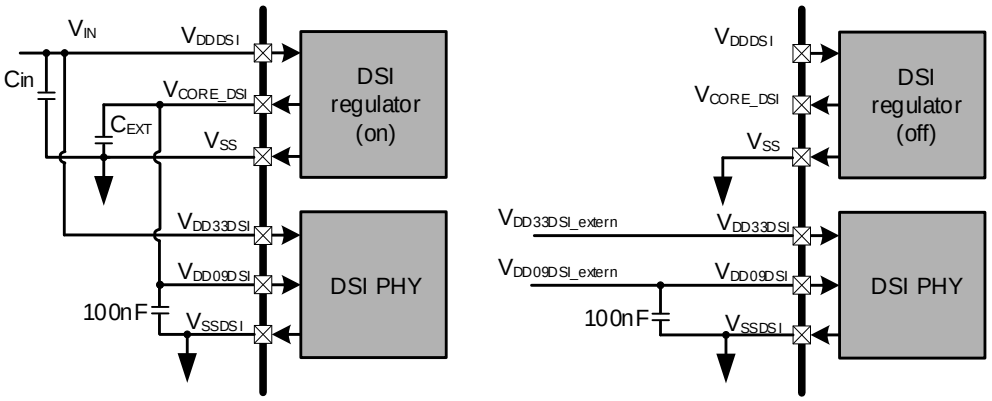


Table 4-25. DSI regulator characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDDSI}	Supply voltage	-	1.71	3.3	3.6	V
$V_{DD33DSI}$	Supply DSI analog high voltage area	-	1.71	3.3	3.6	V
I_{DDDSI}	Current consumption at no load	-	-	112	-	μA
V_{CORE_DSI}	Regulated output voltage	-	0.85	0.9	0.95	V
C_{EXT}	External capacitor on V_{CORE_DSI}	-	1.1	2.2	3.3	μF
I_{LOAD}	Output current load	-	-	-	50	mA
T_{WKUP}(2)	V_{CORE_DSI} setting time	-	-	182	-	μs
I_{INRUSH}	Inrush current on voltage regulator power-on	C_{EXT} = 2.2uF	-	45	65	mA

(1) Value guaranteed by design, not 100% tested in production.

(2) The time from the enable signal issuance to the voltage ready signal.

4.13. Typical SMPS efficiency versus load current and temperature

Figure 4-9. Typical SMPS efficiency (%) vs load current(A) in Run mode at T_J = 25 °C

when V_{FBSMPS} = 0.9 V

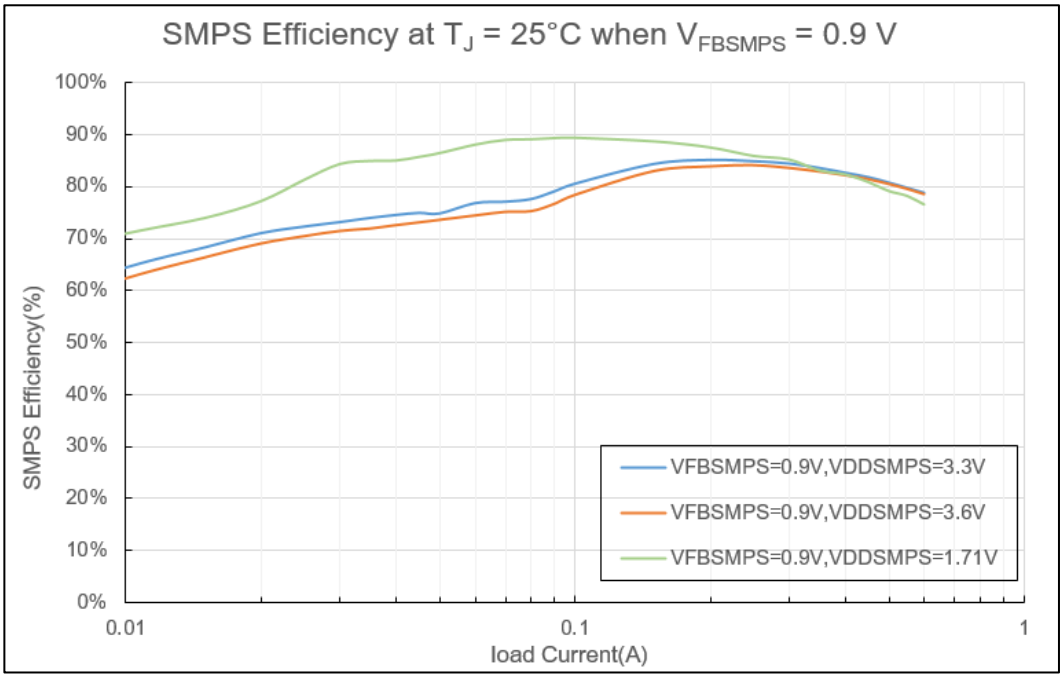


Figure 4-10. Typical SMPS efficiency (%) vs load current(A) in Run mode at T_J = -40 °C when V_{FBSMPS} = 0.9 V

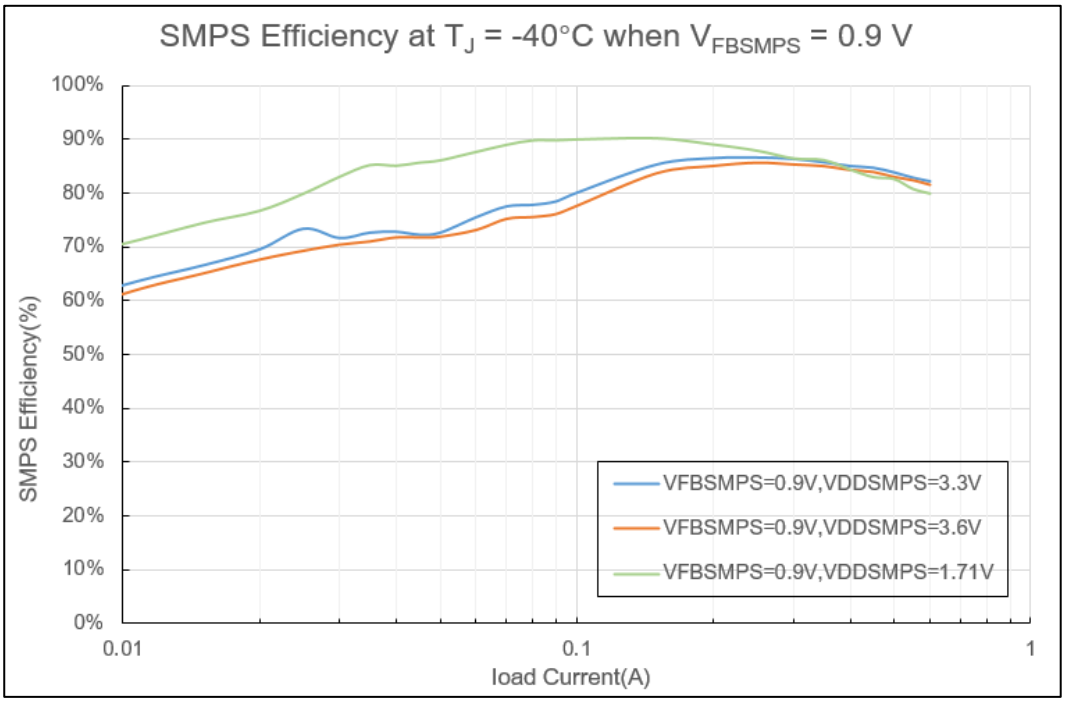
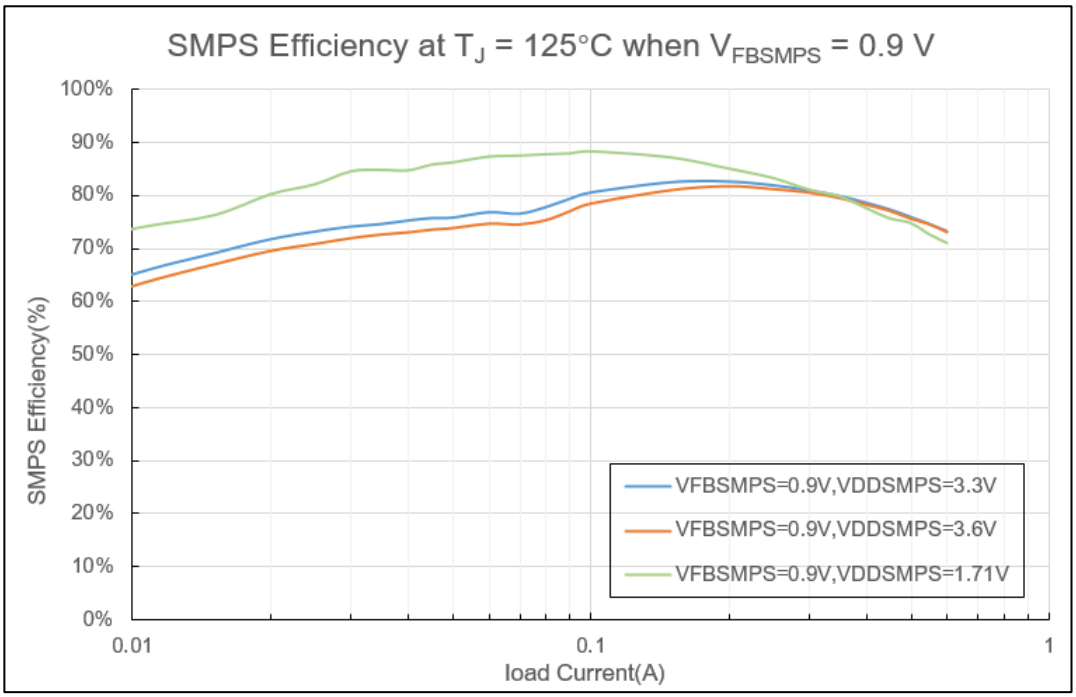


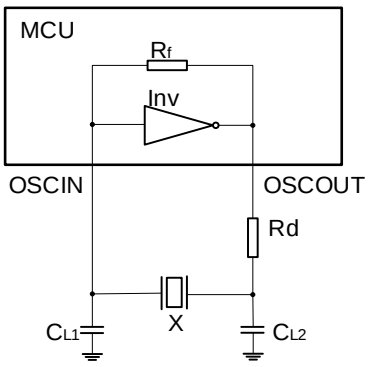
Figure 4-11. Typical SMPS efficiency (%) vs load current(A) in Run mode at T_J = 125 °C

when V_{FBSMPS} = 0.9 V



4.14. External clock characteristics

Figure 4-12. Internal structure diagram of OSCIN and OSCOUT pin



It is strongly recommended to meature the oscillation allowance (negative resistance) in the final target system (layout) to determine which load capacitors will best tune their resonator/crystal to the microcontroller device for optimum start-up and operation over temperature/voltage extremes.

Table 4-26. High speed external clock (HXTAL) generated from a crystal/ceramic characteristics(1)(4)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{HXTAL}	Crystal or ceramic frequency	1.71 V <= V_{DD} <= 3.6 V	4	25	50	MHz
R_F	Feedback resistor	V_{DD} = 3.3 V	-	400	-	kΩ
C_{HXTAL}(2)	Recommended matching capacitance on OSCIN and OSCOUT	-	-	20	30	pF
$Duty_{HXTAL}$	Crystal or ceramic duty cycle	-	30	50	70	%
g_m	Oscillator transconductance	Startup	-	27	-	mA/V
$I_{DD(HXTAL)}$	Crystal or ceramic operating current	-	-	0.85	-	mA
$t_{ST(HXTAL)}$(3)	Crystal or ceramic startup time	-	-	450	-	ms

(1) Value guaranteed by design, not 100% tested in production.

(2) C_{HXTAL1} = C_{HXTAL2} = 2*(C_{LOAD} - C_S), For C_{HXTAL1} and C_{HXTAL2}, it is recommended matching capacitance on OSCIN and OSCOUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

(3) $t_{ST(HXTAL)}$ is the startup time measured from the moment it is enabled (by software) to the 32 MHz oscillator stabilization flags is SET. This value varies significantly with the crystal manufacturer.

(4) More details about g_m could be found in ***AN052 GD32 MCU Resonator-Based Clock Circuits.***

Table 4-27. High speed external clock characteristics (HXTAL in bypass mode)(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{HXTAL_ext}	External clock source or oscillator frequency	-	1	-	50	MHz
$V_{H(HXTAL)}$	OSCIN input pin high level voltage	-	0.7V_{DD}	-	V_{DD}	V
$V_{L(HXTAL)}$	OSCIN input pin low level voltage		V_{SS}	-	0.3V_{DD}	V
$t_{H/L(HXTAL)}$	OSCIN high or low time	-	5	-	-	ns
$t_{R/F(HXTAL)}$	OSCIN rise or fall time	-	-	-	10	ns
C_{IN}	OSCIN input capacitance	-	40	-	60	pF
$Duty_{HXTAL}$	Duty cycle	-	1	-	50	%

(1) Value guaranteed by design, not 100% tested in production.

Table 4-28. Low speed external clock (LXTAL) generated from a crystal/ceramic

characteristics (1)(4)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{LXTAL}	Crystal or ceramic frequency	-	-	32.768	-	kHz
R_F	Internal feedback resistor	-	-	10	-	MΩ
C_{LXTAL}(2)	Recommended matching capacitance on OSC32IN and OSC32OUT	-	-	10	-	pF
$Duty_{LXTA}$	Crystal or ceramic duty cycle	-	30	-	70	%
g_m	Oscillator transconductance	LXTALDRI[1:0] = 00	-	5	6.3	μA/V
		LXTALDRI[1:0] = 01	-	7.5	9.3	
		LXTALDRI[1:0] = 10	-	14.8	18.5	
		LXTALDRI[1:0] = 11	-	22.2	27.8	
$I_{DD(LXTAL)}$	Crystal or ceramic operating current	LXTALDRI[1:0] = 00	-	0.5	-	μA
		LXTALDRI[1:0] = 01	-	0.6	-	
		LXTALDRI[1:0] = 10	-	0.9	-	
		LXTALDRI[1:0] = 11	-	1.2	-	
$t_{ST(LXTAL)}$ (3)	Crystal or ceramic startup time	LXTALDRI[1:0] = 00	-	350	-	ms
		LXTALDRI[1:0] = 01	-	260	-	
		LXTALDRI[1:0] = 10	-	200	-	
		LXTALDRI[1:0] = 11	-	180	-	

(1) Value guaranteed by design, not 100% tested in production.

(2) $C_{LXTAL1} = C_{LXTAL2} = 2*(C_{LOAD} - C_S)$, For C_{LXTAL1} and C_{LXTAL2}, it is recommended matching capacitance on OSC32IN and OSC32OUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

(3) $t_{ST(LXTAL)}$ is the startup time measured from the moment it is enabled (by software) to the 32.768 kHz oscillator stabilization flags is SET. This value varies significantly with the crystal manufacturer.

(4) More details about gm could be found in ***AN052 GD32 MCU Resonator-Based Clock Circuits.***

Table 4-29. Low speed external user clock characteristics (LXTAL in bypass mode) (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{LXTAL_ext}	External clock source or oscillator frequency	1.71 V <= V_{DD} <= 3.6 V	-	32.768	1000	kHz
$V_{H(LXTAL)}$	OSC32IN input pin high level voltage	-	0.7V_{DD}	-	V_{DD}	V
$V_{L(LXTAL)}$	OSC32IN input pin low level voltage	-	V_{SS}	-	0.3V_{DD}	
$t_{H/L(LXTAL)}$	OSC32IN high or low time	-	450	-	-	ns
$t_{R/F(LXTAL)}$	OSC32IN rise or fall time	-	-	-	50	
C_{IN}	OSC32IN input capacitance	-	-	5	-	pF
$Duty_{LXTAL}$	Duty cycle	-	30	50	70	%

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-13. Recommended external OSCIN and OSCOUT pins circuit for crystal

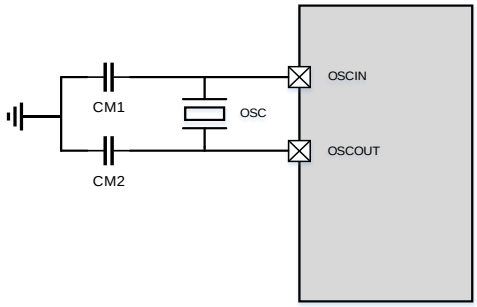
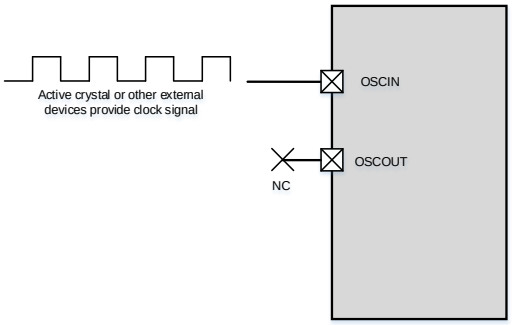


Figure 4-14. Recommended external OSCIN and OSCOUT pins circuit for oscillator



4.15. Internal clock characteristics

Table 4-30. High speed internal clock (IRC48M) characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{IRC48M}	High Speed Internal Oscillator (IRC48M) frequency	V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C	-	48	-	MHz
$Drift_{IRC48M}$	IRC48M oscillator Frequency drift, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +105 °C (2)	-3	-	+3	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C (3)	-1	-	+1	%
$Trim_{IRC48M}$	IRC48M oscillator Frequency drift, User trimming step	V_{DD} = V_{DDA} = 3.3 V	-	0.14	-	%
$Duty_{IRC48M}$	IRC48M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V	45	50	55	%
$I_{DDA(IRC48M)}$	IRC48M oscillator operating current	f_{IRC48M} = 48 MHz	-	300	-	μA
$t_{ST(IRC48M)}$	IRC48M oscillator startup time	f_{IRC48M} = 48 MHz	-	2.5	-	μs

(1) Value guaranteed by design, not 100% tested in production.
(2) Value guaranteed by characterization, not 100% tested in production.
(3) Value guaranteed by production.

Table 4-31. High speed internal clock (IRC64M) characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{IRC64M}	High Speed Internal Oscillator (IRC64M) frequency	V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C	-	64	-	MHz
$Drift_{IRC64M}$	IRC64M oscillator Frequency drift, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +105 °C (2)	-2.5	-	2.5	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C (3)	-1	-	+1	%
$Duty_{IRC64M}$	IRC64M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V	45	50	55	%
$I_{DDA(IRC64M)}$	IRC64M oscillator operating current	f_{IRC64M} = 64 MHz	-	500	-	μA
$t_{ST(IRC64M)}$	IRC64M oscillator startup time	f_{IRC64M} = 64 MHz	-	2.5	-	μs

(1) Value guaranteed by design, not 100% tested in production.
(2) Value guaranteed by characterization, not 100% tested in production.
(3) Value guaranteed by production.

Table 4-32. Low power internal clock (LPIRC4M) characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{LPIRC4M}$	High Speed Internal Oscillator (LPIRC4M) frequency	V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C	-	4	-	MHz
$Drift_{LPIRC4M}$	LPIRC4M oscillator Frequency accuracy, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +105 °C (2)	-2	-	+2	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C (3)	-1	-	+1	%
$Duty_{LPIRC4M}$	LPIRC4M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V	45	50	55	%
$I_{DDALPIRC4M}$	LPIRC4M oscillator operating current	$f_{LPIRC4M}$ = 4 MHz	-	42	-	μA
$t_{SULPIRC4M}$	LPIRC4M oscillator startup time	$f_{LPIRC4M}$ = 4 MHz	-	1.1	-	μs

(1) Value guaranteed by design, not 100% tested in production.
(2) Value guaranteed by characterization, not 100% tested in production.
(3) Value guaranteed by production.

Table 4-33. Low speed internal clock (IRC32K) characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{IRC32K}	Low Speed Internal oscillator (IRC32K) frequency	V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C	-	32	-	kHz
$Drift_{IRC32K}$	IRC32K oscillator Frequency accuracy, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +105 °C (2)	29.4	-	34.6	kHz
		V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C (3)	30	-	34	kHz
$I_{DDAIRC32K}$	IRC32K oscillator operating current	-	-	0.19	-	μA
$t_{SULPIRC32K}$	IRC32K oscillator startup time	-	-	60	-	μs

(1) Value guaranteed by design, not 100% tested in production.
(2) Value guaranteed by characterization, not 100% tested in production.
(3) Value guaranteed by production.

4.16. PLL characteristics

Table 4-34. PLL0/1/2 characteristics (wide VCO frequency range) (1)

Symbol	Description	Conditions		Min	Typ	Max	Unit
$f_{IN(PLL)}$	PLL input clock frequency	-		2	-	16	MHz
	PLL input clock duty cycle	-		10	-	90	%
f_{VCO}	PLL VCO output clock frequency	-		100	-	850	MHz
$t_{LK(PLL)}$	PLL lock time	-		-	200	500	μs
$I_{DDA(PLL)}$	Current consumption from V_{DDA}	VCO freq = 800 MHz		-	1.6	-	μA
J_{PLL}	Cycle to cycle Jitter (rms)	f_{PLL_OUT} = f_{VCO_OUT} / 10	f_{VCO_OUT}= 100 MHz	-	110	-	ps
			f_{VCO_OUT}= 400 MHz	-	19	-	
			f_{VCO_OUT}= 800 MHz	-	15	-	
	Cycle to cycle Jitter (peak to peak)	f_{PLL_OUT} = f_{VCO_OUT} / 10	f_{VCO_OUT}= 100 MHz	-	900	-	ps
			f_{VCO_OUT}= 400 MHz	-	150	-	
			f_{VCO_OUT}= 800 MHz	-	120	-	
	Period jitter(rms)	f_{PLL_OUT} = f_{VCO_OUT} / 10	f_{VCO_OUT}= 100 MHz	-	90	-	ps
			f_{VCO_OUT}= 400 MHz	-	12	-	
			f_{VCO_OUT}= 800 MHz	-	8	-	
	Period jitter(peak to peak)	f_{PLL_OUT} = f_{VCO_OUT} / 10	f_{VCO_OUT}= 100 MHz	-	750	-	ps
			f_{VCO_OUT}= 400 MHz	-	100	-	
			f_{VCO_OUT}= 800 MHz	-	70	-	

(1) Value guaranteed by design, not 100% tested in production.

Table 4-35. PLL0/1/2 characteristics (narrow VCO frequency range) (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{IN(PLL)}$	PLL input clock frequency	-	1	-	2	MHz
	PLL input clock duty cycle	-	10	-	90	%
f_{VCO}	PLL VCO output clock frequency	-	100	-	500	MHz

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{LK(PLL)}$	PLL lock time	-		-	200	500	µs
$I_{DDA(PLL)}$	Current consumption on V_{DDA}	VCO freq = 500 MHz		-	1.1	-	mA
J_{PLL}	Cycle to cycle Jitter(rms)	f_{PLL_OUT} = f_{VCO_OUT} / 10	f_{VCO_OUT} = 500 MHz	-	16	-	ps
	Cycle to cycle Jitter(peak to peak)		f_{VCO_OUT} = 500 MHz	-	140	-	
	Period jitter(rms)	f_{PLL_OUT} = f_{VCO_OUT} / 10	f_{VCO_OUT} = 500 MHz	-	10	-	ps
	Period jitter(peak to peak)		f_{VCO_OUT} = 500 MHz	-	90	-	

(1) Value guaranteed by design, not 100% tested in production.

Table 4-36. PLLUSBHS characteristics (1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{IN(PLL)}$	PLL input clock frequency	-	4	-	30	MHz
$f_{OUT(PLL)}$	PLL output clock frequency	-	-	480	-	MHz
f_{VCO}	PLL VCO output clock frequency	-	-	480	-	MHz
$t_{LK(PLL)}$	PLL lock time	-	-	160	520	µs
$I_{DD33USB(PLL)}$	Current consumption on $V_{DD33USB}$	-	-	1.7	-	mA
J_{PLL}	Cycle to cycle Jitter(rms)	System clock	-	15	-	ps
	Cycle to cycle Jitter (peak to peak)		-	170	-	
	Period jitter(rms)		-	10	-	ps
	Period jitter(peak to peak)		-	135	-	

(1) Value guaranteed by design, not 100% tested in production.

(2) Value given with main PLL running.

4.17. Memory characteristics

Table 4-37. Code non-volatile memory characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
$I_{DD(CNVM)}$(2)	Average supply current from V_{DD} during code non-volatile memory operation, VDD = 3.3 V	Code non-volatile memory write 256-bit mode, form 0x55…55 to 0xAA…AA	-	18	-	mA
PE_{CYC}(1)	Number of guaranteed program / erase cycles before failure (Endurance)	T_J = -40 °C ~ +125 °C	10	-	-	kcycles
t_{RET}(1)	Data retention time	T_J = 125 °C after up to 10 kcycles	10	-	-	years
N_{WS}(1)(3)	Code non-volatile memory wait states	64 MHz < f_{HCLK} <= 99 MHz	-	1	-	HCLK cycles
		100 MHz < f_{HCLK} <= 149 MHz	-	2	-	
		f_{HCLK} =300 MHz	-	5	-	
t_{PROG}(2)(4)	Code non-volatile memory word programming time	Programming 256-bit data, with 128 bits written from 0 to 1	-	76	-	µs
		Programming 256-bit data, with 256 bits written from 0 to 1	-	76	-	
		Programming 256-bit data, with 256 bits written from 0x55…55 to 0xAA…AA	-	170	-	
$t_{SER(64K)}$(2)	Code non-volatile memory Sector erase time	-	-	0.082	-	s
t_{MER}	Mass erase time	-	-	2.66(2)	-	s

(1) Value guaranteed by design, not 100% tested in production.

(2) Value guaranteed by sample, not 100% tested in production.

(3) The WSCNT bits in the NVMC_PERFCTL register needs to be configured correctly depend on the AHB clock frequency when reading the memory.

(4) For memory range outside the Data Integrity Enhancement area, please refer to this data. For the memory range within the Data Integrity Enhancement area, please refer to ECNVM t_{PROG}.

Table 4-38. Extended code non-volatile memory characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
$I_{DD(ECNVM)}$(2)	Average supply current from V_{DD} during extended code non-volatile memory operation, VDD = 3.3 V	Extended code non-volatile memory write 256-bit mode, form 0xFF…FF to 0x00…00	-	13	-	mA
PE_{CYC}(1)	Number of guaranteed program /erase cycles before failure (Endurance)	T_J = -40 °C ~ +125 °C	100	-	-	kcycles
t_{RET}(1)	Data retention time	T_A = 70 °C after up to 0 kcycles	-	20	-	years
$t_{PROG(64bit)}$(2)	Extended code non-volatile memory 64-bit programming time	-	-	117	360	µs
$t_{PROG(256bit)}$(2)	Extended code non-volatile memory 256-bit programming time	-	-	447	1080	µs
$t_{PER(4K)}$	Page erase time	-	-	27(2)	1200(1)	ms
$t_{SER(64K)}$	Sector erase time	-	-	0.121(2)	6(1)	s
t_{MER}(1)	Mass erase time	-	-	-	$t_{SER(64K)}$* number of sectors	s

(1) Value guaranteed by design, not 100% tested in production.
(2) Value guaranteed by sample, not 100% tested in production.

4.18. NRST pin characteristics

Table 4-39. NRST pin characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST Input low level voltage	-	-0.3	-	0.3V_{DD}	V
$V_{IH(NRST)}$	NRST Input high level voltage	-	0.7V_{DD}	-	V_{DD}+0.3	
V_{HYST}	Schmidt trigger Voltage hysteresis	V_{DD} = V_{DDA} = 1.71 V	-	300	-	mV
		V_{DD} = V_{DDA} = 3.3 V	-	280	-	
		V_{DD} = V_{DDA} = 3.6 V	-	295	-	
R_{PU}	Pull-up equivalent resistor	V_{IN} = V_{SS}	-	40	-	kΩ
t_{Pulse_glitch}	NRST pin glitch pulse duration	-	-	-	100	ns
t_{Pulse_reset}	NRST pin reset pulse duration	-	350	-	-	
t_{Reset}	Reset stretch time	-	20	-	-	us
t_{NRST_delay}	System reset delay time	-	-	-	145	ns

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-15. NRST pin level and system reset timing diagram

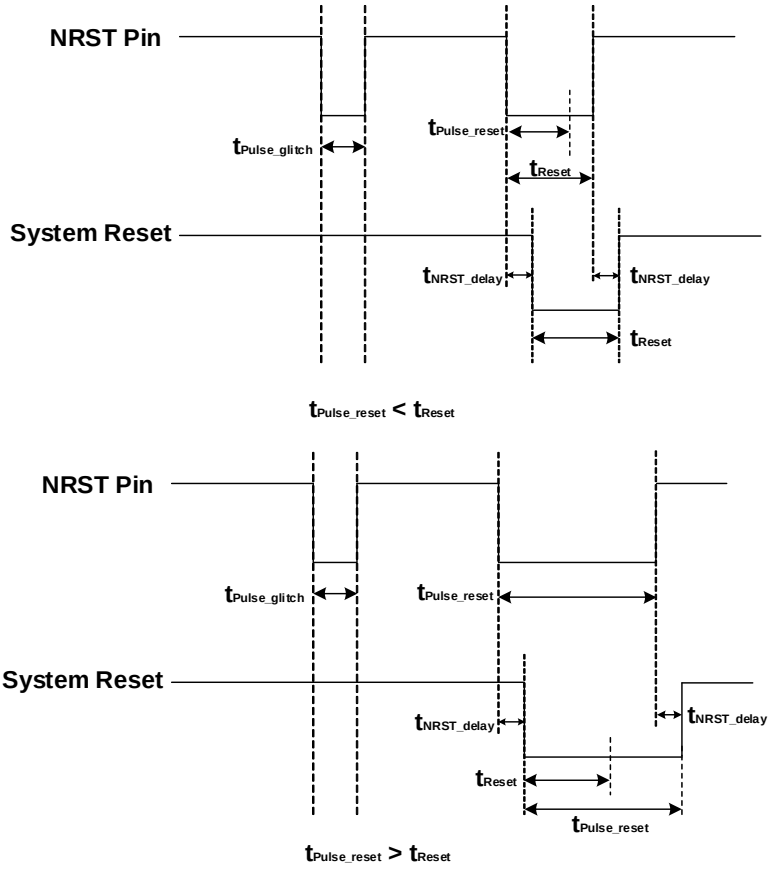
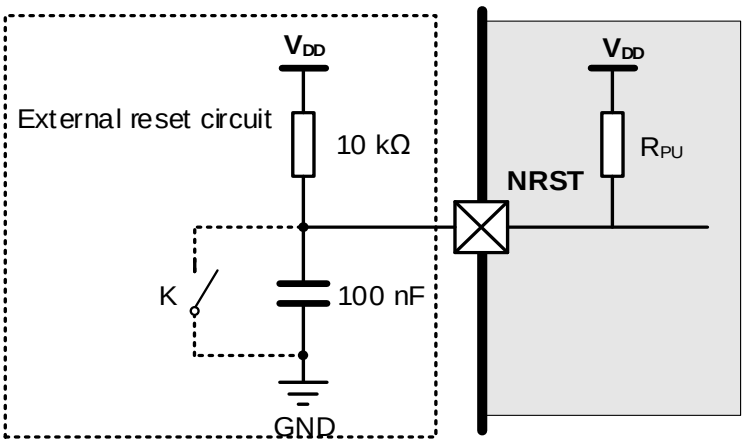


Figure 4-16. Recommended external NRST pin circuit(1)



(1) Unless the voltage on NRST pin go below $V_{IL(NRST)}$ level, the device would not generate a reliable reset.

4.19. GPIO current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below VSS or above VDD (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation.

However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures. The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the -5 μA/+0 μA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Table 4-40. GPIO current injection susceptibility(1)

Symbol	Description		Functional susceptibility		Unit
			Negative injection	Positive injection	
I_{INJ}(1)	Injected current on pin	Input current on 5V tolerant pin	-5	-	mA
		Input current on other I/O(Except PA0、PA1、PC2、PC3、PC10、PC9、PC6、PB6)	-5	-	
		PA0、PA1、PC2、PC3、PC10、PC9、PC6、PB6	-5	0	

(1) Value guaranteed by design, not 100% tested in production.

4.20. GPIO characteristics

More details about GPIO could be found in ***AN092 GD32 MCU GPIO structure and precautions***.

Table 4-41. I/O static characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{IL}(1)	Standard IO low level input voltage	1.71 V < V_{DD} = V_{DDA} < 3.6 V	-	-	0.3V_{DD}	V
	5V-tolerant IO low level input voltage	1.71V < V_{DD} = V_{DDA} < 3.6 V	-	-	0.3V_{DD}	V
V_{IH}(1)	Standard IO high level input voltage	1.71 V < V_{DD} = V_{DDA} < 3.6 V	0.7V_{DD}	-	-	V
	5V-tolerant IO high level input voltage	1.71V < V_{DD} = V_{DDA} < 3.6 V	0.7V_{DD}	-	-	V
V_{HYS}(1)	Input hysteresis	VDD = 3.3V	-	300	-	mV
I_{LEAK}(2)	Input leakage current	V_{SS} <= V_{IN} <= V_{DD}	-	-	+/-2	uA

Symbol	Description	Conditions	Min	Typ	Max	Unit
R_{PU}(1)	Weak pull-up equivalent resistor	$V_{IN} = V_{SS}$	-	40	-	kΩ
R_{PD}(1)	Weak pull-down equivalent resistor	$V_{IN} = V_{DD}$	-	40	-	kΩ
C_{IO}(1)	I/O pin capacitance	-	-	5	-	pF

(1) Value guaranteed by design, not 100% tested in production.

(2) Value guaranteed by production.

Table 4-42. Output voltage characteristics for all I/Os except PC13, PC14, PC15(1)(2)

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{OL} (IO_speed=max)	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.71 V	-	0.12	-	V
		V_{DD} = 3.3 V	-	0.08	-	
		V_{DD} = 3.6 V	-	0.075	-	
	Low level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 1.71 V	-	0.28	-	
		V_{DD} = 3.3 V	-	0.16	-	
		V_{DD} = 3.6 V	-	0.15	-	
V_{OH} (IO_speed=max)	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.71V	-	1.59	-	
		V_{DD} = 3.3 V	-	3.22	-	
		V_{DD} = 3.6 V	-	3.53	-	
	High level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 1.71V	-	1.43	-	
		V_{DD} = 3.3 V	-	3.12	-	
		V_{DD} = 3.6 V	-	3.43	-	
V_{OL} (IO_speed=85MHz)	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.71 V	-	0.16	-	V
		V_{DD} = 3.3 V	-	0.09	-	
		V_{DD} = 3.6 V	-	0.08	-	
	Low level output voltage for an IO Pin (I_{IO} = +16 mA)	V_{DD} = 1.71 V	-	0.34	-	
		V_{DD} = 3.3 V	-	0.18	-	
		V_{DD} = 3.6 V	-	0.17	-	
V_{OH} (IO_speed=85MHz)	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.71 V	-	1.54	-	
		V_{DD} = 3.3 V	-	3.2	-	
		V_{DD} = 3.6 V	-	3.5	-	
	High level output voltage for an IO Pin (I_{IO} = +16 mA)	V_{DD} = 1.71 V	-	1.35	-	
		V_{DD} = 3.3 V	-	3.09	-	
		V_{DD} = 3.6 V	-	3.4	-	
V_{OL} (IO_speed=60MHz)	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.71 V	-	0.18	-	V
		V_{DD} = 3.3 V	-	0.1	-	
		V_{DD} = 3.6 V	-	0.09	-	
	Low level output voltage for an IO Pin (I_{IO} = +16 mA)	V_{DD} = 1.71 V	-	0.41	-	
		V_{DD} = 3.3 V	-	0.2	-	
		V_{DD} = 3.6 V	-	0.19	-	
V_{OH} (IO_speed=60MHz)	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.71 V	-	1.51	-	
		V_{DD} = 3.3 V	-	3.18	-	
		V_{DD} = 3.6 V	-	3.49	-	

Symbol	Description	Conditions	Min	Typ	Max	Unit
	High level output voltage for an IO Pin (I_{IO} = +16 mA)	V_{DD} = 1.71 V	-	1.28	-	
		V_{DD} = 3.3 V	-	3.06	-	
		V_{DD} = 3.6 V	-	3.37	-	
V_{OL} (IO_speed=12MHz)	Low level output voltage for an IO Pin (I_{IO} = +1 mA)	V_{DD} = 1.71 V	-	0.07	-	V
		V_{DD} = 3.3 V	-	0.03	-	
		V_{DD} = 3.6 V	-	0.03	-	
	Low level output voltage for an IO Pin (I_{IO} = +4 mA)	V_{DD} = 1.71 V	-	0.27	-	
		V_{DD} = 3.3 V	-	0.14	-	
		V_{DD} = 3.6 V	-	0.13	-	
V_{OH} (IO_speed=12MHz)	High level output voltage for an IO Pin (I_{IO} = +1 mA)	V_{DD} = 1.71 V	-	1.64	-	V
		V_{DD} = 3.3 V	-	3.26	-	
		V_{DD} = 3.6 V	-	3.56	-	
	High level output voltage for an IO Pin (I_{IO} = +4 mA)	V_{DD} = 1.71 V	-	1.42	-	
		V_{DD} = 3.3 V	-	3.14	-	
		V_{DD} = 3.6 V	-	3.45	-	

(1) Value guaranteed by sample, not 100% tested in production.

(2) All pins except PC13 / PC14 / PC15. Since PC13 to PC15 are supplied through the Power Switch, which can only be obtained by a small current(typical source capability:3 mA shared between these Ios, but sink capability is same as other IO), the speed of GPIOs PC13 to PC15 should not exceed 2 MHz when they are in output mode (maximum load: 30 pF).

Table 4-43. I/O port AC characteristics(IOSPDOP OFF)(1)(3)(4)

Speed	Symbol	Description	Conditions	Min	Typ	Max	Unit
00	t_R/t_F (2)	Output high to low level fall time and output low to high level rise time	2.7 V<= VDD<= 3.6 V, C_L = 50 pF	-	-	10	ns
			1.71 V<= VDD<= 2.7 V, C_L = 50 pF	-	-	20	
			2.7 V<= VDD<= 3.6 V, C_L = 30 pF	-	-	7.6	
			1.71 V<= VDD<= 2.7 V, C_L = 30 pF	-	-	14	
			2.7 V<= VDD<= 3.6 V, C_L = 10 pF	-	-	5	
			1.71 V<= VDD<= 2.7 V, C_L = 10 pF	-	-	10	
01	t_R/t_F (2)	Output high to low level fall time and output low to high level rise time	2.7 V<= VDD<= 3.6 V, C_L = 50 pF	-	-	4	ns
			1.71 V<= VDD<= 2.7 V, C_L = 50 pF	-	-	7	
			2.7 V<= VDD<= 3.6 V, C_L = 30 pF	-	-	2.9	
			1.71 V<= VDD<= 2.7 V, C_L = 30 pF	-	-	5	
			2.7 V<= VDD<= 3.6 V, C_L = 10	-	-	1.8	

Speed	Symbol	Description	Conditions	Min	Typ	Max	Unit
			pF				
			1.71 V<= VDD<= 2.7 V, C_L = 10 pF	-	-	3.5	
10	t_R/t_F (2)	Output high to low level fall time and output low to high level rise time	2.7 V<= VDD<= 3.6 V, C_L = 50 pF	-	-	3.1	ns
			1.71 V<= VDD<= 2.7 V, C_L = 50 pF	-	-	5	
			2.7 V<= VDD<= 3.6 V, C_L = 30 pF	-	-	2.2	
			1.71 V<= VDD<= 2.7 V, C_L = 30 pF	-	-	3.8	
			2.7 V<= VDD<= 3.6 V, C_L = 10 pF	-	-	1.5	
			1.71 V<= VDD<= 2.7 V, C_L = 10 pF	-	-	2.5	
11	t_R/t_F (2)	Output high to low level fall time and output low to high level rise time	2.7 V<= VDD<= 3.6 V, C_L = 50 pF	-	-	2.3	ns
			1.71 V<= VDD<= 2.7 V, C_L = 50 pF	-	-	3.5	
			2.7 V<= VDD<= 3.6 V, C_L = 30 pF	-	-	1.8	
			1.71 V<= VDD<= 2.7 V, C_L = 30 pF	-	-	2.7	
			2.7 V<= VDD<= 3.6 V, C_L = 10 pF	-	-	1.2	
			1.71 V<= VDD<= 2.7 V, C_L = 10 pF	-	-	1.6	

(1) The maximum frequency is defined with the following conditions: (tr+tf) <= 2/3 T Skew <= 1/20 T 45%<Duty cycle<55%

(2) The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.

(3) Value guaranteed by design, not 100% tested in production.

(4) The data is for reference only, and the specific values are related to PCB Layout.

Table 4-44. I/O port AC characteristics (IOSPDOP ON)(1)(3)(4)

Speed	Symbol	Description	Conditions	Min	Typ	Max	Unit
00	tr/tf(2)	Output high to low level fall time and output low to high level rise time	1.71 V<= VDD<=2.7 V, C_L = 50 pF	-	-	13	ns
			1.71 V<= VDD<=2.7 V, C_L = 30 pF	-	-	15	
			1.71 V<= VDD<=2.7 V, C_L = 10 pF	-	-	20	
01	tr/tf(2)	Output high to low level fall time and	1.71 V<= VDD<=2.7 V, C_L = 50 pF	-	-	6.4	ns

Speed	Symbol	Description	Conditions	Min	Typ	Max	Unit
		output low to high level rise time	1.71 V<= VDD<=2.7 V, C_L = 30 pF	-	-	4.8	
			1.71 V<= VDD<=2.7 V, C_L = 10 pF	-	-	3	
10	tr/tf(2)	Output high to low level fall time and output low to high level rise time	1.71 V<= VDD<=2.7 V, C_L = 50 pF	-	-	5	ns
			1.71 V<= VDD<=2.7 V, C_L = 30 pF	-	-	3.6	
			1.71 V<= VDD<=2.7 V, C_L = 10 pF	-	-	2.3	
11	tr/tf(2)	Output high to low level fall time and output low to high level rise time	1.71 V<= VDD<=2.7 V, C_L = 50 pF	-	-	4.3	ns
			1.71 V<= VDD<=2.7 V, C_L = 30 pF	-	-	3.2	
			1.71 V<= VDD<=2.7 V, C_L = 10 pF	-	-	1.8	

(1) The maximum frequency is defined with the following conditions: (tr+tf) <= 2/3 T Skew <= 1/20 T 45%<Duty cycle<55%.

(2) The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.

(3) Value guaranteed by design, not 100% tested in production.

(4) The data is for reference only, and the specific values are related to PCB Layout.

4.21. Internal reference voltage characteristics

Table 4-45. Internal reference voltage characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	T_A = -40 °C ~ +105 °C (2)	1.18	1.2	1.22	V
		T_A = 25 °C (3)	1.18	1.2	1.22	
$t_{S_VREFINT}$(4)	ADC sampling time when reading the internal reference voltage	-	5	-	-	µs
$I_{DD(VREFINT_BUF)}$	V_{REFINT} buffer consumption from V_{DD} when converted by ADC	-	-	82	94	µA
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	T_j = -40°C ~ +125 °C	-	0.3	20	mV
T_{Coeff}	Average temperature coefficient	-	-	-	100	ppm/°C
$V_{Ddcoeff}$	Average Voltage coefficient	1.71 V < VDD < 3.6V	-	246	1980	ppm/V

(1) Value guaranteed by design, not 100% tested in production.

(2) Value guaranteed by characterization, not 100% tested in production.

(3) Value guaranteed by production.

(4) The shortest sampling time can be determined in the application by multiple iterations.

Table 4-46. Internal reference voltage calibration values

Symbol	Test conditions	Memory address
V_{REFINT}(1)	V_{DD} = V_{DDA} = V_{REFP} = 3.3 V (+/- 10 mV), Temperature = 25 °C (+/- 5 °C)	0x1FF0F7D0 ~ 0x1FF0F7D1

(1) V_{REFINT} is internally connected to the ADC0_CH21/ADC1_CH17 input channel.

4.22. 14-bit ADC characteristics

Table 4-47. 14-bit ADC characteristics (1)(3)

Symbol	Parameter	Conditions				Min	Typ	Max	Unit
V_{DDA}	Operating voltage	-				2.0	-	3.6	V
V_{REFP}(2)	Positive Reference Voltage	V_{DDA}>=2.4 V				2.4	-	V_{DDA}	V
		V_{DDA}<2.4 V				2.0	-	V_{DDA}	V
V_{REFN}(2)	Negative Reference Voltage	-				V_{SSA}			V
f_{ADC}	ADC clock	2.4 V<=V_{DDA}<=3.6 V 2.4 V<=V_{REFP}<=V_{DDA}				0.1	-	80	MHz
		2.0 V<=V_{DDA}<=2.4 V 2.0 V<=V_{REFP}<=V_{DDA}				0.1	-	30	MHz
f_S	Sampling rate	Resolution = 14 bits	2.4 V<=V_{DDA}<=3.6 V 2.4 V<=V_{REFP}<=V_{DDA}	f_{ADC} = 80 MHz	SMP= 3.5	-	-	4	MSPS
			2.0 V<=V_{DDA}<=2.4 V 2.0 V<=V_{REFP}<=V_{DDA}	f_{ADC} = 30 MHz	SMP= 3.5	-	-	1.5	
		Resolution = 12 bits	2.4 V<=V_{DDA}<=3.6 V 2.4 V<=V_{REFP}<=V_{DDA}	f_{ADC} = 80 MHz	SMP= 3.5	-	-	4.44	
			2.0 V<=V_{DDA}<=2.4 V 2.0 V<=V_{REFP}<=V_{DDA}	f_{ADC} = 30 MHz	SMP= 3.5	-	-	1.67	
		Resolution = 10 bits	2.4 V<=V_{DDA}<=3.6 V 2.4 V<=V_{REFP}<=V_{DDA}	f_{ADC} = 80 MHz	SMP= 3.5	-	-	5	
			2.0 V<=V_{DDA}<=2.4 V 2.0	f_{ADC} = 30 MHz	SMP= 3.5	-	-	1.875	

Symbol	Parameter	Conditions				Min	Typ	Max	Unit
			V<=V_{REFP}<=V_{DDA}						
		Resolution = 8 bits	2.4 V<=V_{DDA}<=3.6 V 2.4 V<=V_{REFP}<=V_{DDA}	f_{ADC} = 80 MHz	SMP= 3.5	-	-	5.71	
			2.0 V<=V_{DDA}<=2.4 V 2.0 V<=V_{REFP}<=V_{DDA}	f_{ADC} = 30 MHz	SMP= 3.5	-	-	2.14	
t_{TRIG}	External trigger period	Resolution = 14 bits				20	-	-	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-				V_{REFN}	-	V_{REFP}	V
V_{CMIV}	Common mode input voltage	-				V_{REF}/2 -10%	V_{REF}/2	V_{REF}/2 +10%	V
R_{AIN}	External input impedance	Resolution = 14 bits				-	-	114	Ω
		Resolution = 12 bits				-	-	130	
		Resolution = 10 bits				-	-	152	
		Resolution = 8 bits				-	-	182	
R_{ADC}	Internal resistance					-	200	-	Ω
C_{ADC}	Input sampling capacitance	-				-	8	-	pF
t_{STAB}	ADC Power-up time	-				1	-	-	μs
t_{OFF_CAL}	Offset calibration time	-				-	-	2500	$1/f_{ADC}$
t_s	Sampling time	-				3.5	-	810.5	$1/f_{ADC}$
t_{CONV}	Total conversion time (including sampling time)	Resolution = N bits				N+3	-	-	1/ f_{ADC}
$I_{DDA (ADC)}$	ADC consumption on V_{DDA}	Resolution = 14 bits				-	2800	-	μA
$I_{VREF (ADC)}$	ADC consumption on V_{REFP}	f_{ADC}= 80 MHz				-	180	-	

(1) Value guaranteed by design, not 100% tested in production.

(2) Depending on the package, V_{REFP} can be internally connected to V_{DDA} and V_{REFN} to V_{SSA}.

(3) V_{REFP} should always be equal to or less than V_{DDA}, especially during power up.

Equation 1: R_{AIN} max formula $$R_{AIN} < \frac{T_s}{f_{ADC} * C_{ADC} * \ln(2^{N+2})} - R_{ADC}$$

The formula above Equation 1 is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 14 (from 14-bit resolution).

Table 4-48. ADC R_{AIN} max for f_{ADC} = 80 MHz (14-bit ADC) (1)(2)

Resolution	Sampling cycles @ 80 MHz	R_{AIN} max (kΩ)
14 bits	3.5	0.29
	6.5	0.72
	12.5	1.56
	24.5	3.25
	47.5	6.49
	92.5	12.83
	247.5	34.67
	810.5	114
12 bits	3.5	0.36
	6.5	0.85
	12.5	1.81
	24.5	3.74
	47.5	7.45
	92.5	14.69
	247.5	39.65
	810.5	130
10 bits	3.5	0.46
	6.5	1.02
	12.5	2.15
	24.5	4.40
	47.5	8.72
	92.5	17.18
	247.5	46.29
	810.5	152
8 bits	3.5	0.59
	6.5	1.27
	12.5	2.62
	24.5	5.32
	47.5	10.51
	92.5	20.65
	247.5	55.59
	810.5	182

(1) Value guaranteed by design, not 100% tested in production.

(2) The R_{AIN} value was calculated by theory and stray capacitance of actual pcb has not been taken into account.

Table 4-49. 14-bit ADC accuracy for f_{ADC} = 40 MHz (1)(2)(3)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
EO	Offset error	Single ended	-	+/-1	-	LSB
		Differential	-	+/-1	-	
EG	Gain error	Single ended	-	+/-1	-	
		Differential	-	+/-1	-	

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
DNL	Differential linearity error	Single ended	-	-1/+1.8	-	
		Differential	-	+/-1	-	
INL	Integral linearity error	Single ended	-	-2.5/+1	-	
		Differential	-	+/-1	-	
ENOB	Effective number of bits	Single ended	-	12.5	-	Bits
		Differential	-	13.4	-	
SNDR	Signal-to-noise and distortion ratio	Single ended	-	77.01	-	dB
		Differential	-	82.43	-	
SNR	Signal-to-noise ratio	Single ended	-	77.20	-	
		Differential	-	82.60	-	
THD	Total harmonic distortion	Single ended	-	-87.62	-	
		Differential	-	-90.41	-	

(1) Guaranteed by sample results for BGA176 packages. The values for LQFP packages might differ.

(2) Test condition: V_{DD} = V_{DDA} = V_{REFP} = 3.3 V, ADC_CLK = 40 MHz, external VREF were adopted.

(3) Some guidance is provided to improve the sampling accuracy of ADC. Refer to ***AN059 Methods to improve ADC sampling accuracy.***

Table 4-50. 14-bit ADC accuracy for f_{ADC} = 80 MHz (1)(2)(3)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
EO	Offset error	Single ended	-	TBD	-	LSB
		Differential	-	TBD	-	
EG	Gain error	Single ended	-	TBD	-	
		Differential	-	TBD	-	
DNL	Differential linearity error	Single ended	-	TBD	-	
		Differential	-	TBD	-	
INL	Integral linearity error	Single ended	-	TBD	-	
		Differential	-	TBD	-	
ENOB	Effective number of bits	Single ended	-	TBD	-	Bits
		Differential	-	TBD	-	
SNDR	Signal-to-noise and distortion ratio	Single ended	-	TBD	-	dB
		Differential	-	TBD	-	
SNR	Signal-to-noise ratio	Single ended	-	TBD	-	
		Differential	-	TBD	-	
THD	Total harmonic distortion	Single ended	-	TBD	-	
		Differential	-	TBD	-	

(1) Guaranteed by sample results for BGA176 packages. The values for LQFP packages might differ.

(2) Test condition: V_{DD} = V_{DDA} = V_{REFP} = 3.3 V, ADC_CLK = 80 MHz, external VREF were adopted.

(3) Some guidance is provided to improve the sampling accuracy of ADC. Refer to ***AN059 Methods to improve ADC sampling accuracy.***

Figure 4-17. Differential linearity error

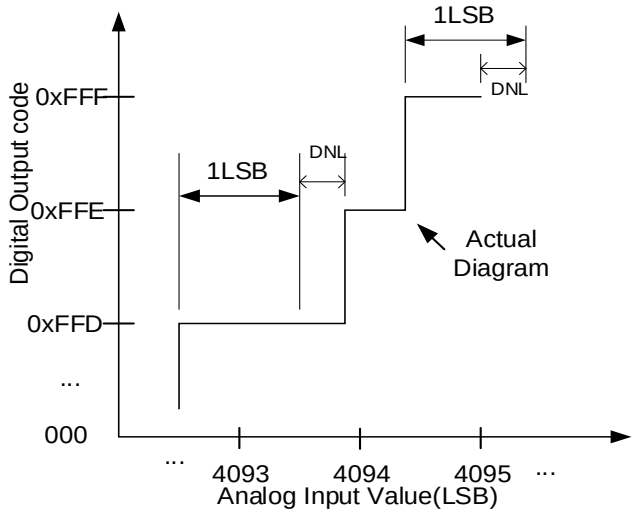
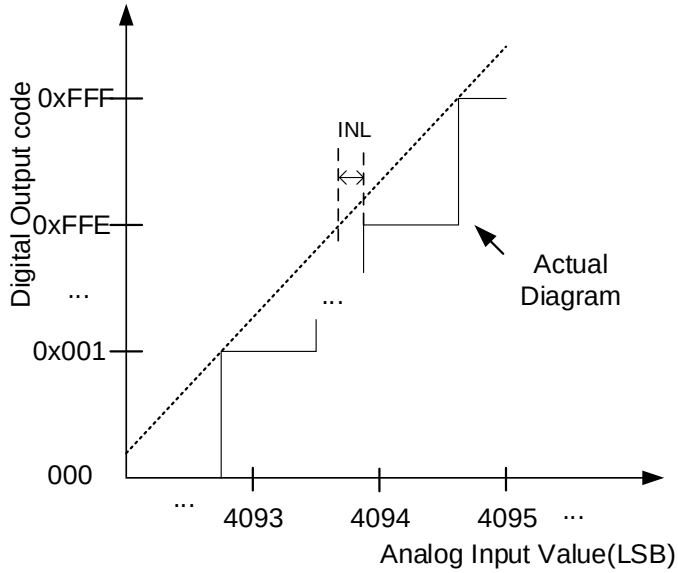


Figure 4-18. Integral linearity error



4.23. 12-bit ADC characteristics

Table 4-51. 12-bit ADC characteristics (1)(3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage	-	1.71	-	3.6	V
V_{REFP}(2)	Positive Reference Voltage	V_{DDA}>=V_{REFP}	1.71	-	3.6	V
V_{REFN}(2)	Negative Reference	-	V_{SSA}			V

Symbol	Parameter	Conditions					Min	Typ	Max	Unit
	Voltage									
f_{ADC}	ADC clock	2.4 V<=V_{DDA}<=3.6 V 2.4 V<=V_{REFP}<=V_{DDA}					1.5	-	85	MHz
		1.71 V<=V_{DDA}<=2.4 V 1.71 V<=V_{REFP}<=V_{DDA}					1.5	-	85	MHz
f_S	-	Resolution = 12 bits	2.4 V<=V_{DDA}<=3.6 V 2.4 V<=V_{REFP}<=V_{DDA}	-40 °C <= T_J <= 125 °C	f_{ADC} = 85 MHz	SMP = 2.5	-	-	5	MSPS
			1.71 V<=V_{DDA}<=2.4 V 1.71 V<=V_{REFP}<=V_{DDA}		f_{ADC} = 68 MHz		-	-	4	
		Resolution = 10 bits	2.4 V<=V_{DDA}<=3.6 V 2.4 V<=V_{REFP}<=V_{DDA}	-40 °C <= T_J <= 125 °C	f_{ADC} = 85 MHz	SMP = 2.5	-	-	5.67	
			1.71 V<=V_{DDA}<=2.4 V 1.71 V<=V_{REFP}<=V_{DDA}		f_{ADC} = 68 MHz		-	-	4.53	
		Resolution = 8 bits	2.4 V<=V_{DDA}<=3.6 V 2.4 V<=V_{REFP}<=V_{DDA}	-40 °C <= T_J <= 125 °C	f_{ADC} = 85 MHz	SMP = 2.5	-	-	6.53	
			1.71 V<=V_{DDA}<=2.4 V 1.71 V<=V_{REFP}<=V_{DDA}		f_{ADC} = 68 MHz		-	-	5.23	
		Resolution = 6 bits	2.4 V<=V_{DDA}<		f_{ADC} = 85 MHz	SMP = 2.5	-	-	7.72	

Symbol	Parameter	Conditions					Min	Typ	Max	Unit
			=3.6 V 2.4 V<=V_{REFP} <=V_{DDA}	-40 °C <= T_J <= 125 °C						
			1.71 V<=V_{DDA}<=2.4 V 1.71 V<=V_{REFP} <=V_{DDA}		f_{ADC} = 68 MHz		-	-	6.18	
t_{TRIG}	External trigger period	Resolution = 12 bits					17	-	-	1/f_{ADC}
V_{AIN}	Conversion voltage range	-					0	-	V_{REFP}	V
V_{CMIV}	Common mode input voltage	-					V_{REF}/2 -10%	V_{REFP}/2	V_{REF}/2 + 10%	
R_{AIN}	External input impedance	Resolution = 12 bits					-	-	96.81	kΩ
		Resolution = 10 bits					-	-	112.99	
		Resolution = 8 bits					-	-	135.63	
		Resolution = 6 bits					-	-	169.61	
R_{ADC}	Internal resistance	-					-	250	-	Ω
C_{ADC}	Input capacitance	-					-	8	-	pF
t_{STAB}	ADC Power-up time	-					-	1	-	μs
t_{OFF_CAL}	Offset calibration time	-					164	-	-	1/f_{ADC}
t_s	Sampling time	-					2.5	-	640.5	1/f_{ADC}
t_{CONV}	Total conversion time (including sampling time)	Resolution = N bits					5+N	-	-	1/ f_{ADC}

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DDA_D} (ADC)	ADC consumption on V_{DDA} and V_{REF}, Differential mode	f_{ADC}= 85 MHz	-	900	-	µA
I_{DDA_SE} (ADC)	ADC consumption on V_{DDA} and V_{REF}, Single-ended mode	f_{ADC}= 85 MHz	-	815	-	

(1) Value guaranteed by design, not 100% tested in production.

(2) Depending on the package, V_{REFP} can be internally connected to V_{DDA} and V_{REFN} to V_{SSA}.

(3) V_{REFP} should always be equal to or less than V_{DDA}, especially during power up.

Table 4-52. ADC R_{AIN} max for f_{ADC} = 85 MHz (12-bit ADC) (1)(2)

Resolution	Sampling cycles @80MHz	R_{AIN} max (kΩ)
12 bits	2.5	0.12
	6.5	0.73
	12.5	1.64
	24.5	3.46
	47.5	6.94
	92.5	13.76
	247.5	37.25
	640.5	96.81
10 bits	2.5	0.36
	6.5	0.89
	12.5	1.96
	24.5	4.08
	47.5	8.14
	92.5	16.10
	247.5	43.50
	640.5	112.99
8 bits	2.5	0.49
	6.5	1.12
	12.5	2.40
	24.5	4.94
	47.5	9.82
	92.5	19.37
	247.5	52.25
	640.5	135.63
6 bits	2.5	0.67

Resolution	Sampling cycles @80MHz	R_{AIN} max (kΩ)
	6.5	1.47
	12.5	3.06
	24.5	6.24
	47.5	12.34
	92.5	24.28
	247.5	65.38
	640.5	169.61

(1) Value guaranteed by design, not 100% tested in production.

(2) The R_{AIN} value was calculated by theory and stray capacitance of actual pcb has not been taken into account.

Table 4-53. 12-bit ADC accuracy at f_{ADC} = 85 MHz V_{REFP} = 3.3 V(1)(2)(3)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
EO	Offset error	Single ended	-	+/-1	-	LSB
		Differential	-	+/-1	-	
DNL	Differential linearity error	Single ended	-	+/-0.5	-	
		Differential	-	+/-0.8	-	
INL	Integral linearity error	Single ended	-	+/-1.2	-	
		Differential	-	+/-1	-	
ENOB	Effective number of bits	Single ended	-	11.2	-	Bits
		Differential	-	11.5	-	
SNDR	Signal-to-noise and distortion ratio	Single ended	-	69.21	-	dB
		Differential	-	71.49	-	
SNR	Signal-to-noise ratio	Single ended	-	69.32	-	
		Differential	-	71.57	-	
THD	Total harmonic distortion	Single ended	-	-84.32	-	
		Differential	-	-87.75	-	

(1) Guaranteed by sample results for BGA176 packages. The values for LQFP packages might differ.

(2) Test condition: V_{DD} = V_{DDA} = V_{REFP} = 3.3 V, ADC_CLK = 85 MHz, external VREF were adopted.

(3) Some guidance is provided to improve the sampling accuracy of ADC. Refer to ***AN059 Methods to improve ADC sampling accuracy.***

4.24. High-precision temperature sensor characteristics

Table 4-54. High-precision temperature sensor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{25}(1)	Uncalibrated Offset	T_J = 25°C	-	1012	-	mV
E_{OFF}(1)	Uncalibrated Offset Error	T_J = 25°C	-	+/-4	-	mV
Avg_Slope(1)	Average slope	-	-	3.305	-	mV/°C
E_M(1)	Slope Error	-	-	16	-	µV/°C
LIN	Linearity	T_J = -40 °C to +125 °C	-	+/-0.6(5)	-	°C
t_{s_temp}(1)	ADC sampling time when reading the temperature	-	5	-	-	µs
t_{ON}(1)	Turn-on Time	f_{ADC} = 85 MHz, t_{s_temp} = 5 µs	-	50	-	µs
ETOT(2)(3)(4)	Temp Sensor Error Using Typical Slope and Factory-Calibrated Offset	T_J = -40 °C to +125 °C	-	+/- 5	-	°C

(1) Value guaranteed by design, not 100% tested in production.

(2) The error is the average result of 100 times and represents the chip junction temperature error. The chip self-heating shall be considered when testing ambient temperature

(3) The error caused by ADC conversion and provided temperature calculation formula is not included.

(4) The sampling time should greater than ts_temp when use the high precision temperature sensor by ADC conversion.

(5) Value guaranteed by sample, not 100% tested in production.

Table 4-55. High-precision temperature sensor calibration values

Symbol	Parameter	Memory address
HPTS_CAL	High-precision temperature sensor raw data acquired value at 25 °C(+/-2°C), V_{REFP} = 3.3 V(+/-3 mV)	0x1FF0F7CC

4.25. Temperature sensor characteristics

Table 4-56. Temperature sensor characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{25}	Uncalibrated Offset	T_J = 25°C	-	688	-	mV
Avg_Slope	Average slope	-	-	1.77	-	mV/°C
T_{LIN}	Linearity	T_J = -40 °C to 125 °C	-	+/-3.5	-	°C
t_{s_temp}(2)	ADC sampling time when reading the temperature	-	-	17.1	-	µs

(1) Value guaranteed by design, not 100% tested in production.

(2) Shortest sampling time can be determined in the application by multiple iterations.

Table 4-57. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	Temperature sensor raw data acquired value at 25 °C(+/-2°C), V_{REFP} = 3.3 V(+/-3 mV)	0x1FF0F7C8

4.26. Low power digital temperature sensor characteristics

Table 4-58. Low power digital temperature sensor characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Supply voltage	-	1.71	3.3	3.6	V
f_{DTS}	Output Clock frequency	-	426	751	1412	kHz
T_{LC}	Temperature linearity coefficient	-	1551	2282	3360	Hz/°C
$T_{TOTAL(ERROR)}$	Temperature offset measurement	T_J = -40 °C to 25 °C	-3.67	-	1.53	°C
		T_J = 25 °C to T_{JMAX}	-9.6	-	0.78	
tWAKE_UP	Wake-up time from off state until DTS ready bit is set	-	-	350	-	μs
ILPDTS	LPDTS consumption	-	-	22	-	μA

(1) Value guaranteed by design, not 100% tested in production.

4.27. Voltage reference buffer characteristics

Table 4-59. Voltage reference buffer characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Supply voltage	Normal mode, V_{DDA}=3.3V	VREFS = 00	2.8	3.3	3.6	V
			VREFS = 01	2.4	-	3.6	
			VREFS = 10	2.1	-	3.6	
			VREFS = 11	1.8	-	3.6	
		Degraded mode	VREFS = 00	1.71	-	2.8	
			VREFS = 01	1.71	-	2.4	
			VREFS = 10	1.71	-	2.1	
			VREFS = 11	1.71	-	1.8	
V_{REFBUF_OUT}	Voltage Reference Buffer Output	Normal mode, at V_{DDA}=3.3V(2)	VREFS = 00	-	2.501	-	
			VREFS = 01	-	2.049	-	
			VREFS = 10	-	1.8	-	
			VREFS = 11	-	1.5	-	
		Degraded mode	VREFS = 00	V_{DDA}-100mV	-	V_{DDA}	
			VREFS = 01	V_{DDA}-100mV	-	V_{DDA}	

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
			VREFS = 10	V_{DDA}-100mV	-	V_{DDA}	
			VREFS = 11	V_{DDA}-100mV	-	V_{DDA}	
TRIM	Trim step resolution	-		-	+/-0.07	+/-0.1	%
C_L	Load capacitor	-		0.5	1	1.5	µF
ESR	Equivalent Serial Resistor of CL	-		-	-	2	Ω
I_{LOAD}	Load current	-		-	-	4	mA
t_{START}	Start-up time	-		-	770	-	µs
I_{DDA} (V_{REFBUF})	V_{REFBUF} consumption from V_{DDA}	-		-	73	81	µA
I_{INRUSH}	Control of maximum DC current drive on V_{REFBUF_OUT} during startup phase	-		-	11	-	mA
$Regu_{(LINE)}$	Line regulation	2.8 V <= V_{DDA} <= 3.6 V	I_{load} = 500 µA	-	786	-	ppm /V
			I_{load} = 4 mA	-	765	-	
$Regu_{(LOAD)}$	Load regulation	500 µA <= I_{LOAD} <=4 mA	Normal mode	-	55	-	ppm / mA
T_{COEFF}	Temperature drift	-40 °C < T_J < +125 °C		-	-	50	ppm / °C
PSRR	Power supply rejection	DC	-	-	58	-	dB
		100 kHz	-	-	40	-	

(1) Value guaranteed by design, not 100% tested in production.

(2) Value guaranteed by sample, not 100% tested in production.

(3) In degraded mode, the voltage reference buffer cannot accurately maintain the output voltage (V_{DDA}-drop voltage).

(4) To properly control VREFBUF I_{INRUSH} current during the startup phase and the change of scaling, V_{DDA} voltage should be in the range of 1.8 V-3.6 V, 2.1 V-3.6 V, 2.4 V-3.6 V and 2.8 V-3.6 V for VREFS = 11, 10, 01 and 00, respectively.

4.28. CMP characteristics

Table 4-60. CMP characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage	-	1.71	3.3	3.6	V
V_{IN}	Input voltage range	-	0	-	V_{DDA}	V

Symbol	Description	Conditions		Min	Typ	Max	Unit
V_{BG}	Scaler input voltage	-		Refer to V_{REFINT}			V
V_{SC}	Scaler offset voltage	-		-	3.5	11	mV
$I_{DDA(SCALER)}$	Scaler static consumption from V_{DDA}	BEN=0 (bridge disable)		-	175	190	nA
		BEN=1 (bridge enable)		-	775	915	
$t_{ST(SCALER)}$	Scaler startup time	-		-	-	100	µs
t_D(2)	Propagation delay for 200mV step with 100 mV overdrive	Ultra-low power mode		-	1768	-	µs
		Medium power mode		-	126	-	ns
		High speed power mode		-	55	-	ns
	Propagation delay for step > 200 mV with 100 mV overdrive only on positive inputs	Ultra-low power mode		-	1768	-	µs
		Medium power mode		-	154	-	ns
		High speed power mode		-	74	-	ns
$t_{ST(CMP)}$	Comparator startup time to reach propagation delay specification	High-speed mode		-	-	1.4	µs
		Medium mode		-	-	1.4	
		Ultra-low-power mode		-	-	11	
$I_{DDA(CMP)}$	Current consumption from V_{DDA}	Ultra-low power mode	Static	-	400	425	nA
			With 50 kHz +/- 100 mV overdrive square signal	-	2600	-	
		Medium power mode	Static	-	4300	4500	nA
			With 50 kHz +/- 100 mV overdrive square signal	-	4300	-	
		High speed power mode	Static	-	43	45	µA
			With 50 kHz +/- 100 mV overdrive square signal	-	40	-	
V_{OFFSET}	Offset error	-		-	+/-5	+/-15	mV
V_{HYST}	Hysteresis Voltage	No Hysteresis		-	0	-	mV
		Low Hysteresis		8	10	17	
		Medium Hysteresis		16	20	34	
		High Hysteresis		24	30	52	

(1) Value guaranteed by design, not 100% tested in production.

(2) Value guaranteed by sample, not 100% tested in production.

4.29. Temperature and VBAT monitoring

Table 4-61. VBAT monitoring characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	25	-	kΩ
Q	Ratio on V_{BAT} measurement	-	4	-	-
Er	Error on Q	-10	-	10	%
$t_{SAMPLE(VBAT)}$	ADC sampling time when reading V_{BAT} input	10	-	-	μs
$V_{BAT(high)}$	High supply monitoring	-	3.56	-	V
$V_{BAT(low)}$	Low supply monitoring	-	1.36	-	

(1) Value guaranteed by design, not 100% tested in production.

Table 4-62. V_{BAT} charging characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VCRSEL = 0	-	5	-	kΩ
		VCRSEL = 1	-	1.5	-	

(1) Value guaranteed by design, not 100% tested in production.

Table 4-63. Temperature monitoring characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
$TEMP_{high}$	High temperature monitoring	-	117	-	°C
$TEMP_{low}$	Low temperature monitoring	-	-27	-	

(1) Value guaranteed by design, not 100% tested in production.

4.30. DAC characteristics

Table 4-64. DAC characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Operating voltage	-		1.8	3.3	3.6	V
V_{REFP}	Positive Reference Voltage	-		1.8	-	V_{DDA}	V
V_{REFN}	Negative Reference Voltage	-		-	V_{SSA}	-	V
R_{LOAD}	Resistive load	Resistive load with buffer ON	Connected to V_{SSA}	5	-	-	kΩ
			Connected to V_{DDA}	5	-	-	
Ro	Impedance output	Impedance output with buffer OFF		-	-	15	kΩ
R_{BON}	Output impedance sample and hold mode, output buffer ON	DAC output buffer ON		-	-	1.5	kΩ
R_{BOFF}	Output impedance sample and hold mode, output buffer OFF	DAC output buffer OFF		-	-	15	

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_{LOAD}	Capacitive load	DAC output buffer ON		-	-	50	pF
C_{SH}		Sample and Hold mode		-	0.1	1	µF
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON		0.2	-	V_{DDA}-0.2	V
		DAC output buffer OFF		0	-	V_{REFP}	V
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches the final value of +/-1 LSB, +/-2 LSB, +/-4LSB, +/-8 LSB)	Normal mode, DAC output buffer ON, CL <= 50 pF,RL >= 5 kΩ	+/-1 LSB	-	1.11	-	µs
			+/-2 LSB	-	0.62	-	
			+/-4 LSB	-	0.37	-	
			+/-8 LSB	-	0.3	-	
		Normal mode, DAC output buffer OFF, +/-1LSB CL = 10 pF		-	3.4	7	
t_{WAKEUP}	Wakeup time from off state (setting the Enx bit in the DAC Control register) until the final value of +/-1LSB is reached	Normal mode, DAC output buffer ON, CL <= 50 pF, RL = 5 kΩ		-	6	10	µs
		Normal mode, DAC output buffer OFF, CL <= 10 pF		-	3	5	
Update rate	Max frequency for a correct DAC_OUT change from code new to i+/-1LSBs	C_{LOAD} <= 50 pF, R_{LOAD} >= 5 kΩ		-	-	2	MS/s
PSRR	Power supply rejection ratio(to V_{DDA})	No R_{Load}, C_{LOAD} = 50 pF		40	80	-	dB
t_{SAMP}	Sampling time in Sample and Hold mode C_L = 100 nF (code transition between the lowest input code and the highest input code when DAC_OUT reaches the +/-1 LSB final value)	MODE<2:0>_V12 = 100 / 101 (BUFFER ON)		-	0.9	1.1	ms
		MODE<2:0>_V12 = 110 (BUFFER OFF)		-	9.7	11.5	
		MODE<2:0>_V12 = 111 (INTERNAL BUFFER OFF)		-	3	5	µs
C_{lint}	Internal sample and hold capacitor	-		5.5	7	8.5	pF
t_{TRIM}	Middle code offset trim time	Minimum time to verify the each code		50	-	-	µs
V_{offset}	Middle code offset for 1 trim code step	V_{REFP} = 3.6 V		-	1.68	-	mV
		V_{REFP} = 1.8 V		-	0.84	-	
I_{DDA}(3)	DAC current consumption in quiescent mode	DAC output buffer ON	No load, middle code (0x800)	-	330	-	µA

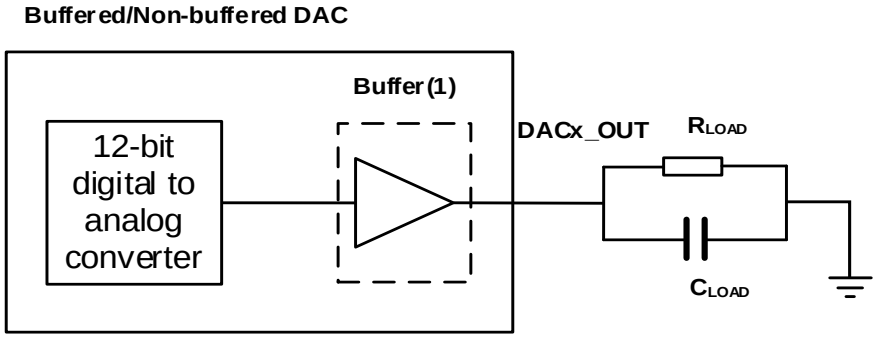
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
			No load, worst code (0xF1C)	-	330	-	
		DAC output buffer OFF	No load, middle/ worst code (0x800)	-	0.1	-	
		Sample and Hold mode, C_{SH} = 100 nF		-	330*T_{ON}/(T_{ON}+T_{OFF})	-	
$I_{DDVREFP}$	DAC current consumption from V_{REFP} in quiescent mode	DAC output buffer ON	No load, middle code (0x800)	100	100	-	µA
			No load, worst code (0xF1C)	450	450	-	
		DAC output buffer OFF	No load, middle code (0x800)	85	85	-	
		Sample and Hold mode, Buffer ON, C_{SH} = 100 nF (middle code)		-	100*T_{ON}/(T_{ON}+T_{OFF})	-	
		Sample and Hold mode, Buffer OFF, C_{SH} = 100 nF (middle code)		-	85*T_{ON}/(T_{ON}+T_{OFF})	-	
DNL(2)	Differential non linearity	DAC output buffer ON		-	+/-2	-	LSB
		DAC output buffer OFF		-	+/-2	-	
-	Monotonicity	10 bits		Guaranteed			
INL(2)	Integral non linearity	DAC output buffer ON		-	+/-4	-	LSB
		DAC output buffer OFF		-	+/-4	-	
Offset(2)	Offset error at code 0x800	DAC output buffer OFF		-	+/-6	-	
OffsetCal(2)	Offset error at code 0x800 after factory calibration	DAC output buffer ON	V_{REFP} = 3.6 V	-	+/-6	-	
			V_{REFP} = 1.8 V	-	+/-6	-	
Gain(2)	Gain error	DAC output buffer ON		-	+/-0.5	-	%
		DAC output buffer OFF		-	+/-0.5	-	

(1) Value guaranteed by design, not 100% tested in production.

(2) Value guaranteed by sample, not 100% tested in production.

(3) T_{ON} is the refresh phase duration, while T_{OFF} is the hold phase duration. Refer to the product reference manual for more details.

Figure 4-19. 12-bit buffered /non-buffered DAC



(1) The DAC integrates an output buffer to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

4.31. I2C characteristics

Table 4-65. I2C characteristics(1)(2)

Symbol	Description	Conditions	Standard mode		Fast mode		Fast mode plus		Unit
			Min	Max	Min	Max	Min	Max	
$t_{SCL(H)}$	SCL clock high time	-	4	-	0.6	-	0.2	-	μs
$t_{SCL(L)}$	SCL clock low time	-	4.7	-	1.3	-	0.5	-	μs
$t_{SU(SDA)}$	SDA setup time	-	250	-	100	-	50	-	ns
$t_{H(SDA)}$	SDA data hold time	-	0(3)	3450	0	900	0	450	ns
$t_{R(SDA/SCL)}$	SDA and SCL rise time	-	-	1000	-	300	-	120	ns
$t_{F(SDA/SCL)}$	SDA and SCL fall time	-	-	300	-	300	-	120	ns
$t_{H(STA)}$	Start condition hold time	-	4	-	0.6	-	0.26	-	μs
$t_{SU(STA)}$	Repeated Start condition setup time	-	4.7	-	0.6	-	0.26	-	μs
$t_{SU(STO)}$	Stop condition setup time	-	4.7	-	0.6	-	0.26	-	μs
t_{BUFF}	Stop to Start condition time (bus free)	-	4.7	-	1.3	-	0.5	-	μs

(1) Value guaranteed by design, not 100% tested in production.

(2) To ensure the standard mode I2C frequency, f_{PCLK1} must be at least 2 MHz. To ensure the fast mode I2C frequency, f_{PCLK1} must be at least 4 MHz. To ensure the fast mode plus I2C frequency, f_{PCLK1} must be at least a multiple of 10 MHz.

(3) The device should provide a data hold time of 300 ns at least in order to bridge the undefined region of the falling edge of SCL.

Figure 4-20. I2C bus timing diagram

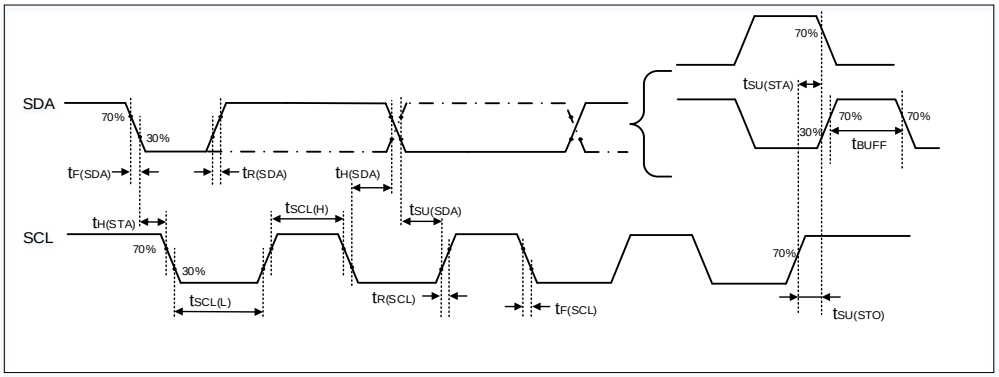


Table 4-66. I2C analog filter delay characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{AF}	Analog filter delay time	-	42	72	174	ns

(1) Value guaranteed by design, not 100% tested in production.

4.32. SPI characteristics

Table 4-67. Standard SPI characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	Master mode、(Moto mode)	-	-	150	MHz
		Master mode (TI mode)	-	-	53	
		Slave mode	-	-	40	
$t_{SCK(H)}$	SCK clock high time	Moto mode	2.33	3.33	4.33	ns
		TI mode	8.43	9.43	10.43	
$t_{SCK(L)}$	SCK clock low time	Moto mode	2.33	3.33	4.33	
		TI mode	8.43	9.43	10.43	
SPI master mode						
$t_{V(MO)}$	Data output valid time	-	-	1.8	3	ns
$t_{H(MO)}$	Data output hold time	-	0	-	-	
$t_{SU(MI)}$	Data input setup time	-	1	-	-	
$t_{H(MI)}$	Data input hold time	-	2	-	-	
SPI slave mode						
$t_{SU(NSS)}$	NSS enable setup time	-	2.5	-	-	ns
$t_{H(NSS)}$	NSS enable hold time	-	1	-	-	
$t_{A(SO)}$	Data output access time	-	-	7	-	
$t_{DIS(SO)}$	Data output disable time	-	0	-	-	
$t_{V(SO)}$	Data output valid time	-	-	8	-	
$t_{H(SO)}$	Data output hold time	-	-	8	-	

Symbol	Description	Conditions	Min	Typ	Max	Unit
$t_{SU(SI)}$	Data input setup time	-	1	-	-	
$t_{H(SI)}$	Data input hold time	-	2.5	-	-	

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-21. SPI timing diagram - master mode

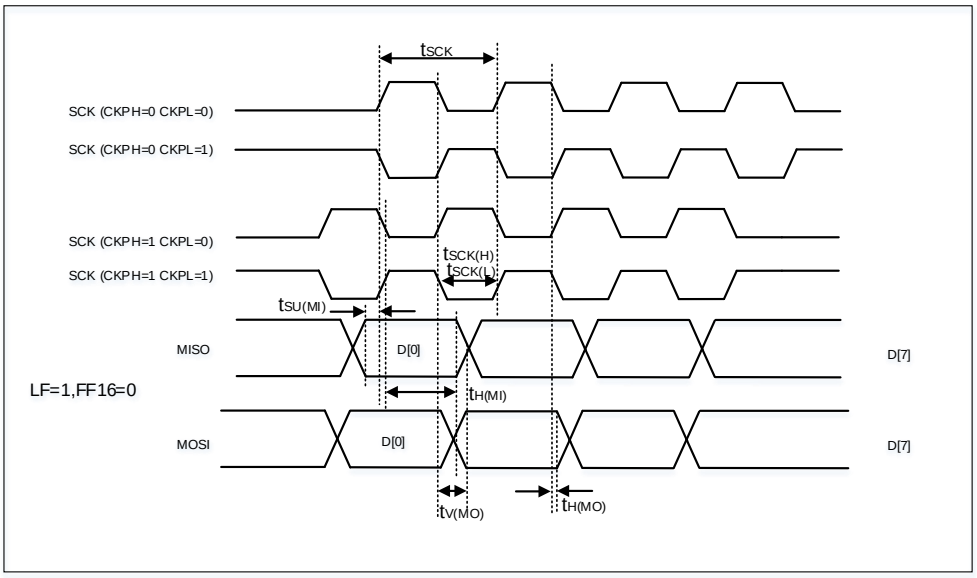


Figure 4-22. SPI timing diagram - slave mode(CKPH=0)

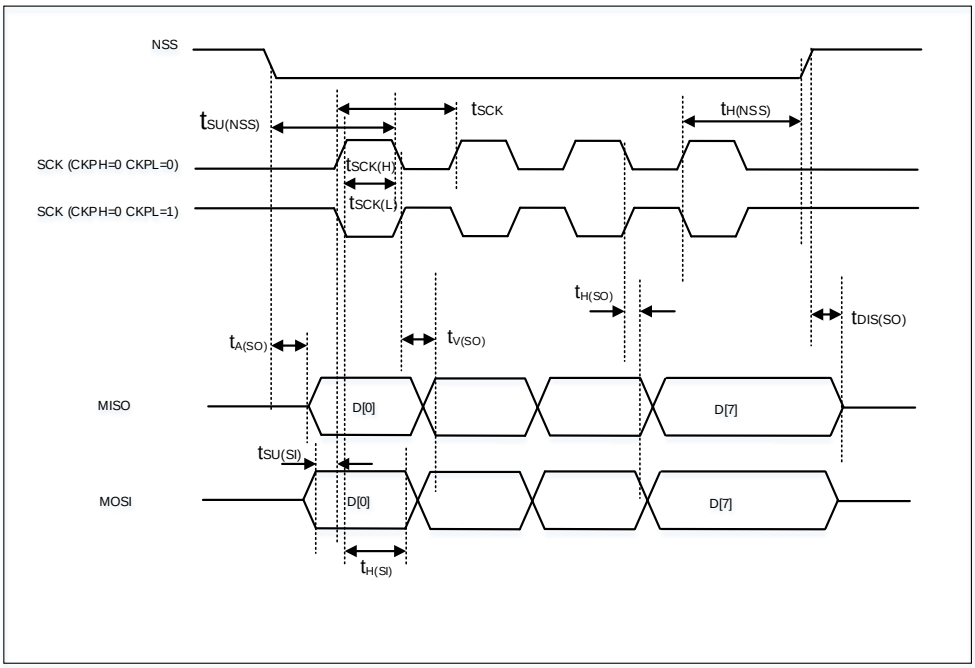
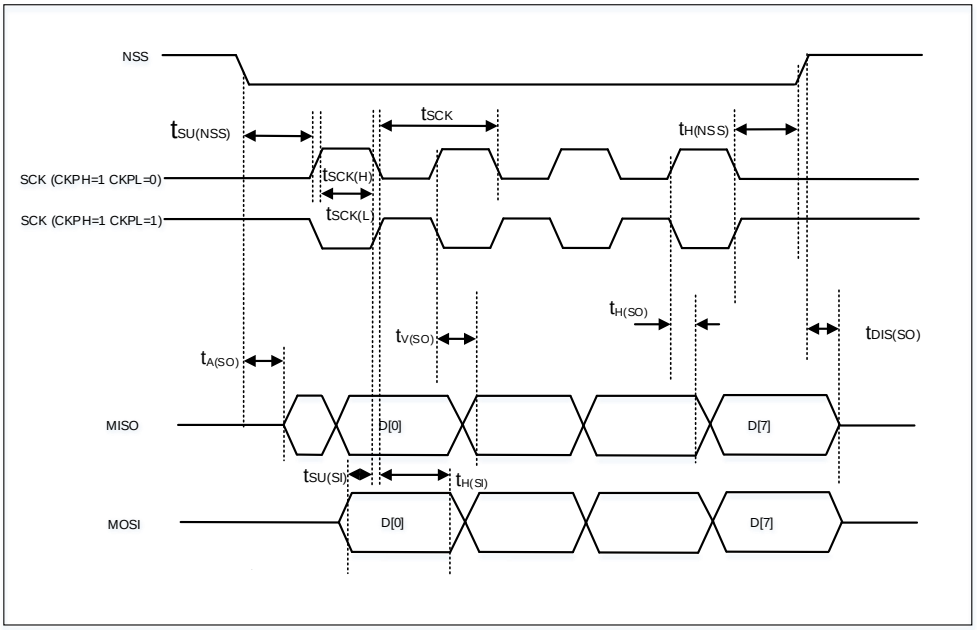


Figure 4-23. SPI timing diagram - slave mode(CKPH=1)



4.33. OSPI characteristics

Table 4-68. Standard OSPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SDR mode						
f_{SCK}	SCK clock frequency	-	-	-	200	MHz
$t_{SCK(H)}$	SCK clock high time, even division	-	$t_{(CK)}/2$	-	$t_{(CK)}/2+1$	ns
	SCK clock high time, odd division	-	$(n/2)*t_{(CK)}/(n+1)$	-	$(n/2)*t_{(CK)}/(n+1)+1$	ns
$t_{SCK(L)}$	SCK clock low time, even division	-	$t_{(CK)}/2-1$	-	$t_{(CK)}/2$	ns
	SCK clock low time, odd division	-	$(n/2+1)*t_{(CK)}/(n+1)-1$	-	$(n/2+1)*t_{(CK)}/(n+1)$	ns
$t_{V(MO)}$	Data output valid time	-	-	-	1.5	ns
$t_{H(MO)}$	Data output hold time	-	0	-	-	ns
$t_{SU(MI)}$(2)	Data input setup time	-	0	-	-	ns
$t_{H(MI)}$(2)	Data input hold time	-	-	-	5	ns
DTR mode(no DQS)						
f_{SCK}	SCK clock frequency	-	-	-	200	MHz
$t_{SCK(H)}$	SCK clock high time, even division	-	$t_{(CK)}/2$	-	$t_{(CK)}/2+1$	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	SCK clock high time, odd division	-	$(n/2)*t_{(CK)}/(n+1)$	-	$(n/2)*t_{(CK)}/(n+1)+1$	ns
$t_{SCK(L)}$	SCK clock high time, even division	-	$t_{(CK)}/2-1$	-	$t_{(CK)}/2$	ns
	SCK clock high time, odd division	-	$(n/2+1)*t_{(CK)}/(n+1)-1$	-	$(n/2+1)*t_{(CK)}/(n+1)$	ns
$t_{VR(SO)}$ $t_{VF(SO)}$	Data output valid time	DHQC = 1, Prescaler = 1,2 …	-	$t_{pclk}/4+1$	$t_{pclk}/4+1.25$	ns
$t_{HR(SO)}$ $t_{HF(SO)}$	Data output hold time	DHQC = 1, Prescaler = 1,2 …	$t_{pclk}/4$	-	-	ns
$t_{SUR(SI)}$ $t_{SUF(SI)}$(2)	Data input setup time	-	0	-	-	ns
$t_{HR(SI)}$ $t_{HF(SI)}$(2)	Data input hold time	-	-	-	2.5	ns
DTR mode(with DQS)						
f_{SCK}	SCK clock frequency	-	-	-	200	MHz
$t_{SCK(H)}$	SCK clock high time, even division	-	$t_{(CK)}/2$	-	$t_{(CK)}/2+1$	ns
	SCK clock high time, odd division	-	$(n/2)*t_{(CK)}/(n+1)$	-	$(n/2)*t_{(CK)}/(n+1)+1$	ns
$t_{SCK(L)}$	SCK clock high time, even division	-	$t_{(CK)}/2-1$	-	$t_{(CK)}/2$	ns
	SCK clock high time, odd division	-	$(n/2+1)*t_{(CK)}/(n+1)-1$	-	$(n/2+1)*t_{(CK)}/(n+1)$	ns
$t_{v(CK)}$	Clock valid time	-	-	-	$t_{(CK)}+t_{(CK)}/2$	ns
$t_{h(CK)}$	Clock hold time	-	$t_{(CK)}/2$	-	-	
$t_{w(CS)}$	Chip select high time	-	$3*t_{(CK)}$	-	-	ns
$t_{VR(SO)}$ $t_{VF(SO)}$	Data output valid time	DHQC = 1, Prescaler = 1,2 …	-	$t_{pclk}/4+1$	$t_{pclk}/4+1.25$	ns
$t_{HR(SO)}$ $t_{HF(SO)}$	Data output hold time	DHQC = 1, Prescaler = 1,2 …	$t_{pclk}/4$	-	-	
$t_{SUR(SI)}$ $t_{SUF(SI)}$	Data input setup time	-	0	-	-	
$t_{HR(SI)}$ $t_{HF(SI)}$	Data input hold time	-	-	-	2.5	

(1) Value guaranteed by design, not 100% tested in production.

(2) Delay block bypassed.

Figure 4-24. OSPI timing diagram - SDR mode

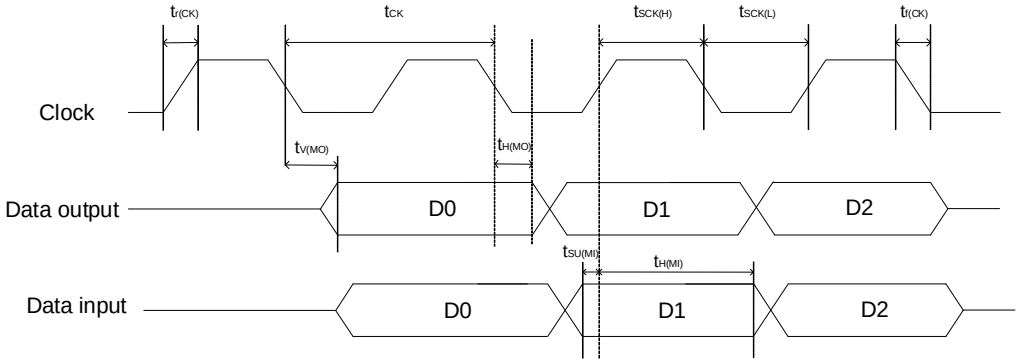
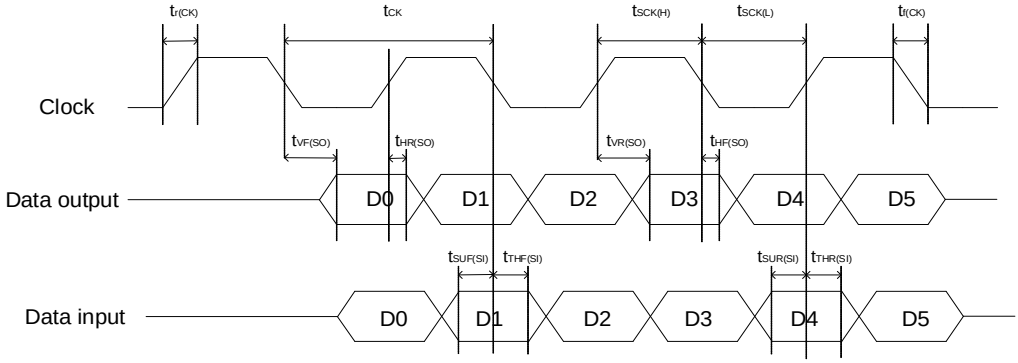


Figure 4-25. OSPI timing diagram - DTR mode



4.34. CPDM characteristics

Table 4-69. CPDM characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{init}	Initial delay	-	706	948	1589	ps
t_{Δ}	Unit Delay	-	35	47	62	ps

(1) Value guaranteed by design, not 100% tested in production.

4.35. HPDF characteristics

Table 4-70. HPDF characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{HPDFCLK}$	HPDF clock	-	-	-	133	MHz
f_{CKIN} ($1 / T_{CKIN}$)	Input clock frequency	SPI mode(SITYP[1:0] = 01)	-	-	20	
f_{CKOUT}	Output clock frequency	-	-	-	20	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Duty_{CKOUT}$	Output clock frequency duty cycle	-	30	50	75	%
$t_{wh(CKIN)}$ $t_{wl(CKIN)}$	Input clock high and low time	SPI mode(SITYP[1:0] = 01), External clock mode(SPICKSS[1:0] = 0)	T_{CKIN} / 2-0.5	T_{CKIN} / 2	-	ns
t_{SU}	Data input setup time	SPI mode(SITYP[1:0] = 01), External clock mode(SPICKSS[1:0] = 0)	1	-	-	
t_h	Data input hold time	SPI mode(SITYP[1:0] = 01), External clock mode(SPICKSS[1:0] = 0)	1	-	-	
$T_{Manchester}$	Manchester data period(recovered clock period)	Manchester mode(SITYP[1:0] = 10 or 11), Internal clock mode(SPICKSS[1:0] != 0)	(CKOUTDIV+1) * $T_{HPDFCLK}$	-	(2*CKOUTDIV) * $T_{HPDFCLK}$	

(1) Value guaranteed by design, not 100% tested in production.

(2) Output speed is set to OSPEEDRy[1:0] = 10; Capacitive load C = 30 pF; Measurement points are done at COMS levels: 0.5 * V_{DD}.

4.36. SAI characteristics

Table 4-71. SAI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{MCK}	SAI Main clock output	-	-	-	50	MHz
f_{CK}	SAI clock frequency	Master transmitter, 2.7 V <= V_{DD} <= 3.6 V	-	-	45	
		Master transmitter, 1.71 V <= V_{DD} <= 3.6 V	-	-	32	
		Master receiver, 1.71 V <= V_{DD} <= 3.6 V	-	-	32	
		Slave transmitter, 2.7 V <= V_{DD} <= 3.6 V	-	-	47.5	
		Slave transmitter, 1.71 V <= V_{DD} <= 3.6 V	-	-	41.5	
		Slave receiver, 1.71 V <= V_{DD} <= 3.6 V	-	-	50	

(1) Value guaranteed by design, not 100% tested in production.

4.37. I2S characteristics

Table 4-72. I2S characteristics(1)(2)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{CK}	Clock frequency	Master mode (data: 16 bits, Audio frequency = 96 kHz)	-	6.25	-	MHz
		Slave mode	-	-	12.5	
t_H	Clock high time	-	-	80	-	ns
t_L	Clock low time		-	80	-	ns
$t_{V(WS)}$	WS valid time	Master mode	-	3	-	ns
$t_{H(WS)}$	WS hold time	Master mode	-	3	-	ns
$t_{SU(WS)}$	WS setup time	Slave mode	0	-	-	ns
$t_{H(WS)}$	WS hold time	Slave mode	3	-	-	ns
$Duty_{SCK}$	I2S slave input clock duty cycle	Slave mode	-	50	-	%
$t_{SU(SD_MR)}$	Data input setup time	Master mode	0	-	-	ns
$t_{SU(SD_SR)}$	Data input setup time	Slave mode	0	-	-	ns
$t_{H(SD_MR)}$	Data input hold time	Master receiver	1	-	-	ns
$t_{H(SD_SR)}$		Slave receiver	3	-	-	ns
$t_{V(SD_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	-	9	ns
$t_{H(SD_ST)}$	Data output hold time	Slave transmitter (after enable edge)	6	-	-	ns
$t_{V(SD_MT)}$	Data output valid time	Master transmitter (after enable edge)	-	-	6	ns
$t_{H(SD_MT)}$	Data output hold time	Master transmitter (after enable edge)	0	-	-	ns

(1) Value guaranteed by design, not 100% tested in production.

(2) Output speed is set to OSPDy[1:0] = 10.

Figure 4-26. I2S timing diagram - master mode

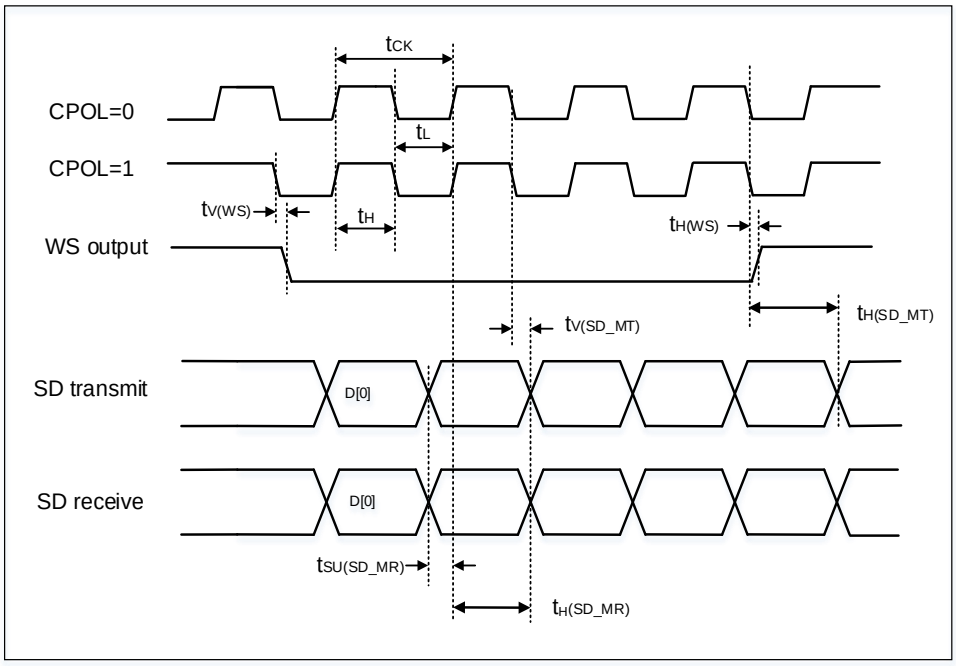
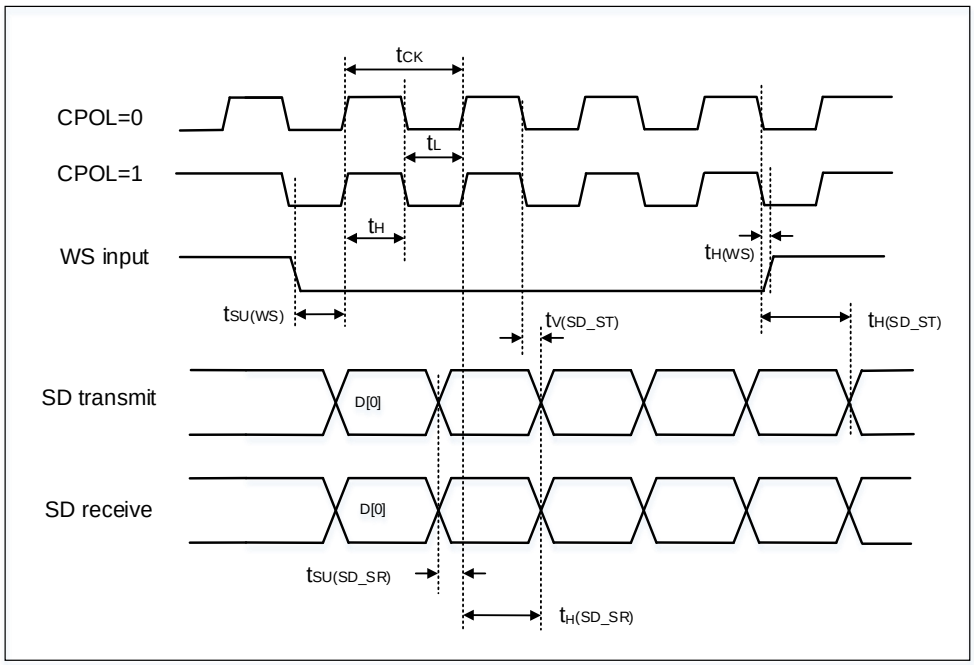


Figure 4-27. I2S timing diagram - slave mode



4.38. USART characteristics

Table 4-73. USART characteristics is Synchronous mode (1)(2)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	f_{PCLK2} = 300 MHz	-	-	37.5	MHz
$f_{SCK(H)}$	SCK clock high time		13.3	-	-	ns
$f_{SCK(L)}$	SCK clock low time		13.3	-	-	

(1) Value guaranteed by design, not 100% tested in production.

(2) Output speed is set to OSPDy[1:0] = 10.

Table 4-74. USART characteristics is Smartcard mode (1)(2)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	f_{PCLK2} = 300 MHz	-	-	150	MHz
$f_{SCK(H)}$	SCK clock high time		3.3	-	-	ns
$f_{SCK(L)}$	SCK clock low time		3.3	-	-	

(1) Value guaranteed by design, not 100% tested in production.

(2) Output speed is set to OSPDy[1:0] = 10.

4.39. SDIO characteristics

Table 4-68. SDIO characteristics(1)(2)(3)

Symbol	Mode	Description	Conditions	Min	Typ	Max	Unit
f_{PP}	-	Clock frequency in data transfer mode	-	-	-	208	MHz
$t_{W(CKL)}$		Clock low time	f_{pp} = 208 MHz	1.8	2.4	-	ns
$t_{W(CKH)}$		Clock high time		1.8	2.4	-	ns
t_{ISU}	CMD,MMC and SD HS mode	D input setup time HS(4)	f_{pp} = 120 MHz	2.5	-	-	ns
t_{IH}		D input hold time HS(4)		0.5	-	-	ns
t_{OV}		D output valid time HS(4)		-	5.5	6	ns
t_{OH}		D output hold time HS(4)		4.5	-	-	ns
t_{ISUD}	CMD,SD default mode	D input setup time SD(4)	f_{pp} = 52 MHz	2.5	-	-	ns
t_{IHD}		D input hold time SD(4)		1.5	-	-	ns
t_{OVD}		D output valid default time SD(4)		-	6	6.5	ns
t_{OHD}		D output hold default time SD(4)		5.5	-	-	ns

(1) CLK timing is measured at V_{DD} = 2.7 to 3.6V.

(2) Capacitive load C_L = 20 pF.

(3) Value guaranteed by design, not 100% tested in production.

(4) D Output/Input are referenced to CK.

Figure 4-28. SDIO high-speed mode

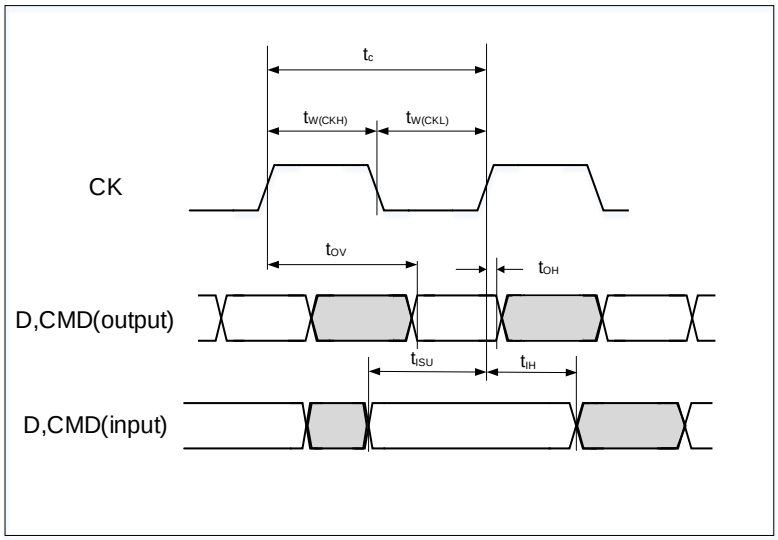


Figure 4-29. SD default mode

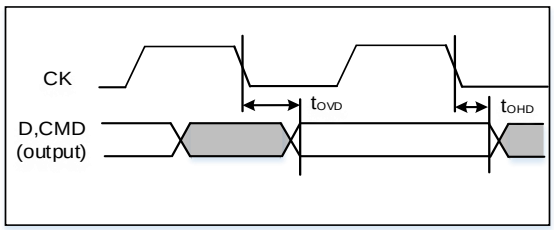
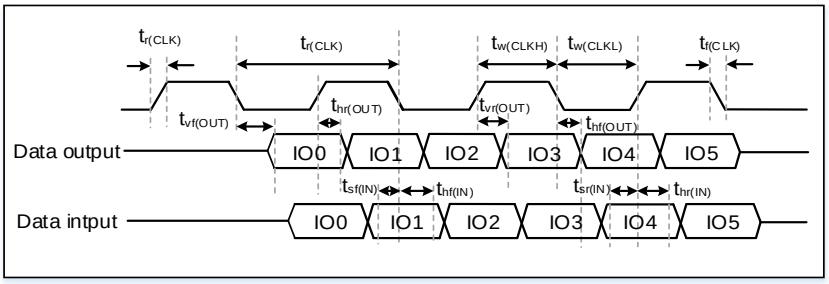


Figure 4-30. DDR mode



4.40. TLI characteristics

Table 4-75. TLI characteristics(1)

Symbol	Parameter		Min	Max	Unit
f_{SCK}	TLI clock output frequency	2.7 V < VDD <3.6 V, 20pF	-	166	MHz
		2.7 V < VDD < 3.6 V		166	
		1.71 V < VDD <3.6 V		166	
D_{CLK}	TLI clock output duty cycle		49.8	50.2	%
$t_{w(CLKH)}$, $t_{w(CLKL)}$	Clock High time, low time		$t_{w(CLK)}/2$-0.5	$t_{w(CLK)}/$0.5	ns

Symbol	Parameter		Min	Max	Unit
$t_{V(DATA)}$	Data output valid time	2.7 V < VDD <3.6 V	-	2.0	
		1.71 V < VDD <3.6 V		2.0	
$t_{h(DATA)}$	Data output hold time		0	-	
$t_{v(HSYNC)}$, $t_{v(VSYNC)}$, $t_{v(DE)}$	HSYNC / VSYNC / DE output valid time	2.7 V < VDD <3.6 V	-	2.0	
		1.71 V < VDD <3.6 V	-	2.0	
$t_{h(HSYNC)}$, $t_{h(VSYNC)}$, $t_{h(DE)}$	HSYNC / VSYNC / DE output hold time		0	-	

(1) Guaranteed by design, not 100% tested in production.

Figure 4-31. TLI horizontal timing diagram

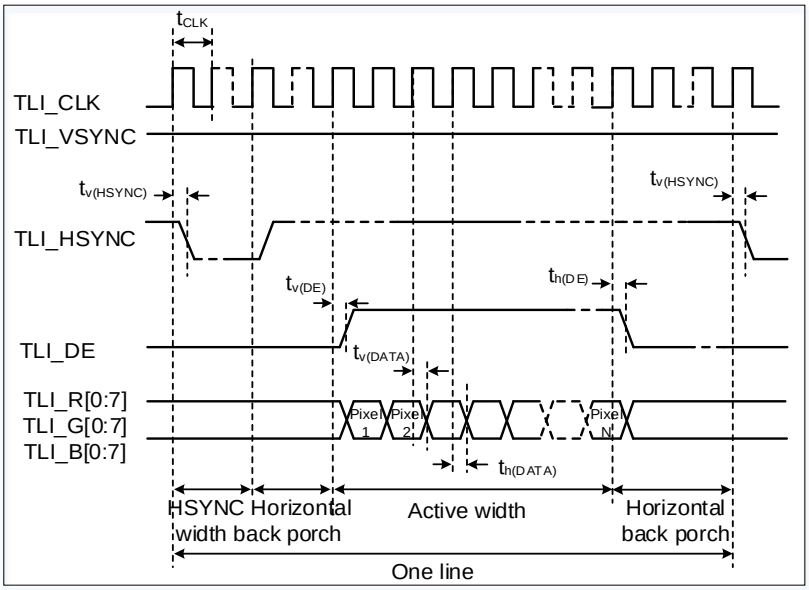
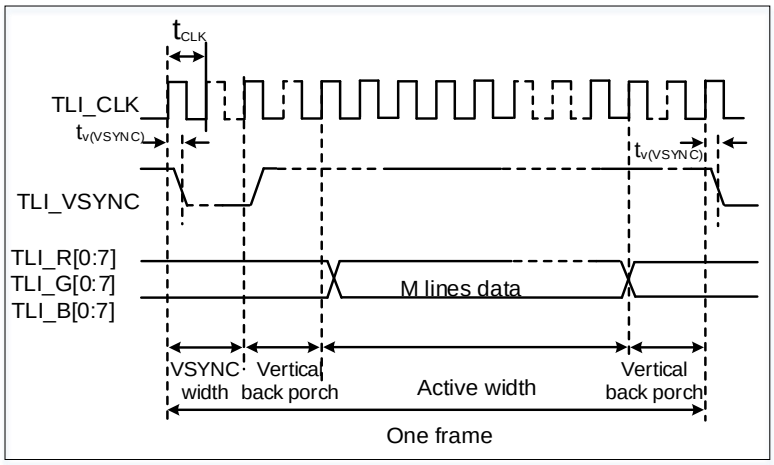


Figure 4-32. TLI vertical timing diagram



4.41. CAN characteristics

Refer to *Table 4-41. I/O static characteristics* for more details on the input/output alternate function characteristics (CAN TX and CAN RX).

4.42. USBHS characteristics

Table 4-76. USBHS start up time (1)

Symbol	Parameter	Max	Unit
$t_{STARTUP}$	USBHS startup time	1	µs

(1) Value guaranteed by design, not 100% tested in production.

Table 4-77. USBHS DC electrical characteristics(1)

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD33USB}$		USB operating voltage	-	3.0	-	3.6	V
LS/FS FUNCTIONALITY							
Input levels	V_{DIFS}	Differential input sensitivity(FS / LS)	-	0.2	-	-	V
	V_{CMFS}	Differential common mode range(FS / LS)	Includes V_{DI} range	0.8	-	2.5	
	V_{ILSE}	Single ended receiver low level input voltage(FS / LS)	-	-	-	0.8	
	V_{IHSE}	Single ended receiver high level input voltage(FS / LS)	-	2	-	-	
Output levels	V_{OLFS}	Static output level low(FS / LS)	R_L of 1.5 kΩ to VDD	-	-	0.3	V
	V_{OHFS}	Static output level high(FS / LS)	R_L of 15 kΩ to V_{SS}	2.8	-	-	
	V_{CRS}	Output signal crossover voltage	-	1.3	-	2.0	
R_{PD}		USBHS_DM / DP	V_{IN} = V_{DD}	14.25	21	24.8	kΩ
		PA9(USBHS_VBUS)(2)		0.77	0.9	1.1	
R_{PU}		USBHS_DM / DP	V_{IN} = V_{SS}	0.9	1.5	3.09	
		PA9(USBHS_VBUS) (2)		0.28	0.3	0.42	
Z_{FSDRV}		Driver Output Impedance	Steady state drive	6	-	22	Ω
HS FUNCTIONALITY							
Input levels	V_{CMHS}	Differential common mode range(HS)	-	-50	-	500	mV
	V_{HSSQ}	HS Squelch Detection Threshold	-	100	-	150	mV
	V_{HSDSC}	HS Disconnect Threshold	-	525	-	625	mV
Output levels	V_{HSOI}	High speed idle level	45 Ω load	-10	-	10	mV
	V_{OLHS}	High speed low level output voltage	45 Ω load	-10	-	10	mV
	V_{OHHS}	High speed high level output voltage	45 Ω load	360	400	440	mV
Z_{HSDRV}		Driver Output Impedance	Steady state drive	40.5	-	49.5	Ω

(1) Value guaranteed by design, not 100% tested in production.
(2) USBFS does not have VBUS-related functions.

Table 4-78. USBHS dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_R	Rise time(FS)	C_L = 50 pF	4	-	20	ns
t_{HSR}	Differential Rise Time(HS)	-	500	-	-	ps
t_F	Fall time(FS)	C_L = 50 pF	4	-	20	ns
t_{HSF}	Differential Fall Time(HS)	-	500	-	-	ps
t_{RFM}	Rise/ fall time matching(FS)	t_R / t_F	90	-	110	%

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-33. USBHS/FS timings: definition of data signal rise and fall time

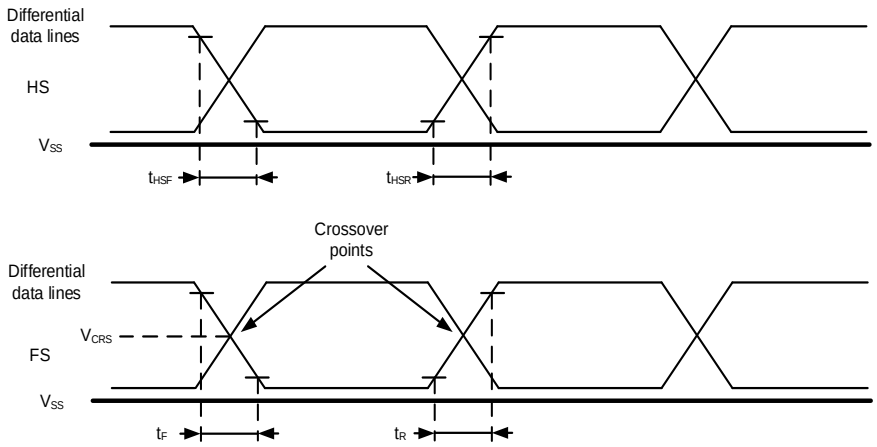


Table 4-79. USBHS Charger Detection characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DAT_SRC}	Data Source Voltage	-	0.5	-	0.7	V
I_{DP_SRC}	Data Connect Current	-	7	-	13	uA
V_{DAT_REF}	Data Detect Voltage	-	0.25	-	0.4	V
I_{DAT_sink}	Data(DP/DM) sink current	-	25	-	175	uA

(1) Value guaranteed by design, not 100% tested in production.

Table 4-80. USBHS clock timing parameters(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{HCLK}	f_{HCLK} value to guarantee proper operation of USBHS interface	30	-	-	MHz
F_{START_8BIT}	Frequency (first transition) 8-bit +/- 10%	54	60	66	MHz
F_{STEADY}	Frequency (steady state) +/-500 ppm	59.97	60	60.63	MHz
D_{START_8BIT}	Duty cycle (first transition) 8-bit +/- 10%	40	50	60	%
D_{STEADY}	Duty cycle (steady state) +/-500 ppm	49.975	50	50.025	%

(1) Value guaranteed by design, not 100% tested in production.

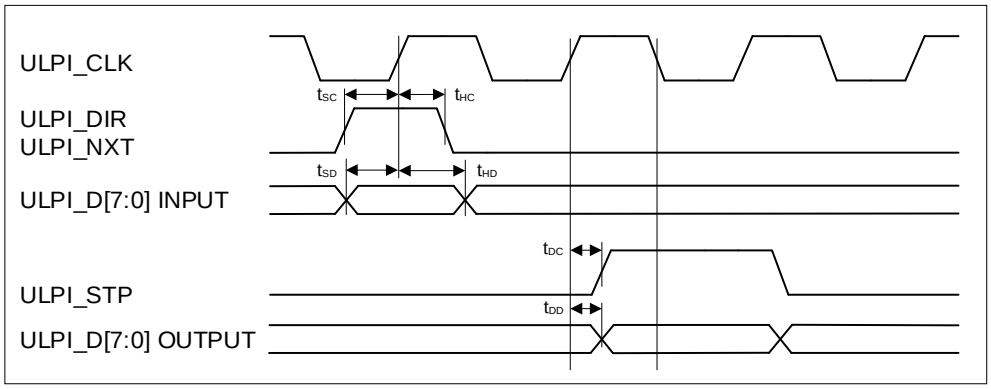
Table 4-81. USB-ULPI Dynamic characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
t_{SC}	Control in (ULPI_DIR, ULPI_NXT) setup time	-	-	2	ns

t_{HC}	Control in (ULPI_DIR, ULPI_NXT) hold time	0.5	-	-	ns
t_{SD}	Data in setup time	-	-	2	ns
t_{HD}	Data in hold time	0	-	-	ns

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-34. USBHS-ULPI timing diagram



4.43. EXMC characteristics

Table 4-82. Read timings of asynchronous non-multiplexed SRAM/PSRAM/NOR(1)(2)(3)

Symbol	Description	Min	Max	Unit
$t_{W(NE)}$	EXMC_NE low time	3*TCK_EXMC -1	3*TCK_EXMC +1	ns
$t_{V(NOE_NE)}$	EXMC_Nex low to EXMC_NOE low	0	-	ns
$t_{W(NOE)}$	EXMC_NOE low time	2*TCK_EXMC -1	2*TCK_EXMC +1	ns
$t_{H(NE_NOE)}$	EXMC_NOE high to EXMC_NE high hold time	TCK_EXMC -1	-	ns
$t_{V(A_NE)}$	EXMC_Nex low to EXMC_A valid	0	-	ns
$t_{V(BL_NE)}$	EXMC_Nex low to EXMC_BL valid	0	-	ns
$t_{SU(DATA_NE)}$	Data to EXMC_Nex high setup time	2*TCK_EXMC -1	-	ns
$t_{SU(DATA_NOE)}$	Data to EXMC_NOEx high setup time	TCK_EXMC -1	-	ns
$t_{H(DATA_NOE)}$	Data hold time after EXMC_NOE high	TCK_EXMC -1	-	ns
$t_{H(DATA_NE)}$	Data hold time after EXMC_Nex high	0	-	ns
$t_{V(NADV_NE)}$	EXMC_Nex low to EXMC_NADV low	0	-	ns
$t_{W(NADV)}$	EXMC_NADV low time	TCK_EXMC -1	TCK_EXMC +1	ns

(1) C_L = 30 pF.

(2) Value guaranteed by design, not 100% tested in production.

(3) Based on configure: f_{CK_EXMC} = 300 MHz, AddressSetupTime = 1, AddressHoldTime = 1, DataSetupTime = 1, DataHoldTime = 1.

Table 4-83. Write timings of asynchronous non-multiplexed SRAM/PSRAM/NOR(1)(2)(3)

Symbol	Description	Min	Max	Unit
$t_{W(NE)}$	EXMC_NE low time	3*TCK_EXMC -1	3*TCK_EXMC +1	ns
$t_{V(NEW_NE)}$	EXMC_Nex low to EXMC_NWE low	TCK_EXMC -1	-	ns
$t_{W(NEW)}$	EXMC_NWE low time	TCK_EXMC -1	TCK_EXMC +1	ns
$t_{H(NE_NWE)}$	EXMC_NWE high to EXMC_NE high hold time	TCK_EXMC -1	TCK_EXMC +1	ns
$t_{V(A_NE)}$	EXMC_Nex low to EXMC_A valid	0	-	ns
$t_{V(NADV_NE)}$	EXMC_Nex low to EXMC_NADV low	0	-	ns
$t_{W(NADV)}$	EXMC_NADV low time	TCK_EXMC -1	TCK_EXMC +1	ns
$t_{H(AD_NADV)}$	EXMC_AD(address) valid hold time after EXMC_NADV high	2*TCK_EXMC -1	-	ns
$t_{H(A_NWE)}$	Address hold time after EXMC_NWE high	TCK_EXMC -1	-	ns
$t_{H(BL_NWE)}$	EXMC_BL hold time after EXMC_NWE high	TCK_EXMC -1	-	ns
$t_{V(BL_NE)}$	EXMC_Nex low to EXMC_BL valid	0	-	ns
$t_{V(DATA_NADV)}$	EXMC_NADV high to DATA valid	0	-	ns
$t_{H(DATA_NWE)}$	Data hold time after EXMC_NWE high	TCK_EXMC -1	-	ns

(1) C_L = 30 pF.

(2) Value guaranteed by design, not 100% tested in production.

(3) Based on configure: f_{CK_EXMC} = 300 MHz, AddressSetupTime = 1, AddressHoldTime = 1, DataSetupTime = 1, DataHoldTime = 0.

Table 4-84. Read timings of asynchronous multiplexed PSRAM/NOR(1)(2)(3)

Symbol	Description	Min	Max	Unit
$t_{W(NE)}$	EXMC_NE low time	4*TCK_EXMC -1	4*TCK_EXMC +1	ns
$t_{V(NOE_NE)}$	EXMC_Nex low to EXMC_NOE low	2*TCK_EXMC -1	-	ns
$t_{W(NOE)}$	EXMC_NOE low time	TCK_EXMC -1	TCK_EXMC +1	ns
$t_{H(NE_NOE)}$	EXMC_NOE high to EXMC_NE high hold time	TCK_EXMC -1	-	ns
$t_{V(A_NE)}$	EXMC_Nex low to EXMC_A valid	0	-	ns
$t_{V(A_NOE)}$	Address hold time after EXMC_NOE high	TCK_EXMC -1	-	ns
$t_{V(BL_NE)}$	EXMC_Nex low to EXMC_BL valid	0	-	ns
$t_{H(BL_NOE)}$	EXMC_BL hold time after EXMC_NOE high	0	-	ns
$t_{SU(DATA_NE)}$	Data to EXMC_Nex high setup time	2*TCK_EXMC -1	-	ns
$t_{SU(DATA_NOE)}$	Data to EXMC_NOEx high setup time	TCK_EXMC -1	-	ns
$t_{H(DATA_NOE)}$	Data hold time after EXMC_NOE high	TCK_EXMC -1	-	ns
$t_{H(DATA_NE)}$	Data hold time after EXMC_Nex high	0	-	ns
$t_{V(NADV_NE)}$	EXMC_Nex low to EXMC_NADV low	0	-	ns
$t_{W(NADV)}$	EXMC_NADV low time	TCK_EXMC -1	TCK_EXMC +1	ns
$t_{H(AD_NADV)}$	EXMC_AD(162ddress) valid hold time after EXMC_NADV high	TCK_EXMC -1	TCK_EXMC +1	ns

(1) C_L = 30 pF.

(2) Value guaranteed by design, not 100% tested in production.

(3) Based on configure: f_{CK_EXMC} = 300 MHz, AddressSetupTime = 1, AddressHoldTime = 1, DataSetupTime = 1, DataHoldTime = 1.

Table 4-85. Write timings of asynchronous multiplexed PSRAM/NOR(1)(2)(3)

Symbol	Description	Min	Max	Unit
$t_{W(NE)}$	EXMC_NE low time	4*TCK_EXMC -1	4*TCK_EXMC +1	ns
$t_{V(NEW_NE)}$	EXMC_Nex low to EXMC_NWE low	TCK_EXMC -1	-	ns
$t_{W(NEW)}$	EXMC_NWE low time	2*TCK_EXMC -1	2*TCK_EXMC +1	ns
$t_{H(NE_NWE)}$	EXMC_NWE high to EXMC_NE high hold time	TCK_EXMC -1	-	ns
$t_{V(A_NE)}$	EXMC_Nex low to EXMC_A valid	0	-	ns
$t_{V(NADV_NE)}$	EXMC_Nex low to EXMC_NADV low	0	-	ns
$t_{W(NADV)}$	EXMC_NADV low time	TCK_EXMC -1	TCK_EXMC +1	ns
$t_{H(AD_NADV)}$	EXMC_AD(address) valid hold time after EXMC_NADV high	TCK_EXMC -1	-	ns
$t_{H(A_NWE)}$	Address hold time after EXMC_NWE high	TCK_EXMC -1	-	ns
$t_{H(BL_NWE)}$	EXMC_BL hold time after EXMC_NWE high	TCK_EXMC -1	-	ns
$t_{V(BL_NE)}$	EXMC_Nex low to EXMC_BL valid	0	-	ns
$t_{V(DATA_NADV)}$	EXMC_NADV high to DATA valid	TCK_EXMC -1	-	ns
$t_{H(DATA_NWE)}$	Data hold time after EXMC_NWE high	TCK_EXMC -1	-	ns

(1) C_L = 30 pF.

(2) Value guaranteed by design, not 100% tested in production.

(3) Based on configure: f_{CK_EXMC} = 300 MHz, AddressSetupTime = 1, AddressHoldTime = 1, DataSetupTime = 1, DataHoldTime = 0.

Table 4-86. Read timings of synchronous multiplexed PSRAM/NOR(1)(2)(3)

Symbol	Description	Min	Max	Unit
$t_{W\ (CLK)}$	EXMC_CLK period	T_{EXMC_CLK}	-	ns
$t_{D(CLKL-NexL)}$	EXMC_CLK low to EXMC_Nex low	0	-	ns
$t_{D(CLKH-NexH)}$	EXMC_CLK high to EXMC_Nex high	2*TCK_EXMC -1	-	ns
$t_{D(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	-	ns
$t_{D(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	-	ns
$t_{D(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	0	-	ns
$t_{D(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	2*TCK_EXMC -1	-	ns
$t_{D(CLKL-NOEL)}$	EXMC_CLK low to EXMC_NOE low	0	-	ns
$t_{D(CLKH-NOEH)}$	EXMC_CLK high to EXMC_NOE high	2*TCK_EXMC -1	-	ns
$t_{D(CLKL-ADV)}$	EXMC_CLK low to EXMC_AD valid	0	-	ns
$t_{D(CLKL-ADIV)}$	EXMC_CLK low to EXMC_AD invalid	0	-	ns

(1) C_L = 30 pF.

(2) Value guaranteed by design, not 100% tested in production.

(3) Based on configure: f_{CK_EXMC} = 400 MHz, BurstAccessMode = Enable; Memory Type = PSRAM; WriteBurst = Enable; CLKDivision = 3(EXMC_CLK is 4 divided by CK_EXMC); Data Latency = 1.

Table 4-87. Write timings of synchronous multiplexed PSRAM(1)(2)(3)

Symbol	Description	Min	Max	Unit
$t_{W(CLK)}$	EXMC_CLK period	TEXMC_CLK	-	ns
$t_{D(CLKL-NexL)}$	EXMC_CLK low to EXMC_Nex low	0	-	ns
$t_{D(CLKH-NexH)}$	EXMC_CLK high to EXMC_Nex high	2*TCK_EXMC - 1	-	ns
$t_{D(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	-	ns
$t_{D(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	-	ns
$t_{D(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	0	-	ns
$t_{D(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	2*TCK_EXMC - 1	-	ns
$t_{D(CLKL-NWEL)}$	EXMC_CLK low to EXMC_NWE low	0	-	ns
$t_{D(CLKH-NWEH)}$	EXMC_CLK high to EXMC_NWE high	2*TCK_EXMC - 1	-	ns
$t_{D(CLKL-ADIV)}$	EXMC_CLK low to EXMC_AD invalid	0	-	ns
$t_{D(CLKL-DATA)}$	EXMC_A/D valid data after EXMC_CLK low	0	-	ns
$t_{H(CLKL-NBLH)}$	EXMC_CLK low to EXMC_NBL high	0	-	ns

(1) C_L = 30 pF.
(2) Value guaranteed by design, not 100% tested in production.
(3) Based on configure: f_{CK_EXMC} = 400 MHz, BurstAccessMode = Enable; MemoryType = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by CK_EXMC); DataLatency = 1.

Table 4-88. Read timings of synchronous non-multiplexed PSRAM/NOR(1)(2)(3)

Symbol	Description	Min	Max	Unit
$t_{W(CLK)}$	EXMC_CLK period	TEXMC_CLK	-	ns
$t_{D(CLKL-NexL)}$	EXMC_CLK low to EXMC_Nex low	0	-	ns
$t_{D(CLKH-NexH)}$	EXMC_CLK high to EXMC_Nex high	2*TCK_EXMC - 1	-	ns
$t_{D(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	-	ns
$t_{D(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	-	ns
$t_{D(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	0	-	ns
$t_{D(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	2*TCK_EXMC - 1	-	ns
$t_{D(CLKL-NOEL)}$	EXMC_CLK low to EXMC_NOE low	0	-	ns
$t_{D(CLKH-NOEH)}$	EXMC_CLK high to EXMC_NOE high	2*TCK_EXMC - 1	-	ns

(1) C_L = 30 pF.
(2) Value guaranteed by design, not 100% tested in production.
(3) Based on configure: CK_EXMC = 400 MHz, BurstAccessMode = Enable; MemoryType = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by CK_EXMC); DataLatency = 1.

Table 4-89. Write timings of synchronous non-multiplexed PSRAM(1)(2)(3)

Symbol	Description	Min	Max	Unit
$t_{W(CLK)}$	EXMC_CLK period	TEXMC_CLK	-	ns
$t_{D(CLKL-NexL)}$	EXMC_CLK low to EXMC_Nex low	0	-	ns
$t_{D(CLKH-NexH)}$	EXMC_CLK high to EXMC_Nex high	2*TCK_EXMC - 1	-	ns
$t_{D(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	-	ns
$t_{D(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	-	ns
$t_{D(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	0	-	ns
$t_{D(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	2*TCK_EXMC - 1	-	ns
$t_{D(CLKL-NWEL)}$	EXMC_CLK low to EXMC_NWE low	0	-	ns
$t_{D(CLKH-NWEH)}$	EXMC_CLK high to EXMC_NWE high	2*TCK_EXMC - 1	-	ns
$t_{D(CLKL-DATA)}$	EXMC_A/D valid data after EXMC_CLK low	0	-	ns
$t_{H(CLKL-NBLH)}$	EXMC_CLK low to EXMC_NBL high	0	-	ns

(1) C_L = 30 pF.

(2) Value guaranteed by design, not 100% tested in production.

(3) Based on configure: CK_EXMC = 400 MHz, BurstAccessMode = Enable; MemoryType = PSRAM; WriteBurst = Enable; CLKDivision = 3(EXMC_CLK is 4 divided by CK_EXMC); DataLatency = 1.

Table 4-90. Read timings of SDRAM(1)

Symbol	Description	Min	Max	Unit
$t_{w(SDCLK)}$	EXMC_SDCLK period	2*TCK_EXMC-0.5	-	ns
$t_{su(SDCLKH_Data)}$	Data input setup time	2	-	ns
$t_{h(SDCLKH_Data)}$	Data input hold time	1	-	ns
$t_{d(SDCLKL_Add)}$	Address valid time	-	1.5	ns
$t_{d(SDCLKL_SDNE)}$	Chip select valid time	-	1.5	ns
$t_{h(SDCLKL_SDNE)}$	Chip select hold time	0	-	ns
$t_{d(SDCLKL_NRAS)}$	NRAS valid time	-	1.5	ns
$t_{h(SDCLKL_NRAS)}$	NRAS hold time	0	-	ns
$t_{d(SDCLKL_NCAS)}$	NCAS valid time	-	1.5	ns
$t_{h(SDCLKL_NCAS)}$	NCAS hold time	0	-	ns

(1) Value guaranteed by design, not 100% tested in production.

4.44. TIMER characteristics

Table 4-91. TIMER characteristics (1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{res}	Timer resolution time	-	1	-	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 300 MHz	3.3	-	ns
f_{EXT}	Timer external clock	-	0	$f_{TIMERxCLK}/2$	MHz

Symbol	Parameter	Conditions	Min	Max	Unit
	frequency	$f_{TIMERxCLK}$ = 300 MHz	0	150	MHz
RES	Timer resolution	TIMER0 & TIMER2 & TIMER3 & TIMER7& TIMER14 & TIMER15 & TIMER16 & TIMER30 & TIMER31 & TIMER40 & TIMER41 & TIMER42 & TIMER43 & TIMER44	-	16	bit
		TIMER1 & TIMER4 & TIMER5 & TIMER6 & TIMER22 & TIMER23	-	32	bit
		TIMER50 & TIMER51	-	64	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	-	1	65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 300 MHz	0.003	218.45	μs
	32-bit counter clock period when internal clock is selected	-	1	4294967296	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 300 MHz	0.003	14316557.65	μs
	64-bit counter clock period when internal clock is selected	-	1	1.84467E+19	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 300 MHz	0.003	6.14891E+16	μs
t_{MAX_COUNT}	Maximum possible count (16-bit)	-	-	4294967296	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 300 MHz	-	14.31655765	s
	Maximum possible count (32-bit)	-	-	2.81475E+14	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 300 MHz	-	260.6249784	h
	Maximum possible count (64-bit)	-	-	1.20893E+24	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 300 MHz	-	1.11938E+12	h

(1) Guaranteed by design, not 100% tested in production.

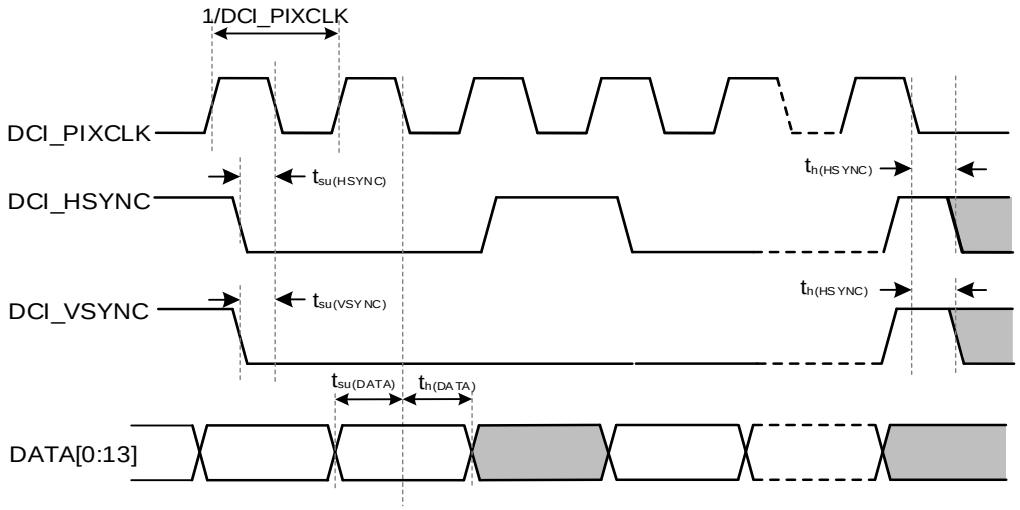
4.45. DCI characteristics

Table 4-92. DCI characteristics (1)

Symbol	Parameter	Min	Max	Unit
Frequency ratio	DCI_PIXCLK / f_{HCLK}	-	0.4	-
DCI_PIXCLK	Pixel clock input	-	110	MHz
Dpixel	Pixel clock input duty cycle	30	70	%
$t_{su(DATA)}$	Data input setup time	2	-	ns
$t_{h(DATA)}$	Data output valid time	1	-	ns
$t_{su(HSYNC)}$	DCI_HS input setup time	2	-	ns
$t_{su(VSYNC)}$	DCI_VS input setup time	2	-	ns
$t_{h(HSYNC)}$	DCI_HS input hold time	1	-	ns
$t_{h(VSYNC)}$	DCI_VS input hold time	1	-	ns

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-35. DCI timing diagram



4.46. GPSI characteristics

Table 4-93. GPSI TX characteristics (1)

Symbol	Parameter	Min	Max	Unit
Frequency ratio	Frequency ratio GPSI_CLK / f_{HCLK}	-	0.4	-
GPSI_CLK	GPSI Clock input	-	50	MHz
D_{Pixel}	Pixel Clock input duty cycle	30	70	%
$t_{ov(GPSI_D)}$	Data output valid time	-	10	ns
$t_{oh(GPSI_D)}$	Data output hold time	4.5	-	
$t_{ov(GPSI_DE)}$	DE output valid time	-	10	
$t_{oh(GPSI_DE)}$	DE output hold time	4	-	
$t_{su(GPSI_RDY)}$	RDY input setup time	0	-	
$t_{h(GPSI_RDY)}$	RDY input hold time	0	-	

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-36. GPSI transmit timing diagram

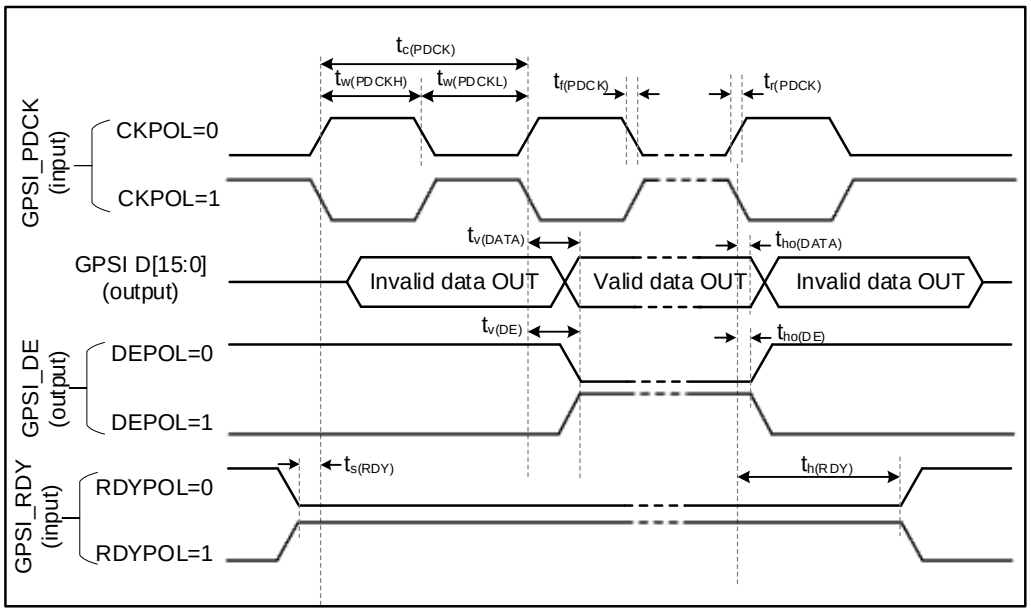
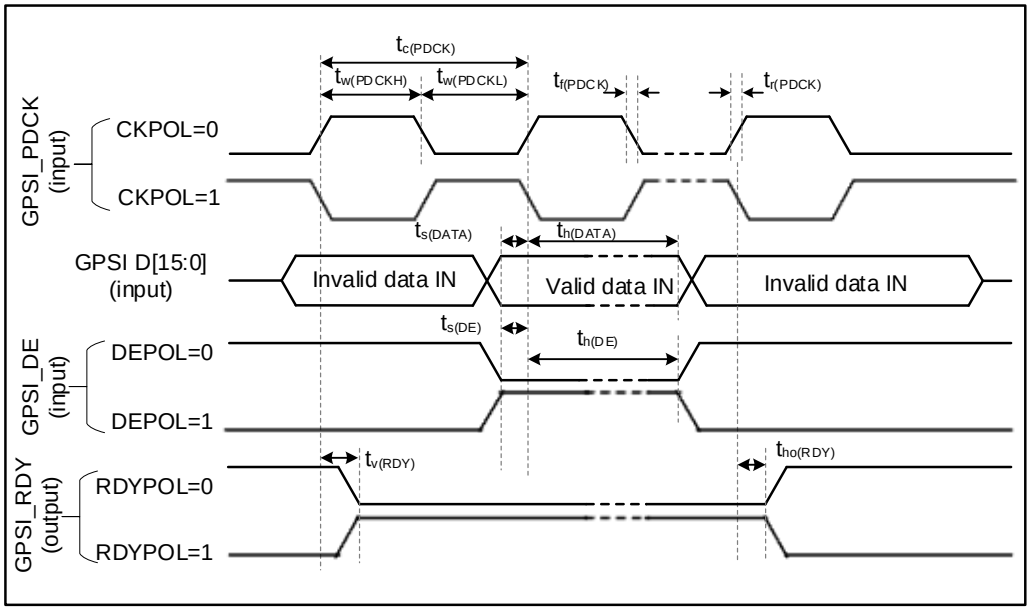


Table 4-94. GPSI RX characteristics(1)

Symbol	Parameter	Min	Max	Unit
Frequency ratio	Frequency ratio GPSI_CLK / f_{HCLK}	-	0.4	-
GPSI _CLK	GPSI Clock input	-	110	MHz
D_{Pixel}	Pixel Clock input duty cycle	30	70	%
$t_{su(GPSI_D)}$	Data input setup time	1.5	-	ns
$t_{h(GPSI_D)}$	Data input hold time	0.5	-	
$t_{su(GPSI_DE)}$	DE input setup time	2	-	
$t_{h(GPSI_DE)}$	DE input hold time	1	-	
$t_{ov(GPSI_RDY)}$	RDY output valid time	-	15	
$t_{oh(GPSI_RDY)}$	RDY output hold time	5.5	-	

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-37. GPSI receive timing diagram



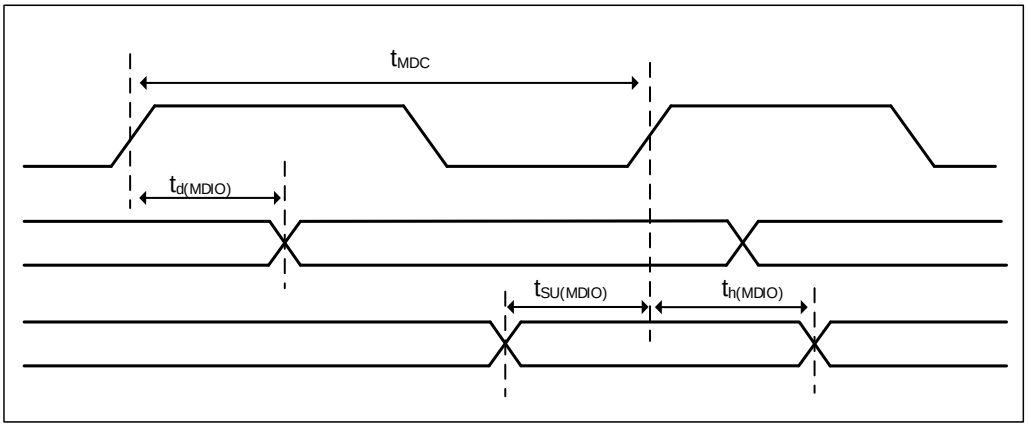
4.47. MDIO characteristics

Table 4-95. MDIO characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
F_{sDC}	Management data clock	-	-	4	MHz
$t_{d(MDIO)}$	Management data input/output output valid time	-	-	22	ns
$t_{su(MDIO)}$	Management data input/output setup time	6	-	-	
$t_{h(MDIO)}$	Management data input/output hold time	6	-	-	

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-38. MDIO Slave timing diagram



4.48. EDIM characteristics

Table 4-96. AFMT individual transmission mode characteristics(1)(2)(3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CK_AFMT	Clock for AFMT module	-	-	80	-	MHz
T1	-	Baud rate = 2.5 Mbps	-	7.2	-	µs
		Baud rate = 4 Mbps	-	4.5	-	
		Baud rate = 6.67 Mbps	-	2.7	-	
		Baud rate = 8 Mbps	-	2.25	-	
		Baud rate = 16 Mbps	-	1.125	-	
T2	-	Baud rate = 2.5 Mbps	1	-	-	µs
		Baud rate = 4 Mbps	1	-	-	
		Baud rate = 6.67 Mbps	1	-	-	
		Baud rate = 8 Mbps	1	-	-	
		Baud rate = 16 Mbps	1	-	-	
T3	-	Baud rate = 2.5 Mbps	-	1.5	-	µs
		Baud rate = 4 Mbps	-	1	-	
		Baud rate = 6.67 Mbps	-	1	-	
		Baud rate = 8 Mbps	-	0.7	-	
		Baud rate = 16 Mbps	-	0.7	-	
T4	-	Baud rate = 2.5 Mbps	1	-	-	µs
		Baud rate = 4 Mbps	1	-	-	
		Baud rate = 6.67 Mbps	1	-	-	
		Baud rate = 8 Mbps	1	-	-	
		Baud rate = 16 Mbps	1	-	-	
T5(4)	-	-	-	-	-	-
T6	-	Baud rate = 2.5 Mbps	-	T1*N(5)	-	µs
		Baud rate = 4 Mbps	-	T1*N(5)	-	
		Baud rate = 6.67 Mbps	-	T1*N(5)	-	
		Baud rate = 8 Mbps	-	T1*N(5)	-	
		Baud rate = 16 Mbps	-	T1*N(5)	-	
T7	-	Baud rate = 2.5 Mbps	-	387.5	-	ns
		Baud rate = 4 Mbps	-	237.5	-	
		Baud rate = 6.67 Mbps	-	137.5	-	
		Baud rate = 8 Mbps	-	112.5	-	
		Baud rate = 16 Mbps	-	50	-	
T8	-	Baud rate = 2.5 Mbps	-	1.2	-	µs
		Baud rate = 4 Mbps	-	0.8	-	
		Baud rate = 6.67 Mbps	-	0.8	-	
		Baud rate = 8 Mbps	-	0.4	-	
		Baud rate = 16 Mbps	-	0.4	-	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T9	-	Baud rate = 2.5 Mbps	3.5	-	-	µs
		Baud rate = 4 Mbps	2.5	-	-	
		Baud rate = 6.67 Mbps	2.5	-	-	
		Baud rate = 8 Mbps	2.2	-	-	
		Baud rate = 16 Mbps	2.2	-	-	

(1) Value guaranteed by design, not 100% tested in production.
(2) It is assumed that both the transmission line delay and the transceiver circuit propagation delay are 0.
(3) The data transmission time varies depending on the command.
(4) This data is determined by the encoder slave.
(5) T1 selects the value corresponding to the baud rate, N = 2 to 10.

Figure 4-39. AFMT individual transmission mode timing diagram

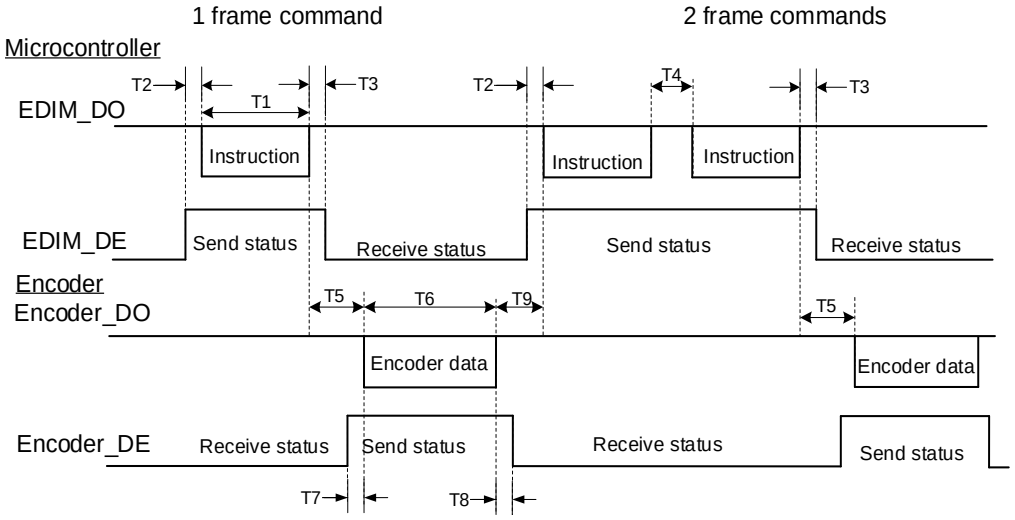


Table 4-97. AFMT broadcast transmission mode characteristics(1)(2)(3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CK_AFMT	Clock for AFMT module	-	-	80	-	MHz
T1	-	Baud rate = 2.5 Mbps	-	7.2	-	µs
		Baud rate = 4 Mbps	-	4.5	-	
		Baud rate = 6.67 Mbps	-	2.7	-	
		Baud rate = 8 Mbps	-	2.25	-	
		Baud rate = 16 Mbps	-	1.125	-	
T2	-	Baud rate = 2.5 Mbps	7.5	-	-	µs
		Baud rate = 4 Mbps	5	-	-	
		Baud rate = 6.67 Mbps	3.2	-	-	
		Baud rate = 8 Mbps	3	-	-	
		Baud rate = 16 Mbps	2	-	-	
T3	-	Baud rate = 2.5 Mbps	-	1.5	-	µs
		Baud rate = 4 Mbps	-	1.0	-	
		Baud rate = 6.67 Mbps	-	1.0	-	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		Baud rate = 8 Mbps	-	0.7	-	
		Baud rate = 16 Mbps	-	0.7	-	
T4	-	Baud rate = 2.5 Mbps	1	-	-	µs
		Baud rate = 4 Mbps	1	-	-	
		Baud rate = 6.67 Mbps	1	-	-	
		Baud rate = 8 Mbps	1	-	-	
		Baud rate = 16 Mbps	1	-	-	
T5(4)	-	-	-	-	-	-
T6	-	Baud rate = 2.5 Mbps	-	T1*N(5)	-	µs
		Baud rate = 4 Mbps	-	T1*N(5)	-	
		Baud rate = 6.67 Mbps	-	T1*N(5)	-	
		Baud rate = 8 Mbps	-	T1*N(5)	-	
		Baud rate = 16 Mbps	-	T1*N(5)	-	
T7	-	Baud rate = 2.5 Mbps	-	387.5	-	ns
		Baud rate = 4 Mbps	-	237.5	-	
		Baud rate = 6.67 Mbps	-	137.5	-	
		Baud rate = 8 Mbps	-	112.5	-	
		Baud rate = 16 Mbps	-	50	-	
T8	-	Baud rate = 2.5 Mbps	-	1.2	-	µs
		Baud rate = 4 Mbps	-	0.8	-	
		Baud rate = 6.67 Mbps	-	0.8	-	
		Baud rate = 8 Mbps	-	0.4	-	
		Baud rate = 16 Mbps	-	0.4	-	
T9	-	Baud rate = 2.5 Mbps	10	-	-	µs
		Baud rate = 4 Mbps	6.5	-	-	
		Baud rate = 6.67 Mbps	5	-	-	
		Baud rate = 8 Mbps	4	-	-	
		Baud rate = 16 Mbps	3	-	-	

(1) Value guaranteed by design, not 100% tested in production.
(2) It is assumed that both the transmission line delay and the transceiver circuit propagation delay are 0.
(3) The data transmission time varies depending on the command.
(4) This data is determined by the encoder slave.
(5) T1 selects the value corresponding to the baud rate, N = 2 to 10.

Figure 4-40. AFMT broadcast transmission mode timing diagram

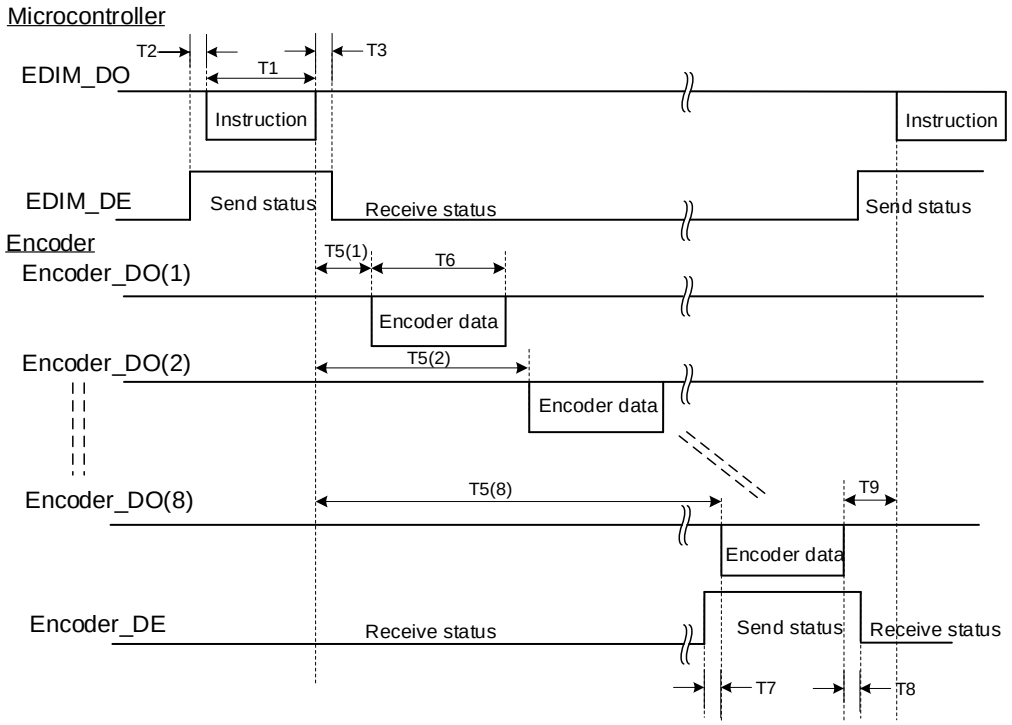


Table 4-98. TFMT characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
CK_TFMT	Clock for TFMT module	-	80	-	MHz
T	-	-	-	0.5	μs

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-41. TFMT detection of start frame timing diagram

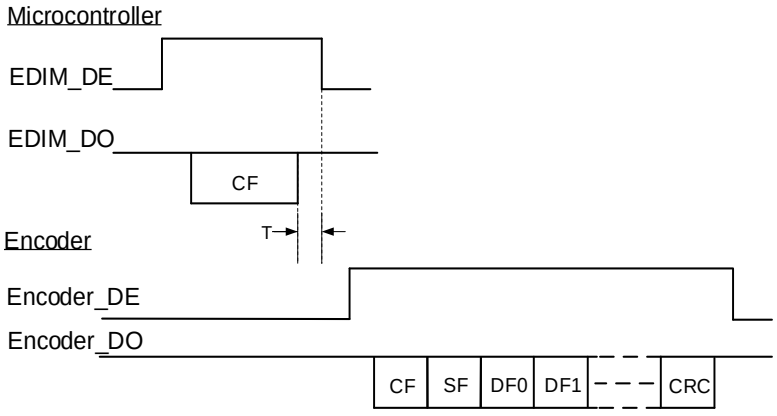


Table 4-99. ENDAT characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CK_ENDAT	Clock for ENDAT module	-	-	100	-	MHz
f_{OUT}	Output clock frequency	Have delay time compensation	0.1	-	8	MHz

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		No delay time compensation	0.1	-	2	
$Duty_{ENDAT}$	Clock duty cycle	-	-	50	-	%

(1) Value guaranteed by design, not 100% tested in production.

Table 4-100. BISS characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OUT}	Output clock frequency($1/T_{MA}$)	Permissible clock frequency	0.08	-	10	MHz
		Required clock frequency(3)(4)	0.25	-	1	
t_{MAI_lo}	Clock signal low level duration	MA = "0" at receiver	40	-	-	$\%T_{MA_min}$(2)
t_{MAI_hi}	Clock signal high level duration	MA = "1" at receiver	40	-	-	$\%T_{MA_min}$(2)
t_{TO}	Static BISS timeout	-	12.5	-	40	µs
t_{TOA}	Adaptive BISS timeout	For slaves with automatic BISS timeout adaption on T_{MA}	t_{TOA_ref}		$t_{TOA_ref} + 3 \cdot T_{CLK}$(5)	µs
$t_{LineDelay}$	Line delay MA -> SL	Measured from second rising edge at MA to first falling edge at SL at re-ceiver	0	-	40	µs
$t_{LineJitter}$	Line delay jitter MA -> SL	Permissible deviation from $t_{LineDelay}$ at receiver	-25	-	25	$\%T_{MA}$
t_{busy}	Processing time	-	$2T_{MA}$	-	40	µs
busy_s	Additional start bit delay (in clocks)	t_{busy} +busy_s <= 40µs	0	-	8	T_{MA}
t_{busy_r}	Processing time for register access	-	0	-	20	ms
t_{Cycle_min}	Minimum cycle time	Supported by all slaves	-	-	250	µs

(1) Value guaranteed by design, not 100% tested in production.

(2) The maximum clock frequency depends on the transmission medium and on the individual devices. The corresponding minimum clock period T_{MAI_min} is usually stored in the EDS.

(3) The required clock frequency has to be supported by any BiSS slave. A BISS master can use it for initial operation to read the slave's EDS.

(4) The maximum cable length is 100 meters.

(5) $1/T_{CLK}$ is the BISS slave's minimum sampling frequency. T_{TOA_ref} is measured from first falling to second rising edge at MAI.

Figure 4-42. BISS slave timings for point-to-point configuration

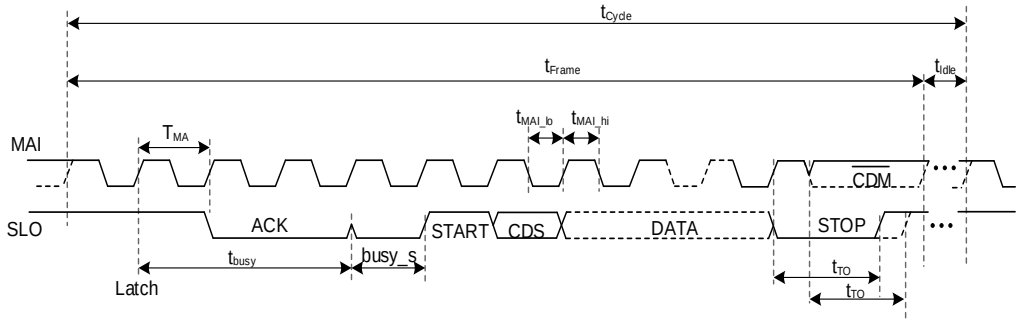


Figure 4-43. BISS master timings for point-to-point configuration

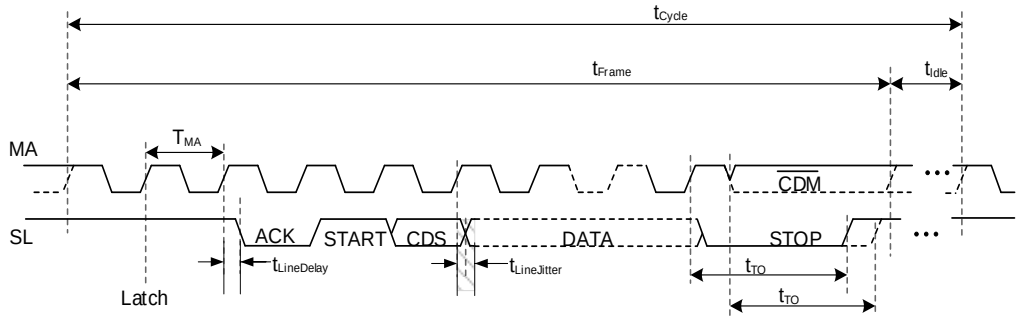


Figure 4-44. Adaptive BISS timeout

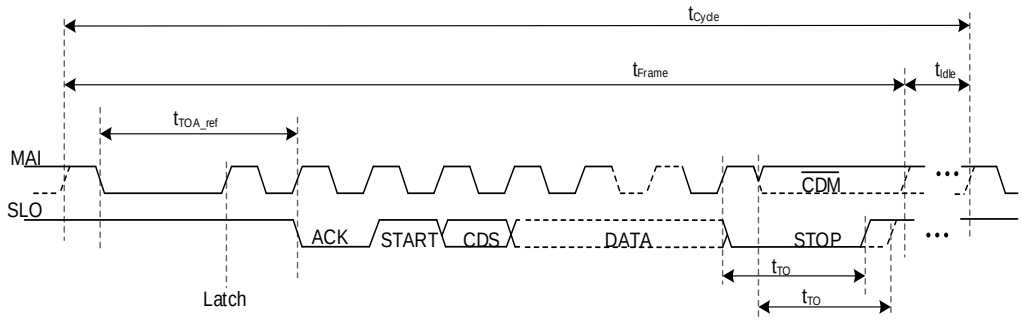
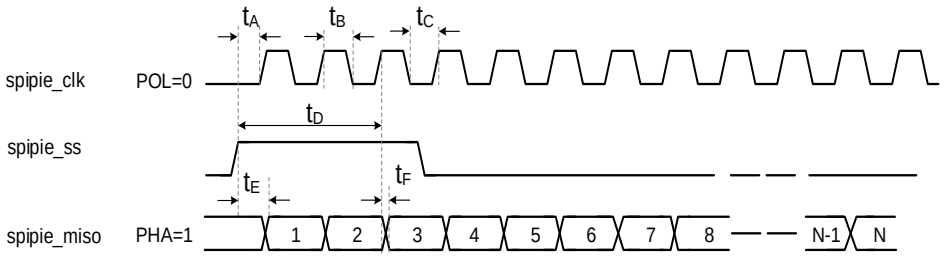


Table 4-101. HDSL SPI-PIPE characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
A	Assertion of spipipe_ss before spipipe_clk	30	-	-	ns
B	Time for spipipe_clk high	30	-	-	
C	Time for spipipe_clk low	30	-	-	
D	Spipipe_ss pulse width	30	-	-	
E	Delay spipipe_miso after spipipe_ss high	25	70	-	
F	Delay spipipe_miso after spipipe_clk high	25	70	-	

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-45. HDSL SPI-PIPE interface time control



4.49. WDGT characteristics

Table 4-102. FWDGT min/max timeout period at 32 kHz (IRC32K) (1)

Prescaler divider	PSC[2:0] bits	Min timeout RLD[11:0]= 0x000	Max timeout RLD[11:0]= 0xFFF	Unit
1/4	000	0.125	512	ms
1/8	001	0.25	1024	
1/16	010	0.5	2048	
1/32	011	1.0	4096	
1/64	100	2.0	8192	
1/128	101	4.0	16384	
1/256	110 or 111	8.0	32768	

(1) Value guaranteed by design, not 100% tested in production.

Table 4-103. WWDGT min-max timeout value at 150 MHz (f_{PCLK3}) (1)

Prescaler divider	PSC[2:0]	Min timeout value CNT[6:0] = 0x40	Unit	Max timeout value CNT[6:0] = 0x7F	Unit
1/1	00	27.3	µs	1.747	ms
1/2	01	54.61		3.495	
1/4	10	109.23		6.99	
1/8	11	218.45		13.98	

(1) Value guaranteed by design, not 100% tested in production.

4.50. ENET characteristics

Table 4-104. Dynamics characteristics: Ethernet MAC signals for SMI(1)

Symbol	Description	Min	Typ	Max	Unit
t_{MDC}	MDC cycle time(2.5 MHz)	400	400	400	ns
$T_{D(MDIO)}$	Write data valid delay time	1/4 t_{MDC}	1/4 t_{MDC}	1/4 t_{MDC}	
$t_{SU(MDIO)}$	Read data setup time	12	-	-	
$t_{H(SD_MR)}$	Read data hold time	0	-	-	

(1) Guaranteed by design, not tested in production.

Figure 4-46. Ethernet SMI timing diagram

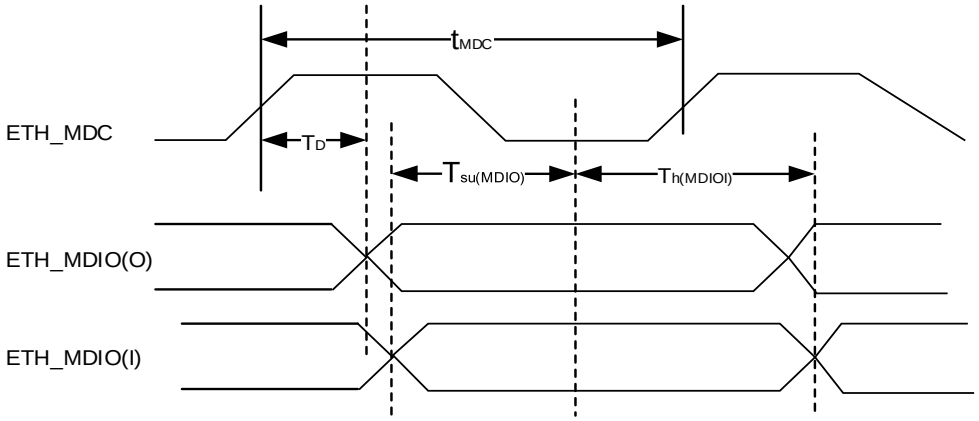


Table 4-105. Ethernet timing for MII (1)

Symbol	Description	Min	Typ	Max	Unit
-	RXCLK frequency	-	25	-	MHz
MII1	RXCLK pulse widthhigh	35	-	65	%RXCLK period
MII2	RXCLK pulse width low	35	-	65	%RXCLK period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	-	-	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	-	-	ns
t_{CYC_TX}	TXCLK frequency	-	25	-	MHz
MII5	TXCLK pulse widthhigh	35	-	65	%TXCLK period
MII6	TXCLK pulse widthlow	35	-	65	%TXCLK period
MII7	TXCLK to TXD[3:0],TXEN, TXER invalid	2	-	-	ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	-	-	25	ns

(1) Guaranteed by design, not 100% tested in production.

Figure 4-47. Ethernet MII receive diagram

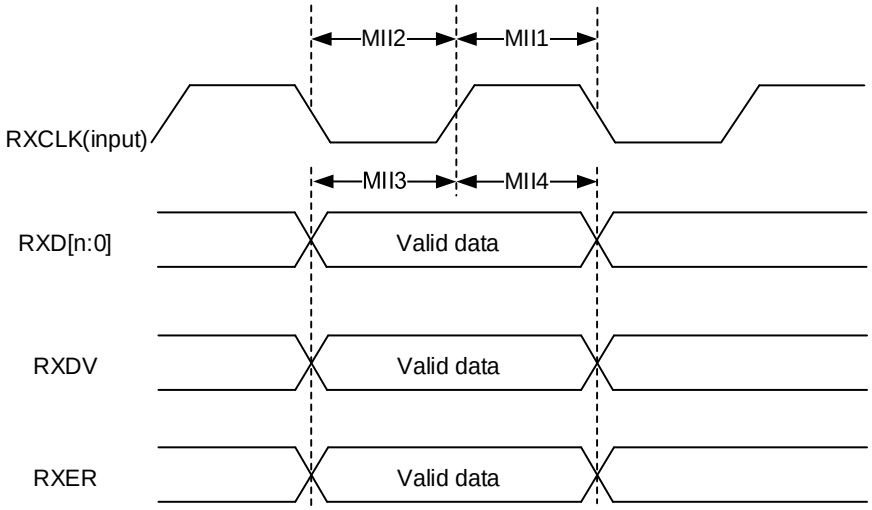


Figure 4-48. Ethernet MII transmit diagram

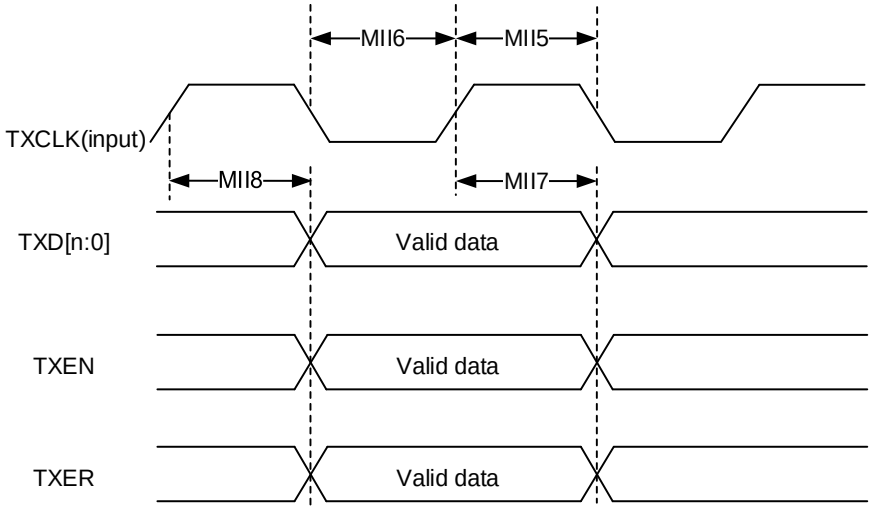


Table 4-106. Ethernet MAC timing for RMII(1)

Symbol	Description	Min	Typ	Max	Unit
-	RMII input clock frequency (RMII_CLK)	-	-	50	MHz
RMII1, RMII5	RMII_CLK pulse widthhigh	35	-	65	%RMII_CLK period
RMII2, RMII6	RMII_CLK pulse widthlow	35	-	65	%RMII_CLK period
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	-	-	ns
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	-	-	ns
RMII8	RMII_CLK to TXD[1:0], TXEN data valid	-	-	14	ns
RMII7	RMII_CLK to TXD[1:0], TXEN data invalid	2	-	-	ns

(1) Guaranteed by design, not 100% tested in production.

Figure 4-49. Ethernet RMII receive diagram

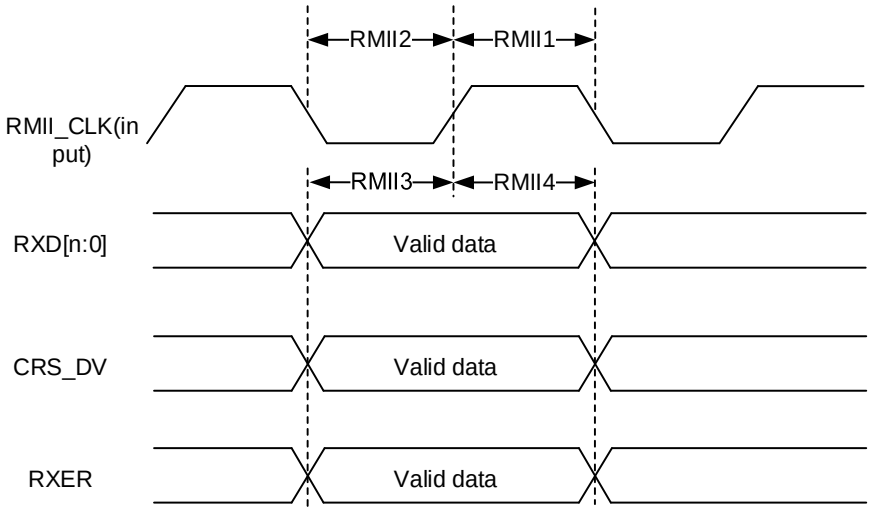
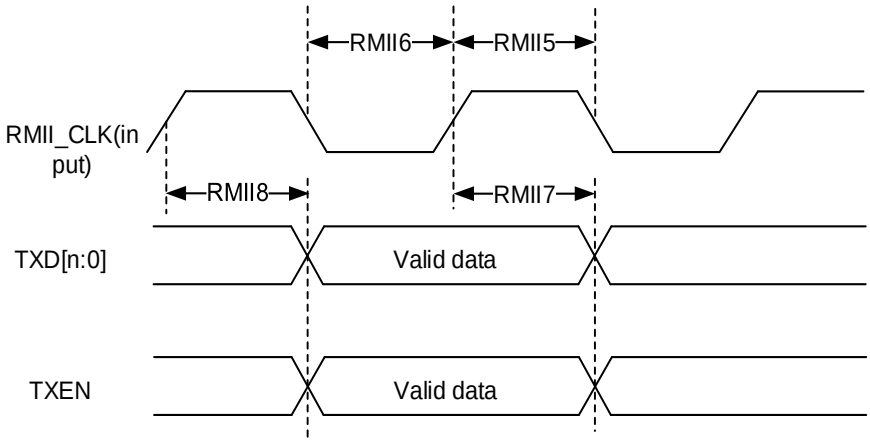


Figure 4-50. Ethernet RMII transmit diagram



4.51. RDCM characteristics

Table 4-107. RDCM characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{RDCM}	Clock for RDCM	-	Refer to ADC0 / 1			MHz
f_{SIN}	Sinusoidal excitor frequency	-	2	-	100	kHz
V_{DAC}	DAC output voltage	V_{DD} = V_{DDA} = V_{REFP} = 3.3 V	Refer to DAC			V

(1) Value guaranteed by design, not 100% tested in production.

4.52. DSI characteristics

Table 4-108. DSI HS-TX DC characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CMTX}	HS transmit common mode voltage	150	200	250	mV
$\|\Delta V_{CMTX(1,0)}\|$	V_{CMTX} mismatch when output is differential-1 or Differential-0	-	-	5	
$\|V_{OD}\|$	HS transmit differential voltage	140	200	270	
$\|\Delta V_{OD}\|$	V_{OD} mismatch when output is differential-1 or Differential-0	-	-	14	
V_{OHHS}	HS output high voltage	-	-	360	mV
Z_{OS}	Single ended output impedance	40	50	62.5	Ω
ΔZ_{OS}	Single ended output impedance mismatch	-	-	10	%

(1) Value guaranteed by design, not 100% tested in production.

Table 4-109. DSI HS-TX AC characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
$\Delta V_{CMTX(HF)}$	Common-level variations above 450MHz	-	-	15	mV_{RMS}
$\Delta V_{CMTX(LF)}$	Common-level variation between 50-450 MHz	-	-	25	mV_{PEAK}
t_R & t_F	20% - 80% rise and fall time	50	-	-	ps

(1) Value guaranteed by design, not 100% tested in production.

Table 4-110. DSI LP-TX DC characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{OL}	Thevenin output low level	-50	-	50	mV
V_{OH}	Thevenin output high level for 1.5Gbps and below	1.1	1.2	1.3	V
Z_{OLP}	Output impedance of LP transmitter	110	-	-	Ω

(1) Value guaranteed by design, not 100% tested in production.

Table 4-111. DSI LP-TX AC characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
t_{RLP} / t_{FLP}	15% - 85% rise time, fall time	-	-	25	ns
t_{REOT}	30% - 85% rise time and fall time	-	-	35	ns

Symbol	Parameter	Min	Typ	Max	Unit
$\Delta V / \Delta t_{SR}$	Slew rate @ Cload = 0 pF	-	-	500	mV/ns
	Slew rate @ Cload = 5 pF	-	-	300	mV/ns
	Slew rate @ Cload = 20 pF	-	-	250	mV/ns
	Slew rate @ Cload = 70 pF	-	-	150	mV/ns

(1) Value guaranteed by design, not 100% tested in production.

Table 4-112. DSI LP-RX DC characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Logic 0 input voltage, not in ULP state	-	-	550	mV
$V_{IL-ULPS}$	Logic 0 input voltage in ULP State	-	-	300	
V_{IH}	Logic 1 input voltage	880	-	-	
V_{hys}	Voltage hysteresis	25	-	-	

(1) Value guaranteed by design, not 100% tested in production.

Table 4-113. DSI LP-RX AC characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
e_{SPIKE}	Input pulse rejection	-	-	300	V_{PS}
T_{MIN-RX}	Minimum pulse width response	20	-	-	ns
V_{INT}	Peak interference amplitude	-	-	200	mV
f_{INT}	Interference frequency	450	-	-	MHz

(1) Value guaranteed by design, not 100% tested in production.

Table 4-114. DSI LP-CD characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{ILCD}	Logic 0 contention threshold	-	-	200	mV
V_{IHCD}	Logic 1 contention threshold	450	-	-	

(1) Value guaranteed by design, not 100% tested in production.

Table 4-115. DSI DC characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PIN}	Pin signal voltage range	-50	-	1350	mV
I_{LEAK}	Pin Leakage current in DPHY function	-10	-	10	μA
V_{GNDSH}	Ground Shift	-50	-	50	mV
$V_{PIN(absmax)}$	Transient pin voltage level	-0.15	-	1.45	V
$T_{VPIN(absmax)}$	Maximum transient time above $V_{PIN(max)}$ or below $V_{PIN(min)}$	-	-	20	ns

(1) Value guaranteed by design, not 100% tested in production.

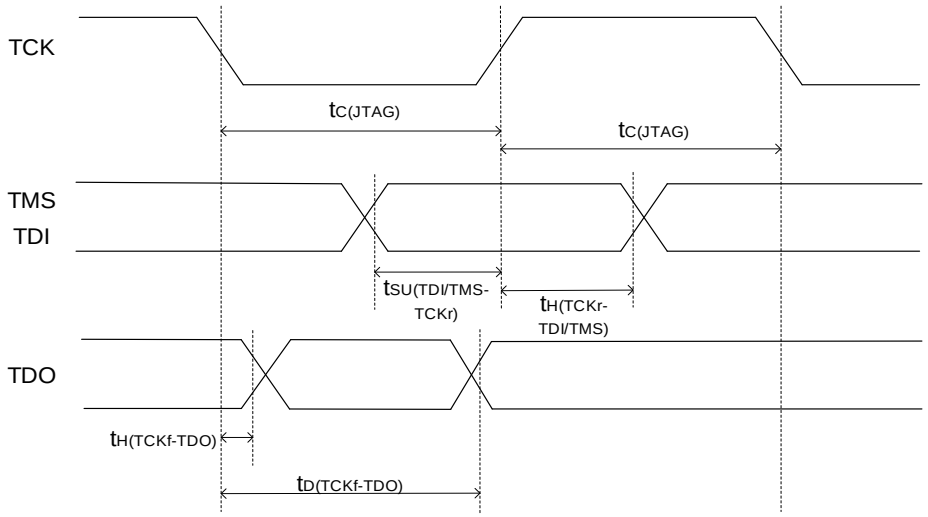
4.53. JTAG Timing

Table 4-116. JTAG Scan Interface Timing(1)

Symbol	Description	Min	Max	Unit
t_{TCK}	TCK clock frequency	-	50	MHz
$t_{C(JTAG)}$	Cycle time, JTAG low and high period	8	-	ns
$t_{SU(TDI/TMS - TCKr)}$	Setup time, TDI, TMS before TCK rise (TCKr)	6	-	ns
$t_{H(TCKr -TDI/TMS)}$	Hold time, TDI, TMS after TCKr	1	-	ns
$t_{H(TCKf -TDO)}$	Hold time, TDO after TCKf	1	-	ns
$t_{D(TCKf -TDO)}$	Delay time, TDO valid after TCK fall (TCKf)	-	6	ns

(1) Guaranteed by design, not 100% tested in production.

Figure 4-51. JTAG timing diagram



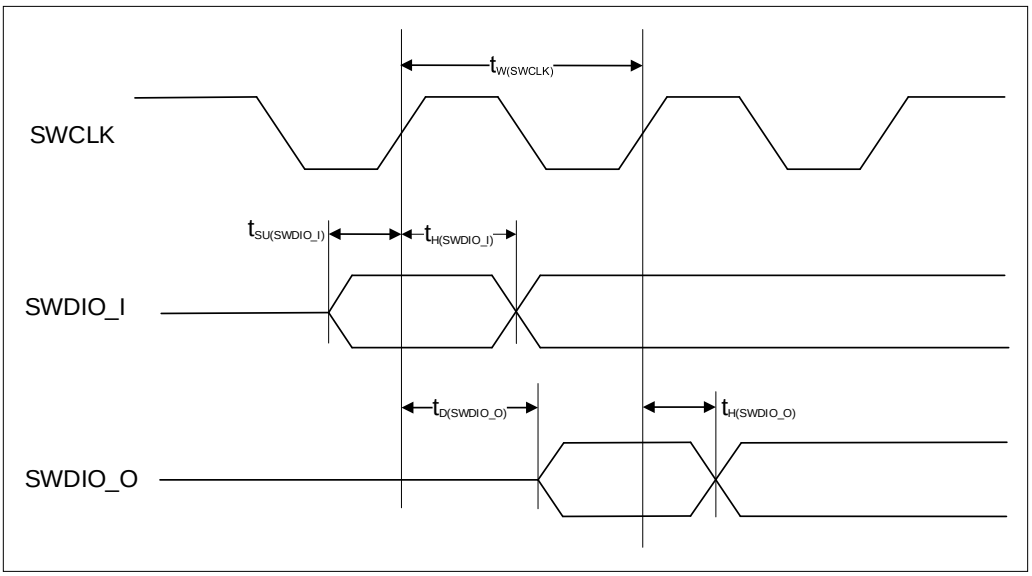
4.54. SWD Timing

Table 4-117. SWD Interface Timing (1)

Symbol	Description	Min	Max	Unit
F_{SWCLK}	SWCLK clock frequency	-	50	MHz
$t_{CYC(SWCLK)}$	SWCLK clock cycle time	20	-	ns
$t_{isu(SWDIO)}$	SWDIO input setup time	6	-	ns
$t_{ih(SWDIO)}$	SWDIO input hold time	1	-	ns
$t_{ov(SWDIO)}$	SWDIO output valid time	-	6	ns
$t_{oh(SWDIO)}$	SWDIO output hold time	1	-	ns

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-52. SWD timing diagram



5. Package information

5.1. BGA176 package outline dimensions

Figure 5-1. BGA176 package outline

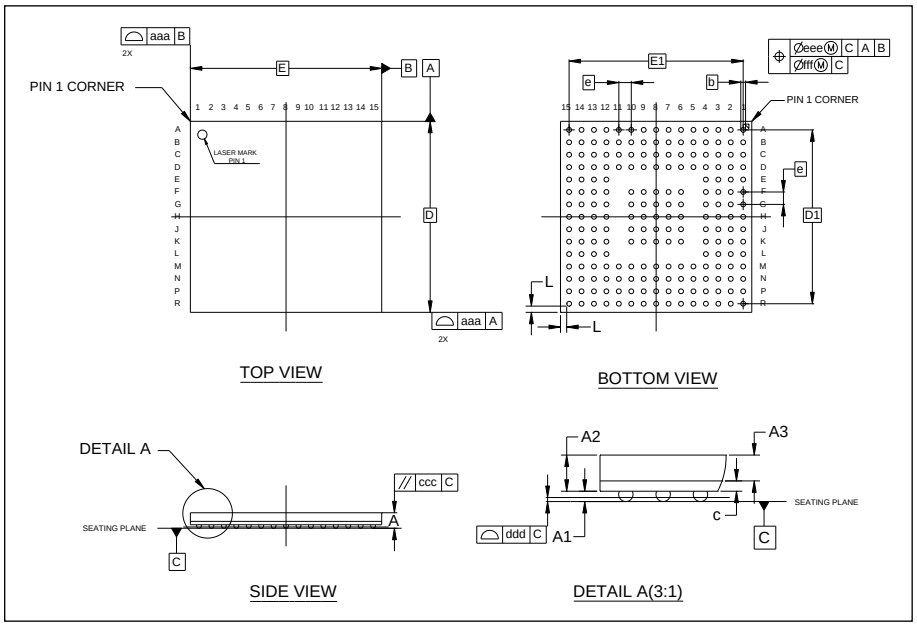
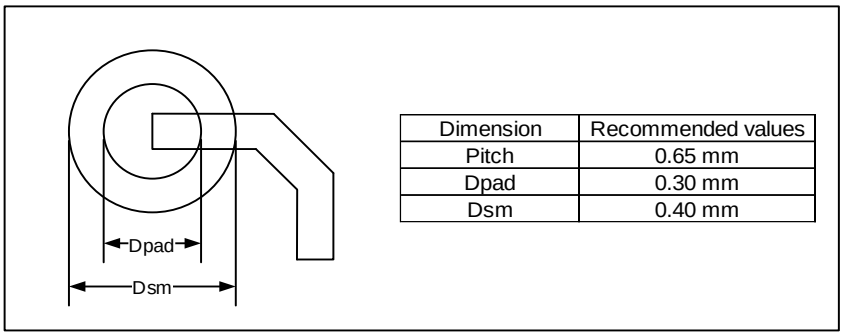


Table 5-1. BGA176 package dimensions

Symbol	Min	Typ	Max
A	0.54	0.61	0.68
A1	0.03	0.08	0.13
A2	0.48	0.53	0.58
A3	-	0.40	-
b	0.22	0.27	0.32
c	0.10	0.13	0.16
D	9.90	10.00	10.10
D1	-	9.10	-
E	9.90	10.00	10.10
E1	-	9.10	-
e	-	0.65	-
L	-	0.315	-
aaa	-	0.10	-
ccc	-	0.08	-
ddd	-	0.08	-
eee	-	0.15	-
fff	-	0.05	-

(Original dimensions are in millimeters)

Figure 5-2. BGA176 recommended footprint



Dimension	Recommended values
Pitch	0.65 mm
Dpad	0.30 mm
Dsm	0.40 mm

(Original dimensions are in millimeters)

5.2. Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter "θ". For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

Θ_{JA}: Thermal resistance, junction-to-ambient.

Θ_{JB}: Thermal resistance, junction-to-board.

Θ_{JC}: Thermal resistance, junction-to-case.

Ψ_{JB}: Thermal characterization parameter, junction-to-board.

Ψ_{JT}: Thermal characterization parameter, junction-to-top center.

$$\Theta_{JA}=(T_J-T_A)/P_D \quad (5\text{-}1)$$

$$\theta_{JB}=(T_J-T_B)/P_D \quad (5\text{-}2)$$

$$\theta_{JC}=(T_J-T_C)/P_D \quad (5\text{-}3)$$

Where, T_J = Junction temperature.

T_A = Ambient temperature

T_B = Board temperature

T_C = Case temperature which is monitoring on package surface

P_D = Total power dissipation

θ_{JA} represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower θ_{JA} can be considerate as better overall thermal performance.

Θ_{JB} is used to measure the heat flow resistance between the chip surface and the PCB board.

Θ_{JC} represents the thermal resistance between the chip surface and the package top case. Θ_{JC} is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

Table 5-2. Package thermal characteristics(1)

Symbol	Condition	Package	Value	Unit
θ_{JA}	Natural convection, 2S2P PCB	BGA176	36.2	°C/W
θ_{JB}	Cold plate, 2S2P PCB	BGA176	24.5	°C/W
θ_{JC}	Cold plate, 2S2P PCB	BGA176	12	°C/W
Ψ_{JB}	Natural convection, 2S2P PCB	BGA176	24.3	°C/W
Ψ_{JT}	Natural convection, 2S2P PCB	BGA176	0.4	°C/W

(1): Thermal characteristics are based on simulation, and meet JEDEC specification.

6. Ordering information

Table 6-1. Part ordering code for GD32H77Dxx devices

Ordering code	NVM (KB)	Package	Package type	Temperature operating range
GD32H77DIWK7	9728	BGA176	Green	Industrial -40°C to +105°C
GD32H77DIPK7	5632	BGA176	Green	Industrial -40°C to +105°C
GD32H77DIIK7	1664	BGA176	Green	Industrial -40°C to +105°C

7. Revision history

Table 7-1. Revision history

Revision No.	Description	Date
0.9RC1	Initial Release	Nov. 9, 2026

Important Notice

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