GigaDevice Semiconductor Inc.

Device limitations of GD32H77x_78x

Errata Sheet

Revision 1.0

(Nov. 2026)

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1. Introduction

This document applies to GD32H77x_78x product series, as shown in ***Table 1-1. Applicable products***. It offers technical guidance for using GD32 MCU and provides workaround to current device limitations.

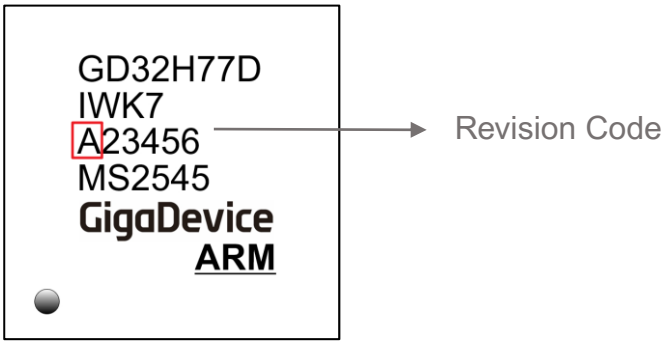
Table 1-1. Applicable products

Type	Part Numbers
MCU	GD32H779xx series
	GD32H77Dxx series
	GD32H77Exx series
	GD32H77Rxx series
	GD32H789xx series
	GD32H78Dxx series
	GD32H78Exx series

1.1. Revision identification

The device revision can be identified according to the mark on the top of the package. The 1st code on Line 3 of the mark is the product revision code, as shown in ***Figure 1-1. Device revision code of GD32H77x_78x***.

Figure 1-1. Device revision code of GD32H77x_78x



1.2. Summary of device limitations

The device limitations of GD32H77x_78x are shown in ***Table 1-2. Device limitations***, please refer to Section 2 for more details.

Table 1-2. Device limitations

Module	Limitations	Workaround
		Rev. Code B
NVMC	***When performing an ECNVM/CNVM address read access, at least***	N

Module	Limitations	Workaround
		Rev. Code B
	256 bits of data are read at a time	
	Perform hardware blank check on the target area before ECNVM programming. If there is an ECC error in the target area, the ECC flag is set, but the ECC address is recorded incorrectly	Y
USART	*The high baud rate of USART will cause data loss when using hardware flow control mode*	Y
SPI	*CRC reception causes overflow when the receive FIFO is full*	Y
	The DMA request signal from the SPI transmitter may not be responded by the DMA	Y
	In master full-duplex mode, the data transmitted from TxFIFO and the corresponding data received by RxFIFO are in reverse byte order	Y
	In slave TI mode, SPI cannot operate correctly when a frame format error occurs	N
I2S	*When a transmit underrun occurs in the left channel of the first frame, failure to clear it in time may cause data swapping between the left and right channels*	Y
	When the data length is 16 bits and a receive overrun occurs, failure to clear it in time will result in the loss of 2 additional frames of data	N
OSPI	*OSPI cannot reach 200MHz when the CPU runs at its maximum frequency*	N
SDIO	*Synchronous interrupt latency triggered during read wait*	N
ESC	*When the SYNC0 signal is used as an IRQ signal, it may cause abnormal interrupt response*	N
USBHS	*USBHS Full-Speed PHY connected to a HUB, followed by a Low-Speed device, is likely to fail in enumeration or communication*	N

Note:

Y = Limitation present, workaround available

N = Limitation present, Not available.

'--' = Limitation fixed

2. Descriptions of device limitations

2.1. NVMC

2.1.1. When performing an ECNVM/CNVM address read access, at least 256 bits of data are read at a time

Description & impact

When performing an ECNVM/CNVM address read access, at least 256 bits of data are read at a time. For example, when the ECNVM buffer prefetch function is disabled, reading ECNVM address 0x08200000 will actually read 256 bits of data into the current buffer. If an ECC error occurs at address 0x08200010 during this time, the system will report an ECNVM ECC error. Similarly, if the ECNVM buffer prefetch is configured as prefetching 1 line or 3 lines, then a single read access will actually read 256*2 or 256*4 bits of data. This may impose certain limitations on application usage, such as ECNVM emulated EEPROM.

For example, when the CPU buffer/general buffer size is configured as 256 bits, reading CNVM address 0x08000000 will actually read 256 bits of data into the CPU/general buffer. If an ECC error occurs at address 0x08000010 during this time, the system will report a CNVM ECC error.

Note: Only the GD32H77xxW/GD32H78xxW architecture supports the ECNVM ECC feature.

Workarounds

Not available.

2.1.2. Perform hardware blank check on the target area before ECNVM programming. If there is an ECC error in the target area, the ECC flag is set, but the ECC address is recorded incorrectly

Description & impact

Before ECNVM programming, perform a hardware blank check on the target area (PGCHEN=1). If there is an ECC error in the target area, the ECC flag is set, but the ECC address is recorded incorrectly.

Note: Only the GD32H77xxW/GD32H78xxW architecture supports the ECNVM ECC feature.

Workarounds

When the above issue occurs, first clear the ECC flag. Then, the software performs a 32-bit

address-aligned read operation on the starting address of the programming area. If the ECC flag is set (ECCDET=1), the ECC error address at this time is the ECC error address when the above issue occurred.

2.2. USART

2.2.1. The high baud rate of USART will cause data loss when using hardware flow control mode

Description & impact

When using hardware flow control, during high baud rate communication of the USART, data loss may occur due to CTS not being pulled low in time (flow control delay).

Workarounds

Avoid using high baud rates, or use 2 stop bits at high baud rates. In flow control mode with 1 stop bit, limit the baud rate to below 4.4 MHz (APB2 = 300MHz) and 2.2 MHz (APB1 = 150MHz).

2.3. SPI

2.3.1. CRC reception causes overflow when the receive FIFO is full

Description & impact

When CRC is enabled, receiving CRC while the RXFIFO is full will set the receiver overrun error flag (RXORERR).

Workarounds

When CRC is enabled, the software should promptly read the received data to keep the RXFIFO in a non-full state.

2.3.2. The DMA request signal from the SPI transmitter may not be responded by the DMA

Description & impact

If the SPI DMA enable bit is cleared during an SPI transmission gap, SPI may already have generated a request signal that was not serviced by DMA. As a result, subsequent new DMA requests issued by SPI may no longer be responded to by DMA.

Workarounds

After disabling SPI DMA function, software should proactively write one dummy value to the TxFIFO, for example, 0xFF.

2.3.3. In master full-duplex mode, the data transmitted from TxFIFO and the corresponding data received by RxFIFO are in reverse byte order

Description & impact

In master full-duplex mode, the data transmitted from TxFIFO and the corresponding data received by RxFIFO are in reverse byte order.

Workarounds

Perform byte-order reversal on the data before transmission, or perform byte-order reversal on the received data after reception.

2.3.4. In slave TI mode, SPI cannot operate correctly when a frame format error occurs

Description & impact

In slave TI mode, SPI cannot operate correctly when a frame format error occurs.

Workarounds

Not available. Do not use slave TI mode.

2.4. I2S

2.4.1. When a transmit underrun occurs in the left channel of the first frame, failure to clear it in time may cause data swapping between the left and right channels

Description & impact

When I2S operates as a slave transmitter, if a transmit underflow occurs in the left channel of the first frame and the transmit underflow flag (TXURERR) is not cleared in time, it may result in data swapping between the left and right channels.

Note: The above issue only occurs when a transmit underrun happens in the left channel of the first frame. Transmit underruns during data transmission do not cause this issue.

Workarounds

Write data to the TXFIFO in advance to ensure no transmit underrun occurs in the first frame.

2.4.2. When the data length is 16 bits and a receive overrun occurs, failure to clear it in time will result in the loss of 2 additional frames of data

Description & impact

When the data length is 16 bits and a receive overrun occurs, if the receive overrun flag (RXORERR) is not cleared in time, it will result in the loss of 2 additional frames of data.

Workarounds

Not available. Evaluate based on the application scenario. For example, when I2S is used for audio data communication, the above issue has minimal impact on the application.

2.5. OSPI

2.5.1. OSPI cannot reach 200MHz when the CPU runs at its maximum frequency

Description & impact

The OSPI clock is sourced from either CK_AHB or CK_PLL0Q. In DTR mode, the OSPI clock prescaler (OSPI_DCFG1.PSC) must be configured to use an even division factor. Therefore, when the CPU and AHB run at their respective maximum frequencies, the maximum OSPI clock frequency is limited as follows, regardless of the selected clock source:

Device and operating mode	CPU frequency	AHB frequency	Maximum OSPI frequency
GD32H77x	600MHz	300MHz	150MHz
GD32H78x general mode	700MHz	350MHz	175MHz
GD32H78x high-performance mode	750MHz	375MHz	187.5MHz

Workarounds

Not available. To achieve an OSPI clock frequency of 200MHz, select CK_PLL0Q as the OSPI clock source, set CK_PLL0Q to 400MHz, and configure OSPI_DCFG1.PSC for division by 2. In this configuration, the system clock must also be set to 400MHz

2.6. SDIO

2.6.1. Synchronous interrupt latency triggered during read wait

Description & impact

The read wait function is configured to clock stop mode (RWTYPE=1). If an interrupt event occurs on the D1 line during the block gap while the read wait function is active, the interrupt flag (SDIOINT) will be set after the read wait stops, specifically after the clock resumes.

Workarounds

Not available.

2.7. ESC

2.7.1. When the SYNC0 signal is used as an IRQ signal, it may cause abnormal interrupt response

Description & impact

When the SYNC0 signal is used as an IRQ signal, since the IRQ duration can be configured via software, a short IRQ duration may cause the CPU to miss the interrupt, while a long IRQ duration may cause the CPU to re-enter the interrupt after exiting.

Workarounds

Not available.

2.8. USBHS

2.8.1. USBHS Full-Speed PHY connected to a HUB, followed by a Low-Speed device, is likely to fail in enumeration or communication

Description & impact

USBHS Full-Speed PHY connected to a Low-Speed device through a HUB may lead to a high probability of enumeration or communication failure for the Low-Speed device.

Workarounds

Not available. It is recommended not to connect Low-Speed devices to the USBHS Full-Speed PHY through a HUB.

2.9. Core

About Cortex-M7(r1p2) limitations, please refer to "Cortex-M7 (AT610) and Cortex-M7 with FPU (AT611) Software Developer Errata Notice". This document can be downloaded on **ARM official website**.

3. Revision history

Table 3-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Nov.9, 2026

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