GigaDevice Semiconductor Inc.

GD32G553xx Series
Software Development Guide

Application Notes
AN204

Version 1.0

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1. Overview

This application note is specifically provided for the GD32G553xx series of MCUs, introducing how to build a project based on the GD32G553xx MCU and how to debug it, as well as how to use various modules. The purpose of this application note is to provide exemplary functional introductions to the peripheral resources on the GD32G553xx series of MCUs, enabling users to understand how to use the GD32G553xx series of chips for rapid software development.

Table 1-1. Applicable products

Type	Model
MCU	GD32G553xx Series

2. Development of software functions

2.1. Boot mode selection and configuration

2.1.1. DBS function

When the DBS bit in the FMC_OBCTL register is configured to 0, there is one bank of flash memory. When the DBS bit is set to 1, there are two banks of flash memory. The total capacities of flash memory in various models are 128KB, 256KB, and 512KB. When there are two banks of flash memory, the starting address of bank0 is 0x08000000, and the starting addresses of bank1 are 0x08010000, 0x08020000, and 0x08040000, respectively. If there is application data in the flash memory, and you switch from dual-bank to single-bank, or from single-bank to dual-bank, and the data in the flash memory is significantly different from the previous data, preventing normal execution, it is recommended to perform an erase operation on the flash memory.

When the DBS bit in the FMC_OBCTL register is set to 0, the flash memory has one bank. When the DBS bit is set to 1, the flash memory has two banks. The total capacities of flash memory in various models are 128KB, 256KB, and 512KB. When there are two banks of flash memory, the starting address of bank0 is always 0x08000000, and the starting addresses of bank1 are 0x08010000, 0x08020000, and 0x08040000, respectively. If there is application data in the flash memory, switching from dual-bank to single-bank or from single-bank to dual-bank results in significant differences in the data within the flash memory, preventing normal execution. It is recommended to perform an erase operation on the flash memory.

2.1.2. BB function

If users need to configure bank switching functionality, they must set both the DBS bit and the BB bit to 1 in the FMC_OBCTL register. Code should be downloaded at the starting address of bank0 or bank1. The application code downloaded in bank1 is compiled with a starting address of 0x08000000. If the MCU is set to boot from system memory, upon entering the bootloader, if there is application code in bank1, the data contents of bank1 and bank0 will be swapped, and its code will be executed. If bank1 does not have code but bank0 does, the code saved in bank0 will be executed. If neither bank has code, the bootloader will continue to run.

After the aforementioned code switching in bank0 or bank1 is completed, if it is still necessary to execute the bootloader functions, the application code must include operations related to clearing the BB bit. Otherwise, whether starting from flash or system memory, only the code in the flash can be executed. Even if briefly entering the bootloader and executing some judgment logic code, it will jump back to the flash to continue executing the application code, rather than executing the subsequent functional code of the bootloader.

2.2. Option byte modification

During the modification of the option byte, it is essential to ensure a stable working environment; otherwise, a reset or power loss during the modification process will cause the chip to report an OBERR and enter a strong protection state.

2.3. Use of CMP

For details, please refer to *《AN198 GD32G5x3 Comparator User Guide》*.

2.4. Precautions for using SPI

The GD32G5x3 series includes 3 SPI modules, and each SPI has FIFO. It includes separate 32-bit receive buffers (RXFIFO) and transmit buffers (TXFIFO) for different directions of SPI data transmission, enabling continuous operation of the SPI.

When configuring the SPI, after setting the relevant parameters of the SPI, it is necessary to configure the SPI's FIFO, and whichever SPI is used requires the configuration of the corresponding FIFO. For specific details, refer to *Figure 2-1. SPI configuration*.

Figure 2-1. SPI configuration

```
void spi_config(void)
{
    spi_parameter_struct spi_init_struct;

    /* deinitilize SPI and the parameters */
    spi_deinit(SPI0);
    spi_deinit(SPI1);
    spi_struct_para_init(&spi_init_struct);

    /* SPI0 parameter configuration */
    spi_init_struct.trans_mode           = SPI_TRANSMODE_FULLDUPLEX;
    spi_init_struct.device_mode          = SPI_MASTER;
    spi_init_struct.frame_size           = SPI_FRAMESIZE_8BIT;
    spi_init_struct.clock_polarity_phase = SPI_CK_PL_HIGH_PH_2EDGE;
    spi_init_struct.nss                  = SPI_NSS_SOFT;
    spi_init_struct.prescale             = SPI_PSC_32;
    spi_init_struct.endian               = SPI_ENDIAN_MSB;
    spi_init(SPI0, &spi_init_struct);

    /* SPI1 parameter configuration */
    spi_init_struct.trans_mode           = SPI_TRANSMODE_FULLDUPLEX;
    spi_init_struct.device_mode          = SPI_SLAVE;
    spi_init(SPI1, &spi_init_struct);

    /* configure SPI byte access to FIFO */
    spi_fifo_access_size_config(SPI0, SPI_BYTE_ACCESS);
    spi_fifo_access_size_config(SPI1, SPI_BYTE_ACCESS);
```

The function spi_fifo_access_size_config() configures the SPI FIFO access, including byte mode 8-bit and half-word mode 16-bit.

Note:

The GD32G5x3 series does not have I2S module. It does not support communication with external devices using the I2S audio protocol.

2.5. Use of HRTIMER

For details, please refer to ***《AN203 GD32G5x3 High-Resolution Timer User Guide》***.

2.6. Use of TMU

For details, please refer to ***《AN207 GD32G5x3 Trigonometric Math Unit User Guide》***.

2.7. Use of FIR_IIR filter

For details, please refer to***《AN208 GD32G5x3 Proper of FIR_IIR》***.

3. Revision history

Table 3-1. Revision history

Revision No.	Description	Date
1.0	Initial release	Dec.05, 2025

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