GigaDevice Semiconductor Inc.

GD32F505xx
Arm® Cortex®-M33 32-bit MCU

Datasheet

Revision 1.0

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1. General description

The GD32F505xx device belongs to the high-performance line of GD32 MCU family. It is a new 32-bit general-purpose microcontroller based on the Arm® Cortex®-M33 core. The Cortex®-M33 processor is a 32-bit processor that possesses low interrupt latency and low-cost debug. The characteristics of integrated and advanced make the Cortex®-M33 processor suitable for market products that require microcontrollers with high performance and low power consumption. The Cortex®-M33 processor is based on the Armv8 architecture and supports a powerful and scalable instruction set including general data processing I/O control tasks, advanced data processing bit field manipulations and DSP.

The GD32F505xx device incorporates the Arm® Cortex®-M33 32-bit processor core operating at 280 MHz frequency with Flash security protection to prevent illegal code/data access. It provides up to 1024 KB main Flash memory, 192KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer three 12-bit ADCs, one 12-bit DAC, five general 16-bit timers, two 16-bit PWM advanced timers, one 32-bit general timer, and two 16-bit basic timers, as well as standard and advanced communication interfaces: up to three SPIs, two I2Ss, two I2Cs, three USARTs and two UARTs, two CANs and a USBFS. Additional peripherals as an EXMC interface, one comparator (CMP), a cryptographic acceleration unit (CAU), Hash Acceleration Unit (HAU), CRC calculation unit (CRC), true random number generator (TRNG) and a trigger selection controller (TRIGSEL) are included.

The device operates from a 2.6V to 3.6V power supply and available in –40 to +105 °C temperature range. Three power saving modes provide the flexibility for maximum optimization of power consumption, an especially important consideration in low power applications.

The above features make GD32F505xx devices suitable for a wide range of interconnection and advanced applications, especially in areas such as industrial control, consumer and handheld equipment, embedded modules, human machine interface, security and alarm systems, graphic display, audio player, automotive navigation, drone, IoT and so on.



2. Device overview

2.1. Device information

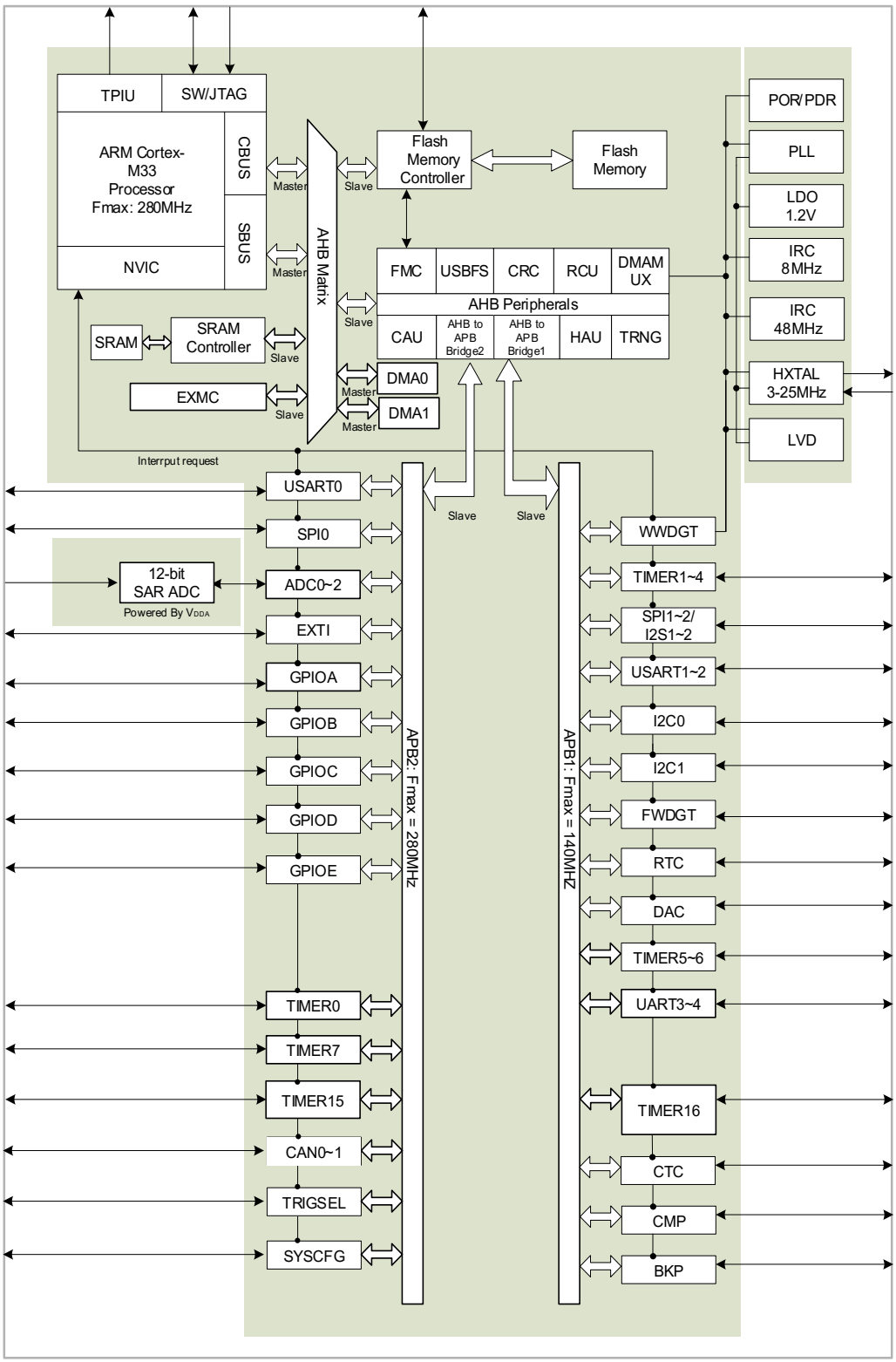
Table 2-1. GD32F505xx devices features and peripheral list (Industrial -40 °C to +105 °C)

Part Number			GD32F505								
			CGO7	CET7	CGT7	RGO7	RET7	RGT7	RGL7	VET7	VGT7
FLASH (KB)	BANK0	Code area	128	192	128	128	192	128	128	192	128
	BANK0	Data area	384	320	384	384	320	384	384	320	384
	BANK1	Data area	512	0	512	512	0	512	512	0	512
	Total		1024	512	1024	1024	512	1024	1024	512	1024
SRAM (KB)			192	128	192	192	128	192	192	128	192
Timers	General timer (16-bit)		5 (2-4,15-16)	5 (2-4,15-16)	5 (2-4,15-16)	5 (2-4,15-16)	5 (2-4,15-16)	5 (2-4,15-16)	5 (2-4,15-16)	5 (2-4,15-16)	5 (2-4,15-16)
	General timer (32-bit)		1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)	1 (1)
	Advanced timer(16-bit)		2 (0,7)	2 (0,7)	2 (0,7)	2 (0,7)	2 (0,7)	2 (0,7)	2 (0,7)	2 (0,7)	2 (0,7)
	Basic timer (16-bit)		2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)
	SysTick		1	1	1	1	1	1	1	1	1
	Watchdog		2	2	2	2	2	2	2	2	2
	RTC		1	1	1	1	1	1	1	1	1
Connectivity	USART		3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)	3 (0-2)
	UART		0	0	0	2	2	2	2	2	2

Part Number		GD32F505								
		CGO7	CET7	CGT7	RGO7	RET7	RGT7	RGL7	VET7	VGT7
					(3,4)	(3,4)	(3,4)	(3,4)	(3,4)	(3,4)
	I2C	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)
	SPI/I2S	3/2 (0-2)/(1-2)	3/2 (0-2)/(1-2)	3/2 (0-2)/(1-2)	3/2 (0-2)/(1-2)	3/2 (0-2)/(1-2)	3/2 (0-2)/(1-2)	3/2 (0-2)/(1-2)	3/2 (0-2)/(1-2)	3/2 (0-2)/(1-2)
	CAN	2xFD	2xFD	2xFD	2xFD	2xFD	2xFD	2xFD	2xFD	2xFD
	USBFS	1	1	1	1	1	1	1	1	1
GPIO		41	37	37	56	51	51	51	80	80
5VT GPIO		24	21	21	34	29	29	29	60	60
EXMC		0	0	0	1	1	1	1	1	1
CAU		1	1	1	1	1	1	1	1	1
HAU		1	1	1	1	1	1	1	1	1
TRIGSEL		1	1	1	1	1	1	1	1	1
CRC		1	1	1	1	1	1	1	1	1
TRNG		1	1	1	1	1	1	1	1	1
12bit ADC	Units	3	3	3	3	3	3	3	3	3
	Channels	14	12	12	19	18	18	18	25	25
DAC	Units	1	1	1	1	1	1	1	1	1
	Channels	1	1	1	1	1	1	1	1	1
CMP		1	1	1	1	1	1	1	1	1
Package		QFN48	LQFP48		QFN64	LQFP64		BGA64	LQFP100	

2.2. Block diagram

Figure 2-1. GD32F505xx block diagram



2.3. Pinouts and pin assignment

Figure 2-2. GD32F505Vx LQFP100 pinouts

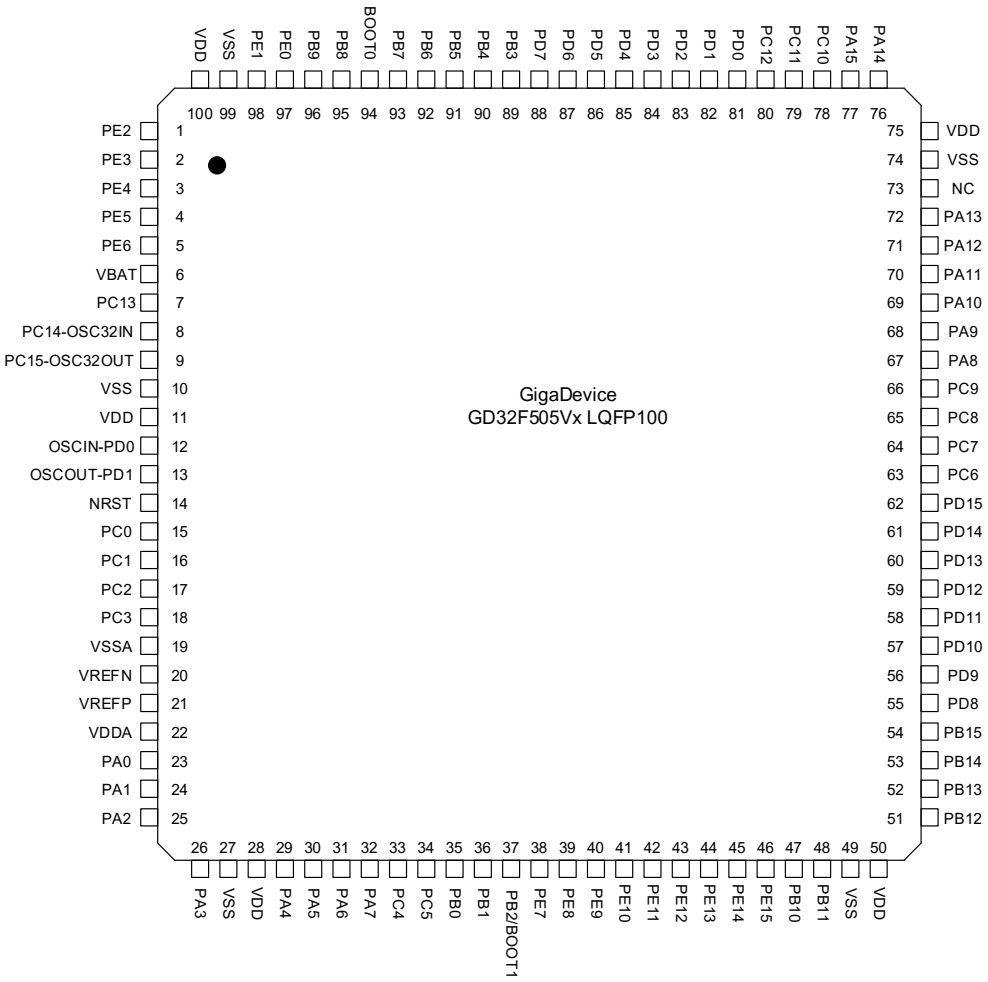


Figure 2-3. GD32F505Rx LQFP64 pinouts

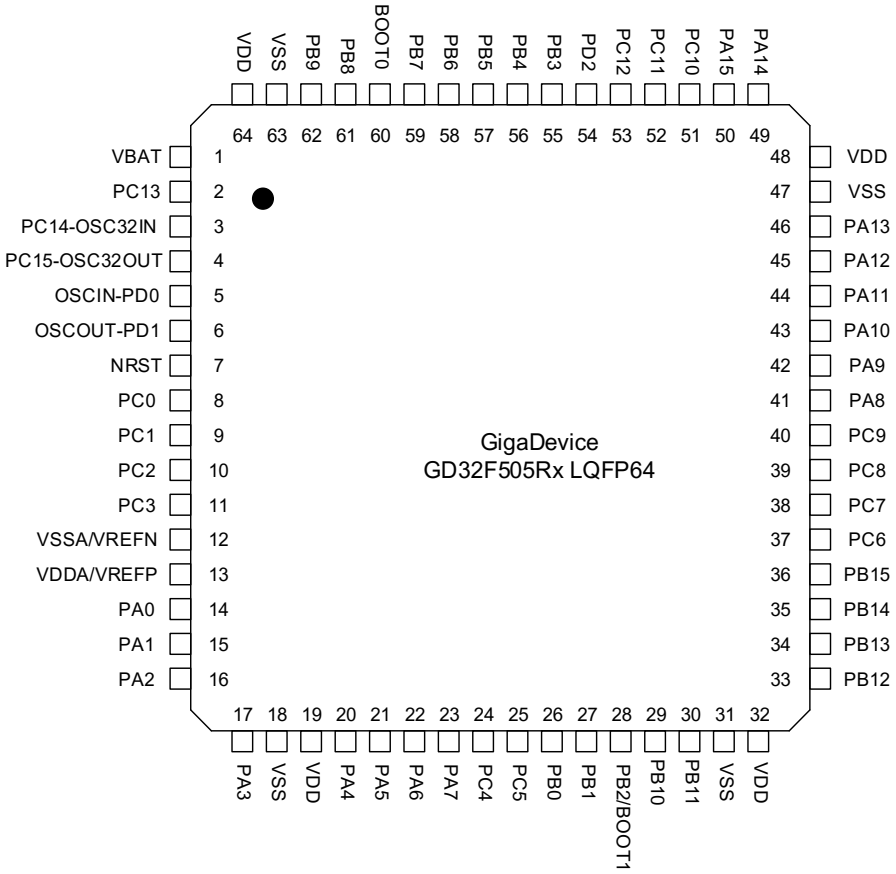


Figure 2-4. GD32F505Rx QFN64 pinouts

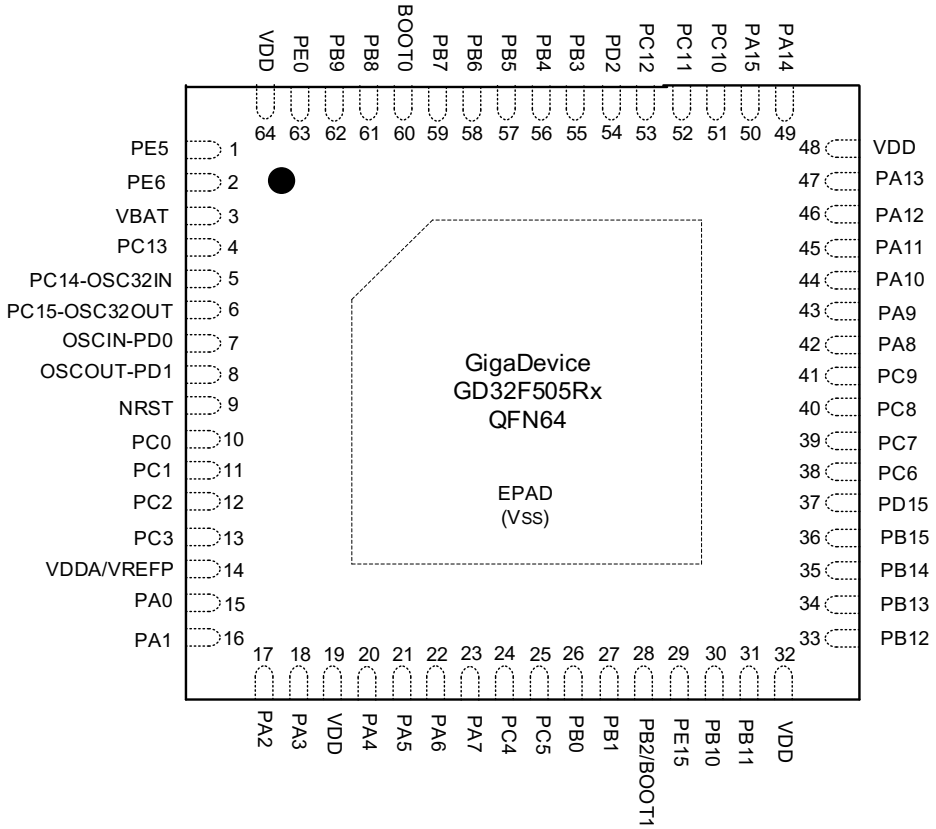


Figure 2-5. GD32F505Rx BGA64 pinouts

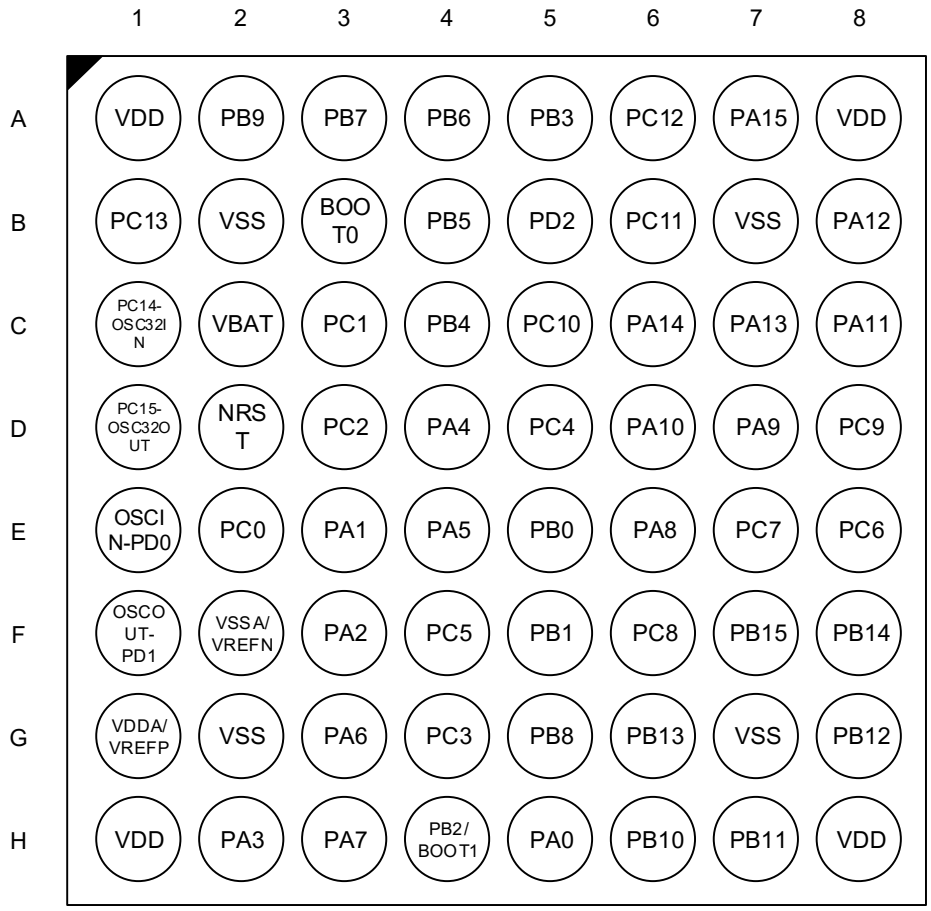


Figure 2-6. GD32F505Cx LQFP48 pinouts

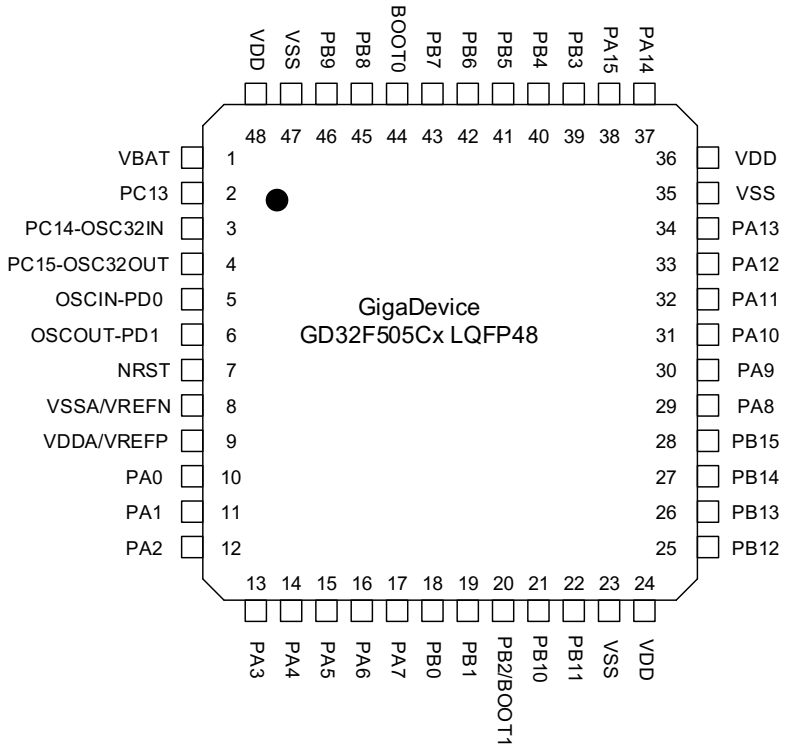
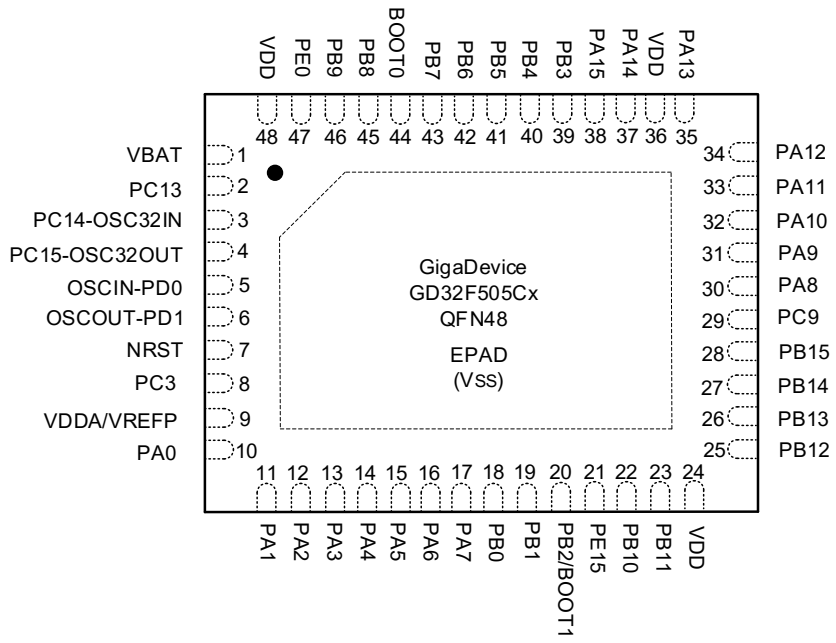


Figure 2-7. GD32F505Cx QFN48 pinouts



2.4. Memory map

Table 2-2. GD32F505xx memory map

Pre-defined Regions	Bus	Address	Peripherals
External device	AHB3	0xA000 0000 - 0xA000 0FFF	EXMC - SWREG
External RAM		0x9000 0000 - 0x9FFF FFFF	Reserved
		0x7000 0000 - 0x8FFF FFFF	EXMC - NAND
		0x6000 0000 - 0x6FFF FFFF	EXMC - NOR/PSRAM
Peripheral	AHB1	0x5000 0000 - 0x5003 FFFF	USBFS
		0x4008 0000 - 0x4FFF FFFF	Reserved
		0x4004 0000 - 0x4007 FFFF	Reserved
		0x4002 BC00 - 0x4003 FFFF	Reserved
		0x4002 B000 - 0x4002 BBFF	Reserved
		0x4002 A000 - 0x4002 AFFF	Reserved
		0x4002 8000 - 0x4002 9FFF	Reserved
		0x4002 6800 - 0x4002 7FFF	Reserved
		0x4002 6400 - 0x4002 67FF	Reserved
		0x4002 6000 - 0x4002 63FF	Reserved
		0x4002 5000 - 0x4002 5FFF	Reserved
		0x4002 4000 - 0x4002 4FFF	Reserved
		0x4002 3C00 - 0x4002 3FFF	TRNG
		0x4002 3800 - 0x4002 3BFF	HAU
		0x4002 3400 - 0x4002 37FF	CAU
		0x4002 3000 - 0x4002 33FF	CRC
		0x4002 2C00 - 0x4002 2FFF	Reserved
		0x4002 2800 - 0x4002 2BFF	Reserved
		0x4002 2400 - 0x4002 27FF	Reserved
		0x4002 2000 - 0x4002 23FF	FMC
		0x4002 1C00 - 0x4002 1FFF	Reserved
		0x4002 1800 - 0x4002 1BFF	Reserved
		0x4002 1400 - 0x4002 17FF	Reserved
		0x4002 1000 - 0x4002 13FF	RCU
		0x4002 0C00 - 0x4002 0FFF	Reserved
		0x4002 0800 - 0x4002 0BFF	DMAMUX
		0x4002 0400 - 0x4002 07FF	DMA1
		0x4002 0000 - 0x4002 03FF	DMA0
		0x4001 8400 - 0x4001 FFFF	Reserved
		0x4001 8000 - 0x4001 83FF	Reserved
	APB2	0x4001 7C00 - 0x4001 7FFF	Reserved

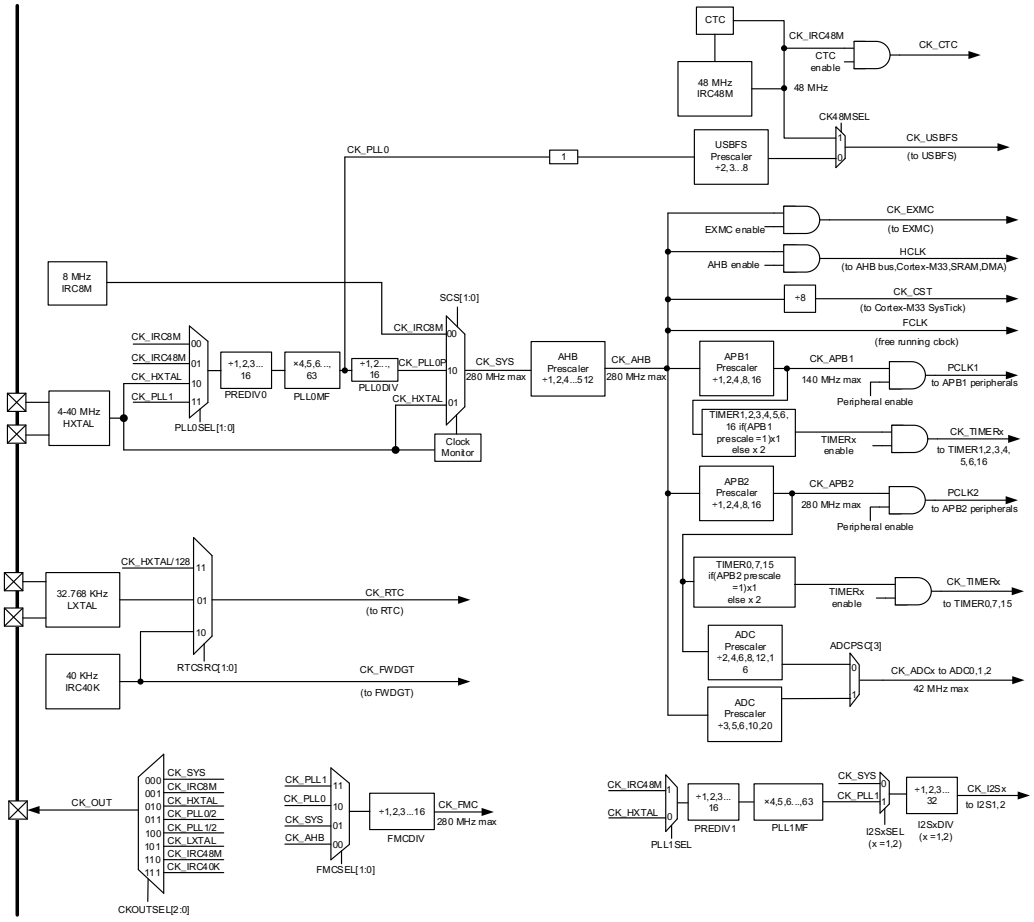
Pre-defined Regions	Bus	Address	Peripherals
		0x4001 7800 - 0x4001 7BFF	Reserved
		0x4001 7400 - 0x4001 77FF	Reserved
		0x4001 7000 - 0x4001 73FF	Reserved
		0x4001 6C00 - 0x4001 6FFF	Reserved
		0x4001 6800 - 0x4001 6BFF	Reserved
		0x4001 6500 - 0x4001 67FF	Reserved
		0x4001 6400 - 0x4001 64FF	Shared CAN/APB SRAM1
		0x4001 6000 - 0x4001 63FF	Shared CAN/APB SRAM0
		0x4001 5C00 - 0x4001 5FFF	CAN1
		0x4001 5800 - 0x4001 5BFF	CAN0
		0x4001 5400 - 0x4001 57FF	Reserved
		0x4001 5000 - 0x4001 53FF	TIMER15
		0x4001 4C00 - 0x4001 4FFF	Reserved
		0x4001 4800 - 0x4001 4BFF	Reserved
		0x4001 4400 - 0x4001 47FF	TRIGSEL
		0x4001 4000 - 0x4001 43FF	SYSCFG
		0x4001 3C00 - 0x4001 3FFF	ADC2
		0x4001 3800 - 0x4001 3BFF	USART0
		0x4001 3400 - 0x4001 37FF	TIMER7
		0x4001 3000 - 0x4001 33FF	SPI0
		0x4001 2C00 - 0x4001 2FFF	TIMER0
		0x4001 2800 - 0x4001 2BFF	ADC1
		0x4001 2400 - 0x4001 27FF	ADC0
		0x4001 2000 - 0x4001 23FF	Reserved
		0x4001 1C00 - 0x4001 1FFF	Reserved
		0x4001 1800 - 0x4001 1BFF	GPIOE
		0x4001 1400 - 0x4001 17FF	GPIOD
		0x4001 1000 - 0x4001 13FF	GPIOC
		0x4001 0C00 - 0x4001 0FFF	GPIOB
		0x4001 0800 - 0x4001 0BFF	GPIOA
		0x4001 0400 - 0x4001 07FF	EXTI
		0x4001 0000 - 0x4001 03FF	AFIO
	APB1	0x4000 CC00 - 0x4000 FFFF	Reserved
		0x4000 C800 - 0x4000 CBFF	CTC
		0x4000 C400 - 0x4000 C7FF	Reserved
		0x4000 C000 - 0x4000 C3FF	Reserved
		0x4000 8000 - 0x4000 BFFF	Reserved
		0x4000 7C00 - 0x4000 7FFF	Reserved
		0x4000 7800 - 0x4000 7BFF	CMP

Pre-defined Regions	Bus	Address	Peripherals
		0x4000 7400 - 0x4000 77FF	DAC
		0x4000 7000 - 0x4000 73FF	PMU
		0x4000 6C00 - 0x4000 6FFF	BKP
		0x4000 6800 - 0x4000 6BFF	Reserved
		0x4000 6400 - 0x4000 67FF	Reserved
		0x4000 6000 - 0x4000 63FF	Reserved
		0x4000 5C00 - 0x4000 5FFF	Reserved
		0x4000 5800 - 0x4000 5BFF	I2C1
		0x4000 5400 - 0x4000 57FF	I2C0
		0x4000 5000 - 0x4000 53FF	UART4
		0x4000 4C00 - 0x4000 4FFF	UART3
		0x4000 4800 - 0x4000 4BFF	USART2
		0x4000 4400 - 0x4000 47FF	USART1
		0x4000 4000 - 0x4000 43FF	Reserved
		0x4000 3C00 - 0x4000 3FFF	SPI2/I2S2
		0x4000 3800 - 0x4000 3BFF	SPI1/I2S1
		0x4000 3400 - 0x4000 37FF	Reserved
		0x4000 3000 - 0x4000 33FF	FWDGT
		0x4000 2C00 - 0x4000 2FFF	WWDGT
		0x4000 2800 - 0x4000 2BFF	RTC
		0x4000 2400 - 0x4000 27FF	Reserved
		0x4000 2000 - 0x4000 23FF	Reserved
		0x4000 1C00 - 0x4000 1FFF	Reserved
		0x4000 1800 - 0x4000 1BFF	TIMER16
		0x4000 1400 - 0x4000 17FF	TIMER6
		0x4000 1000 - 0x4000 13FF	TIMER5
		0x4000 0C00 - 0x4000 0FFF	TIMER4
		0x4000 0800 - 0x4000 0BFF	TIMER3
		0x4000 0400 - 0x4000 07FF	TIMER2
		0x4000 0000 - 0x4000 03FF	TIMER1
SRAM	AHB	0x2007 0000 - 0x3FFF FFFF	Reserved
		0x2006 0000 - 0x2006 FFFF	Reserved
		0x2003 0000 - 0x2005 FFFF	Reserved
		0x2000 0000 - 0x2002 FFFF	SRAM
Code	AHB	0x1FFF F810 - 0x1FFF FFFF	Reserved
		0x1FFF F800 - 0x1FFF F80F	Option Bytes
		0x1FFF B000 - 0x1FFF F7FF	Boot loader
		0x1FFF 7A10 - 0x1FFF AFFF	Reserved

Pre-defined Regions	Bus	Address	Peripherals
		0x1FFF 7940 - 0x1FFF 7A0F	Reserved
		0x1FFF 7930 - 0x1FFF 793F	OTP3(lock area)
		0x1FFF 7900 - 0x1FFF 792F	OTP3(data area)
		0x1FFF 7880 - 0x1FFF 788F	Reserved
		0x1FFF 7840 - 0x1FFF 787F	OTP0(lock area)
		0x1FFF 7800 - 0x1FFF 783F	OTP0(data area)
		0x1FFF 0000 - 0x1FFF 77FF	Reserved
		0x1FFE C010 - 0x1FFE FFFF	Reserved
		0x1FFE C000 - 0x1FFE C00F	Reserved
		0x1FF2 0190 - 0x1FFE BFFF	Reserved
		0x1FF2 0110 - 0x1FF2 018F	OTP2 (lock area)
		0x1FF2 0100 - 0x1FF2 010F	OTP1 (lock area)
		0x1FF2 0000 - 0x1FF2 00FF	OTP2 (data area)
		0x1FF0 0000 - 0x1FF1 FFFF	OTP1 (data area)
		0x1001 0000 - 0x1FEF FFFF	Reserved
		0x1000 0000 - 0x1000 FFFF	Reserved
		0x083C 0000 - 0x0FFF FFFF	Reserved
		0x0830 0000 - 0x083B FFFF	Reserved
		0x0810 0000 - 0x082F FFFF	Reserved
		0x0800 0000 - 0x080F FFFF	Main Flash
		0x0030 0000 - 0x07FF FFFF	Reserved
		0x0010 0000 - 0x002F FFFF	Aliased to Main Flash or Boot loader
		0x0002 0000 - 0x000F FFFF	
		0x0000 0000 - 0x0001 FFFF	

2.5. Clock tree

Figure 2-8. GD32F505xx clock tree



Legend:

HXTAL: High speed crystal oscillator

LXTAL: Low speed crystal oscillator

IRC8M: Internal 8M RC oscillators

IRC40K: Internal 40K RC oscillator

IRC48M: Internal 48M RC oscillators

2.6. Pin definitions

2.6.1. GD32F505Vx LQFP100 pin definitions

Table 2-3. GD32F505Vx LQFP100 pin definitions

GD32F505Vx LQFP100				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PE2	1	I/O	5VT	Default: PE2 Alternate: EXMC_A23, EVENTOUT
PE3	2	I/O	5VT	Default: PE3 Alternate: EXMC_A19, TIMER15_BRKIN, EVENTOUT
PE4	3	I/O	5VT	Default: PE4 Alternate: EXMC_A20, TIMER15_MCH0, EVENTOUT
PE5	4	I/O	5VT	Default: PE5 Alternate: EXMC_A21, TIMER15_CH0, EVENTOUT
PE6	5	I/O	5VT	Default: PE6 Alternate: EXMC_A22, TIMER15_CH1, EVENTOUT
VBAT	6	P	-	Default: VBAT
PC13	7	I/O	-	Default: PC13 Alternate: EVENTOUT Additional: TAMPER-RTC
PC14-OSC32IN	8	I/O	-	Default: PC14, OSC32IN Alternate: EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	9	I/O	-	Default: PC15, OSC32OUT Alternate: EVENTOUT Additional: OSC32OUT
VSS	10	P	-	Default: VSS
VDD	11	P	-	Default: VDD
OSCIN-PD0	12	I/O	-	Default: OSCIN, PD0 Alternate: EVENTOUT Additional: OSCIN
OSCOUT-PD1	13	I/O	-	Default: OSCOUT, PD1 Alternate: EVENTOUT Additional: OSCOUT
NRST	14	-	-	Default: NRST
PC0	15	I/O	-	Default: PC0 Alternate: TIMER7_CH0_ON, EXMC_NL, EXMC_NADV, EVENTOUT Additional: ADC012_IN10
PC1	16	I/O	-	Default: PC1 Alternate: TIMER7_CH1_ON, EVENTOUT Additional: ADC012_IN11
PC2	17	I/O	-	Default: PC2 Alternate: TIMER7_CH2_ON, EXMC_NWE,

GD32F505Vx LQFP100				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				EVENTOUT Additional: ADC012_IN12
PC3	18	I/O	-	Default: PC3 Alternate: TIMER7_CH3_ON, EVENTOUT Additional: ADC012_IN13
VSSA	19	P	-	Default: VSSA
VREFN	20	P	-	Default: VREFN
VREFP	21	P	-	Default: VREFP
VDDA	22	P	-	Default: VDDA
PA0	23	I/O	-	Default: PA0 Alternate: USART1_CTS, TIMER1_CH0, TIMER1_ETI, TIMER16_BRKIN, TIMER4_CH0, TIMER7_ETI, CMP0_OUT, TRGSEL_IN5, EVENTOUT Additional: ADC012_IN0, WKUP
PA1	24	I/O	-	Default: PA1 Alternate: USART1_RTS, TIMER1_CH1, TIMER16_MCH0, TIMER4_CH1, CMP0_OUT, TRGSEL_IN6, EVENTOUT Additional: ADC012_IN1
PA2	25	I/O	-	Default: PA2 Alternate: USART1_TX, TIMER1_CH2, TIMER16_CH0, TIMER4_CH2, SPI0_IO2, TRGSEL_OUT0, EXMC_D4, EVENTOUT Additional: ADC012_IN2, CMP0_IM2
PA3	26	I/O	-	Default: PA3 Alternate: USART1_RX, TIMER1_CH3, TIMER16_CH1, TIMER4_CH3, TIMER0_CH3_ON, SPI0_IO3, TRGSEL_OUT1, EXMC_D5, EVENTOUT Additional: ADC012_IN3
VSS	27	P	-	Default: VSS
VDD	28	P	-	Default: VDD
PA4	29	I/O	-	Default: PA4 Alternate: SPI0_NSS, USART1_CK, SPI2_NSS, I2S2_WS, TIMER15_BRKIN, TIMER7_CH1BRKIN, EXMC_D6, EVENTOUT Additional: ADC01_IN4, DAC0_OUT0, CMP0_IM0
PA5	30	I/O	-	Default: PA5 Alternate: SPI0_SCK, TIMER4_ETI, TIMER15_MCH0, TIMER7_CH0BRKIN, EXMC_D7, EVENTOUT Additional: ADC01_IN5, DAC0_OUT0, CMP0_IM1
PA6	31	I/O	-	Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, TIMER7_BRKIN, CMP0_OUT, TRGSEL_OUT2, EVENTOUT

GD32F505Vx LQFP100				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Additional: ADC01_IN6
PA7	32	I/O	-	Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, TIMER0_CH0_ON, TIMER15_CH1, TIMER7_CH0_ON, TRGSEL_OUT3, EVENTOUT Additional: ADC01_IN7, CMP0_IP
PC4	33	I/O	-	Default: PC4 Alternate: TIMER7_CH3, EXMC_NE0, EVENTOUT Additional: ADC01_IN14
PC5	34	I/O	-	Default: PC5 Alternate: EXMC_NOE, EVENTOUT Additional: ADC01_IN15
PB0	35	I/O	-	Default: PB0 Alternate: TIMER0_CH1_ON, TIMER2_CH2, TIMER7_CH1_ON, CMP0_OUT, EVENTOUT Additional: ADC01_IN8
PB1	36	I/O	-	Default: PB1 Alternate: TIMER0_CH2_ON, TIMER2_CH3, TIMER7_CH2_ON, CMP0_OUT, EVENTOUT Additional: ADC01_IN9
PB2/BOOT1	37	I/O	5VT	Default: PB2, BOOT1 Alternate: EVENTOUT
PE7	38	I/O	5VT	Default: PE7 Alternate: TIMER0_ETI, EXMC_D4, EVENTOUT Additional: ADC2_IN4
PE8	39	I/O	5VT	Default: PE8 Alternate: TIMER0_CH0_ON, EXMC_D5, EVENTOUT Additional: ADC2_IN5
PE9	40	I/O	5VT	Default: PE9 Alternate: TIMER0_CH0, EXMC_D6, EVENTOUT Additional: ADC2_IN6
PE10	41	I/O	5VT	Default: PE10 Alternate: TIMER0_CH1_ON, EXMC_D7, EVENTOUT Additional: ADC2_IN7
PE11	42	I/O	5VT	Default: PE11 Alternate: TIMER0_CH1, EXMC_D8, TRGSEL_IN4, EVENTOUT Additional: ADC2_IN8
PE12	43	I/O	5VT	Default: PE12 Alternate: TIMER0_CH2_ON, EXMC_D9, EVENTOUT Additional: ADC2_IN9
PE13	44	I/O	5VT	Default: PE13 Alternate: TIMER0_CH2, EXMC_D10, EVENTOUT
PE14	45	I/O	5VT	Default: PE14 Alternate: TIMER0_CH3, EXMC_D11,

GD32F505Vx LQFP100				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				TIMER0_CH2BRKIN, EVENTOUT
PE15	46	I/O	5VT	Default: PE15 Alternate: TIMER0_BRKIN, EXMC_D12, EVENTOUT Additional: ADC2_IN14
PB10	47	I/O	5VT	Default: PB10 Alternate: TIMER1_CH2, USART2_TX, I2C1_SCL, TIMER0_CH0BRKIN, EVENTOUT Additional: ADC2_IN15, ADC1_IN16
PB11	48	I/O	5VT	Default: PB11 Alternate: TIMER1_CH3, USART2_RX, I2C1_SDA, TIMER0_CH1BRKIN, TRGSEL_IN1, EVENTOUT Additional: ADC2_IN16, ADC1_IN17
VSS	49	P	-	Default: VSS
VDD	50	P	-	Default: VDD
PB12	51	I/O	5VT	Default: PB12 Alternate: USART2_CK, SPI1_NSS, I2S1_WS, I2C1_SMBA, CAN1_RX, TIMER0_BRKIN, TIMER16_CH0, EXMC_D13, EVENTOUT
PB13	52	I/O	5VT	Default: PB13 Alternate: USART2_CTS, SPI1_SCK, I2S1_CK, TIMER0_CH0_ON, CAN1_TX, TIMER16_CH1, EVENTOUT
PB14	53	I/O	5VT	Default: PB14 Alternate: USART2_RTS, SPI1_MISO, TIMER0_CH1_ON, TIMER15_CH0, EXMC_D0, EVENTOUT
PB15	54	I/O	5VT	Default: PB15 Alternate: SPI1_MOSI, I2S1_SD, TIMER0_CH2_ON, TIMER15_CH1, EVENTOUT
PD8	55	I/O	5VT	Default: PD8 Alternate: USART2_TX, EXMC_D13, TIMER0_CH0BRKIN, EVENTOUT
PD9	56	I/O	5VT	Default: PD9 Alternate: USART2_RX, EXMC_D14, TIMER0_CH1BRKIN, EVENTOUT
PD10	57	I/O	5VT	Default: PD10 Alternate: USART2_CK, EXMC_D15, TIMER0_CH2BRKIN, EVENTOUT
PD11	58	I/O	5VT	Default: PD11 Alternate: USART2_CTS, EXMC_A16, TRGSEL_IN3, EVENTOUT
PD12	59	I/O	5VT	Default: PD12 Alternate: USART2_RTS, TIMER3_CH0, EXMC_A17, EVENTOUT
PD13	60	I/O	5VT	Default: PD13

GD32F505Vx LQFP100				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: TIMER3_CH1, EXMC_A18, EVENTOUT
PD14	61	I/O	5VT	Default: PD14 Alternate: TIMER3_CH2, EXMC_D0, EVENTOUT
PD15	62	I/O	5VT	Default: PD15 Alternate: TIMER3_CH3, EXMC_D1, CTC_SYNC, EVENTOUT
PC6	63	I/O	5VT	Default: PC6 Alternate: TIMER2_CH0, I2S1_MCK, TIMER7_CH0, EXMC_D1, EVENTOUT
PC7	64	I/O	5VT	Default: PC7 Alternate: TIMER2_CH1, I2S2_MCK, TIMER7_CH3_ON, TIMER7_CH1, EVENTOUT
PC8	65	I/O	5VT	Default: PC8 Alternate: TIMER2_CH2, TIMER7_CH2, EVENTOUT
PC9	66	I/O	5VT	Default: PC9 Alternate: TIMER2_CH3, TIMER7_CH3, EXMC_NL, EXMC_NADV, EVENTOUT
PA8	67	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, USBFS_SOF, CK_OUT, TIMER7_CH0BRKIN, CTC_SYNC, TRGSEL_OUT4, EVENTOUT
PA9	68	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER7_CH1BRKIN, TRGSEL_OUT5, EVENTOUT
PA10	69	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER0_CH3_ON, TIMER15_BRKIN, TIMER15_CH1, TIMER7_CH2BRKIN, EVENTOUT
PA11	70	I/O	5VT	Default: PA11 Alternate: USART0_CTS, CAN0_RX, TIMER0_CH3, TIMER7_CH0, TIMER15_CH0, TRGSEL_IN0, EVENTOUT Additional: USBFS_DM
PA12	71	I/O	5VT	Default: PA12 Alternate: USART0_RTS, CAN0_TX, TIMER0_ETI, TIMER7_CH1, TIMER15_MCH0, EVENTOUT Additional: USBFS_DP
PA13	72	I/O	5VT	Default: JTMS, SWDIO, PA13 Alternate: EVENTOUT
NC	73	-	-	Default: NC
VSS	74	P	-	Default: VSS
VDD	75	P	-	Default: VDD
PA14	76	I/O	5VT	Default: JTCK, SWCLK, PA14 Alternate: EVENTOUT
PA15	77	I/O	5VT	Default: JTDI, PA15

GD32F505Vx LQFP100				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: TIMER1_CH0, TIMER1_ETI, SPI0_NSS, SPI2_NSS, I2S2_WS, TIMER15_BRKIN, TIMER16_BRKIN, EVENTOUT
PC10	78	I/O	5VT	Default: PC10 Alternate: USART2_TX, UART3_TX, SPI2_SCK, I2S2_CK, TIMER7_CH0BRKIN, TIMER0_CH0BRKIN, EVENTOUT
PC11	79	I/O	5VT	Default: PC11 Alternate: USART2_RX, UART3_RX, SPI2_MISO, TIMER7_CH2BRKIN, TIMER16_CH1, TRGSEL_IN2, EXMC_D2, EVENTOUT
PC12	80	I/O	5VT	Default: PC12 Alternate: USART2_CK, UART4_TX, SPI2_MOSI, I2S2_SD, TIMER16_CH0, EXMC_D3, EVENTOUT
PD0	81	I/O	5VT	Default: PD0 Alternate: CAN0_RX, EXMC_D2, EVENTOUT
PD1	82	I/O	5VT	Default: PD1 Alternate: CAN0_TX, EXMC_D3, EVENTOUT
PD2	83	I/O	5VT	Default: PD2 Alternate: TIMER2_ETI, UART4_RX, TIMER16_MCH0, EXMC_NWE, EVENTOUT
PD3	84	I/O	5VT	Default: PD3 Alternate: USART1_CTS, EXMC_CLK, EVENTOUT
PD4	85	I/O	5VT	Default: PD4 Alternate: USART1_RTS, EXMC_NOE, EVENTOUT
PD5	86	I/O	5VT	Default: PD5 Alternate: USART1_TX, EXMC_NWE, EVENTOUT
PD6	87	I/O	5VT	Default: PD6 Alternate: USART1_RX, EXMC_NWAIT, EVENTOUT
PD7	88	I/O	5VT	Default: PD7 Alternate: USART1_CK, EXMC_NE0, EXMC_NCE1, EVENTOUT
PB3	89	I/O	5VT	Default: JTDO, PB3 Alternate: TRACESWO, TIMER1_CH1, SPI0_SCK, SPI2_SCK, I2S2_CK, CK_OUT, EVENTOUT
PB4	90	I/O	5VT	Default: NJTRST, PB4 Alternate: TIMER2_CH0, SPI0_MISO, SPI2_MISO, TIMER7_CH2, TRGSEL_OUT6, EVENTOUT
PB5	91	I/O	-	Default: PB5 Alternate: TIMER2_CH1, SPI0_MOSI, I2C0_SMBA, CAN1_RX, TIMER7_CH0BRKIN, SPI2_MOSI, I2S2_SD, TIMER0_CH0BRKIN, EVENTOUT
PB6	92	I/O	5VT	Default: PB6 Alternate: USART0_TX, I2C0_SCL, TIMER3_CH0, CAN1_TX, TIMER7_CH1BRKIN, SPI0_IO2,

GD32F505Vx LQFP100				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				TIMER0_CH1BRKIN, EVENTOUT
PB7	93	I/O	5VT	Default: PB7 Alternate: USART0_RX, I2C0_SDA, TIMER3_CH1, EXMC_NL, EXMC_NADV, TIMER7_CH2BRKIN, SPI0_IO3, TRGSEL_OUT7, TIMER0_CH2BRKIN, EVENTOUT
BOOT0	94	I/O	-	Default: BOOT0
PB8	95	I/O	5VT	Default: PB8 Alternate: TIMER3_CH2, I2C0_SCL, CAN0_RX, TIMER15_CH0, EVENTOUT
PB9	96	I/O	5VT	Default: PB9 Alternate: I2C0_SDA, CAN0_TX, TIMER3_CH3, TIMER16_CH0, EVENTOUT
PE0	97	I/O	5VT	Default: PE0 Alternate: TIMER3_ETI, EXMC_NBL0, TRGSEL_IN7, EVENTOUT
PE1	98	I/O	5VT	Default: PE1 Alternate: EXMC_NBL1, EVENTOUT
VSS	99	P	-	Default: VSS
VDD	100	P	-	Default: VDD

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

2.6.2. GD32F505Rx LQFP64 pin definitions

Table 2-4. GD32F505Rx LQFP64 pin definitions

GD32F505Rx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
VBAT	1	P	-	Default: VBAT
PC13	2	I/O	-	Default: PC13 Alternate: EVENTOUT Additional: TAMPER-RTC
PC14-OSC32IN	3	I/O	-	Default: PC14, OSC32IN Alternate: EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	4	I/O	-	Default: PC15, OSC32OUT Alternate: EVENTOUT Additional: OSC32OUT
OSCIN-PD0	5	I/O	-	Default: OSCIN, PD0 Alternate: EVENTOUT Additional: OSCIN
OSCOUT-PD1	6	I/O	-	Default: OSCOUT, PD1 Alternate: EVENTOUT Additional: OSCOUT
NRST	7	-	-	Default: NRST
PC0	8	I/O	-	Default: PC0 Alternate: TIMER7_CH0_ON, EXMC_NL, EXMC_NADV, EVENTOUT Additional: ADC012_IN10
PC1	9	I/O	-	Default: PC1 Alternate: TIMER7_CH1_ON, EVENTOUT Additional: ADC012_IN11
PC2	10	I/O	-	Default: PC2 Alternate: TIMER7_CH2_ON, EXMC_NWE, EVENTOUT Additional: ADC012_IN12
PC3	11	I/O	-	Default: PC3 Alternate: TIMER7_CH3_ON, EVENTOUT Additional: ADC012_IN13
VSSA/VREFN	12	P	-	Default: VSSA
VDDA/VREFP	13	P	-	Default: VDDA
PA0	14	I/O	-	Default: PA0 Alternate: USART1_CTS, TIMER1_CH0, TIMER1_ETI, TIMER16_BRKIN, TIMER4_CH0, TIMER7_ETI, CMP0_OUT, TRGSEL_IN5, EVENTOUT Additional: ADC012_IN0, WKUP
PA1	15	I/O	-	Default: PA1

GD32F505Rx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: USART1_RTS, TIMER1_CH1, TIMER16_MCH0, TIMER4_CH1, CMP0_OUT, TRGSEL_IN6, EVENTOUT Additional: ADC012_IN1
PA2	16	I/O	-	Default: PA2 Alternate: USART1_TX, TIMER1_CH2, TIMER16_CH0, TIMER4_CH2, SPI0_IO2, TRGSEL_OUT0, EXMC_D4, EVENTOUT Additional: ADC012_IN2, CMP0_IM2
PA3	17	I/O	-	Default: PA3 Alternate: USART1_RX, TIMER1_CH3, TIMER16_CH1, TIMER4_CH3, TIMER0_CH3_ON, SPI0_IO3, TRGSEL_OUT1, EXMC_D5, EVENTOUT Additional: ADC012_IN3
VSS	18	P	-	Default: VSS
VDD	19	P	-	Default: VDD
PA4	20	I/O	-	Default: PA4 Alternate: SPI0_NSS, USART1_CK, SPI2_NSS, I2S2_WS, TIMER15_BRKIN, TIMER7_CH1BRKIN, EXMC_D6, EVENTOUT Additional: ADC01_IN4, DAC0_OUT0, CMP0_IM0
PA5	21	I/O	-	Default: PA5 Alternate: SPI0_SCK, TIMER4_ETI, TIMER15_MCH0, TIMER7_CH0BRKIN, EXMC_D7, EVENTOUT Additional: ADC01_IN5, DAC0_OUT0, CMP0_IM1
PA6	22	I/O	-	Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, TIMER7_BRKIN, CMP0_OUT, TRGSEL_OUT2, EVENTOUT Additional: ADC01_IN6
PA7	23	I/O	-	Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, TIMER0_CH0_ON, TIMER15_CH1, TIMER7_CH0_ON, TRGSEL_OUT3, EVENTOUT Additional: ADC01_IN7, CMP0_IP
PC4	24	I/O	-	Default: PC4 Alternate: TIMER7_CH3, EXMC_NE0, EVENTOUT Additional: ADC01_IN14
PC5	25	I/O	-	Default: PC5 Alternate: EXMC_NOE, EVENTOUT Additional: ADC01_IN15
PB0	26	I/O	-	Default: PB0 Alternate: TIMER0_CH1_ON, TIMER2_CH2, TIMER7_CH1_ON, CMP0_OUT, EVENTOUT Additional: ADC01_IN8

GD32F505Rx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PB1	27	I/O	-	Default: PB1 Alternate: TIMER0_CH2_ON, TIMER2_CH3, TIMER7_CH2_ON, CMP0_OUT, EVENTOUT Additional: ADC01_IN9
PB2/BOOT1	28	I/O	5VT	Default: PB2, BOOT1 Alternate: EVENTOUT
PB10	29	I/O	5VT	Default: PB10 Alternate: TIMER1_CH2, USART2_TX, I2C1_SCL, TIMER0_CH0BRKIN, EVENTOUT Additional: ADC2_IN15, ADC1_IN16
PB11	30	I/O	5VT	Default: PB11 Alternate: TIMER1_CH3, USART2_RX, I2C1_SDA, TIMER0_CH1BRKIN, TRGSEL_IN1, EVENTOUT Additional: ADC2_IN16, ADC1_IN17
VSS	31	P	-	Default: VSS
VDD	32	P	-	Default: VDD
PB12	33	I/O	5VT	Default: PB12 Alternate: USART2_CK, SPI1_NSS, I2S1_WS, I2C1_SMBA, CAN1_RX, TIMER0_BRKIN, TIMER16_CH0, EXMC_D13, EVENTOUT
PB13	34	I/O	5VT	Default: PB13 Alternate: USART2_CTS, SPI1_SCK, I2S1_CK, TIMER0_CH0_ON, CAN1_TX, TIMER16_CH1, EVENTOUT
PB14	35	I/O	5VT	Default: PB14 Alternate: USART2_RTS, SPI1_MISO, TIMER0_CH1_ON, TIMER15_CH0, EXMC_D0, EVENTOUT
PB15	36	I/O	5VT	Default: PB15 Alternate: SPI1_MOSI, I2S1_SD, TIMER0_CH2_ON, TIMER15_CH1, EVENTOUT
PC6	37	I/O	5VT	Default: PC6 Alternate: TIMER2_CH0, I2S1_MCK, TIMER7_CH0, EXMC_D1, EVENTOUT
PC7	38	I/O	5VT	Default: PC7 Alternate: TIMER2_CH1, I2S2_MCK, TIMER7_CH3_ON, TIMER7_CH1, EVENTOUT
PC8	39	I/O	5VT	Default: PC8 Alternate: TIMER2_CH2, TIMER7_CH2, EVENTOUT
PC9	40	I/O	5VT	Default: PC9 Alternate: TIMER2_CH3, TIMER7_CH3, EXMC_NL, EXMC_NADV, EVENTOUT
PA8	41	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, USBFS_SOF, CK_OUT, TIMER7_CH0BRKIN, CTC_SYNC,

GD32F505Rx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				TRGSEL_OUT4, EVENTOUT
PA9	42	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER7_CH1BRKIN, TRGSEL_OUT5, EVENTOUT
PA10	43	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER0_CH3_ON, TIMER15_BRKIN, TIMER15_CH1, TIMER7_CH2BRKIN, EVENTOUT
PA11	44	I/O	5VT	Default: PA11 Alternate: USART0_CTS, CAN0_RX, TIMER0_CH3, TIMER7_CH0, TIMER15_CH0, TRGSEL_IN0, EVENTOUT Additional: USBFS_DM
PA12	45	I/O	5VT	Default: PA12 Alternate: USART0_RTS, CAN0_TX, TIMER0_ETI, TIMER7_CH1, TIMER15_MCH0, EVENTOUT Additional: USBFS_DP
PA13	46	I/O	5VT	Default: JTMS, SWDIO, PA13 Alternate: EVENTOUT
VSS	47	P	-	Default: VSS
VDD	48	P	-	Default: VDD
PA14	49	I/O	5VT	Default: JTCK, SWCLK, PA14 Alternate: EVENTOUT
PA15	50	I/O	5VT	Default: JTDI, PA15 Alternate: TIMER1_CH0, TIMER1_ETI, SPI0_NSS, SPI2_NSS, I2S2_WS, TIMER15_BRKIN, TIMER16_BRKIN, EVENTOUT
PC10	51	I/O	5VT	Default: PC10 Alternate: USART2_TX, UART3_TX, SPI2_SCK, I2S2_CK, TIMER7_CH0BRKIN, TIMER0_CH0BRKIN, EVENTOUT
PC11	52	I/O	5VT	Default: PC11 Alternate: USART2_RX, UART3_RX, SPI2_MISO, TIMER7_CH2BRKIN, TIMER16_CH1, TRGSEL_IN2, EXMC_D2, EVENTOUT
PC12	53	I/O	5VT	Default: PC12 Alternate: USART2_CK, UART4_TX, SPI2_MOSI, I2S2_SD, TIMER16_CH0, EXMC_D3, EVENTOUT
PD2	54	I/O	5VT	Default: PD2 Alternate: TIMER2_ETI, UART4_RX, TIMER16_MCH0, EXMC_NWE, EVENTOUT
PB3	55	I/O	5VT	Default: JTDO, PB3 Alternate: TRACESWO, TIMER1_CH1, SPI0_SCK, SPI2_SCK, I2S2_CK, CK_OUT, EVENTOUT
PB4	56	I/O	5VT	Default: NJTRST, PB4

GD32F505Rx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: TIMER2_CH0, SPI0_MISO, SPI2_MISO, TIMER7_CH2, TRGSEL_OUT6, EVENTOUT
PB5	57	I/O	-	Default: PB5 Alternate: TIMER2_CH1, SPI0_MOSI, I2C0_SMBA, CAN1_RX, TIMER7_CH0BRKIN, SPI2_MOSI, I2S2_SD, TIMER0_CH0BRKIN, EVENTOUT
PB6	58	I/O	5VT	Default: PB6 Alternate: USART0_TX, I2C0_SCL, TIMER3_CH0, CAN1_TX, TIMER7_CH1BRKIN, SPI0_IO2, TIMER0_CH1BRKIN, EVENTOUT
PB7	59	I/O	5VT	Default: PB7 Alternate: USART0_RX, I2C0_SDA, TIMER3_CH1, EXMC_NL, EXMC_NADV, TIMER7_CH2BRKIN, SPI0_IO3, TRGSEL_OUT7, TIMER0_CH2BRKIN, EVENTOUT
BOOT0	60	I/O	-	Default: BOOT0
PB8	61	I/O	5VT	Default: PB8 Alternate: TIMER3_CH2, I2C0_SCL, CAN0_RX, TIMER15_CH0, EVENTOUT
PB9	62	I/O	5VT	Default: PB9 Alternate: I2C0_SDA, CAN0_TX, TIMER3_CH3, TIMER16_CH0, EVENTOUT
VSS	63	P	-	Default: VSS
VDD	64	P	-	Default: VDD

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

2.6.3. GD32F505Rx QFN64 pin definitions

Table 2-5. GD32F505Rx QFN64 pin definitions

GD32F505Rx QFN64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PE5	1	I/O	5VT	Default: PE5 Alternate: EXMC_A21, TIMER15_CH0, EVENTOUT
PE6	2	I/O	5VT	Default: PE6 Alternate: EXMC_A22, TIMER15_CH1, EVENTOUT
VBAT	3	P	-	Default: VBAT
PC13	4	I/O	-	Default: PC13 Alternate: EVENTOUT Additional: TAMPER-RTC
PC14-OSC32IN	5	I/O	-	Default: PC14, OSC32IN Alternate: EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	6	I/O	-	Default: PC15, OSC32OUT Alternate: EVENTOUT Additional: OSC32OUT
OSCIN-PD0	7	I/O	-	Default: OSCIN, PD0 Alternate: EVENTOUT Additional: OSCIN
OSCOUT-PD1	8	I/O	-	Default: OSCOUT, PD1 Alternate: EVENTOUT Additional: OSCOUT
NRST	9	-	-	Default: NRST
PC0	10	I/O	-	Default: PC0 Alternate: TIMER7_CH0_ON, EXMC_NL, EXMC_NADV, EVENTOUT Additional: ADC012_IN10
PC1	11	I/O	-	Default: PC1 Alternate: TIMER7_CH1_ON, EVENTOUT Additional: ADC012_IN11
PC2	12	I/O	-	Default: PC2 Alternate: TIMER7_CH2_ON, EXMC_NWE, EVENTOUT Additional: ADC012_IN12
PC3	13	I/O	-	Default: PC3 Alternate: TIMER7_CH3_ON, EVENTOUT Additional: ADC012_IN13
VDDA/VREFP	14	P	-	Default: VDDA
PA0	15	I/O	-	Default: PA0 Alternate: USART1_CTS, TIMER1_CH0, TIMER1_ETI, TIMER16_BRKIN, TIMER4_CH0, TIMER7_ETI, CMP0_OUT, TRGSEL_IN5, EVENTOUT

GD32F505Rx QFN64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Additional: ADC012_IN0, WKUP
PA1	16	I/O	-	Default: PA1 Alternate: USART1_RTS, TIMER1_CH1, TIMER16_MCH0, TIMER4_CH1, CMP0_OUT, TRGSEL_IN6, EVENTOUT Additional: ADC012_IN1
PA2	17	I/O	-	Default: PA2 Alternate: USART1_TX, TIMER1_CH2, TIMER16_CH0, TIMER4_CH2, SPI0_IO2, TRGSEL_OUT0, EXMC_D4, EVENTOUT Additional: ADC012_IN2, CMP0_IM2
PA3	18	I/O	-	Default: PA3 Alternate: USART1_RX, TIMER1_CH3, TIMER16_CH1, TIMER4_CH3, TIMER0_CH3_ON, SPI0_IO3, TRGSEL_OUT1, EXMC_D5, EVENTOUT Additional: ADC012_IN3
VDD	19	P	-	Default: VDD
PA4	20	I/O	-	Default: PA4 Alternate: SPI0_NSS, USART1_CK, SPI2_NSS, I2S2_WS, TIMER15_BRKIN, TIMER7_CH1BRKIN, EXMC_D6, EVENTOUT Additional: ADC01_IN4, DAC0_OUT0, CMP0_IM0
PA5	21	I/O	-	Default: PA5 Alternate: SPI0_SCK, TIMER4_ETI, TIMER15_MCH0, TIMER7_CH0BRKIN, EXMC_D7, EVENTOUT Additional: ADC01_IN5, DAC0_OUT0, CMP0_IM1
PA6	22	I/O	-	Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, TIMER7_BRKIN, CMP0_OUT, TRGSEL_OUT2, EVENTOUT Additional: ADC01_IN6
PA7	23	I/O	-	Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, TIMER0_CH0_ON, TIMER15_CH1, TIMER7_CH0_ON, TRGSEL_OUT3, EVENTOUT Additional: ADC01_IN7, CMP0_IP
PC4	24	I/O	-	Default: PC4 Alternate: TIMER7_CH3, EXMC_NE0, EVENTOUT Additional: ADC01_IN14
PC5	25	I/O	-	Default: PC5 Alternate: EXMC_NOE, EVENTOUT Additional: ADC01_IN15
PB0	26	I/O	-	Default: PB0 Alternate: TIMER0_CH1_ON, TIMER2_CH2, TIMER7_CH1_ON, CMP0_OUT, EVENTOUT

GD32F505Rx QFN64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Additional: ADC01_IN8
PB1	27	I/O	-	Default: PB1 Alternate: TIMER0_CH2_ON, TIMER2_CH3, TIMER7_CH2_ON, CMP0_OUT, EVENTOUT Additional: ADC01_IN9
PB2/BOOT1	28	I/O	5VT	Default: PB2, BOOT1 Alternate: EVENTOUT
PE15	29	I/O	5VT	Default: PE15 Alternate: TIMER0_BRKIN, EXMC_D12, EVENTOUT Additional: ADC2_IN14
PB10	30	I/O	5VT	Default: PB10 Alternate: TIMER1_CH2, USART2_TX, I2C1_SCL, TIMER0_CH0BRKIN, EVENTOUT Additional: ADC2_IN15, ADC1_IN16
PB11	31	I/O	5VT	Default: PB11 Alternate: TIMER1_CH3, USART2_RX, I2C1_SDA, TIMER0_CH1BRKIN, TRGSEL_IN1, EVENTOUT Additional: ADC2_IN16, ADC1_IN17
VDD	32	P	-	Default: VDD
PB12	33	I/O	5VT	Default: PB12 Alternate: USART2_CK, SPI1_NSS, I2S1_WS, I2C1_SMBA, CAN1_RX, TIMER0_BRKIN, TIMER16_CH0, EXMC_D13, EVENTOUT
PB13	34	I/O	5VT	Default: PB13 Alternate: USART2_CTS, SPI1_SCK, I2S1_CK, TIMER0_CH0_ON, CAN1_TX, TIMER16_CH1, EVENTOUT
PB14	35	I/O	5VT	Default: PB14 Alternate: USART2_RTS, SPI1_MISO, TIMER0_CH1_ON, TIMER15_CH0, EXMC_D0, EVENTOUT
PB15	36	I/O	5VT	Default: PB15 Alternate: SPI1_MOSI, I2S1_SD, TIMER0_CH2_ON, TIMER15_CH1, EVENTOUT
PD15	37	I/O	5VT	Default: PD15 Alternate: TIMER3_CH3, EXMC_D1, CTC_SYNC, EVENTOUT
PC6	38	I/O	5VT	Default: PC6 Alternate: TIMER2_CH0, I2S1_MCK, TIMER7_CH0, EXMC_D1, EVENTOUT
PC7	39	I/O	5VT	Default: PC7 Alternate: TIMER2_CH1, I2S2_MCK, TIMER7_CH3_ON, TIMER7_CH1, EVENTOUT
PC8	40	I/O	5VT	Default: PC8 Alternate: TIMER2_CH2, TIMER7_CH2, EVENTOUT

GD32F505Rx QFN64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PC9	41	I/O	5VT	Default: PC9 Alternate: TIMER2_CH3, TIMER7_CH3, EXMC_NL, EXMC_NADV, EVENTOUT
PA8	42	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, USBFS_SOF, CK_OUT, TIMER7_CH0BRKIN, CTC_SYNC, TRGSEL_OUT4, EVENTOUT
PA9	43	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER7_CH1BRKIN, TRGSEL_OUT5, EVENTOUT
PA10	44	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER0_CH3_ON, TIMER15_BRKIN, TIMER15_CH1, TIMER7_CH2BRKIN, EVENTOUT
PA11	45	I/O	5VT	Default: PA11 Alternate: USART0_CTS, CAN0_RX, TIMER0_CH3, TIMER7_CH0, TIMER15_CH0, TRGSEL_IN0, EVENTOUT Additional: USBFS_DM
PA12	46	I/O	5VT	Default: PA12 Alternate: USART0_RTS, CAN0_TX, TIMER0_ETI, TIMER7_CH1, TIMER15_MCH0, EVENTOUT Additional: USBFS_DP
PA13	47	I/O	5VT	Default: JTMS, SWDIO, PA13 Alternate: EVENTOUT
VDD	48	P	-	Default: VDD
PA14	49	I/O	5VT	Default: JTCK, SWCLK, PA14 Alternate: EVENTOUT
PA15	50	I/O	5VT	Default: JTDI, PA15 Alternate: TIMER1_CH0, TIMER1_ETI, SPI0_NSS, SPI2_NSS, I2S2_WS, TIMER15_BRKIN, TIMER16_BRKIN, EVENTOUT
PC10	51	I/O	5VT	Default: PC10 Alternate: USART2_TX, UART3_TX, SPI2_SCK, I2S2_CK, TIMER7_CH0BRKIN, TIMER0_CH0BRKIN, EVENTOUT
PC11	52	I/O	5VT	Default: PC11 Alternate: USART2_RX, UART3_RX, SPI2_MISO, TIMER7_CH2BRKIN, TIMER16_CH1, TRGSEL_IN2, EXMC_D2, EVENTOUT
PC12	53	I/O	5VT	Default: PC12 Alternate: USART2_CK, UART4_TX, SPI2_MOSI, I2S2_SD, TIMER16_CH0, EXMC_D3, EVENTOUT
PD2	54	I/O	5VT	Default: PD2

GD32F505Rx QFN64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: TIMER2_ETI, UART4_RX, TIMER16_MCH0, EXMC_NWE, EVENTOUT
PB3	55	I/O	5VT	Default: JTDO, PB3 Alternate: TRACESWO, TIMER1_CH1, SPI0_SCK, SPI2_SCK, I2S2_CK, CK_OUT, EVENTOUT
PB4	56	I/O	5VT	Default: NJTRST, PB4 Alternate: TIMER2_CH0, SPI0_MISO, SPI2_MISO, TIMER7_CH2, TRGSEL_OUT6, EVENTOUT
PB5	57	I/O	-	Default: PB5 Alternate: TIMER2_CH1, SPI0_MOSI, I2C0_SMBA, CAN1_RX, TIMER7_CH0BRKIN, SPI2_MOSI, I2S2_SD, TIMER0_CH0BRKIN, EVENTOUT
PB6	58	I/O	5VT	Default: PB6 Alternate: USART0_TX, I2C0_SCL, TIMER3_CH0, CAN1_TX, TIMER7_CH1BRKIN, SPI0_IO2, TIMER0_CH1BRKIN, EVENTOUT
PB7	59	I/O	5VT	Default: PB7 Alternate: USART0_RX, I2C0_SDA, TIMER3_CH1, EXMC_NL, EXMC_NADV, TIMER7_CH2BRKIN, SPI0_IO3, TRGSEL_OUT7, TIMER0_CH2BRKIN, EVENTOUT
BOOT0	60	I/O	-	Default: BOOT0
PB8	61	I/O	5VT	Default: PB8 Alternate: TIMER3_CH2, I2C0_SCL, CAN0_RX, TIMER15_CH0, EVENTOUT
PB9	62	I/O	5VT	Default: PB9 Alternate: I2C0_SDA, CAN0_TX, TIMER3_CH3, TIMER16_CH0, EVENTOUT
PE0	63	I/O	5VT	Default: PE0 Alternate: TIMER3_ETI, EXMC_NBL0, TRGSEL_IN7, EVENTOUT
VDD	64	P	-	Default: VDD

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

2.6.4. GD32F505Rx BGA64 pin definitions

Table 2-6. GD32F505Rx BGA64 pin definitions

GD32F505Rx BGA64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
VBAT	C2	P	-	Default: VBAT
PC13	B1	I/O	-	Default: PC13 Alternate: EVENTOUT Additional: TAMPER-RTC
PC14-OSC32IN	C1	I/O	-	Default: PC14, OSC32IN Alternate: EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	D1	I/O	-	Default: PC15, OSC32OUT Alternate: EVENTOUT Additional: OSC32OUT
OSCIN-PD0	E1	I/O	-	Default: OSCIN, PD0 Alternate: EVENTOUT Additional: OSCIN
OSCOUT-PD1	F1	I/O	-	Default: OSCOUT, PD1 Alternate: EVENTOUT Additional: OSCOUT
NRST	D2	-	-	Default: NRST
PC0	E2	I/O	-	Default: PC0 Alternate: TIMER7_CH0_ON, EXMC_NL, EXMC_NADV, EVENTOUT Additional: ADC012_IN10
PC1	C3	I/O	-	Default: PC1 Alternate: TIMER7_CH1_ON, EVENTOUT Additional: ADC012_IN11
PC2	D3	I/O	-	Default: PC2 Alternate: TIMER7_CH2_ON, EXMC_NWE, EVENTOUT Additional: ADC012_IN12
PC3	G4	I/O	-	Default: PC3 Alternate: TIMER7_CH3_ON, EVENTOUT Additional: ADC012_IN13
VSSA/VREFN	F2	P	-	Default: VSSA
VDDA/VREFP	G1	P	-	Default: VDDA
PA0	H5	I/O	-	Default: PA0 Alternate: USART1_CTS, TIMER1_CH0, TIMER1_ETI, TIMER16_BRKIN, TIMER4_CH0, TIMER7_ETI, CMP0_OUT, TRGSEL_IN5, EVENTOUT Additional: ADC012_IN0, WKUP
PA1	E3	I/O	-	Default: PA1

GD32F505Rx BGA64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: USART1_RTS, TIMER1_CH1, TIMER16_MCH0, TIMER4_CH1, CMP0_OUT, TRGSEL_IN6, EVENTOUT Additional: ADC012_IN1
PA2	F3	I/O	-	Default: PA2 Alternate: USART1_TX, TIMER1_CH2, TIMER16_CH0, TIMER4_CH2, SPI0_IO2, TRGSEL_OUT0, EXMC_D4, EVENTOUT Additional: ADC012_IN2, CMP0_IM2
PA3	H2	I/O	-	Default: PA3 Alternate: USART1_RX, TIMER1_CH3, TIMER16_CH1, TIMER4_CH3, TIMER0_CH3_ON, SPI0_IO3, TRGSEL_OUT1, EXMC_D5, EVENTOUT Additional: ADC012_IN3
VSS	G2	P	-	Default: VSS
VDD	H1	P	-	Default: VDD
PA4	D4	I/O	-	Default: PA4 Alternate: SPI0_NSS, USART1_CK, SPI2_NSS, I2S2_WS, TIMER15_BRKIN, TIMER7_CH1BRKIN, EXMC_D6, EVENTOUT Additional: ADC01_IN4, DAC0_OUT0, CMP0_IM0
PA5	E4	I/O	-	Default: PA5 Alternate: SPI0_SCK, TIMER4_ETI, TIMER15_MCH0, TIMER7_CH0BRKIN, EXMC_D7, EVENTOUT Additional: ADC01_IN5, DAC0_OUT0, CMP0_IM1
PA6	G3	I/O	-	Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, TIMER7_BRKIN, CMP0_OUT, TRGSEL_OUT2, EVENTOUT Additional: ADC01_IN6
PA7	H3	I/O	-	Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, TIMER0_CH0_ON, TIMER15_CH1, TIMER7_CH0_ON, TRGSEL_OUT3, EVENTOUT Additional: ADC01_IN7, CMP0_IP
PC4	D5	I/O	-	Default: PC4 Alternate: TIMER7_CH3, EXMC_NE0, EVENTOUT Additional: ADC01_IN14
PC5	F4	I/O	-	Default: PC5 Alternate: EXMC_NOE, EVENTOUT Additional: ADC01_IN15
PB0	E5	I/O	-	Default: PB0 Alternate: TIMER0_CH1_ON, TIMER2_CH2, TIMER7_CH1_ON, CMP0_OUT, EVENTOUT Additional: ADC01_IN8

GD32F505Rx BGA64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PB1	F5	I/O	-	Default: PB1 Alternate: TIMER0_CH2_ON, TIMER2_CH3, TIMER7_CH2_ON, CMP0_OUT, EVENTOUT Additional: ADC01_IN9
PB2/BOOT1	H4	I/O	5VT	Default: PB2, BOOT1 Alternate: EVENTOUT
PB10	H6	I/O	5VT	Default: PB10 Alternate: TIMER1_CH2, USART2_TX, I2C1_SCL, TIMER0_CH0BRKIN, EVENTOUT Additional: ADC2_IN15, ADC1_IN16
PB11	H7	I/O	5VT	Default: PB11 Alternate: TIMER1_CH3, USART2_RX, I2C1_SDA, TIMER0_CH1BRKIN, TRGSEL_IN1, EVENTOUT Additional: ADC2_IN16, ADC1_IN17
VSS	G7	P	-	Default: VSS
VDD	H8	P	-	Default: VDD
PB12	G8	I/O	5VT	Default: PB12 Alternate: USART2_CK, SPI1_NSS, I2S1_WS, I2C1_SMBA, CAN1_RX, TIMER0_BRKIN, TIMER16_CH0, EXMC_D13, EVENTOUT
PB13	G6	I/O	5VT	Default: PB13 Alternate: USART2_CTS, SPI1_SCK, I2S1_CK, TIMER0_CH0_ON, CAN1_TX, TIMER16_CH1, EVENTOUT
PB14	F8	I/O	5VT	Default: PB14 Alternate: USART2_RTS, SPI1_MISO, TIMER0_CH1_ON, TIMER15_CH0, EXMC_D0, EVENTOUT
PB15	F7	I/O	5VT	Default: PB15 Alternate: SPI1_MOSI, I2S1_SD, TIMER0_CH2_ON, TIMER15_CH1, EVENTOUT
PC6	E8	I/O	5VT	Default: PC6 Alternate: TIMER2_CH0, I2S1_MCK, TIMER7_CH0, EXMC_D1, EVENTOUT
PC7	E7	I/O	5VT	Default: PC7 Alternate: TIMER2_CH1, I2S2_MCK, TIMER7_CH3_ON, TIMER7_CH1, EVENTOUT
PC8	F6	I/O	5VT	Default: PC8 Alternate: TIMER2_CH2, TIMER7_CH2, EVENTOUT
PC9	D8	I/O	5VT	Default: PC9 Alternate: TIMER2_CH3, TIMER7_CH3, EXMC_NL, EXMC_NADV, EVENTOUT
PA8	E6	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, USBFS_SOF, CK_OUT, TIMER7_CH0BRKIN, CTC_SYNC,

GD32F505Rx BGA64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				TRGSEL_OUT4, EVENTOUT
PA9	D7	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER7_CH1BRKIN, TRGSEL_OUT5, EVENTOUT
PA10	D6	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER0_CH3_ON, TIMER15_BRKIN, TIMER15_CH1, TIMER7_CH2BRKIN, EVENTOUT
PA11	C8	I/O	5VT	Default: PA11 Alternate: USART0_CTS, CAN0_RX, TIMER0_CH3, TIMER7_CH0, TIMER15_CH0, TRGSEL_IN0, EVENTOUT Additional: USBFS_DM
PA12	B8	I/O	5VT	Default: PA12 Alternate: USART0_RTS, CAN0_TX, TIMER0_ETI, TIMER7_CH1, TIMER15_MCH0, EVENTOUT Additional: USBFS_DP
PA13	C7	I/O	5VT	Default: JTMS, SWDIO, PA13 Alternate: EVENTOUT
VSS	B7	P	-	Default: VSS
VDD	A8	P	-	Default: VDD
PA14	C6	I/O	5VT	Default: JTCK, SWCLK, PA14 Alternate: EVENTOUT
PA15	A7	I/O	5VT	Default: JTDI, PA15 Alternate: TIMER1_CH0, TIMER1_ETI, SPI0_NSS, SPI2_NSS, I2S2_WS, TIMER15_BRKIN, TIMER16_BRKIN, EVENTOUT
PC10	C5	I/O	5VT	Default: PC10 Alternate: USART2_TX, UART3_TX, SPI2_SCK, I2S2_CK, TIMER7_CH0BRKIN, TIMER0_CH0BRKIN, EVENTOUT
PC11	B6	I/O	5VT	Default: PC11 Alternate: USART2_RX, UART3_RX, SPI2_MISO, TIMER7_CH2BRKIN, TIMER16_CH1, TRGSEL_IN2, EXMC_D2, EVENTOUT
PC12	A6	I/O	5VT	Default: PC12 Alternate: USART2_CK, UART4_TX, SPI2_MOSI, I2S2_SD, TIMER16_CH0, EXMC_D3, EVENTOUT
PD2	B5	I/O	5VT	Default: PD2 Alternate: TIMER2_ETI, UART4_RX, TIMER16_MCH0, EXMC_NWE, EVENTOUT
PB3	A5	I/O	5VT	Default: JTDO, PB3 Alternate: TRACESWO, TIMER1_CH1, SPI0_SCK, SPI2_SCK, I2S2_CK, CK_OUT, EVENTOUT
PB4	C4	I/O	5VT	Default: NJTRST, PB4

GD32F505Rx BGA64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: TIMER2_CH0, SPI0_MISO, SPI2_MISO, TIMER7_CH2, TRGSEL_OUT6, EVENTOUT
PB5	B4	I/O	-	Default: PB5 Alternate: TIMER2_CH1, SPI0_MOSI, I2C0_SMBA, CAN1_RX, TIMER7_CH0BRKIN, SPI2_MOSI, I2S2_SD, TIMER0_CH0BRKIN, EVENTOUT
PB6	A4	I/O	5VT	Default: PB6 Alternate: USART0_TX, I2C0_SCL, TIMER3_CH0, CAN1_TX, TIMER7_CH1BRKIN, SPI0_IO2, TIMER0_CH1BRKIN, EVENTOUT
PB7	A3	I/O	5VT	Default: PB7 Alternate: USART0_RX, I2C0_SDA, TIMER3_CH1, EXMC_NL, EXMC_NADV, TIMER7_CH2BRKIN, SPI0_IO3, TRGSEL_OUT7, TIMER0_CH2BRKIN, EVENTOUT
BOOT0	B3	I/O	-	Default: BOOT0
PB8	G5	I/O	5VT	Default: PB8 Alternate: TIMER3_CH2, I2C0_SCL, CAN0_RX, TIMER15_CH0, EVENTOUT
PB9	A2	I/O	5VT	Default: PB9 Alternate: I2C0_SDA, CAN0_TX, TIMER3_CH3, TIMER16_CH0, EVENTOUT
VSS	B2	P	-	Default: VSS
VDD	A1	P	-	Default: VDD

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

2.6.5. GD32F505Cx LQFP48 pin definitions

Table 2-7. GD32F505Cx LQFP48 pin definitions

GD32F505Cx LQFP48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
VBAT	1	P	-	Default: VBAT
PC13	2	I/O	-	Default: PC13 Alternate: EVENTOUT Additional: TAMPER-RTC
PC14-OSC32IN	3	I/O	-	Default: PC14, OSC32IN Alternate: EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	4	I/O	-	Default: PC15, OSC32OUT Alternate: EVENTOUT Additional: OSC32OUT
OSCIN-PD0	5	I/O	-	Default: OSCIN, PD0 Alternate: EVENTOUT Additional: OSCIN
OSCOUT-PD1	6	I/O	-	Default: OSCOUT, PD1 Alternate: EVENTOUT Additional: OSCOUT
NRST	7	-	-	Default: NRST
VSSA/VREFN	8	P	-	Default: VSSA
VDDA/VREFP	9	P	-	Default: VDDA
PA0	10	I/O	-	Default: PA0 Alternate: USART1_CTS, TIMER1_CH0, TIMER1_ETI, TIMER16_BRKIN, TIMER4_CH0, TIMER7_ETI, CMP0_OUT, TRGSEL_IN5, EVENTOUT Additional: ADC012_IN0, WKUP
PA1	11	I/O	-	Default: PA1 Alternate: USART1_RTS, TIMER1_CH1, TIMER16_MCH0, TIMER4_CH1, CMP0_OUT, TRGSEL_IN6, EVENTOUT Additional: ADC012_IN1
PA2	12	I/O	-	Default: PA2 Alternate: USART1_TX, TIMER1_CH2, TIMER16_CH0, TIMER4_CH2, SPI0_IO2, TRGSEL_OUT0, EVENTOUT Additional: ADC012_IN2, CMP0_IM2
PA3	13	I/O	-	Default: PA3 Alternate: USART1_RX, TIMER1_CH3, TIMER16_CH1, TIMER4_CH3, TIMER0_CH3_ON, SPI0_IO3, TRGSEL_OUT1, EVENTOUT Additional: ADC012_IN3
PA4	14	I/O	-	Default: PA4

GD32F505Cx LQFP48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: SPI0_NSS, USART1_CK, SPI2_NSS, I2S2_WS, TIMER15_BRKIN, TIMER7_CH1BRKIN, EVENTOUT Additional: ADC01_IN4, DAC0_OUT0, CMP0_IM0
PA5	15	I/O	-	Default: PA5 Alternate: SPI0_SCK, TIMER4_ETI, TIMER15_MCH0, TIMER7_CH0BRKIN, EVENTOUT Additional: ADC01_IN5, DAC0_OUT0, CMP0_IM1
PA6	16	I/O	-	Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, TIMER7_BRKIN, CMP0_OUT, TRGSEL_OUT2, EVENTOUT Additional: ADC01_IN6
PA7	17	I/O	-	Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, TIMER0_CH0_ON, TIMER15_CH1, TIMER7_CH0_ON, TRGSEL_OUT3, EVENTOUT Additional: ADC01_IN7, CMP0_IP
PB0	18	I/O	-	Default: PB0 Alternate: TIMER0_CH1_ON, TIMER2_CH2, TIMER7_CH1_ON, CMP0_OUT, EVENTOUT Additional: ADC01_IN8
PB1	19	I/O	-	Default: PB1 Alternate: TIMER0_CH2_ON, TIMER2_CH3, TIMER7_CH2_ON, CMP0_OUT, EVENTOUT Additional: ADC01_IN9
PB2/BOOT1	20	I/O	5VT	Default: PB2, BOOT1 Alternate: EVENTOUT
PB10	21	I/O	5VT	Default: PB10 Alternate: TIMER1_CH2, USART2_TX, I2C1_SCL, TIMER0_CH0BRKIN, EVENTOUT Additional: ADC2_IN15, ADC1_IN16
PB11	22	I/O	5VT	Default: PB11 Alternate: TIMER1_CH3, USART2_RX, I2C1_SDA, TIMER0_CH1BRKIN, TRGSEL_IN1, EVENTOUT Additional: ADC2_IN16, ADC1_IN17
VSS	23	P	-	Default: VSS
VDD	24	P	-	Default: VDD
PB12	25	I/O	5VT	Default: PB12 Alternate: USART2_CK, SPI1_NSS, I2S1_WS, I2C1_SMBA, CAN1_RX, TIMER0_BRKIN, TIMER16_CH0, EVENTOUT
PB13	26	I/O	5VT	Default: PB13 Alternate: USART2_CTS, SPI1_SCK, I2S1_CK, TIMER0_CH0_ON, CAN1_TX, TIMER16_CH1,

GD32F505Cx LQFP48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				EVENTOUT
PB14	27	I/O	5VT	Default: PB14 Alternate: USART2_RTS, SPI1_MISO, TIMER0_CH1_ON, TIMER15_CH0, EVENTOUT
PB15	28	I/O	5VT	Default: PB15 Alternate: SPI1_MOSI, I2S1_SD, TIMER0_CH2_ON, TIMER15_CH1, EVENTOUT
PA8	29	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, USBFS_SOF, CK_OUT, TIMER7_CH0BRKIN, CTC_SYNC, TRGSEL_OUT4, EVENTOUT
PA9	30	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER7_CH1BRKIN, TRGSEL_OUT5, EVENTOUT
PA10	31	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER0_CH3_ON, TIMER15_BRKIN, TIMER15_CH1, TIMER7_CH2BRKIN, EVENTOUT
PA11	32	I/O	5VT	Default: PA11 Alternate: USART0_CTS, CAN0_RX, TIMER0_CH3, TIMER7_CH0, TIMER15_CH0, TRGSEL_IN0, EVENTOUT Additional: USBFS_DM
PA12	33	I/O	5VT	Default: PA12 Alternate: USART0_RTS, CAN0_TX, TIMER0_ETI, TIMER7_CH1, TIMER15_MCH0, EVENTOUT Additional: USBFS_DP
PA13	34	I/O	5VT	Default: JTMS, SWDIO, PA13 Alternate: EVENTOUT
VSS	35	P	-	Default: VSS
VDD	36	P	-	Default: VDD
PA14	37	I/O	5VT	Default: JTCK, SWCLK, PA14 Alternate: EVENTOUT
PA15	38	I/O	5VT	Default: JTDI, PA15 Alternate: TIMER1_CH0, TIMER1_ETI, SPI0_NSS, SPI2_NSS, I2S2_WS, TIMER15_BRKIN, TIMER16_BRKIN, EVENTOUT
PB3	39	I/O	5VT	Default: JTDO, PB3 Alternate: TRACESWO, TIMER1_CH1, SPI0_SCK, SPI2_SCK, I2S2_CK, CK_OUT, EVENTOUT
PB4	40	I/O	5VT	Default: NJTRST, PB4 Alternate: TIMER2_CH0, SPI0_MISO, SPI2_MISO, TIMER7_CH2, TRGSEL_OUT6, EVENTOUT
PB5	41	I/O	-	Default: PB5 Alternate: TIMER2_CH1, SPI0_MOSI, I2C0_SMBA,

GD32F505Cx LQFP48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				CAN1_RX, TIMER7_CH0BRKIN, SPI2_MOSI, I2S2_SD, TIMER0_CH0BRKIN, EVENTOUT
PB6	42	I/O	5VT	Default: PB6 Alternate: USART0_TX, I2C0_SCL, TIMER3_CH0, CAN1_TX, TIMER7_CH1BRKIN, SPI0_IO2, TIMER0_CH1BRKIN, EVENTOUT
PB7	43	I/O	5VT	Default: PB7 Alternate: USART0_RX, I2C0_SDA, TIMER3_CH1, TIMER7_CH2BRKIN, SPI0_IO3, TRGSEL_OUT7, TIMER0_CH2BRKIN, EVENTOUT
BOOT0	44	I/O	-	Default: BOOT0
PB8	45	I/O	5VT	Default: PB8 Alternate: TIMER3_CH2, I2C0_SCL, CAN0_RX, TIMER15_CH0, EVENTOUT
PB9	46	I/O	5VT	Default: PB9 Alternate: I2C0_SDA, CAN0_TX, TIMER3_CH3, TIMER16_CH0, EVENTOUT
VSS	47	P	-	Default: VSS
VDD	48	P	-	Default: VDD

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

2.6.6. GD32F505Cx QFN48 pin definitions

Table 2-8. GD32F505Cx QFN48 pin definitions

GD32F505Cx QFN48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
VBAT	1	P	-	Default: VBAT
PC13	2	I/O	-	Default: PC13 Alternate: EVENTOUT Additional: TAMPER-RTC
PC14-OSC32IN	3	I/O	-	Default: PC14, OSC32IN Alternate: EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	4	I/O	-	Default: PC15, OSC32OUT Alternate: EVENTOUT Additional: OSC32OUT
OSCIN-PD0	5	I/O	-	Default: OSCIN, PD0 Alternate: EVENTOUT Additional: OSCIN
OSCOUT-PD1	6	I/O	-	Default: OSCOUT, PD1 Alternate: EVENTOUT Additional: OSCOUT
NRST	7	-	-	Default: NRST
PC3	8	I/O	-	Default: PC3 Alternate: TIMER7_CH3_ON, EVENTOUT Additional: ADC012_IN13
VDDA/VREFP	9	P	-	Default: VDDA
PA0	10	I/O	-	Default: PA0 Alternate: USART1_CTS, TIMER1_CH0, TIMER1_ETI, TIMER16_BRKIN, TIMER4_CH0, TIMER7_ETI, CMP0_OUT, TRGSEL_IN5, EVENTOUT Additional: ADC012_IN0, WKUP
PA1	11	I/O	-	Default: PA1 Alternate: USART1_RTS, TIMER1_CH1, TIMER16_MCH0, TIMER4_CH1, CMP0_OUT, TRGSEL_IN6, EVENTOUT Additional: ADC012_IN1
PA2	12	I/O	-	Default: PA2 Alternate: USART1_TX, TIMER1_CH2, TIMER16_CH0, TIMER4_CH2, SPI0_IO2, TRGSEL_OUT0, EVENTOUT Additional: ADC012_IN2, CMP0_IM2
PA3	13	I/O	-	Default: PA3 Alternate: USART1_RX, TIMER1_CH3, TIMER16_CH1, TIMER4_CH3, TIMER0_CH3_ON, SPI0_IO3, TRGSEL_OUT1, EVENTOUT Additional: ADC012_IN3

GD32F505Cx QFN48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PA4	14	I/O	-	Default: PA4 Alternate: SPI0_NSS, USART1_CK, SPI2_NSS, I2S2_WS, TIMER15_BRKIN, TIMER7_CH1BRKIN, EVENTOUT Additional: ADC01_IN4, DAC0_OUT0, CMP0_IM0
PA5	15	I/O	-	Default: PA5 Alternate: SPI0_SCK, TIMER4_ETI, TIMER15_MCH0, TIMER7_CH0BRKIN, EVENTOUT Additional: ADC01_IN5, DAC0_OUT0, CMP0_IM1
PA6	16	I/O	-	Default: PA6 Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, TIMER7_BRKIN, CMP0_OUT, TRGSEL_OUT2, EVENTOUT Additional: ADC01_IN6
PA7	17	I/O	-	Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, TIMER0_CH0_ON, TIMER15_CH1, TIMER7_CH0_ON, TRGSEL_OUT3, EVENTOUT Additional: ADC01_IN7, CMP0_IP
PB0	18	I/O	-	Default: PB0 Alternate: TIMER0_CH1_ON, TIMER2_CH2, TIMER7_CH1_ON, CMP0_OUT, EVENTOUT Additional: ADC01_IN8
PB1	19	I/O	-	Default: PB1 Alternate: TIMER0_CH2_ON, TIMER2_CH3, TIMER7_CH2_ON, CMP0_OUT, EVENTOUT Additional: ADC01_IN9
PB2/BOOT1	20	I/O	5VT	Default: PB2, BOOT1 Alternate: EVENTOUT
PE15	21	I/O	5VT	Default: PE15 Alternate: TIMER0_BRKIN, EVENTOUT Additional: ADC2_IN14
PB10	22	I/O	5VT	Default: PB10 Alternate: TIMER1_CH2, USART2_TX, I2C1_SCL, TIMER0_CH0BRKIN, EVENTOUT Additional: ADC2_IN15, ADC1_IN16
PB11	23	I/O	5VT	Default: PB11 Alternate: TIMER1_CH3, USART2_RX, I2C1_SDA, TIMER0_CH1BRKIN, TRGSEL_IN1, EVENTOUT Additional: ADC2_IN16, ADC1_IN17
VDD	24	P	-	Default: VDD
PB12	25	I/O	5VT	Default: PB12 Alternate: USART2_CK, SPI1_NSS, I2S1_WS, I2C1_SMBA, CAN1_RX, TIMER0_BRKIN, TIMER16_CH0, EVENTOUT

GD32F505Cx QFN48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PB13	26	I/O	5VT	Default: PB13 Alternate: USART2_CTS, SPI1_SCK, I2S1_CK, TIMER0_CH0_ON, CAN1_TX, TIMER16_CH1, EVENTOUT
PB14	27	I/O	5VT	Default: PB14 Alternate: USART2_RTS, SPI1_MISO, TIMER0_CH1_ON, TIMER15_CH0, EVENTOUT
PB15	28	I/O	5VT	Default: PB15 Alternate: SPI1_MOSI, I2S1_SD, TIMER0_CH2_ON, TIMER15_CH1, EVENTOUT
PC9	29	I/O	5VT	Default: PC9 Alternate: TIMER2_CH3, TIMER7_CH3, EVENTOUT
PA8	30	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, USBFS_SOF, CK_OUT, TIMER7_CH0BRKIN, CTC_SYNC, TRGSEL_OUT4, EVENTOUT
PA9	31	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER7_CH1BRKIN, TRGSEL_OUT5, EVENTOUT
PA10	32	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER0_CH3_ON, TIMER15_BRKIN, TIMER15_CH1, TIMER7_CH2BRKIN, EVENTOUT
PA11	33	I/O	5VT	Default: PA11 Alternate: USART0_CTS, CAN0_RX, TIMER0_CH3, TIMER7_CH0, TIMER15_CH0, TRGSEL_IN0, EVENTOUT Additional: USBFS_DM
PA12	34	I/O	5VT	Default: PA12 Alternate: USART0_RTS, CAN0_TX, TIMER0_ETI, TIMER7_CH1, TIMER15_MCH0, EVENTOUT Additional: USBFS_DP
PA13	35	I/O	5VT	Default: JTMS, SWDIO, PA13 Alternate: EVENTOUT
VDD	36	P	-	Default: VDD
PA14	37	I/O	5VT	Default: JTCK, SWCLK, PA14 Alternate: EVENTOUT
PA15	38	I/O	5VT	Default: JTDI, PA15 Alternate: TIMER1_CH0, TIMER1_ETI, SPI0_NSS, SPI2_NSS, I2S2_WS, TIMER15_BRKIN, TIMER16_BRKIN, EVENTOUT
PB3	39	I/O	5VT	Default: JTDO, PB3 Alternate: TRACESWO, TIMER1_CH1, SPI0_SCK, SPI2_SCK, I2S2_CK, CK_OUT, EVENTOUT
PB4	40	I/O	5VT	Default: NJTRST, PB4

GD32F505Cx QFN48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: TIMER2_CH0, SPI0_MISO, SPI2_MISO, TIMER7_CH2, TRGSEL_OUT6, EVENTOUT
PB5	41	I/O	-	Default: PB5 Alternate: TIMER2_CH1, SPI0_MOSI, I2C0_SMBA, CAN1_RX, TIMER7_CH0BRKIN, SPI2_MOSI, I2S2_SD, TIMER0_CH0BRKIN, EVENTOUT
PB6	42	I/O	5VT	Default: PB6 Alternate: USART0_TX, I2C0_SCL, TIMER3_CH0, CAN1_TX, TIMER7_CH1BRKIN, SPI0_IO2, TIMER0_CH1BRKIN, EVENTOUT
PB7	43	I/O	5VT	Default: PB7 Alternate: USART0_RX, I2C0_SDA, TIMER3_CH1, TIMER7_CH2BRKIN, SPI0_IO3, TRGSEL_OUT7, TIMER0_CH2BRKIN, EVENTOUT
BOOT0	44	I/O	-	Default: BOOT0
PB8	45	I/O	5VT	Default: PB8 Alternate: TIMER3_CH2, I2C0_SCL, CAN0_RX, TIMER15_CH0, EVENTOUT
PB9	46	I/O	5VT	Default: PB9 Alternate: I2C0_SDA, CAN0_TX, TIMER3_CH3, TIMER16_CH0, EVENTOUT
PE0	47	I/O	5VT	Default: PE0 Alternate: TIMER3_ETI, TRGSEL_IN7, EVENTOUT
VDD	48	P	-	Default: VDD

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

2.6.7. GD32F505xx pin alternate functions

Table 2-9. Port A alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8
PA0	USART1_CTS	TIMER1_CH0/TIMER1_ETI	TIMER16_BRKIN	TIMER4_CH0	TIMER7_ETI	CMP0_OUT	TRGSEL_IN5		EVENTOUT
PA1	USART1_RTS	TIMER1_CH1	TIMER16_MCH0	TIMER4_CH1		CMP0_OUT	TRGSEL_IN6		EVENTOUT
PA2	USART1_TX	TIMER1_CH2	TIMER16_CH0	TIMER4_CH2		SPI0_IO2	TRGSEL_OUT0	EXMC_D4	EVENTOUT
PA3	USART1_RX	TIMER1_CH3	TIMER16_CH1	TIMER4_CH3	TIMER0_CH3_ON	SPI0_IO3	TRGSEL_OUT1	EXMC_D5	EVENTOUT
PA4	SPI0_NSS	USART1_CK	SPI2_NSS/I2S2_WS	TIMER15_BRKIN	TIMER7_CH1BRKIN			EXMC_D6	EVENTOUT
PA5	SPI0_SCK		TIMER4_ETI	TIMER15_MCH0	TIMER7_CH0BRKIN			EXMC_D7	EVENTOUT
PA6	SPI0_MISO	TIMER2_CH0	TIMER0_BRKIN	TIMER15_CH0	TIMER7_BRKIN	CMP0_OUT	TRGSEL_OUT2		EVENTOUT
PA7	SPI0_MOSI	TIMER2_CH1	TIMER0_CH0_ON	TIMER15_CH1	TIMER7_CH0_ON		TRGSEL_OUT3		EVENTOUT
PA8	USART0_CK	TIMER0_CH0	USBFS_SOF	CK_OUT	TIMER7_CH0BRKIN	CTC_SYNC	TRGSEL_OUT4		EVENTOUT
PA9	USART0_TX	TIMER0_CH1			TIMER7_CH1BRKIN		TRGSEL_OUT5		EVENTOUT
PA10	USART0_RX	TIMER0_CH2	TIMER0_CH3_ON	TIMER15_BRKIN	TIMER15_CH1	TIMER7_CH2BRKIN			EVENTOUT
PA11	USART0_CTS	CAN0_RX	TIMER0_CH3	TIMER7_CH0	TIMER15_CH0		TRGSEL_IN0		EVENTOUT
PA12	USART0_RTS	CAN0_TX	TIMER0_ETI	TIMER7_CH1	TIMER15_MCH0				EVENTOUT
PA13	JTMS/SWDIO								EVENTOUT
PA14	JTCK/SWCLK								EVENTOUT
PA15	JTDI	TIMER1_CH0/TIMER1_ETI	SPI0_NSS	SPI2_NSS/I2S2_WS	TIMER15_BRKIN	TIMER16_BRKIN			EVENTOUT

Table 2-10. Port B alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8
PB0	TIMER0_CH1_ON	TIMER2_CH2		TIMER7_CH1_ON		CMP0_OUT			EVENTOUT
PB1	TIMER0_CH2_ON	TIMER2_CH3		TIMER7_CH2_ON		CMP0_OUT			EVENTOUT
PB2	BOOT1								EVENTOUT
PB3	JTDO/TRACESWO	TIMER1_CH1	SPI0_SCK	SPI2_SCK/I2S2_CK	CK_OUT				EVENTOUT
PB4	NJTRST	TIMER2_CH0	SPI0_MISO	SPI2_MISO	TIMER7_CH2		TRGSEL_OUT6		EVENTOUT
PB5	TIMER2_CH1	SPI0_MOSI	I2C0_SMBA	CAN1_RX	TIMER7_CH0BRKIN	SPI2_MOSI/I2S2_SD	TIMER0_CH0BRKIN		EVENTOUT
PB6	USART0_TX	I2C0_SCL	TIMER3_CH0	CAN1_TX	TIMER7_CH1BRKIN	SPI0_IO2	TIMER0_CH1BRKIN		EVENTOUT
PB7	USART0_RX	I2C0_SDA	TIMER3_CH1	EXMC_NL/EXMC_NADV	TIMER7_CH2BRKIN	SPI0_IO3	TRGSEL_OUT7	TIMER0_CH2BRKIN	EVENTOUT
PB8	I2C0_SCL	CAN0_RX	TIMER3_CH2		TIMER15_CH0				EVENTOUT
PB9	I2C0_SDA	CAN0_TX	TIMER3_CH3		TIMER16_CH0				EVENTOUT
PB10	TIMER1_CH2	USART2_TX	I2C1_SCL		TIMER0_CH0BRKIN				EVENTOUT

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8
PB11	TIMER1_CH3	USART2_RX	I2C1_SDA		TIMER0_CH1BRKIN		TRGSEL_IN1		EVENTOUT
PB12	USART2_CK	SPI1_NSS/I2S1_WS	I2C1_SMBA	CAN1_RX	TIMER0_BRKIN		TIMER16_CH0	EXMC_D13	EVENTOUT
PB13	USART2_CTS	SPI1_SCK/I2S1_CK	TIMER0_CH0_ON	CAN1_TX			TIMER16_CH1		EVENTOUT
PB14	USART2_RTS	SPI1_MISO	TIMER0_CH1_ON		TIMER15_CH0			EXMC_D0	EVENTOUT
PB15	SPI1_MOSI/I2S1_SD	TIMER0_CH2_ON			TIMER15_CH1				EVENTOUT

Table 2-11. Port C alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8
PC0	TIMER7_CH0_ON							EXMC_NL/EXMC_NADV	EVENTOUT
PC1	TIMER7_CH1_ON								EVENTOUT
PC2	TIMER7_CH2_ON							EXMC_NWE	EVENTOUT
PC3	TIMER7_CH3_ON								EVENTOUT
PC4	TIMER7_CH3							EXMC_NE0	EVENTOUT
PC5								EXMC_NOE	EVENTOUT
PC6	TIMER2_CH0	I2S1_MCK		TIMER7_CH0				EXMC_D1	EVENTOUT
PC7	TIMER2_CH1	I2S2_MCK	TIMER7_CH3_ON	TIMER7_CH1					EVENTOUT
PC8	TIMER2_CH2		TIMER7_CH2						EVENTOUT
PC9	TIMER2_CH3		TIMER7_CH3					EXMC_NL/EXMC_NADV	EVENTOUT
PC10	USART2_TX	UART3_TX	SPI2_SCK/I2S2_CK	TIMER7_CH0BRKIN	TIMER0_CH0BRKIN				EVENTOUT
PC11	USART2_RX	UART3_RX	SPI2_MISO	TIMER7_CH2BRKIN	TIMER16_CH1		TRGSEL_IN2	EXMC_D2	EVENTOUT
PC12	USART2_CK	UART4_TX	SPI2_MOSI/I2S2_SD		TIMER16_CH0			EXMC_D3	EVENTOUT
PC13									EVENTOUT
PC14									EVENTOUT
PC15									EVENTOUT

Table 2-12. Port D alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8
PD0	CAN0_RX	EXMC_D2							EVENTOUT
PD1	CAN0_TX	EXMC_D3							EVENTOUT
PD2	TIMER2_ETI	UART4_RX			TIMER16_MCH0			EXMC_NWE	EVENTOUT
PD3	USART1_CTS	EXMC_CLK							EVENTOUT
PD4	USART1_RTS	EXMC_NOE							EVENTOUT
PD5	USART1_TX	EXMC_NWE							EVENTOUT
PD6	USART1_RX	EXMC_NWAIT							EVENTOUT
PD7	USART1_CK	EXMC_NE0/EXMC_NCE							EVENTOUT

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8
		1							
PD8	USART2_TX	EXMC_D13			TIMER0_CH0BRKIN				EVENTOUT
PD9	USART2_RX	EXMC_D14			TIMER0_CH1BRKIN				EVENTOUT
PD10	USART2_CK	EXMC_D15			TIMER0_CH2BRKIN				EVENTOUT
PD11	USART2_CTS	EXMC_A16					TRGSEL_IN3		EVENTOUT
PD12	USART2_RTS	TIMER3_CH0	EXMC_A17						EVENTOUT
PD13	TIMER3_CH1	EXMC_A18							EVENTOUT
PD14	TIMER3_CH2	EXMC_D0							EVENTOUT
PD15	TIMER3_CH3	EXMC_D1	CTC_SYNC						EVENTOUT

Table 2-13. Port E alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8
PE0	TIMER3_ETI	EXMC_NBL0					TRGSEL_IN7		EVENTOUT
PE1	EXMC_NBL1								EVENTOUT
PE2		EXMC_A23							EVENTOUT
PE3		EXMC_A19		TIMER15_BRKIN					EVENTOUT
PE4		EXMC_A20		TIMER15_MCH0					EVENTOUT
PE5		EXMC_A21		TIMER15_CH0					EVENTOUT
PE6		EXMC_A22		TIMER15_CH1					EVENTOUT
PE7	TIMER0_ETI	EXMC_D4							EVENTOUT
PE8	TIMER0_CH0_ON	EXMC_D5							EVENTOUT
PE9	TIMER0_CH0	EXMC_D6							EVENTOUT
PE10	TIMER0_CH1_ON	EXMC_D7							EVENTOUT
PE11	TIMER0_CH1	EXMC_D8					TRGSEL_IN4		EVENTOUT
PE12	TIMER0_CH2_ON	EXMC_D9							EVENTOUT
PE13	TIMER0_CH2	EXMC_D10							EVENTOUT
PE14	TIMER0_CH3	EXMC_D11			TIMER0_CH2BRKIN				EVENTOUT
PE15	TIMER0_BRKIN	EXMC_D12							EVENTOUT

3. Functional description

3.1. Arm® Cortex®-M33 core

The Cortex®-M33 processor is a 32-bit processor that possesses low interrupt latency and low-cost debug. The characteristics of integrated and advanced make the Cortex®-M33 processor suitable for market products that require microcontrollers with high performance and low power consumption. The Cortex®-M33 processor is based on the Armv8 architecture and supports a powerful and scalable instruction set including general data processing I/O control tasks, advanced data processing bit field manipulations and DSP. Some system peripherals listed below are also provided by Cortex®-M33:

- Internal Bus Matrix connected with Code bus, System bus, and Private Peripheral Bus (PPB) and debug accesses.
- Nested Vectored Interrupt Controller (NVIC).
- Breakpoint Unit (BPU).
- Data Watchpoint and Trace (DWT).
- Instrumentation Trace Macrocell (ITM).
- Serial Wire JTAG Debug Port (SWJ-DP).
- Trace Port Interface Unit (TPIU).
- Memory Protection Unit (MPU).
- Floating Point Unit (FPU).
- DSP Extension (DSP).
- Software Built-In Self Test (SBIST) controller

3.2. On-chip memory

- Up to 1024KB of main flash memory for instruction and data.
- No waiting time within maximum first 192K bytes when CPU executes instructions. A long delay when CPU fetches the instructions out of the range.
- 16B option bytes block for user application requirements.
- 64Byte OTP0 (One-time program) block used for user data storage.
- 128K byte OTP1 used for BOOT entry or user data storage.
- 256Byte OTP2 with write lock and read lock, used for user data storage.
- 48Byte OTP3 used for critical security configuration.
- Up to 192KB of SRAM.
- Supports 7-bit ECC function when reading and writing first 32KB SRAM.

The GD32F505xx has up to 1024KB of main flash memory for instruction and data. The flash memory consists of 1024KB main flash organized into 384 pages. The flash page size is 2KB for bank0 and 4KB for bank1. Each page of main flash memory can be erased individually. *Table 2-2. GD32F505xx memory map* shows the memory map of the GD32F505xx series of devices, including Flash, SRAM, peripheral, and other pre-defined regions.

3.3. Clock, reset and supply management

- External 4 to 40 MHz crystal oscillator.
- Internal 8 MHz RC oscillator.
- Internal 48 MHz RC oscillator.
- Internal 40 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator.
- Integrated system clock PLL.
- 2.6V to 3.6V application supply and I/Os.
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), low voltage detector (LVD), VAVD (V_{DDA} voltage detector), VUVD (V_{CORE} Under Voltage Detector), VOVD (V_{CORE} Over Voltage Detector), VBAT for Backup domain.

The Clock Control Unit (CCTL) provides a range of oscillator and clock functions. These include internal RC oscillator and external crystal oscillator, high speed and low speed two types. The frequency of AHB, APB2 and the APB1 domains can be configured by each prescaler. The maximum frequency of the AHB, APB2 and APB1 domains is 280 / 280 / 140MHz, the maximum frequency of the system clock can be up to 280 MHz. See ***Figure 2-8. GD32F505xx clock tree*** for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components except for the SW-DP controller and the Backup domain. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from 2.40V and down to 2.35V. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- V_{DD} range: 2.6V to 3.6V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}: 0V.
- V_{DDA} range: 2.6V to 3.6V, external analog power supplies for ADC, reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} range: 2.6V to 3.6V, power supply for RTC unit, LXTAL oscillator, BPOR and BREG, and three BKP PADs, including PC13 to PC15.

Note: When the system clock frequency reaches or exceeds 240 MHz, the V_{DD} must be 3.0V or higher.

3.4. Boot modes

GD32F505xx supports three BOOT modes, including:

- Boot from main Flash memory (default).
- Boot from system memory.

- Boot from on-chip SRAM.
- Boot from OTP1.

The GD32F50x devices provide four kinds of boot sources. The boot mode is influenced by Security Protection, NBTSB and BTFOSEL bits in OTP3, and Boot pins. The details are shown in the following table *Table 2-14. Boot modes*.

The value on the BOOT0 and BOOT1 pins is latched on the 4th rising edge of CK_SYS after a reset. It is up to the user to set the BOOT0 and BOOT1 pins after a power-on reset or a system reset to select the required boot source. Once the two pins have been sampled, they are free and can be used for other purposes.

Table 2-14. Boot modes

Security protection	OTP3		Boot pin		BOOT_MODE[2:0]	Boot Select
	NBTSB	BTFOSEL	BOOT0	BOOT1		
No protection/ Protection level low	0	x	1	1	011	SRAM
No protection/ Protection level low	0	x	1	0	001	BootLoader
No protection/ Protection level low	0	0	0	x	000	Main Flash
No protection/ Protection level low	0	1	0	x	101	OTP1
x	1	0	x	x	000	Main Flash
x	1	1	x	x	101	OTP1
Protection level high	x	0	x	x	000	Main Flash
Protection level high	x	1	x	x	101	OTP1

The boot loader is located in non-user system memory. It is used to reprogram the Flash memory by using USART0 (PA9 and PA10), USART1 (PD5 and PD6 for GD32F505Vx or PA2 and PA3 for GD32F505Rx and GD32F505Cx), USBFS (PA11 PA12) in device mode. It also can be used to transfer and update the Flash memory code, the data and the vector table sections.

To ensure system reliability and stability, it is recommended not to connect peripherals that may generate interference signals (such as sensor outputs, watchdog chips, buttons, etc.) to the above-mentioned pins during the hardware design stage, in order to avoid affecting the normal function of the Bootloader and causing abnormal outputs to the connected peripherals.

Note: After the MCU starts from the system memory, the USART interface and the USB

interface are in the detection state. Therefore, the unused USART RX pins (PA10, PD6, PA3) need to be maintained at a stable logic level. Unused USB DP pin (PA12) is prohibited from being pulled down and recommended to pull up. This design is made to prevent false triggering during the connection process.

3.5. Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are sleep mode, deep-sleep mode and standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep mode**

  In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt / event can wake up the system.

- **Deep-sleep mode**

  In deep-sleep mode, all clocks in the V_{CORE} domain are off, and all of the high speed crystal oscillator (IRC8M, IRC48M, HXTAL) and PLL are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the 16 external lines, the RTC alarm, the LVD output, CMP wakeup and USBFS wakeup. When exiting the deep-sleep mode, the IRC8M is selected as the system clock.

- **Standby mode**

  In standby mode, the whole V_{CORE} domain is power off, the LDO is shut down, and all of IRC8M, IRC48M, HXTAL and PLL are disabled. The contents of SRAM and registers (except backup registers) are lost. There are four wakeup sources for the standby mode, including the external reset from NRST pin, the RTC alarm, the FWDGT reset, and the rising edge on WKUP pin.

3.6. Trigger selection controller (TRIGSEL)

- Support up to 74 trigger input signals.
- Each peripheral has its corresponding register to select trigger input signal.
- TRIGSEL register can be configured up to 3 outputs to peripheral.
- Trigger input source could be external input signal or output of peripheral.
- Trigger selection output could be for external output or peripheral input.

The trigger selection controller (TRIGSEL) allows software to select the trigger input signal for various peripherals. TRIGSEL provides a flexible mechanism for a peripheral to select different trigger inputs. With TRIGSEL, there are up to 3 trigger selection outputs could be selected for each peripheral. And every output could be selected from different trigger input signal.

3.7. General-purpose and alternate-function I/Os (GPIO and AFIO)

- Up to 80 general purpose I/O pins (GPIO), all mappable on 16 external interrupt lines.
- Each pin weak pull-up / pull-down function.
- Output push-pull / open drain enable control.
- Analog input / output configuration.
- Alternate function input / output configuration.

GD32F505xx is up to 80 general purpose I/O pins (GPIO), named PA0~PA15, PB0~PB15, PC0~PC15, PD0~PD15, PE0~PE15 for the device to implement logic input/output functions. Each GPIO port has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt / Event Controller Unit (EXTI).

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), input, peripheral alternate function or analog mode. Each GPIO pin can be configured as pull-up, pull-down or floating. All GPIOs are high-current capable except for analog mode.

3.8. Direct memory access controller (DMA)

- 12 channels (7 for DMA0 and 5 for DMA1) and each channel are configurable.
- Support independent 8, 16, 32-bit memory and peripheral transfer.
- Support independent fixed and increasing address generation algorithm of memory and peripheral.
- Peripherals supported: Timers, ADC, DAC, SPI, I2S, I2C, USART, UART, CAU, HAU.

The direct memory access (DMA) controller provides a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory.

There are 12 channels in the DMA controller (7 for DMA0 and 7 for DMA1). Each channel is dedicated to manage memory access requests from one or more peripherals. An arbiter is implemented inside to handle the priority among DMA requests.

3.9. DMA request multiplexer (DMAMUX)

- 12 channels for DMAMUX request multiplexer.
- 4 channels for DMAMUX request generator.
- Support 20 trigger inputs and 20 synchronization inputs.

DMAMUX is a transmission scheduler for DMA requests. The DMAMUX request multiplexer is used for routing a DMA request line between the peripherals / generated DMA request (from the DMAMUX request generator) and the DMA controller. Each DMAMUX request multiplexer channel selects a unique DMA request line, unconditionally or synchronously with

events from its DMAMUX synchronization inputs. The DMA request is pending until it is served by the DMA controller which generates a DMA acknowledge signal (the DMA request signal is de-asserted).

3.10. CRC calculation unit (CRC)

- Supports 8 / 16 / 32 bit data input.
- For 8 / 16 / 32 bit input data length, the calculation cycles are 1 / 2 / 4 AHB clock cycles.
- User configurable polynomial value and size.
- Free 8-bit register is unrelated to calculation and can be used for any other goals by any other peripheral devices.

A cyclic redundancy check (CRC) is an error-detecting code commonly used in digital networks and storage devices to detect accidental changes to raw data. The CRC calculation unit can be used to calculate 7 / 8 / 16 / 32 bit CRC code within user configurable polynomial.

3.11. True random number generator (TRNG)

- About 40 periods of TRNG_CLK are needed between two consecutive random numbers.
- 32-bit random value seed is generated from analog noise, so the random number is a true random number.

The true random number generator (TRNG) module can generate a 32-bit random value by using continuous analog noise.

3.12. Hash Acceleration Unit (HAU)

- 32-bit AHB slave peripheral.
- High performance of computation of hash algorithms.
- Little-endian data representation.
- Multiple data types are supported, including no swapping, half-word swapping, byte swapping, and bit swapping with 32-bit data words.
- Automatic data padding to fill the 512-bit message block for digest computation.
- DMA transfer is supported.

The hash acceleration unit is used for information security. The secure hash algorithm (SHA-256) is supported for various applications. The digest will be computed and the length is 256 bits for a message up to (2^{64} - 1) bits computed by SHA-256 algorithm respectively.

3.13. Cryptographic Acceleration Unit (CAU)

- AES encryption/decryption algorithm is supported.
- DMA transfer for incoming and outgoing data is supported.

- Supports the ECB algorithm.
- Supports 128-bit, 192-bit and 256-bit keys.
- 8*32-bit input and output FIFO.
- Multiple data types are supported, including No swapping, Half-word swapping Byte swapping and Bit swapping.
- Data can be transferred by DMA, CPU during interrupts, or without both of them.

The cryptographic acceleration unit (CAU) is used to encipher and decipher data with AES (128, 192, or 256) algorithm. AES algorithms with different key sizes are supported to perform data encryption and decryption in the CAU in multiple modes. The CAU is a 32-bit peripheral, DMA transfer is supported and data can be accessed in the input and output FIFO.

3.14. Analog to digital converter (ADC)

- 12-bit, 10-bit, 8-bit or 6-bit configurable resolution for ADC.
- Programmable sampling time.
- DMA support.
- Up to 3 analog watchdogs.
- Oversampling ratio arbitrarily adjustable from 2x to 256x.
- Temperature sensor.
- Input voltage range: VREFN to VREFP.
- Start-of-conversion can be initiated by software or TRIGSEL.

A 12-bit successive approximation analog-to-digital converter module ADC) is integrated on the MCU chip. ADC0 has 16 external channels, 2 internal channels (temperature sensor, V_{REFINT} inputs channel), ADC1 has 18 external channels, ADC2 has 17 external channels. Analog watchdog allows the application to detect if the input voltages exceed the user-set high and low thresholds. All ADC sampling channels support a variety of operation modes. After sampling and conversion, the conversion results can be stored in the corresponding data registers according to the least significant bit (LSB) alignment or the most significant bit (MSB) alignment. An on-chip hardware oversample scheme improves performances and reduces the computational burden of MCU.

To ensure a high accuracy on ADC, the ADC independent external reference voltage should be connected to VREFP/VREFN pins. According to the different packages, VREFP pin can be connected to VDDA pin, or external reference voltage, VREFN pin must be connected to VSSA pin. For packages without VREFP and VREFN pins, V_{REFP} is internally connected to V_{DDA}, and V_{REFN} is internally connected to V_{SSA}.

3.15. Digital to analog converter (DAC)

- 8-bit or 12-bit resolution.
- Left or right data alignment.
- DMA capability for each channel.

- Conversion update synchronously.
- Conversion triggered by external triggers.
- Configurable internal buffer.
- Extern voltage reference, VREFP.
- Noise wave generation (LFSR noise mode and triangle noise mode).

The Digital-to-analog converter converts 12-bit digital data to a voltage on the external pins. The digital data can be configured to 8-bit or 12-bit mode, left-aligned or right-aligned mode. DMA can be used to update the digital data on external triggers. The output voltage can be optionally buffered for higher drive capability.

3.16. Comparator (CMP)

- Rail-to-rail comparators.
- Configurable hysteresis.
- Each comparator has configurable analog input source.
- Outputs with blanking source.
- Outputs to I/O.
- Outputs to timers for triggering.
- Outputs to EXTI.
- Outputs to NVIC.
- Outputs to TRIGSEL.

The general purpose CMP can work either standalone (all terminal are available on I/Os) or together with the timers.

It can be used to wake up the MCU from low-power mode by an analog signal, provide a trigger source when an analog signal is in a certain condition, achieve some current control by working together with a PWM output of a timer and the DAC. It blanking function can be used for false overcurrent detection in motor control applications.

3.17. Real time clock (RTC)

- 32-bit up-counter with a programmable 20-bit prescaler
- Alarm function

The real time clock is an independent timer which provides a set of continuously running counters in backup registers to provide a real calendar function, and provides an alarm interrupt. The RTC features a 32-bit programmable counter for long-term measurement using the compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock of HXTAL clock divided by 128, or LXTAL oscillator clock, or IRC40K oscillator clock, or AHB clock divided by 10.

3.18. Timers and PWM generation

- Two 16-bit Advanced timer (TIMER0, TIMER7), three 16-bit General-L0 timers (TIMER2, TIMER3, TIMER4), one 32-bit General-L0 timer (TIMER1), two 16-bit General-L3 timer (TIMER15, TIMER16), two 16-bit Basic timer (TIMER5 & TIMER6).
- Up to 4 independent channels of PWM, output compare or input capture for each general timer and external trigger input.
- 16-bit, motor control PWM advanced timer with programmable dead-time generation for output match.
- Decoder interface controller with two inputs using quadrature decoder and decoder modes.
- 24-bit SysTick timer down counter.
- 2 watchdog timers (free watchdog timer and window watchdog timer).

The advanced timer (TIMER0, TIMER7) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general timer. The 4 independent channels can be used for input capture, output compare, PWM generation (edge-aligned or center-aligned counting modes) and single pulse mode output. It can be synchronized with external signals or to interconnect with other general timers together which have the same architecture and features.

The general level 0 timer, can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TIMER1 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TIMER2/3/4 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. The general level 0 timer also supports an encoder interface with two inputs using quadrature decoder mode and decoder mode.

The general level3 timer module (TIMER15/TIMER16) is a three-channel timer that supports both input capture and output compare. They can generate PWM signals to control motor or be used for power management applications. The general level3 timer has a 16-bit counter that can be used as an unsigned counter.

The basic timer module (TIMER5/6) has a 16-bit counter that can be used as an unsigned counter. The basic timer TRGO is connected to DAC by TRIGSEL module.

The GD32F505xx has two watchdog peripherals, free watchdog timer and window watchdog timer. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-bit prescaler. It is clocked from an independent 40 KHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog timer is based on a 7-bit down counter that can be set as free-running.

It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wakeup interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter.
- Auto reload capability.
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source.

3.19. Universal synchronous/asynchronous receiver transmitter (USART/UART)

- Maximum speed up to 35 MBits/s for USART0 when the clock frequency is 280 MHz and oversampling is by 8.
- Maximum speed up to 17.5 MBits/s for USART1, USART2, UART3 and UART4 when the clock frequency is 140 MHz and oversampling is by 8.
- Supports both asynchronous and clocked synchronous serial communication modes.
- IrDA support.
- LIN break generation and detection.
- ISO 7816-3 compliant smartcard interface.

The USART (USART0, USART1, USART2) and UART (UART3, UART4) are used to transfer data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART/UART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART/UART transmitter and receiver.

3.20. Inter-integrated circuit (I2C)

- Up to four I2C bus interfaces can support both master and slave mode with a frequency up to 1 MHz (Fast mode plus).
- Provide arbitration function, optional PEC (packet error checking) generation and checking.
- Supports 7-bit and 10-bit addressing mode and general call addressing mode.
- SMBus 3.0 and PMBus 1.3 compatible.

The I2C (inter-integrated circuit) module provides an I2C interface which is an industry standard two-line serial interface for MCU to communicate with external I2C interface. I2C bus uses two serial lines: a serial data line, SDA, and a serial clock line, SCL. The I2C interface implements standard I2C protocol with standard mode (up to 100KHz), fast mode

(up to 400KHz) and fast mode plus (up to 1MHz) as well as CRC calculation and checking, SMBus (system management bus), and PMBus (power management bus).

3.21. Controller area network (CAN)

- Supports CAN protocols version 2.0A, B.
- Supports CAN FD Frame with up to 64 data bytes (ISO11898-1 and Bosch CAN FD specification V1.0).
- Baud rates up to 1 Mbit/s when classical frames and 8 Mbit/s when FD frames.
- Supports transmitter delay compensation.
- Supports the time-triggered communication.
- Interrupt enable and clear.

CAN bus (Controller Area Network) is a bus standard designed to allow microcontrollers and devices to communicate with each other without a host computer.

As CAN network interface, basic extended CAN supports the CAN protocols version 2.0A, 2.0B, ISO11898-1:2015 and BOSCH CAN FD specification. The CAN interface automatically handles the transmission and the reception of CAN frames. The CAN provides 28 scalable/configurable identifier filter banks. The filters are used for selecting the input message as software requirement and otherwise discarding the message. Three transmit mailboxes are provided to the software for transfer messages. The transmission scheduler decides which mailbox will be transmitted firstly. Three complete messages can be stored in every FIFO. The FIFOs are managed completely by hardware. Two receiving FIFOs are used by hardware to store the incoming messages. In addition, the CAN controller provides all hardware functions, which supports the time-triggered communication option, in safety-critical applications.

3.22. Serial peripheral interface (SPI)

- Master or slave operation with full-duplex or simplex mode.
- Separate transmit and receive buffer, 16 bits wide.
- Data frame size can be 8 or 16 bits.
- Hardware CRC calculation, transmission and checking.
- SPI TI mode supported.
- SPI NSS pulse mode supported.
- Quad-SPI configuration available in master mode (only in SPI0).

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). All SPIs can be served by the DMA controller. The serial peripheral interface (SPI) provides a SPI protocol of data transmission and reception function in master or slave mode. Both full-duplex and simplex communication modes are supported, with hardware CRC calculation and checking. Quad-SPI master mode is also supported in SPI0.

3.23. Inter-IC sound (I2S)

- Master or slave operation with transmission or reception mode
- Four I2S standards supported: Philips, MSB justified, LSB justified and PCM standard
- Data length can be 16 bits, 24 bits or 32 bits
- Channel length can be 16 bits or 32 bits
- Transmission and reception using a 16 bits wide buffer
- Audio sample frequency can be 8 kHz to 192 kHz using I2S clock divider
- Programmable idle state clock polarity
- Master clock (MCK) can be output
- Transmission and reception using DMA

The inter-IC sound (I2S) supports four audio standards: I2S Philips standard, MSB justified standard, LSB justified standard, and PCM standard. I2S works at either master or slave mode for transmission and reception. The audio sampling frequencies from 8 KHz to 192 KHz is supported.

3.24. External memory controller (EXMC)

- Supported external memory: PSRAM, NOR Flash and 8-bit or 16-bit NAND Flash.
- Each bank has its own chip-select signal which can be configured independently.
- 8 or 16 bits bus width.
- Embedded ECC hardware for NAND Flash access.

The external memory controller EXMC, is used as a translator for MCU to access a variety of external memory. By configuring the related registers, it can automatically convert AMBA memory access protocol into a specific memory access protocol, such as PSRAM, NOR Flash, NAND Flash. Users can also adjust the timing parameters in the configuration registers to improve memory access efficiency. EXMC access space is divided into multiple banks; each bank is assigned to access a specific memory type with flexible parameter configuration as defined in the control registers.

3.25. Universal serial bus full-speed interface (USBFS)

- Supports USB 2.0 host mode at Full-Speed(12Mb/s) or Low-Speed(1.5Mb/s)
- Supports USB 2.0 device mode at Full-Speed(12Mb/s)

USB Full-Speed (USBFS) controller provides a USB-connection solution for portable devices. USBFS supports host and device modes. USBFS contains a full-speed internal USB PHY and external PHY chip is not contained. USBFS supports all the four types of transfer (control, bulk, Interrupt and isochronous) which defined in USB 2.0 protocol.

3.26. Debug mode

- Serial wire JTAG debug port (SWJ-DP).

The GD32F505xx series provide a large variety of debug, trace and test features. They are implemented with a standard configuration of the Arm® CoreSight™ module together with a daisy chained standard TAP controller. Debug and trace functions are integrated into the Arm® Cortex®-M33. The debug system supports serial wire debug (SWD) and trace functions in addition to standard JTAG debug.

3.27. Package and operation temperature

- LQFP100 (GD32F505Vx), LQFP64 (GD32F505Rx), QFN64 (GD32F505Rx), BGA64 (GD32F505Rx), LQFP48 (GD32F505Cx) and QFN48 (GD32F505Cx).
- Operation temperature range: -40°C to +105°C (industrial level).

4. Electrical characteristics

4.1. Parameter introduction

- Parameter conditions: Unless otherwise specified, all values given for V_{DD} = V_{DDA} = 3.3 V, V_{CORE} = 1.2 V, T_A = 25°C, and all voltages are referenced to Vss.
- Value guaranteed by design, not 100% tested in production indicates that the value is derived from design or simulation and/or process characteristics.
- Value guaranteed by characterization, not 100% tested in production indicates that the value is derived from comprehensive evaluation after random test.
- Value guaranteed by sample, not 100% tested in production indicates that the value is derived from testing parameters with a small sample size.
- Guaranteed by characterization, the minimum and maximum values refer to random tests and represent the mean value plus or minus three times the standard deviation (mean +/-3σ).
- If the value is not specially indicated, it means the value guaranteed by 100% tested in production.

See the following table for some abbreviation terms and their descriptions in this chapter.

Table 4-1. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
CAN	Controller Area Network
DAC	Digital-to-Analog Converter
DMA	Direct Memory Access
GPIO	General Purpose Input/Output
JTAG	Joint Test Action Group
PLL	Phase-Locked Loop
SPI	Serial Peripheral Interface

4.2. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-2. Absolute maximum ratings(1)

Symbol	Description	Min	Max	Unit
V_{DD}	External digital supply voltage(2)	V_{SS} - 0.3	V_{SS} + 4	V
V_{DDA}	External analog supply voltage(3)	V_{SSA} - 0.3	V_{SSA} + 4	V
V_{BAT}	External battery supply voltage	V_{SS} - 0.3	V_{SS} + 4	V
V_{IN}	Input voltage on 5V tolerant pin(4)	V_{SS} - 0.3	V_{DD} + 4	V
	Input voltage on other I/O	V_{SS} - 0.3	V_{DD} + 0.3	V
$\|\Delta V_{DDx}\|$	Variations between VDD power supply pins	-	50	mV
$\|\Delta V_{SSx}\|$	Variations between VSS ground pins	-	50	mV
I_{IO}	Maximum current for each GPIO pin	-	+/-25	mA
$\sum I_{IO}$	Maximum current sunk/sourced by all GPIO pin	-	+/-100	
I_{DD}	Maximum current into each VDD pin	-	100	
I_{SS}	Maximum current into each VSS pin	-	100	
$\sum I_{DD}$	Total current into all VDD pins	-	200	
$\sum I_{SS}$	Total current into all VSS pins	-	200	
I_{INJ}	Injected current on each GPIO pin(5)	-	-5/0	
$\sum I_{INJ}$	Total injected current on all GPIO pins(6)	-	+/-25	
T_{STG}	Storage temperature	-65	150	°C
T_J	Maximum junction temperature	-	125	°C

(1) Value guaranteed by design, not 100% tested in production.

(2) All power supply pins must be connected to the correct voltage range.

(3) It is recommended that VDD and VDDA are powered by the same source. The maximum difference between VDD and VDDA does not exceed 300 mV during power-up and operation.

(4) V_{IN} maximum value cannot exceed 5.5 V.

(5) I_{INJ} must never be exceeded. Negative injection on any analog input pins disturbs the analog performance of the device.

(6) When several inputs are submitted to a current injection, the maximum ΣI_{INJ} is the absolute sum of the positive and negative injected currents (instantaneous values).

4.3. General operating conditions

The parameters are applicable to the full range of ambient temperature and voltage.

Table 4-3. General operating conditions(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Digital supply voltage	—	2.6	3.3	3.6	V
V_{DDA}	Analog supply voltage	Same as V_{DD}	2.6	3.3	3.6	
V_{BAT}(2)	Battery supply voltage	—	1.8	3.3	3.6	
V_{CORE}	Core logic supply voltage powered by internal voltage regulator	LDOVS[2:0] =111	—	1.20	—	V
		LDOVS[2:0] =110	—	1.15	—	
		LDOVS[2:0] =101	—	1.10	—	
f_{HCLK}(3)	AHB clock frequency	V_{CORE} = 1.2V	—	—	280	MHz
		V_{CORE} = 1.15V	—	—	200	
		V_{CORE} = 1.1V	—	—	200	
f_{APB1}	APB1 clock frequency	V_{CORE} = 1.2V	—	—	140	
		V_{CORE} = 1.15V	—	—	100	
		V_{CORE} = 1.1V	—	—	100	
f_{APB2}	APB2 clock frequency	V_{CORE} = 1.2V	—	—	280	
		V_{CORE} = 1.15V	—	—	200	
		V_{CORE} = 1.1V	—	—	200	
P_D(4)	Power dissipation at T_A = 105°C of LQFP100	—	—	—	359	mW
	Power dissipation at T_A = 105°C of BGA64	—	—	—	255	
	Power dissipation at T_A = 105°C of LQFP64	—	—	—	413	
	Power dissipation at T_A = 105°C of QFN64	—	—	—	645	
	Power dissipation at T_A = 105°C of LQFP48	—	—	—	361	
	Power dissipation at T_A = 105°C of QFN48	—	—	—	595	
T_A	Operating temperature range	—	-40	—	105	°C
T_J(5)	Junction temperature	—	-40	—	125	°C

(1) Value guaranteed by design, not 100% tested in production.

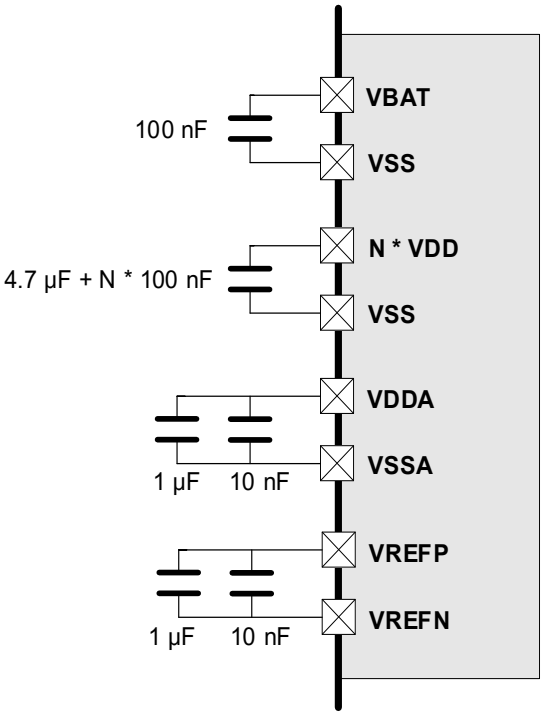
(2) In the application which V_{BAT} supply the backup domains, if the V_{BAT} voltage drops below the minimum value, when V_{DD} is powered on again, it is necessary to refresh the registers of backup domains and enable LXTAL again.

(3) When the system clock frequency reaches or exceeds 240 MHz, the V_{DD} must be 3.0V or higher.

(4) If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.

(5) The device junction temperature must be kept below maximum T_J, otherwise it may cause permanent damage to the device.

Figure 4-1. Recommended power supply decoupling capacitors(1)(2)



(1) It is recommended to configure a 100nF capacitor for each VDD pin.

(2) The V_{REFP} and V_{REFN} pins are only available on no less than 100-pin packages, or else the V_{REFP} and V_{REFN} pins are not available and internally connected to V_{DDA} and V_{SSA} pins.

(3) All decoupling capacitors need to be as close as possible to the pins on the PCB board.

4.4. Power supply requirement characteristics

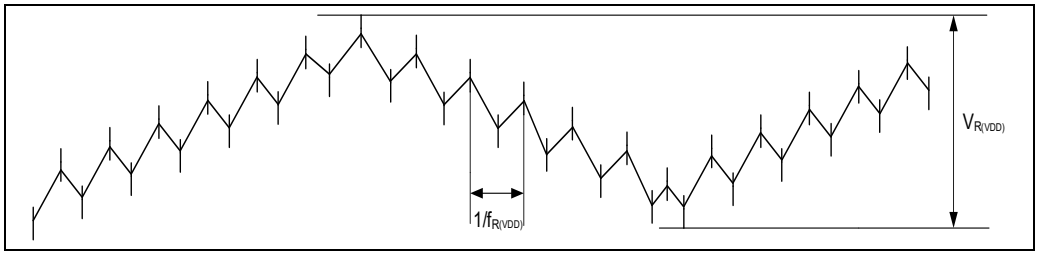
Table 4-4. Power supply requirement characteristics(1)

Symbol	Description	Conditions	Min	Max	Unit
t_{VDD}(1)	V_{DD}/V_{DDA} rise time rate	-	0	∞	µs/V
	V_{DD}/V_{DDA} fall time rate		20	∞	
$f_{R(VDD/VDDA)}$	Allowable ripple frequency	$V_{R(VDD/VDDA)}$ <= 0.2 V_{DD}/V_{DDA}	-	10	kHz
		$V_{R(VDD/VDDA)}$ <= 0.08 V_{DD}/V_{DDA}	-	0.1	MHz
		$V_{R(VDD/VDDA)}$ <= 0.06 V_{DD}/V_{DDA}	-	1	
$\Delta V_{DD}/V_{DDA}$ (2)	Allowable voltage change rising and falling gradient	When V_{DD}/V_{DDA} change exceeds V_{DD}/V_{DDA} +/- 10%	1	-	ms/V

(1) Value guaranteed by design, not 100% tested in production.

(2) The ripple voltage must meet the allowable ripple frequency $f_{R(VDD/VDDA)}$ within the range between the V_{DD}/V_{DDA} upper limit (3.6 V) and lower limit (2.6 V). When the V_{DD}/V_{DDA} change exceeds V_{DD}/V_{DDA} +/- 10%, the allowable voltage change rising and falling gradient $\Delta V_{DD}/V_{DDA}$ must be met.

Figure 4-2. Rise and fall gradient and ripple frequency characteristics



4.5. Start-up timings of Operating conditions

Table 4-5. Start-up timings of Operating conditions(1)(2)

Symbol	Description	Conditions	Min	Typ	Max	Unit
t_{ST}(1)(2)	Start-up time	NWLD_CLK[1:0] = 00 Code area in FLASH = 192 KB	6.9	7.2	7.5	ms
		NWLD_CLK[1:0] = 00 Code area in FLASH = 128 KB	6.1	6.3	6.5	
		NWLD_CLK[1:0] = 01 Code area in FLASH = 192 KB	8.5	8.8	9.1	
		NWLD_CLK[1:0] = 01 Code area in FLASH = 128 KB	6.8	7.1	7.4	
		NWLD_CLK[1:0] = 10 Code area in FLASH = 192 KB	10.2	10.6	11	
		NWLD_CLK[1:0] = 10 Code area in FLASH = 128 KB	8.1	8.4	8.7	
		NWLD_CLK[1:0] = 11 Code area in FLASH = 192 KB	109.6	113	116.4	
		NWLD_CLK[1:0] = 11 Code area in FLASH = 128 KB	76.1	78.5	80.9	

(1) Value guaranteed by design, not 100% tested in production.

(2) After power-up, the start-up time is the time between the rising edge of NRST high and the first I/O instruction conversion in SystemInit function.

4.6. Wake-up times from power saving modes

Table 4-6. Wake-up times from power saving modes(3)

Symbol	Description	Conditions	Min	Typ	Max	Unit
t_{Sleep}(1)	Wakeup from Sleep mode	—	—	2.1	—	μs
$t_{Deep-sleep}$(1)	Wakeup from Deep-sleep mode（LDO On）	—	—	3.8	—	μs
	Wakeup from Deep-sleep mode（LDO in low power mode）	—	—	3.8	—	μs
$t_{Standby}$(2)	Wakeup from Standby mode	NWLD_CLK[1:0] = 00 Code area in FLASH = 192 KB	6.9	7.2	7.5	ms
		NWLD_CLK[1:0] = 00 Code area in FLASH = 128 KB	6.1	6.3	6.5	
		NWLD_CLK[1:0] = 01 Code area in FLASH = 192 KB	8.5	8.8	9.1	
		NWLD_CLK[1:0] = 01 Code area in FLASH = 128 KB	6.8	7.1	7.4	
		NWLD_CLK[1:0] = 10 Code area in FLASH = 192 KB	10.2	10.6	11	
		NWLD_CLK[1:0] = 10 Code area in FLASH = 128 KB	8.1	8.4	8.7	
		NWLD_CLK[1:0] = 11 Code area in FLASH = 192 KB	109.6	113	116.4	
		NWLD_CLK[1:0] = 11 Code area in FLASH = 128 KB	76.1	78.5	80.9	

(1) Value guaranteed by sample, not 100% tested in production.

(2) Value guaranteed by design, not 100% tested in production.

(3) The wakeup time is measured from the wakeup event to the point at which the application code reads the first instruction under the below conditions: V_{DD} = V_{DDA} = 3.3 V, IRC8M = System clock = 8 MHz.

4.7. Power consumption

The power consumption is measured as described in ***Figure 4-3. Power consumption measurement diagram***. The current consumption values are derived from the tests

powered by V_{DD} = V_{DDA} except BKP_ONLY mode, while the current is I_{SUM}. In BKP_ONLY mode, the RTC unit and LXTAL oscillator are powered by the V_{BAT}, while the current is I_{BAT}. Unless otherwise stated, V_{DD} = V_{DDA} = 3.3 V is applied to supply pins in typical current consumption columns, and V_{DD} = V_{DDA} = $V_{DD(MAX)}$ is applied in maximum current consumption columns.

The MCU is configured under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- When the peripherals are enabled f_{APB1} = f_{APB2} / 2= f_{HCLK} / 2.

Figure 4-3. Power consumption measurement diagram

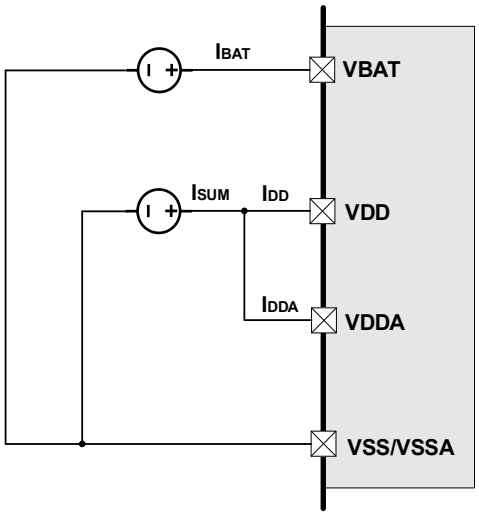


Table 4-7. Power consumption in Run mode(1) (2)

Symbol	Description	Conditions					Typ			Max			Unit
		Execute from	Peripherals	General	Vcore	f_{HCLK}	25°C	85°C	105°C	25°C	85°C	105°C	
I_{SUM}	Sum of supply current from VDD and VDDA (Run mode)	FLASH	All disabled	External Clock(HXTAL_ bypass = 8 MHz, PLL on, System clock = f_{HCLK})	1.2 V	280 MHz	28.09	30.01	30.95	30.66	33.78	36.28	mA
						252 MHz	25.75	27.64	28.58	27.64	31.37	33.83	
						220 MHz	22.57	24.41	25.32	24.23	28.07	30.52	
						168 MHz	17.41	19.16	20.04	18.72	22.78	25.15	
						108 MHz	11.45	13.12	13.96	12.23	16.73	19.01	
						72 MHz	7.88	9.50	10.31	8.61	13.12	15.31	
						36 MHz	4.31	5.87	6.66	4.95	9.51	11.59	
						8 MHz	1.34	2.88	3.67	1.94	6.48	8.51	
					1.1 V	200 MHz	19.14	20.59	21.35	20.60	23.30	25.24	
						168 MHz	16.18	17.59	18.34	17.41	20.30	22.16	
						108 MHz	10.64	12.00	12.71	11.42	14.78	16.55	
				Internal Clock(IRC 8M = 8 MHz, PLL on, System clock = f_{HCLK})	1.2 V	280 MHz	28.48	30.37	31.30	31.40	34.14	36.67	
						252 MHz	25.72	27.58	28.51	27.61	31.31	33.78	
						220 MHz	22.54	24.36	25.27	24.14	28.07	30.51	
						168 MHz	17.38	19.12	20.01	18.60	22.84	25.16	
						108 MHz	11.42	13.09	13.94	12.19	16.80	19.03	
						72 MHz	7.86	9.48	10.31	8.52	13.18	15.34	
						36 MHz	4.28	5.86	6.68	4.89	9.59	11.73	
						8 MHz	1.36	2.91	3.71	1.97	6.61	8.72	
					1.1 V	200 MHz	18.79	20.21	20.97	20.20	22.90	24.77	
						168 MHz	15.88	17.28	18.02	17.08	19.88	21.87	
						108 MHz	10.44	11.79	12.50	11.18	14.46	16.35	
			All enabled	External	1.2 V	280 MHz	56.37	58.62	59.67	59.23	63.29	65.94	

Symbol	Description	Conditions					Typ			Max			Unit
		Execute from	Peripherals	General	Vcore	f_{HCLK}	25°C	85°C	105°C	25°C	85°C	105°C	
				Clock(HXTAL_ bypass = 8 MHz, PLL on, System clock = f_{HCLK})		252 MHz	50.87	53.14	54.18	53.28	57.60	60.20	
						220 MHz	44.51	46.68	47.70	46.61	51.04	53.61	
					1.1 V	200 MHz	36.78	38.46	39.28	38.53	41.62	43.73	
				Internal Clock(IRC8M = 8 MHz, PLL on, System clock = f_{HCLK})	1.2 V	280 MHz	56.75	58.63	59.65	59.24	63.21	65.89	
						252 MHz	50.82	53.03	54.05	53.39	57.49	60.12	
						220 MHz	44.45	46.57	47.57	46.69	50.91	53.47	
					1.1 V	200 MHz	36.73	38.33	39.13	38.61	41.45	43.47	
		SRAM[5]	All disabled	External Clock(HXTAL_ bypass = 8 MHz, PLL on, System clock = f_{HCLK})	1.2 V	280 MHz	26.28	28.15	29.02	27.77	32.37	34.81	
						252 MHz	23.71	25.57	26.43	25.15	29.53	31.88	
						220 MHz	20.78	22.60	23.46	21.99	26.57	28.87	
						168 MHz	16.04	17.79	18.64	16.94	21.65	23.93	
						108 MHz	10.57	12.25	13.08	11.27	16.03	18.30	
						72 MHz	7.30	8.93	9.75	7.91	12.72	14.88	
						36 MHz	4.02	5.60	6.42	4.65	9.36	11.49	
						8 MHz	1.28	2.83	3.63	1.89	6.52	8.69	
					1.1 V	200 MHz	17.75	19.17	19.88	18.92	22.14	24.05	
						168 MHz	15.01	16.41	17.11	16.02	19.37	21.25	
						108 MHz	9.89	11.23	11.92	10.51	14.16	15.97	

Symbol	Description	Conditions					Typ			Max			Unit
		Execute from	Peripherals	General	Vcore	f_{HCLK}	25°C	85°C	105°C	25°C	85°C	105°C	
				Internal Clock(IRC 8M = 8 MHz, PLL on, System clock = f_{HCLK})	1.2 V	280 MHz	26.25	28.11	28.97	27.76	32.29	34.69	
						252 MHz	23.67	25.50	26.36	25.13	29.45	31.85	
						220 MHz	20.75	22.54	23.39	22.04	26.48	28.83	
						168 MHz	16.01	17.74	18.58	16.98	21.60	23.95	
						108 MHz	10.54	12.21	13.04	11.22	16.01	18.33	
						72 MHz	7.27	8.89	9.71	7.89	12.67	14.93	
						36 MHz	3.99	5.57	6.39	4.62	9.32	11.58	
						8 MHz	1.25	2.80	3.61	1.88	6.52	8.69	
					1.1 V	200 MHz	17.71	19.11	19.81	18.88	22.11	23.98	
						168 MHz	14.98	16.36	17.06	15.99	19.34	21.21	
						108 MHz	9.86	11.19	11.88	10.50	14.13	15.91	
			All enabled	External Clock(HXTAL_ bypass = 8 MHz, PLL on, System clock = f_{HCLK})	1.2 V	280 MHz	52.62	54.97	55.70	57.05	60.10	62.78	
						252 MHz	47.83	50.02	50.99	50.23	54.49	57.15	
						220 MHz	41.85	43.96	44.91	43.97	48.37	50.90	
					1.1 V	200 MHz	37.64	39.28	40.04	39.73	42.72	44.71	
				Internal Clock(IRC 8M = 8 MHz, PLL on, System	1.2 V	280 MHz	52.67	54.94	55.64	57.89	59.94	62.76	
						252 MHz	47.88	50.03	50.98	50.47	54.50	57.13	
						220 MHz	41.89	43.97	44.90	44.07	48.28	50.92	
					1.1 V	200 MHz	37.38	38.98	39.72	39.47	42.43	44.44	

Symbol	Description	Conditions					Typ			Max			Unit
		Execute from	Peripherals	General	Vcore	f_{HCLK}	25°C	85°C	105°C	25°C	85°C	105°C	
				clock = f_{HCLK})									

(1) During power consumption test, GPIO needs to be configure as Analog Input mode.

(2) Value guaranteed by characterization, not 100% tested in production.

Table 4-8. Power consumption in Run mode with different codes(1) (2)

Symbol	Description	Conditions				Typ	Unit	Typ	Unit
		Execute from	General	Vcore	Code				
I_{SUM}	Sum of supply current from VDD and VDDA (Run mode)	FLASH	HXTAL = 8 MHz, PLL on, System clock = 280 MHz, f_{HCLK} = 280 MHz, All peripherals disabled	1.2 V	Coremark	34.1	mA	122	µA /MHz
			HXTAL = 8 MHz, PLL on, System clock = 252 MHz, f_{HCLK} = 252 MHz, All peripherals disabled		Coremark	31		123	
			HXTAL = 8 MHz, PLL on, System clock = 220 MHz, f_{HCLK} = 220 MHz, All peripherals disabled		Coremark	27.9		127	
			HXTAL = 8 MHz, PLL on, System clock = 200 MHz, f_{HCLK} = 200 MHz, All peripherals disabled	1.1 V	Coremark	23.4		117	
		SRAM(3)	HXTAL = 8 MHz, PLL on, System clock = 280 MHz, f_{HCLK} = 280 MHz, All peripherals disabled	1.2 V	Coremark	32.7		117	

Symbol	Description	Conditions				Typ	Unit	Typ	Unit
		Execute from	General	Vcore	Code				
			HXTAL = 8 MHz, PLL on, System clock = 252 MHz, f_{HCLK} = 252 MHz, All peripherals disabled		Coremark	29.6		117	
			HXTAL = 8 MHz, PLL on, System clock = 220 MHz, f_{HCLK} = 220 MHz, All peripherals disabled		Coremark	27.4		125	
			HXTAL = 8 MHz, PLL on, System clock = 200 MHz, f_{HCLK} = 200 MHz, All peripherals disabled	1.1 V	Coremark	22.6		113	

(1) Value guaranteed by sample, not 100% tested in production.

(2) During power consumption test, GPIO needs to be configure as Analog Input mode.

(3) Code compiled with high optimization for space in SRAM.

Table 4-9. Power consumption in Sleep mode(1) (2)

Symbol	Description	Conditions				Typ			Max			Unit
		peripherals	General	Vcore	f_{HCLK}	25°C	85°C	105°C	25°C	85°C	105°C	
I_{SUM}	Sum of supply current from VDD and VDDA (Sleep mode)	All disabled	External Clock(HXTAL_ bypass = 8 MHz, PLL on, System clock = f_{HCLK}, CPU clock off)	1.2 V	280 MHz	10.26	11.73	12.60	10.64	14.01	15.97	mA
					252 MHz	9.05	10.65	11.45	9.64	12.92	14.61	
					220 MHz	7.98	9.56	10.36	8.54	11.81	13.49	
					168 MHz	6.26	7.80	8.59	6.77	10.00	11.67	
					108 MHz	4.27	5.78	6.57	4.73	7.91	9.60	
					72 MHz	3.08	4.59	5.37	3.52	6.68	8.34	
					36 MHz	1.89	3.38	4.16	2.30	5.44	7.09	
					8 MHz	0.86	2.33	3.11	1.24	4.36	6.02	
				1.1 V	200 MHz	6.81	8.07	8.74	7.24	9.79	11.12	
					168 MHz	5.22	6.47	7.13	5.57	8.09	9.43	
					108 MHz	3.59	4.81	8.47	3.91	6.40	7.75	

Symbol	Description	Conditions				Typ			Max			Unit
		peripherals	General	Vcore	f_{HCLK}	25°C	85°C	105°C	25°C	85°C	105°C	
			Internal Clock(IRC8M = 8 MHz, PLL on, System clock = f_{HCLK}, CPU clock off)	1.2 V	280 MHz	10.21	11.70	12.52	10.62	13.95	15.82	
					252 MHz	9.02	10.60	11.40	9.61	12.88	14.58	
					220 MHz	7.95	9.52	10.31	8.51	11.76	13.45	
					168 MHz	6.22	7.76	8.56	6.74	9.96	11.65	
					108 MHz	4.24	5.75	6.54	4.71	7.88	9.56	
					72 MHz	3.05	4.56	5.34	3.49	6.64	8.32	
					36 MHz	1.87	3.35	4.13	2.28	5.41	7.09	
					8 MHz	0.83	2.31	3.08	1.21	4.32	5.94	
				1.1 V	200 MHz	6.78	8.03	8.70	7.22	9.74	11.08	
					168 MHz	5.19	6.44	7.10	5.55	8.06	9.41	
					108 MHz	3.56	4.78	5.44	3.88	6.37	7.71	
		All enabled	External Clock(HXTAL_bypass = 8 MHz, PLL on, System clock = f_{HCLK}, CPU clock off)	1.2 V	280 MHz	40.37	42.34	43.22	42.01	45.33	47.17	
					252 MHz	36.56	38.54	39.43	37.90	41.26	43.12	
					220 MHz	32.01	33.92	34.80	33.18	36.54	38.39	
				1.1 V	200 MHz	26.85	28.35	29.08	27.81	30.32	31.74	
			Internal Clock(IRC8M = 8 MHz, PLL on, System clock = f_{HCLK}, CPU clock off)	1.2 V	280 MHz	40.31	42.29	43.16	41.20	45.32	47.15	
					252 MHz	36.51	38.45	39.33	37.86	41.21	42.98	
					220 MHz	31.96	33.83	34.70	33.16	36.50	38.29	
				1.1 V	200 MHz	26.80	28.25	28.96	27.77	30.21	31.64	

(1) During power consumption test, GPIO needs to be configure as Analog Input mode.

(2) Value guaranteed by characterization, not 100% tested in production.

Table 4-10. Power consumption in Deep-sleep mode(1) (2)

Symbol	Description	Conditions		Typ			Max			Unit
		General	V_{CORE}	25°C	85°C	105°C	25°C	85°C	105°C	
I_{SUM}	Sum of supply current from VDD and VDDA (Deep-sleep mode)	LDO in normal power and normal driver mode, IRC40K off, RTC off	1.2 V	240	1210	2200	480	2690	3870	µA
			1.1 V	200	1010	1820	370	2130	3080	
			0.95 V	170	780	1400	270	1520	2220	
		LDO in normal power and low driver mode, IRC40K off, RTC off	1.2 V	190	1150	2130	420	2620	3790	
			1.1 V	150	950	1760	320	2070	3020	
			0.95 V	120	730	1340	220	1470	2160	
		LDO in low power and normal driver mode, IRC40K off, RTC off	1.2 V	210	1180	2160	450	2650	3820	
			1.1 V	180	980	1790	350	2090	3060	
			0.95 V	140	760	1370	250	1490	2200	
		LDO in low power and low driver mode, IRC40K off, RTC off	1.2 V	160	1120	2100	390	2590	3770	
			1.1 V	120	930	1730	290	2040	2990	
			0.95 V	87.9	700	1310	190	1440	2130	

(1) During power consumption test, GPIO needs to be configure as Analog Input mode.

(2) Value guaranteed by characterization, not 100% tested in production.

Table 4-11. Power consumption in Standby mode(1)

Symbol	Description	Conditions		Typ			Max			Unit
		General	V_{DD}	25°C	85°C	105°C	25°C	85°C	105°C	
I_{SUM}	Sum of supply current from VDD and VDDA (Standby mode)	LXTAL off, IRC40K on, RTC on	2.6V	2.96	4.13	5.11	3.42	4.63	5.81	µA
			3.3V	3.7	5.43	6.71	4.24	5.99	7.56	
			3.6V	4.16	6.35	7.87	4.63	6.92	8.85	
		LXTAL off, IRC40K on, RTC off	2.6V	2.77	3.93	4.91	3.15	4.44	5.56	
			3.3V	3.44	5.16	6.44	3.92	5.68	7.19	
			3.6V	3.86	6.05	7.57	4.31	6.64	8.61	
		LXTAL off, IRC40K off, RTC off	2.6V	2.21	3.37	4.36	2.85	3.93	5.1	
			3.3V	2.78	4.52	5.81	3.25	4.99	6.71	

Symbol	Description	Conditions		Typ			Max			Unit
		General	V_{DD}	25°C	85°C	105°C	25°C	85°C	105°C	
			3.6V	3.16	5.37	6.89	3.6	6.04	7.82	

(1) Value guaranteed by characterization, not 100% tested in production.

Table 4-12. Power consumption in BKP_ONLY mode(1)

Symbol	Description	Conditions		Typ			Unit
		General	V_{BAT}	25°C	85°C	105°C	
I_{BAT}	LXTAL+RTC current from VBAT (BKP_ONLY mode)	VDD off, LXTAL on with external crystal, RTC on, LXTAL High driving	1.8V	1.7	2.1	2.3	µA
			2.6V	1.8	2.2	2.5	
			3.3V	1.9	2.4	2.7	
			3.6V	2.0	2.5	2.9	
		VDD off, LXTAL on with external crystal, RTC on, LXTAL Medium High driving	1.8V	1.3	1.6	1.8	
			2.6V	1.4	1.7	1.9	
			3.3V	1.5	1.8	2.2	
			3.6V	1.6	2.0	2.3	
		VDD off, LXTAL on with external crystal, RTC on, LXTAL Medium Low driving	1.8V	0.8	1.0	1.3	
			2.6V	0.9	1.2	1.4	
			3.3V	1.0	1.3	1.6	
			3.6V	1.1	1.5	1.8	
		VDD off, LXTAL on with external crystal, RTC on, LXTAL Low driving	1.8V	0.7	0.9	1.1	
			2.6V	0.8	1.0	1.2	
			3.3V	0.9	1.1	1.4	
			3.6V	1.0	1.3	1.6	

(1) Value guaranteed by sample, not 100% tested in production.

The current consumption of the on-chip peripherals is given in the following table. To avoid adding the CPU dynamic power consumption to the peripheral power consumption, the MCU needs to enter sleep mode to stop the CPU operation during current measurement. The MCU is configured under the following conditions:

· All I/O pins are in analog input mode

· The given value is in the table calculated by measuring the difference of the current consumptions:

-- The target peripheral is clocked on and enters sleep mode

-- All peripherals are clocked off and enter sleep mode

The power consumption of the digital part of the on-chip peripherals is given in the following table. The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

The values in the table are equal to the peripheral current divided by the clock frequency of the corresponding BUS.

Table 4-13. Peripheral current consumption characteristics(1)

Peripherials		Typical consumption	Unit
APB1	CTC	0.061	μA/MHz
	DAC	0.084	
	PMU	1.794	
	BKP	2.274	
	CMP	0.039	
	I2C1	0.463	
	I2C0	0.477	
	UART4	0.308	
	UART3	0.309	
	USART2	0.515	
	USART1	0.479	
	SPI2	0.413	
	SPI1	0.408	
	WWDGT	0.053	
	TIMER16	2.033	
	TIMER6	0.218	
	TIMER5	0.196	
	TIMER4	1.687	
	TIMER3	1.678	
	TIMER2	1.610	
	TIMER1	1.855	
APB2	TIMER15	4.655	
	SYSCFG	0.004	

Peripherials		Typical consumption	Unit
	TRIGSEL	0.346	
	CAN1	2.925	
	CAN0	3.120	
	USART0	2.108	
	TIMER7	8.744	
	SPI0	0.609	
	TIMER0	8.763	
	ADC2	1.008	
	ADC1	0.923	
	ADC0	0.956	
	GPIOE	0.752	
	GPIOD	0.757	
	GPIOC	0.729	
	GPIOB	0.766	
	GPIOA	0.722	
	AF	0.046	
AHB	FMC	10.152	
	SRAM	1.064	
	EXMC	2.582	
	USBFS	5.236	
	CRC	0.180	
	CAU	16.198	
	HAU	0.498	
	TRNG	0.295	
	DMA1	1.162	
	DMA0	1.454	
	DMAMUX	2.043	

(1) Value guaranteed by sample, not 100% tested in production.

4.8. EMC characteristics

System level ESD (Electrostatic discharge, according to IEC 61000-4-2) and EFT (Electrical Fast Transient/burst, according to IEC 61000-4-4) testing result is given in the ***Table 4-14. System level ESD and EFT characteristics***(1). System level ESD is for end-customer operation, it includes ESD field events on system level occur in an unprotected area (outside EPA). System level ESD protection necessary to satisfy higher ESD levels.

Table 4-14. System level ESD and EFT characteristics(1)

Symbol	Description	Conditions	Package	Class	Level
V_{ESD}	Contact / Air mode high voltage stressed on few special I/O pins	V_{DD}/ V_{DDA} = 3.3 V, T_J = 25 °C, f_{HCLK} = 280 MHz IEC 61000-4-2	LQFP100	CD 8KV AD 15KV	4A
V_{EFT}	Fast transient high voltage burst stressed on Power and GND	V_{DD} = 3.3 V, T_J = 25 °C, f_{HCLK} = 280 MHz IEC 61000-4-4	LQFP100	4KV	4A

(1) Value guaranteed by characterization, not 100% tested in production.

EMI (Electromagnetic Interference) emission test result is given in the ***Table 4-15. EMI characteristics***, The electromagnetic field emitted by the device are monitored while an application, executing EEMBC code, is running. The test is compliant with SAE J1752-3:2017 standard which specifies the test board and the pin loading.

Table 4-15. EMI characteristics(1)

Symbol	Description	Conditions	Package	Max vs. [f_{HXTAL}/f_{HCLK}] 8/280 MHz			Unit
				0.1-30MHz	30-130MHz	130MHz-1GHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_J = 25 °C, f_{HCLK} = 280 MHz, conforms to SAE J1752-3:2017	LQFP100	-5.95	9.81	9.48	dBµV

(1) Value guaranteed by characterization, not 100% tested in production.

Component level ESD include HBM (Human body model, according to ANSI/ESDA/JEDEC JS-001) and CDM (ANSI/ESDA/JEDEC JS-002), that ESD field events during manufacturing in an ESD protected area, such as PCB assembly/repair, IC assembly/test and Fab environment. The ESD protected area (EPA) has many measures, for instance ESD protective packaging, grounding person wrist strap to ground (or flooring/footwear), grounded work surface and ionizer.

Static latch-up (LU, according to JEDEC78) test is based on the two measurement methods, I/O current injection value (I-test) and power supply over-voltage value.

Table 4-14. Component level ESD and latch-up characteristics(1)

Symbol	Description	Conditions	Package	Max	Unit	Level
V_{HBM}	Human body model electrostatic discharge voltage (Any pin combination)	T_A = 25 °C; JS-001-2017	LQFP100	4000	V	3A
V_{CDM}	Charge device model electrostatic discharge voltage (All pins)	T_A = 25 °C; JS-002-2018	LQFP100	1000	V	C3
LU	I-test	T_A = 125 °C; JESD78	LQFP100	+/-200	mA	Class II.A
	V_{supply} over voltage			5.4	V	

(1) Value guaranteed by characterization, not 100% tested in production.

4.9. Power supply supervisor characteristics

Table 4-16. Power supply supervisor characteristics(1)

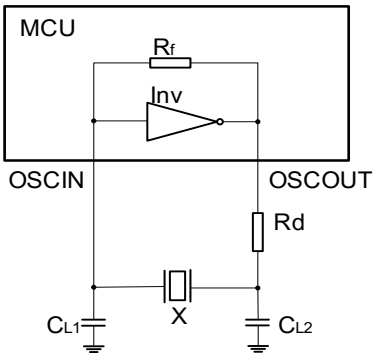
Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{LVD}	Low voltage Detector level selection	LVDT[2:0] = 000(rising edge)	—	2.14	—	V
		LVDT[2:0] = 000(falling edge)	—	2.04	—	
		LVDT[2:0] = 001(rising edge)	—	2.28	—	
		LVDT[2:0] = 001(falling edge)	—	2.18	—	
		LVDT[2:0] = 010(rising edge)	—	2.42	—	
		LVDT[2:0] = 010(falling edge)	—	2.32	—	
		LVDT[2:0] = 011(rising edge)	—	2.56	—	
		LVDT[2:0] = 011(falling edge)	—	2.46	—	
		LVDT[2:0] = 100(rising edge)	—	2.7	—	
		LVDT[2:0] = 100(falling edge)	—	2.6	—	
		LVDT[2:0] = 101(rising edge)	—	2.84	—	
		LVDT[2:0] = 101(falling edge)	—	2.74	—	
		LVDT[2:0] = 110(rising edge)	—	2.98	—	
		LVDT[2:0] = 110(falling edge)	—	2.88	—	
		LVDT[2:0] = 111(rising edge)	—	3.12	—	
		LVDT[2:0] = 111(falling edge)	—	3.02	—	
$V_{HYST(LVD)}$	LVD hystersis	—	—	100	—	mV
V_{POR}	Power on reset threshold	—	—	2.4	—	V
V_{PDR}	Power down reset threshold	PDRVS = 0	—	2.35	—	V
		PDRVS = 1	—	1.8	—	
$V_{HYST(POR_PDR)}$	Hysteresis of POR and PDR	PDRVS = 0	—	50	—	mV
		PDRVS = 1	—	600	—	
$t_{RST(TEMPO)}$	Reset temporization	—	—	2	—	ms
V_{AVD}	Analog voltage detector	VAVDVC[1:0] = 00(rising edge)	—	2.4	—	V

Symbol	Description	Conditions	Min	Typ	Max	Unit
	for V_{DDA} level selection	VAVDVC[1:0] = 00(falling edge)	—	2.3	—	
		VAVDVC[1:0] = 01(rising edge)	—	2.6	—	
		VAVDVC[1:0] = 01(falling edge)	—	2.5	—	
		VAVDVC[1:0] = 10(rising edge)	—	2.8	—	
		VAVDVC[1:0] = 10(falling edge)	—	2.7	—	
		VAVDVC[1:0] = 11(rising edge)	—	3.0	—	
		VAVDVC[1:0] = 11(falling edge)	—	2.9	—	
V_{hyst_AVD}	Hysteresis of V_{DDA} voltage detector	—	—	100	—	mV
V_{OVD}	Analog voltage detector for V_{CORE} over level selection	VOVDVC[1:0] = 00(rising edge)	—	1.25	—	V
		VOVDVC[1:0] = 00(falling edge)	—	1.225	—	
		VOVDVC[1:0] = 01(rising edge)	—	1.30	—	
		VOVDVC[1:0] = 01(falling edge)	—	1.275	—	
		VOVDVC[1:0] = 10(rising edge)	—	1.35	—	
		VOVDVC[1:0] = 10(falling edge)	—	1.325	—	
		VOVDVC[1:0] = 11(rising edge)	—	1.40	—	
		VOVDVC[1:0] = 11(falling edge)	—	1.375	—	
V_{hyst_OVD}	Hysteresis of V_{CORE} over voltage detector	—	—	25	—	mV
V_{UVD}	Analog voltage detector for V_{CORE} under level selection	VUVDVC[1:0] = 00(rising edge)	—	1.075	—	V
		VUVDVC[1:0] = 00(falling edge)	—	1.05	—	
		VUVDVC[1:0] = 01(rising edge)	—	0.975	—	
		VUVDVC[1:0] = 01(falling edge)	—	0.95	—	
		VUVDVC[1:0] = 1x(rising edge)	—	0.875	—	
		VUVDVC[1:0] = 1x(falling edge)	—	0.85	—	
V_{hyst_UVD}	Hysteresis of V_{CORE} voltage under detector	—	—	25	—	mV

(1) Value guaranteed by design, not 100% tested in production.

4.10. External clock characteristics

Figure 4-4. Internal structure diagram of OSCIN and OSCOUT pin



It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine which load capacitors will best tune their resonator/crystal to the microcontroller device for optimum start-up and operation over temperature/voltage extremes.

Table 4-17. High speed external clock (HXTAL) generated from a crystal/ceramic characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{HXTAL}	Crystal or ceramic frequency	2.6 V <= V_{DD} <= 3.6 V	4	32	40	MHz
R_F	Feedback resistor	-	-	400	-	kΩ
C_{HXTAL}(2)	Recommended matching capacitance on OSCIN and OSCOUT	-	-	20	30	pF
$Duty_{HXTAL}$	Crystal or ceramic duty cycle	-	30	-	70	%
g_m(3)	Oscillator transconductance	Startup	-	32	-	mA/V
$I_{DD(HXTAL)}$	Crystal or ceramic operating current	-	-	1.5	-	mA
$t_{ST(HXTAL)}$	Crystal or ceramic startup time	-	-	1	-	ms

(1) Value guaranteed by design, not 100% tested in production.

(2) $C_{HXTAL1} = C_{HXTAL2} = 2*(C_{LOAD} - C_S)$, For C_{HXTAL1} and C_{HXTAL2}, it is recommended matching capacitance on OSCIN and OSCOUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

(3) More details about g_m could be found in ***AN052 GD32 MCU Resonator-Based Clock Circuits***.

Table 4-18. High speed external clock characteristics (HXTAL in bypass mode) (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{HXTAL_ext}	External clock source or oscillator frequency	—	1	—	50	MHz
$V_{H(HXTAL)}$	OSCIN input pin high level voltage	—	0.7*V_{DD}	—	V_{DD}	V
$V_{L(HXTAL)}$	OSCIN input pin low level voltage		V_{SS}	—	0.3*V_{SS}	V
$t_{H/L(HXTAL)}$	OSCIN high or low time	—	5	—	—	ns
$t_{R/F(HXTAL)}$	OSCIN rise or fall time	—	—	—	10	ns

Symbol	Description	Conditions	Min	Typ	Max	Unit
C_{IN}	OSCIN input capacitance	—	—	5	—	pF
$Duty_{HXTAL}$	Duty cycle	—	30	—	70	%

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-5. High-speed external clock source AC timing diagram

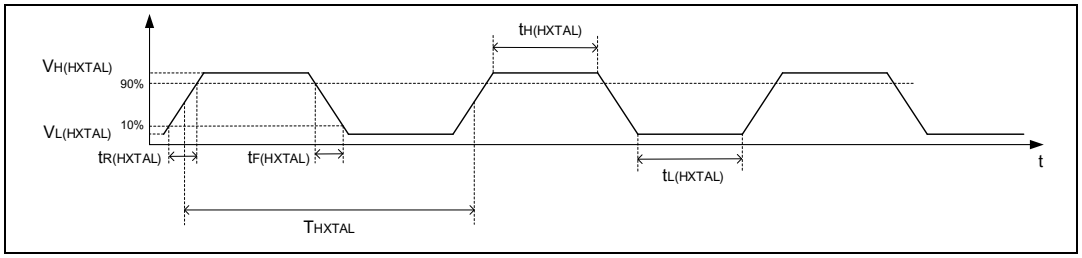


Table 4-19. Low speed external clock (LXTAL) generated from a crystal/ceramic characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{LXTAL}	Crystal or ceramic frequency	—	—	32.768	—	kHz
C_{LXTAL}(2)	Recommended matching capacitance on OSC32IN and OSC32OUT	—	—	15	—	pF
$Duty_{LXTA}$	Crystal or ceramic duty cycle	—	30	—	70	%
GM(4)	Oscillator transconductance	LXTALDRI[1:0] = 00	—	4.6	—	µA/V
		LXTALDRI[1:0] = 01	—	6.9	—	
		LXTALDRI[1:0] = 10	—	13	—	
		LXTALDRI[1:0] = 11	—	20	—	
$I_{DD(LXTAL)}$	Crystal or ceramic operating current	LXTALDRI[1:0] = 00	—	0.5	—	µA
		LXTALDRI[1:0] = 01	—	0.6	—	
		LXTALDRI[1:0] = 10	—	0.9	—	
		LXTALDRI[1:0] = 11	—	1.2	—	
$t_{ST(LXTAL)}$(3)	Crystal or ceramic startup time	V_{DD}=3.3V	—	2	—	s

(1) Value guaranteed by design, not 100% tested in production.

(2) C_{LXTAL1} = C_{LXTAL2} = 2*(C_{LOAD} - C_S), For C_{LXTAL1} and C_{LXTAL2}, it is recommended matching capacitance on OSC32IN and OSC32OUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

(3) $t_{ST(LXTAL)}$ is the startup time measured from the moment it is enabled (by software) to the 32.768 kHz oscillator stabilization flags is SET. This value varies significantly with the crystal manufacturer.

(4) More details about g_m could be found in ***AN052 GD32 MCU Resonator-Based Clock Circuits***.

Table 4-20. Low speed external user clock characteristics (LXTAL in bypass mode) (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{LXTAL_EXT}	External clock source or oscillator frequency	—	—	32.768	1000	kHz
$V_{H(LXTAL)}$	OSC32IN input pin high level	—	0.7*V_{DD}	—	V_{DD}	V

Symbol	Description	Conditions	Min	Typ	Max	Unit
	voltage					
$V_{L(LXTAL)}$	OSC32IN input pin low level voltage	—	V_{SS}	—	0.3*V_{SS}	
$t_{H/L(LXTAL)}$	OSC32IN high or low time	—	450	—	—	ns
$t_{R/F(LXTAL)}$	OSC32IN rise or fall time	—	—	—	50	
C_{IN}	OSC32IN input capacitance	—	—	5	—	pF
$Duty_{LXTAL}$	Duty cycle	—	30	—	70	%

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-6. Low-speed external clock source AC timing diagram

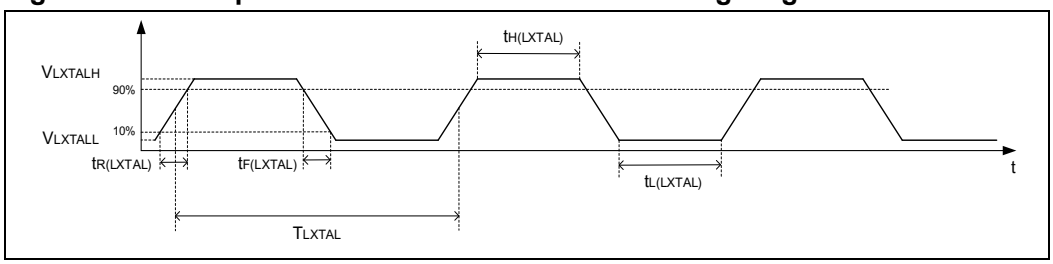


Figure 4-7. Recommended external OSCIN and OSCOUT pins circuit for crystal

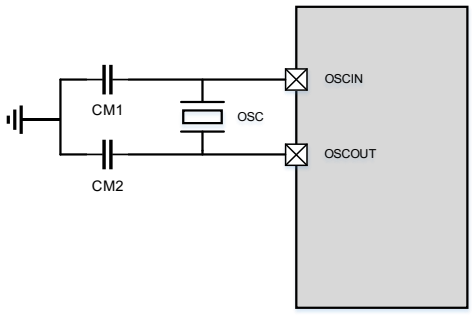
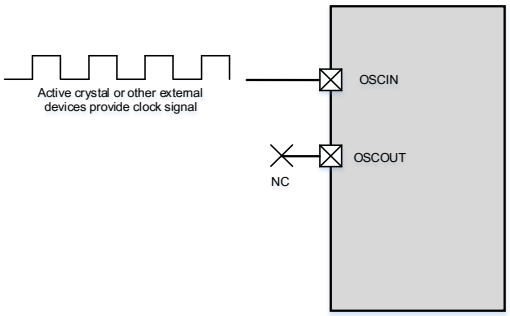


Figure 4-8. Recommended external OSCIN and OSCOUT pins circuit for oscillator



4.11. Internal clock characteristics

Table 4-21. High speed internal clock (IRC48M) characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{IRC48M}(1)	High Speed Internal Oscillator (IRC48M) frequency	—	—	48	—	MHz
$Drift_{IRC48M}$	IRC48M oscillator Frequency drift, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +105 °C	-2(2)	—	+2(2)	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C	-1.5	—	1.5	%
	IRC48M oscillator Frequency drift, User trimming step(1)	—	—	0.13	—	%
$Duty_{IRC48M}$(1)	IRC48M oscillator duty cycle	—	45	50	55	%
$I_{DDA(IRC48M)}$ (1)	IRC48M oscillator operating current	f_{IRC48M} = 48 MHz	—	342	450	μA
$t_{ST(IRC48M)}$ (1)	IRC48M oscillator startup time	f_{IRC48M} = 48 MHz	0.8	—	1.8	μs

(1) Value guaranteed by design, not 100% tested in production.
(2) Value guaranteed by characterization, not 100% tested in production.

Table 4-22. High speed internal clock (IRC8M) characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{IRC8M}(1)	High Speed Internal Oscillator (IRC8M) frequency	—	—	8	—	MHz
$Drift_{IRC8M}$	IRC8M oscillator Frequency drift, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +105 °C	-2 (2)	—	+2 (2)	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C	-1	—	1	%
	IRC8M oscillator Frequency drift, User trimming step(1)	—	—	0.5	—	%
$Duty_{IRC8M}$(1)	IRC8M oscillator duty cycle	—	45	50	55	%
$I_{DDA(IRC8M)}$ (1)	IRC8M oscillator operating current	f_{IRC8M} = 8 MHz	—	66	88	μA
$t_{ST(IRC8M)}$ (1)	IRC8M oscillator startup time	f_{IRC8M} = 8 MHz	1.4	—	2.8	us

(1) Value guaranteed by design, not 100% tested in production.
(2) Value guaranteed by characterization, not 100% tested in production.

Table 4-23. Low speed internal clock (IRC40K) characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{IRC40K}(1)	Low Speed Internal oscillator (IRC40K) frequency	—	—	40	—	kHz
ACC_{IRC40K}	IRC40K oscillator Frequency accuracy, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +105 °C	-5.5(2)	—	+5.5(2)	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C	-3	—	3	%
$I_{DDA(IRC40K)}$ (1)	IRC40K oscillator operating current	—	—	0.5	0.75	μA
$t_{ST(IRC40K)}$ (1)	IRC40K oscillator startup time	—	13	—	36	μs

(1) Value guaranteed by design, not 100% tested in production.
(2) Value guaranteed by characterization, not 100% tested in production.

4.12. PLL characteristics

The parameters given in Table 46 are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in ***Table 4-3. General operating conditions***.

Table 4-24. PLL0 characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
$f_{IN(PLL)}$	PLL input clock frequency	-	2	-	25	MHz
$f_{OUT(PLL)}$	PLL output clock frequency	V_{DD} >= 3.0 V	32	-	280	MHz
		V_{DD} >= 2.6 V	32	-	252	
f_{VCO}	PLL VCO output clock frequency	-	32	-	280	MHz
$t_{LK(PLL)}$	PLL lock time	-	-	-	1000	μs
$I_{DD(PLL)}$	Current consumption from V_{DD}	VCO freq = 280 MHz	-	808	-	μA
J_{PLL}(2)	Period Jitter (rms)	System clock	-	15.9	-	ps
	Cycle to cycle Jitter (rms)		-	23.7	-	

(1) Value guaranteed by design, not 100% tested in production.
(2) System clock = IRC8M = 8 MHz, PLL0 clock source = HSE40/8 = 5 MHz, f_{PLLOUT} = 280 MHz.

Table 4-25. PLL1 characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
$f_{IN(PLL)}$	PLL input clock frequency	-	2	-	25	MHz
$f_{OUT(PLL)}$	PLL output clock frequency	V_{DD} >= 3.0 V	32	-	280	MHz
		V_{DD} >= 2.6 V	32	-	252	
f_{VCO}	PLL VCO output clock frequency	-	32	-	280	MHz
$t_{LK(PLL)}$	PLL lock time	-	-	-	1000	μs
$I_{DD(PLL)}$	Current consumption from V_{DD}	VCO freq = 280 MHz	-	808	-	μA
J_{PLL}(2)	Period Jitter (rms)	System clock	-	15.9	-	ps
	Cycle to cycle Jitter (rms)		-	23.7	-	

(1) Value guaranteed by design, not 100% tested in production.

(2) System clock = IRC8M = 8 MHz, PLL1 clock source = HSE40M/8 = 5 MHz, f_{PLLOUT} = 280 MHz.

4.13. Memory characteristics

Table 4-26. Flash memory characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
PE_{CYC}	Number of guaranteed program /erase cycles before failure (Endurance)	-40°C ~ +105°C	100	—	—	kcycles
t_{RET}	Data retention time	T_A = 70 °C after up to 0 kcycle	—	20	—	years
t_{PROG}	Word programming time	-40°C ~ +105°C	—	47.5	106	μs
t_{PER}	Page erase time		—	45	300	ms
$t_{MER(512K)}$	Mass erase time		—	4	25.6	s
$t_{MER(1MB)}$	Mass erase time		—	6	38.4	s

(1) Value guaranteed by design, not 100% tested in production.

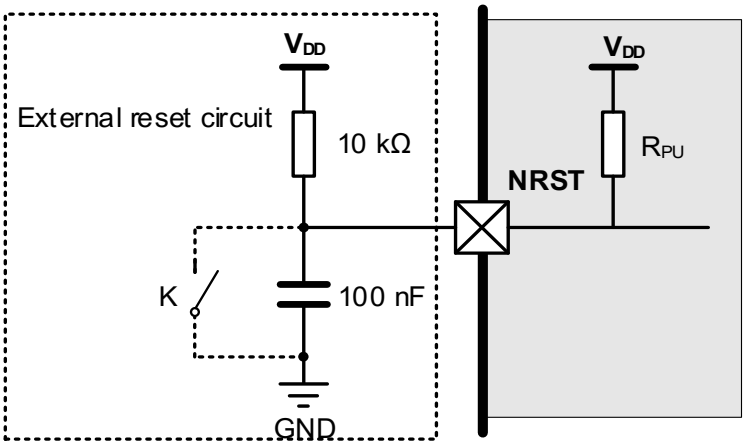
4.14. NRST pin characteristics

Table 4-27. NRST pin characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST Input low level voltage	—	-0.3	—	$0.3V_{DD}$	V
$V_{IH(NRST)}$	NRST Input high level voltage	—	$0.7V_{DD}$	—	V_{DD}+0.3	
V_{HYST}	Schmidt trigger Voltage hysteresis	V_{DD} = V_{DDA} = 2.6 V	—	340	—	mV
		V_{DD} = V_{DDA} = 3.3 V	—	430	—	
		V_{DD} = V_{DDA} = 3.6 V	—	480	—	
R_{PU}	Pull-up equivalent resistor	V_{IN} = V_{SS}	—	40	—	kΩ
t_{NRST_F}	Generated filtered reset pulse duration	—	—	—	100	ns
t_{NRST_NF}	Generated not filtered reset pulse duration	—	350	—	—	

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-9. Recommended external NRST pin circuit(1)



(1) Unless the voltage on NRST pin go below $V_{IL(NRST)}$ level, the device would not generate a reliable reset.

4.15. GPIO current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below VSS or above VDD (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures. The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the -5 μA/+0 μA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Table 4-28. GPIO current injection susceptibility(1)

Symbol	Description		Functional susceptibility		Unit
			Negative injection	Positive injection	
I_{INJ}	Injected current on pin	Input current on 5V tolerant pin	-5	NA	mA
		Input current on other I/O(Except BOOT0)	-5	0	
		BOOT0	0	NA	

(1) Value guaranteed by sample, not 100% tested in production.

4.16. GPIO characteristics

More details about GPIO could be found in ***AN092 GD32 MCU GPIO structure and precautions***.

Table 4-29. I/O static characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{IL}(1)	Standard IO low level input voltage	2.6 V < V_{DD} = V_{DDA} < 3.6 V	-	-	0.3V_{DD}	V
	5V-tolerant IO low level input voltage	2.6 V < V_{DD} = V_{DDA} < 3.6 V	-	-	0.3V_{DD}	V
V_{IH}(1)	Standard IO high level input voltage	2.6 V < V_{DD} = V_{DDA} < 3.6 V	0.7V_{DD}	-	-	V
	5V-tolerant IO high level input voltage	2.6 V < V_{DD} = V_{DDA} < 3.6 V	0.7V_{DD}	-	-	V

Symbol	Description		Conditions	Min	Typ	Max	Unit
V_{HYS}(1)	Input hysteresis		-	-	320	-	mV
I_{LEAK}	IO input leakage current		V_{SS} <= V_{IN} <= V_{DD}/V_{DDA}	-	-	2	μA
R_{PU}(1)	Weak pull-up equivalent resistor	All pins	V_{IN} = V_{SS}	-	40	-	kΩ
		PA10	-	-	10	-	
R_{PD}(1)	Weak pull-down equivalent resistor	All pins	V_{IN} = V_{DD}	-	40	-	kΩ
		PA10	-	-	10	-	
C_{IO}(1)	I/O pin capacitance		-	-	5	-	pF

(1) Value guaranteed by design, not 100% tested in production.

Table 4-30. Output voltage characteristics for all I/Os except PC13, PC14, PC15 (1)(2)

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{OL} (IO_speed=Level 3)	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 2.6 V	—	—	0.16	V
		V_{DD} = 3.3 V	—	—	0.15	
		V_{DD} = 3.6 V	—	—	0.14	
	Low level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 2.6 V	—	—	0.46	
		V_{DD} = 3.3 V	—	—	0.39	
		V_{DD} = 3.6 V	—	—	0.38	
V_{OH} (IO_speed= Level 3)	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 2.6 V	1.92	—	—	V
		V_{DD} = 3.3 V	2.54	—	—	
		V_{DD} = 3.6 V	2.78	—	—	
	High level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 2.6 V	1.78	—	—	
		V_{DD} = 3.3 V	2.40	—	—	
		V_{DD} = 3.6 V	2.64	—	—	
V_{OL} (IO_speed= Level 2)	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 2.6 V	—	—	0.22	V
		V_{DD} = 3.3 V	—	—	0.20	
		V_{DD} = 3.6 V	—	—	0.19	
	Low level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 2.6 V	—	—	0.64	
		V_{DD} = 3.3 V	—	—	0.54	
		V_{DD} = 3.6 V	—	—	0.51	
V_{OH} (IO_speed= Level 2)	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 2.6 V	1.92	—	—	V
		V_{DD} = 3.3 V	2.50	—	—	
		V_{DD} = 3.6 V	2.75	—	—	
	High level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 2.6 V	1.64	—	—	
		V_{DD} = 3.3 V	2.28	—	—	
		V_{DD} = 3.6 V	2.55	—	—	
V_{OL} (IO_speed= Level 1)	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 2.6 V	—	—	0.49	V
		V_{DD} = 3.3 V	—	—	0.40	
		V_{DD} = 3.6 V	—	—	0.39	
	Low level output voltage for an IO Pin (I_{IO} = +15 mA)	V_{DD} = 2.6 V	—	—	1.10	
		V_{DD} = 3.3 V	—	—	0.82	
		V_{DD} = 3.6 V	—	—	0.79	
V_{OH}	High level output	V_{DD} = 2.6 V	1.78	—	—	V

Symbol	Description	Conditions	Min	Typ	Max	Unit
(IO_speed= Level 1)	voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 3.3 V	2.40	—	—	
		V_{DD} = 3.6 V	2.64	—	—	
	High level output voltage for an IO Pin (I_{IO} = +15 mA)	V_{DD} = 2.6 V	1.45	—	—	
		V_{DD} = 3.3 V	2.16	—	—	
		V_{DD} = 3.6 V	2.43	—	—	
V_{OL} (IO_speed= Level 0)	Low level output voltage for an IO Pin (I_{IO} = +1 mA)	V_{DD} = 2.6 V	—	—	0.16	V
		V_{DD} = 3.3 V	—	—	0.14	
		V_{DD} = 3.6 V	—	—	0.14	
	Low level output voltage for an IO Pin (I_{IO} = +4 mA)	V_{DD} = 2.6 V	—	—	0.79	
		V_{DD} = 3.3 V	—	—	0.63	
		V_{DD} = 3.6 V	—	—	0.60	
V_{OH} (IO_speed= Level 0)	High level output voltage for an IO Pin (I_{IO} = +1 mA)	V_{DD} = 2.6 V	1.90	—	—	
		V_{DD} = 3.3 V	2.49	—	—	
		V_{DD} = 3.6 V	2.73	—	—	
	High level output voltage for an IO Pin (I_{IO} = +4 mA)	V_{DD} = 2.6 V	1.15	—	—	
		V_{DD} = 3.3 V	1.99	—	—	
		V_{DD} = 3.6 V	2.28	—	—	

(1) Value guaranteed by characterization, not 100% tested in production.

(2) All pins except PC13 / PC14 / PC15. Since PC13 to PC15 are supplied through the Power Switch, which can only be obtained by a small current (typical source capability:3 mA shared between these IOs, but sink capability is same as other IO), the speed of GPIOs PC13 to PC15 should not exceed 2 MHz when they are in output mode (maximum load: 30 pF).

Table 4-31. I/O port AC characteristics (1)(2)(3)

Speed	Symbol	Description	Conditions	Min	Typ	Max	Unit
00	t_R/t_F	Output high to low level fall time and output low to high level rise time	2.6 <= V_{DD} <= 3.6 V, C_L = 10 pF	-	-	9.5	ns
			2.6 <= V_{DD} <= 3.6 V, C_L = 30 pF	-	-	25	
			2.6 <= V_{DD} <= 3.6 V,C_L = 50 pF	-	-	40	
01	t_R/t_F	Output high to low level fall time and output low to high level rise time	2.6 <= V_{DD} <= 3.6 V, C_L = 10 pF	-	-	2.7	ns
			2.6 <= V_{DD} <= 3.6 V, C_L = 30 pF	-	-	7	
			2.6 <= V_{DD} <= 3.6 V,C_L = 50 pF	-	-	11	
10	t_R/t_F	Output high to low level fall time and output low to high level rise time	2.6 <= V_{DD} <= 3.6 V, C_L = 10 pF	-	-	2	ns
			2.6 <= V_{DD} <= 3.6 V, C_L = 30 pF	-	-	3.5	
			2.6 <= V_{DD} <= 3.6 V,C_L = 50 pF	-	-	5.5	
11	t_R/t_F	Output high to low level fall time and output low to high level rise time	2.6 <= V_{DD} <= 3.6 V, C_L = 10 pF	-	-	1.3	ns
			2.6 <= V_{DD} <= 3.6 V, C_L = 30 pF	-	-	2.6	
			2.6 <= V_{DD} <= 3.6 V, C_L = 50 pF	-	-	4	

(1) The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.

(2) Value guaranteed by design, not 100% tested in production.

(3) The data is for reference only, and the specific values are related to PCB Layout.

4.17. Internal reference voltage characteristics

Table 4-32. Internal reference voltage characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	-40°C ~ +105°C	1.172	—	1.242	V
$t_{S_VREFINT}$(2)	ADC sampling time when reading the internal reference voltage	—	17.1	—	—	µs
$t_{STA_VREFINT}$	Start time of reference voltage buffer when ADC is enable	—	—	3	—	µs
$I_{DD(VREFINT_BUF)}$	V_{REFINT} buffer consumption from V_{DD} when converted by ADC	—	—	4.5	—	µA
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	—	—	—	70	mV
T_{Coeff}	Temperature coefficient	—	—	—	39	ppm/°C

(1) Value guaranteed by design, not 100% tested in production.
(2) The shortest sampling time can be determined in the application by multiple iterations.

Table 4-33. Internal reference voltage calibration values

Symbol	Test conditions	Memory address
V_{REFINT}(1)	V_{DD} = V_{DDA} = V_{REFP} = 3.3 V (+/- 10 mV), Temperature = 25 °C (+/- 5 °C)	0x1FFFF7FC-0x1FFFF7FD

(1) V_{REFINT} is internally connected to the ADC0_IN17 input channel.

4.18. ADC characteristics

Table 4-34. ADC operating conditions(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage	—	2.6	3.3	3.6	V
V_{IN}	ADC input voltage range	—	0	—	V_{REFP}	V
V_{REFP}(2)	Positive Reference Voltage	—	2.6	—	V_{DDA}	V
V_{REFN}	Negative Reference Voltage	—	—	V_{SSA}	—	V
f_{ADC}	ADC clock	—	0.1	—	42	MHz

(1) Value guaranteed by design, not 100% tested in production.
(2) V_{REFP} should always be equal to or less than V_{DDA}, especially during power up.

Table 4-35. ADC characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
R_{AIN}	External input impedance	See ***Equation 1***	-	-	74.16	kΩ
R_{ADC}	Input sampling switch resistance	-	-	-	0.5	kΩ

Symbol	Description	Conditions	Min	Typ	Max	Unit
C_{ADC}	Input sampling capacitance	No pin/pad capacitance included	-	-	2.87	pF
t_S	Sampling time	f_{ADC} = 42 MHz	0.0357	-	5.7	μs
t_{CONV}	Total conversion time(including sampling time)	12-bit	-	14	-	1/ f_{ADC}
		10-bit	-	12	-	
		8-bit	-	10	-	
		6-bit	-	8	-	
f_S	Sampling rate	12-bit	0.007	-	3	MSPS
		10-bit	0.008	-	3.5	
		8-bit	0.01	-	4.2	
		6-bit	0.012	-	5.25	
$t_{ST(ADC)}$	Startup time	-	-	-	1	μs
$I_{DDA (ADC)}$	ADC consumption on V_{DDA} and V_{REF}	-	-	850	-	μA

(1) Value guaranteed by design, not 100% tested in production.

Equation 1: R_{AIN} max formula $R_{AIN} < \frac{T_S}{f_{ADC} * C_{ADC} * \ln(2^{N+2})} - R_{ADC}$

According to the equation, we can determine the maximum external impedance. Here N = 12 when ADC work in 12-bit resolution.

Table 4-36. ADC $R_{AIN\ max}$ for f_{ADC} = 42 MHz(1)

T_s (cycles)	t_s (μs)	$R_{AIN\ max}$ (kΩ) (2)
1.5	0.0357	—
7.5	0.1786	1.83
13.5	0.3214	3.70
28.5	0.6786	8.38
41.5	0.9881	12.43
55.5	1.3214	16.80
71.5	1.7024	21.79
239.5	5.7024	74.16

(1) Value guaranteed by design, not 100% tested in production.

(2) Extra internal capacitors (such as pin capacitors, etc.) need to be considered when calculating the actual R_{AIN}. Here we take 5 pF for the extra internal capacitance, C_{ADC} = 2.87 pF + 5pF =7.87 pF.

Table 4-37. ADC performance characteristics(1)(2)(3)(4)

Symbol	Description	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 42 MHz(2)	10.91	11.16	-	bits
SNDR	Signal-to-noise and distortion ratio	f_{ADC} = 42 MHz(2)	67.47	68.97	-	dB
SNR	Signal-to-noise ratio	f_{ADC} = 42 MHz(2)	68.30	69.23	-	
THD	Total harmonic distortion	f_{ADC} = 42 MHz(2)	-	-82.72	-73.91	
EO	Offset error	f_{ADC} = 42 MHz V_{DDA} = V_{REFP} = 3.3 V	-	+/-0.8	+/-3	LSB
DNL	Differential linearity error		-	+/-0.5	+/-1	
INL	Integral linearity error		-	+/-0.8	+/-1.7	

(1) Value guaranteed by characterization, not 100% tested in production.

(2) V_{DDA} = V_{REFP} = 3.3 V, Input Frequency = 10 kHz.

(3) Some guidance is provided to improve the sampling accuracy of ADC. Refer to ***AN059 Methods to improve ADC sampling accuracy***.

(4) The data comes from LQFP100 package, external VREF were adopted.

Figure 4-10. Differential linearity error

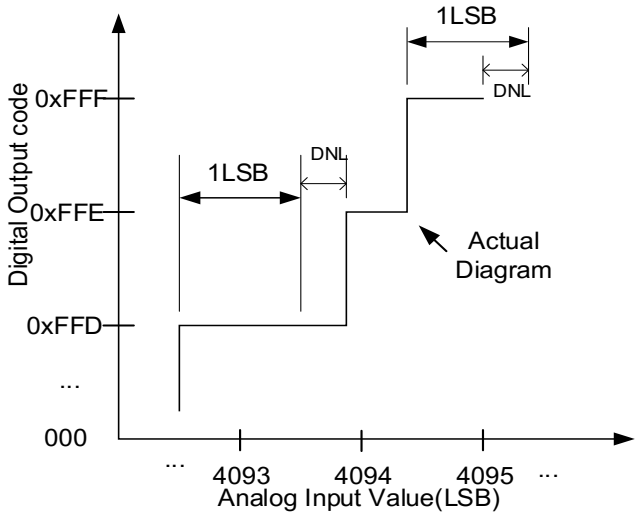
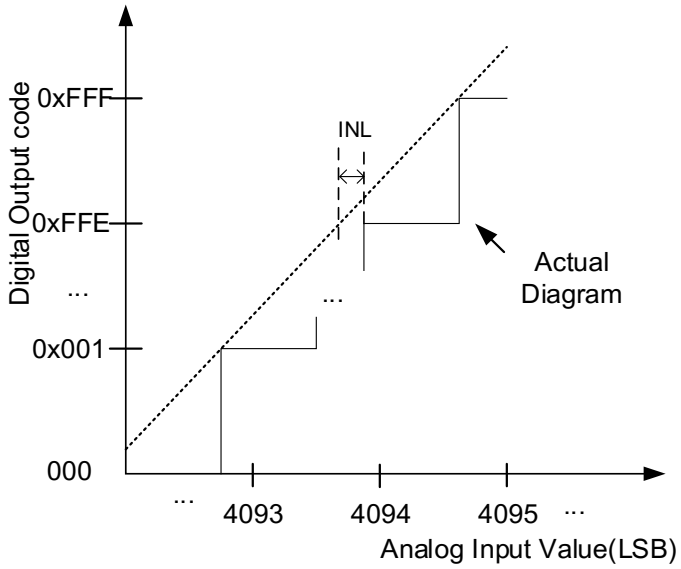


Figure 4-11. Integral linearity error



4.19. Temperature sensor characteristics

Table 4-38. Temperature sensor characteristics(1)

Symbol	Description	Min	Typ	Max	Unit
T_{LIN}	Linearity of temperature sensitive voltage	-	+/-2	-	℃
Avg_Slope	Average slope	-	4.35	-	mV/℃
V_{30}	Voltage at 30 °C	-	1.524	-	V
$t_{ST(TS)}$	Start up time	-	10	-	μs
t_{S_temp}(2)	ADC sampling time when reading the temperature	-	17.1	-	μs

(1) Value guaranteed by design, not 100% tested in production.

(2) Shortest sampling time can be determined in the application by multiple iterations.

Table 4-39. Temperature sensor calibration values

Symbol	Description	Memory address
TS_CAL	Temperature sensor raw data acquired value at 30 °C (+/- 3 °C), V_{DD} = V_{DDA} = V_{REFP} = 3.3V (+/-5 mV)	0x1FFFF7F8 - 0x1FFFF7F9

4.20. DAC characteristics

Table 4-40. DAC characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Operating voltage	—		2.6	3.3	3.6	V
V_{REFP}	Positive Reference Voltage	—		2.6	—	V_{DDA}	V
V_{REFN}	Negative Reference Voltage	—		—	V_{SSA}	—	V
I_{DDA}	DAC current consumption in quiescent mode	DAC output buffer ON	No load, middle code (0x800) , V_{REFP} = 3.6 V	—	400	—	μA
			No load, worst code (0xF1C) , V_{REFP} = 3.6 V	—	420	—	
		DAC output buffer OFF	No load, middle (0x800) , V_{REFP} = 3.6 V	—	5	—	
$I_{DDVREFP}$	DAC current consumption in quiescent mode	DAC output buffer ON	No load, middle code (0x800) , V_{REFP} = 3.6 V	—	100	—	μA
			No load, worst code (0xF1C) , V_{REFP} = 3.6 V	—	360	—	

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		DAC output buffer OFF	No load, middle code (0x800) , V_{REFP} = 3.6 V	—	5	—	

(1) Value guaranteed by design, not 100% tested in production.

Table 4-41. DAC characteristics(1)

Symbol	Description	Conditions		Min	Typ(1)	Max	Unit
R_{LOAD}	Load resistance	Resistive load with buffer ON	connected to V_{SSA}	5	—	—	kΩ
			connected to V_{DDA}	5	—	—	
Ro	Impedance output with buffer OFF	Impedance output with buffer OFF		—	—	15	kΩ
C_{LOAD}	Load capacitance	No pin/pad capacitance included		—	—	50	pF
DAC_OUT	Voltage on DAC_OUT output	buffer OFF		1LSB	—	V_{DDA}-1LSB	V
		buffer ON		0.2	—	V_{DDA}-0.2	V

(1) Value guaranteed by design, not 100% tested in production.

Table 4-42. DAC performance characteristics

Symbol	Description	Conditions		Min	Typ	Max	Unit
DNL(1) (2)	Differential non-linearity	DAC output buffer ON		-	-	+/-2	LSB
		DAC output buffer OFF		-	-	+/-2	
INL(1) (2)	Integral non-linearity	DAC output buffer ON		-	-	+/-2.5	LSB
		DAC output buffer OFF		-	-	+/-3	
Offset(1) (2)	Offset error	DAC output buffer ON		-	-	+/-1.5	LSB
		DAC output buffer OFF		-	-	+/-3.5	
GE(1) (2)	Gain error	DAC output buffer ON		-	-	+/-0.05	%
		DAC output buffer OFF		-	-	+/-0.1	
$t_{SETTLING}$(3)	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches the final value of +/-1LSB, +/-2LSB, +/-4LSB, +/-8LSB)	Normal mode, DAC output buffer ON, CL <= 50 pF, RL >= 5 kΩ	+/-1 LSB	-	0.6	-	µs
			+/-2 LSB	-	0.52	-	
			+/-4 LSB	-	0.51	-	
			+/-8 LSB	-	0.5	-	
		Normal mode, DAC output buffer OFF, +/-1LSB CL=10 pF		-	2	-	
t_{WAKEUP} (3)	Wakeup time from off state (setting the ENx bit in the DAC Control register) until the final value of +/-1LSB is reached	Normal mode, DAC output buffer ON, CL <= 50 pF, RL = 5 kΩ		-	5	10	µs
		Normal mode, DAC output buffer OFF, CL <= 10 pF		-	3	6	

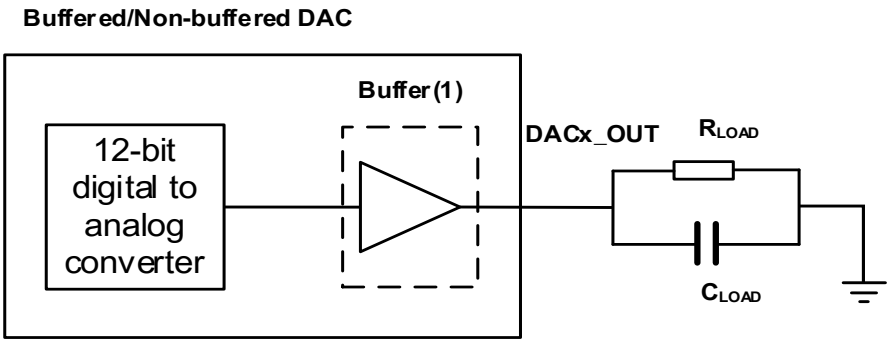
Symbol	Description	Conditions	Min	Typ	Max	Unit
Update rate(3)	Max frequency for a correct DAC_OUT change from code i to i+/- 1LSBs	C_{LOAD} <= 50 pF, R_{LOAD} >= 5 kΩ	-	-	4	MS/s
PSRR(3)	Power supply rejection ratio(to V_{DDA})	No R_{Load}, C_{LOAD}=50 pF	70	90	-	dB

(1) Value guaranteed by characterization, not 100% tested in production.

(2) The parameter computed from code 0x000 and 0xFFF when the buffer is OFF, and from code giving 0.2 V and (V_{REFP} - 0.2 V) when the buffer is ON.

(3) Value guaranteed by design, not 100% tested in production.

Figure 4-12. 12-bit buffered /non-buffered DAC



(1) The DAC integrates an output buffer to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the DBOFFx bit in the DAC_CTL0 register.

4.21. Comparators characteristics

Table 4-43. CMP characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage	—	2.6	3.3	3.63	V
V_{IN}	Input voltage range	—	0	—	V_{DDA}	V
V_{BG}	Scaler input voltage	—	—	1.2	—	V
V_{SC}	Scaler offset voltage	—	—	1.1	4	mV
$I_{DDA(SCALER)}$	Scaler static consumption from V_{DDA}	COMxBEN=0 (bridge disable)	—	6	6.1	μA
		COMxBEN =1 (bridge enable)	—	12	13	
$t_{ST(SCALER)}$	Scaler startup time	—	—	2	3	μs
t_D	Propagation delay for 200mV step with 100 mV overdrive	—	—	10.2	17.2	ns
	Propagation delay for full range step with 100 mV overdrive	—	—	13.2	24.8	ns
$t_{ST(COMP)}$	Comparator startup time to reach propagation delay	—	—	—	0.65	μs

Symbol	Description	Conditions	Min	Typ	Max	Unit
	specification					
$I_{DDA(CMP)}$	Current consumption from V_{DDA}	—	—	280	282	μA
V_{OFFSET}	Offset error	—	—	1.5	8	mV
V_{HYST}	Hysteresis Voltage	No Hysteresis	—	0	—	mV
		Low Hysteresis	—	15	29	
		Medium Hysteresis	—	30	59	
		High Hysteresis	—	46	91	

(1) Value guaranteed by design, not 100% tested in production.

4.22. I2C characteristics

Table 4-44. I2C characteristics(1)(2)

Symbol	Description	Conditions	Standard mode		Fast mode		Fast mode plus		Unit
			Min	Max	Min	Max	Min	Max	
$t_{SCL(H)}$	SCL clock high time	—	4.0	—	0.6	—	0.2	—	μs
$t_{SCL(L)}$	SCL clock low time	—	4.7	—	1.3	—	0.5	—	μs
$t_{SU(SDA)}$	SDA setup time	—	250	—	100	—	50	—	ns
$t_{H(SDA)}$	SDA data hold time	—	0(3)	3450	0(3)	900	0	450	ns
$t_{R(SDA/SCL)}$	SDA and SCL rise time	—	—	1000	—	300	—	120	ns
$t_{F(SDA/SCL)}$	SDA and SCL fall time	—	—	300	—	300	—	120	ns
$t_{H(STA)}$	Start condition hold time	—	4.0	—	0.6	—	0.26	—	μs
$t_{SU(STA)}$	Repeated Start condition setup time	—	4.7	—	0.6	—	0.26	—	μs
$t_{SU(STO)}$	Stop condition setup time	—	4.0	—	0.6	—	0.26	—	μs
t_{BUFF}	Stop to Start condition time (bus free)	—	4.7	—	1.3	—	0.5	—	μs

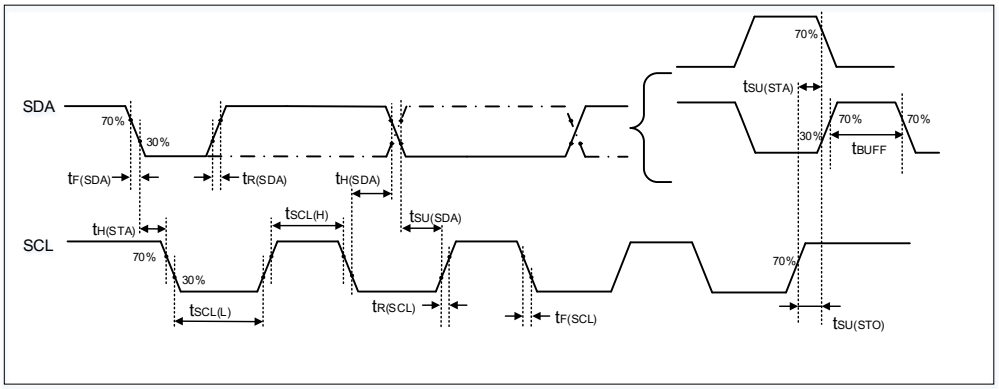
(1) Value guaranteed by design, not 100% tested in production.

(2) To ensure the standard mode I2C frequency, f_{PCLK1} must be at least 2 MHz. To ensure the fast mode I2C frequency, f_{PCLK1} must be at least 4 MHz. To ensure the fast mode plus I2C frequency, f_{PCLK1} must be at least a multiple of 10 MHz.

(3) The device should provide a data hold time of 300 ns at least in order to bridge the undefined region of the

falling edge of SCL.

Figure 4-13. I2C bus timing diagram



4.23. SPI characteristics

Table 4-45. Standard SPI characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	—	—	—	40	MHz
$t_{SCK(H)}$	SCK clock high time	Master mode, f_{PCLKx} = 80 MHz, presc = 2	—	12.5	—	ns
$t_{SCK(L)}$	SCK clock low time	Master mode, f_{PCLKx} = 80 MHz, presc = 2	—	12.5	—	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time	—	—	—	5.5	ns
$t_{SU(MI)}$	Data input setup time	—	1	—	—	ns
$t_{H(MI)}$	Data input hold time	—	2	—	—	ns
SPI slave mode						
$t_{SU(NSS)}$	NSS enable setup time	—	0	—	—	ns
$t_{H(NSS)}$	NSS enable hold time	—	1	—	—	ns
$t_{A(SO)}$	Data output access time	—	5	—	9	ns
$t_{DIS(SO)}$	Data output disable time	—	6	—	10	ns
$t_{V(SO)}$	Data output valid time	—	—	—	12	ns
$t_{SU(SI)}$	Data input setup time	—	0	—	—	ns
$t_{H(SI)}$	Data input hold time	—	1	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-14. SPI timing diagram - master mode

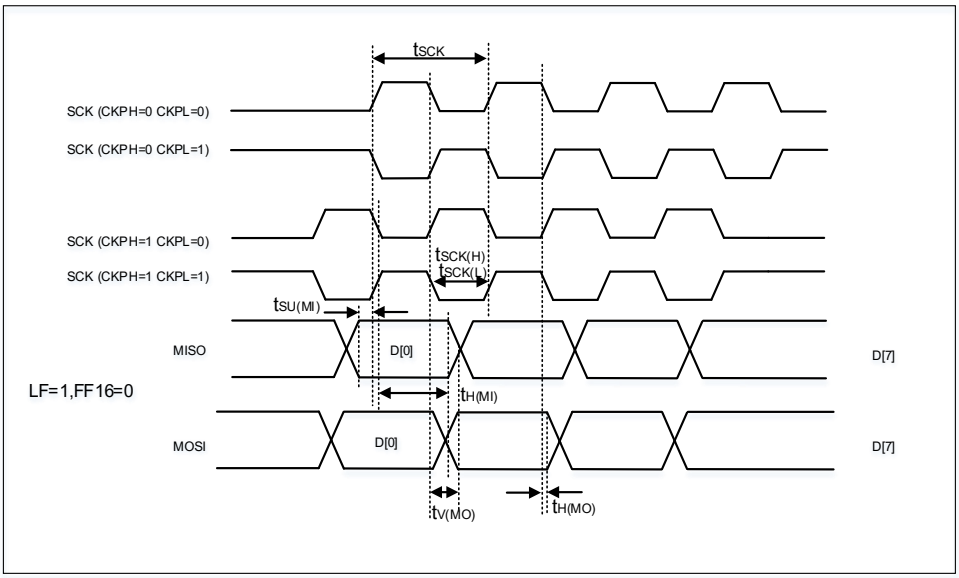


Figure 4-15. SPI timing diagram - slave mode(CKPH=0)

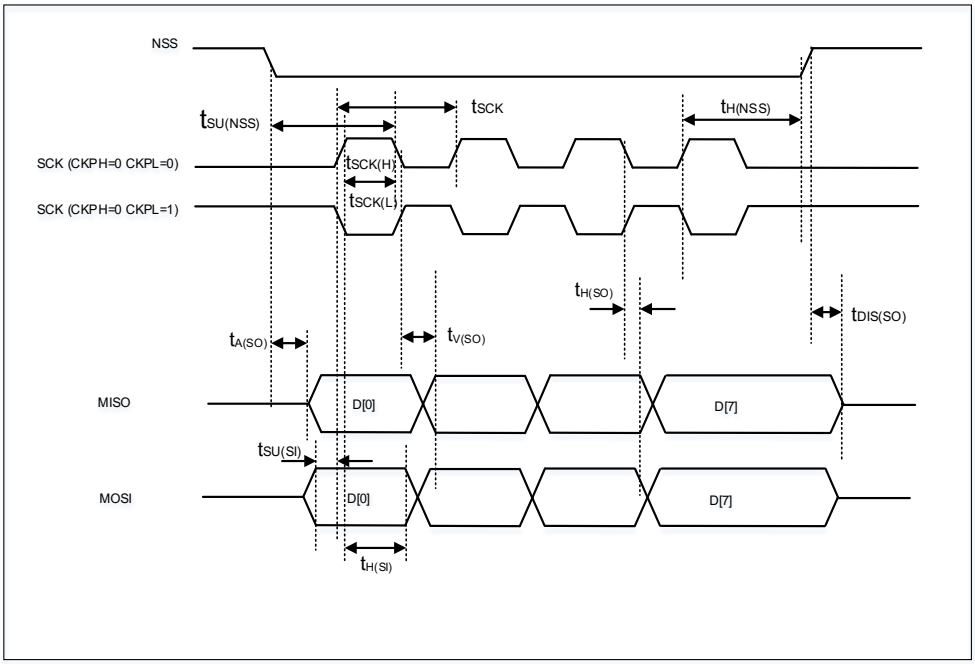
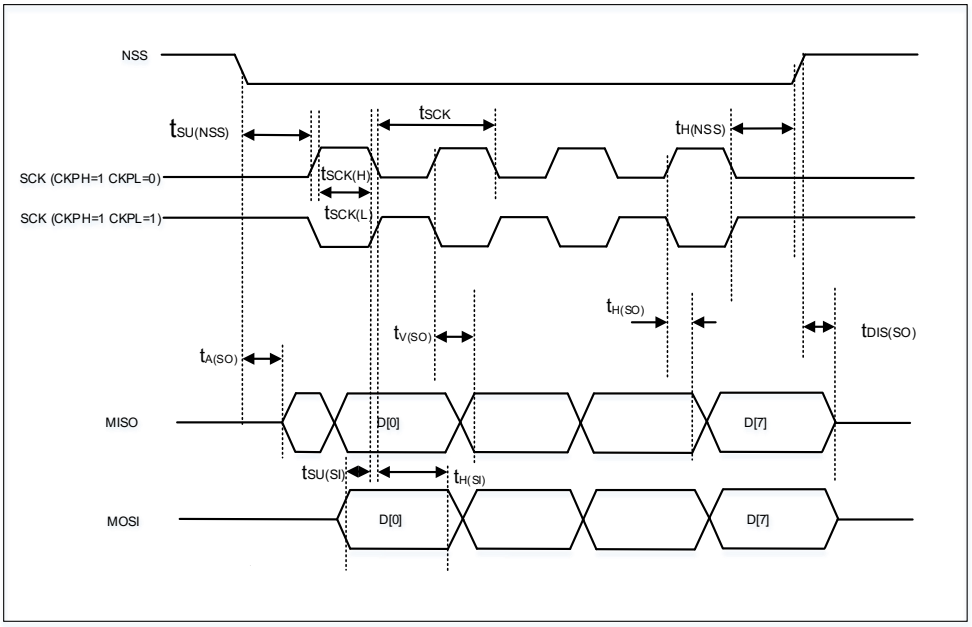


Figure 4-16. SPI timing diagram - slave mode(CKPH=1)



4.24. I2S characteristics

Table 4-46. I2S characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{CK}	Clock frequency	Master mode (data: 16 bits, Audio frequency = 96 kHz)	—	3	—	MHz
		Slave mode	—	—	10	
t_H	Clock high time	—	—	166	—	ns
t_L	Clock low time		—	166	—	ns
$t_{V(WS)}$	WS valid time	Master mode	0	—	—	ns
$t_{H(WS)}$	WS hold time	Master mode	0	—	—	ns
$t_{SU(WS)}$	WS setup time	Slave mode	0	—	—	ns
$t_{H(WS)}$	WS hold time	Slave mode	2	—	—	ns
$Duty_{SCK}$	I2S slave input clock duty cycle	Slave mode	—	50	—	%
$t_{SU(SD_MR)}$	Data input setup time	Master mode	2	—	—	ns
$t_{SU(SD_SR)}$	Data input setup time	Slave mode	0	—	—	ns
$t_{H(SD_MR)}$	Data input hold time	Master receiver	0	—	—	ns
$t_{H(SD_SR)}$		Slave receiver	1	—	—	ns
$t_{V(SD_ST)}$	Data output valid time	Slave transmitter (after enable edge)	—	—	12	ns
$t_{H(SD_ST)}$	Data output hold time	Slave transmitter (after enable edge)	7	—	—	ns
$t_{V(SD_MT)}$	Data output valid time	Master transmitter (after enable edge)	—	—	7	ns
$t_{H(SD_MT)}$	Data output hold time	Master transmitter (after enable edge)	4	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-17. I2S timing diagram - master mode

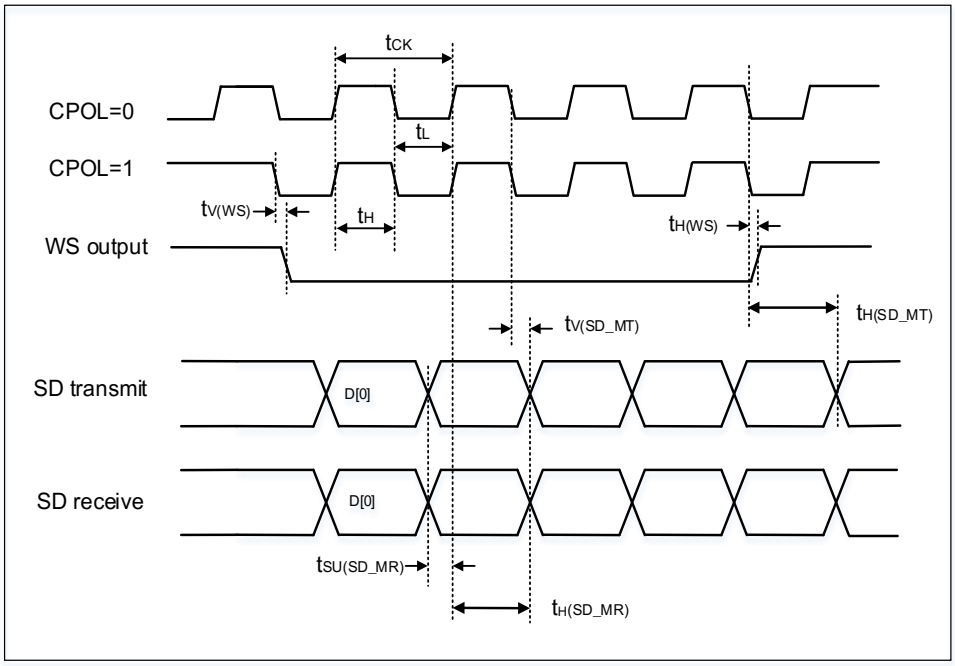
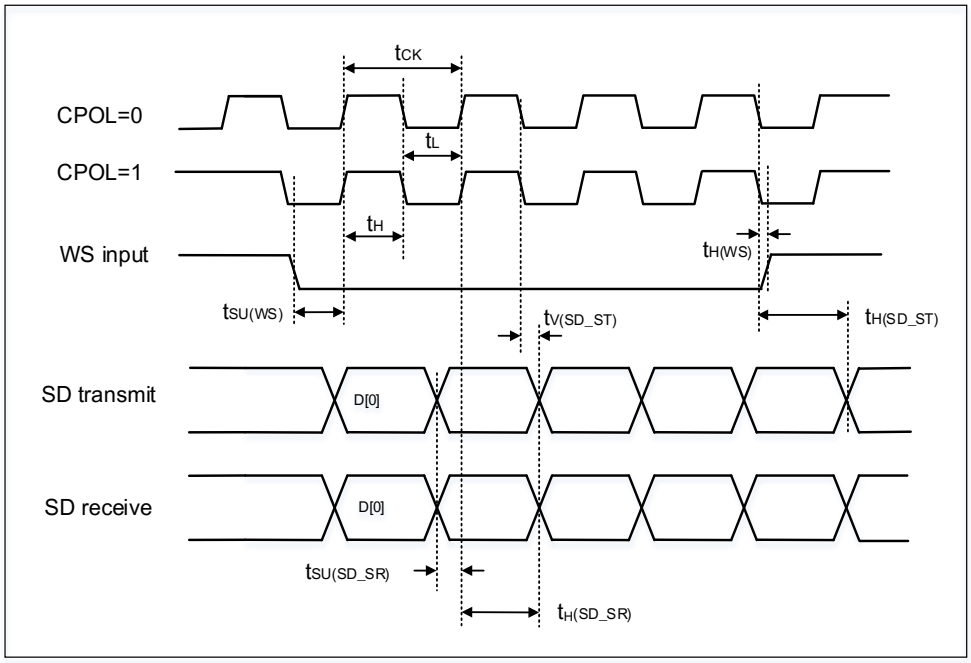


Figure 4-18. I2S timing diagram - slave mode



4.25. USART characteristics

Table 4-47. USART0 characteristics in Synchronous mode(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	f_{PCLK2} =280 MHz	—	—	35	MHz
$t_{SCK(H)}$	SCK clock high time		14.25	—	—	ns
$t_{SCK(L)}$	SCK clock low time		14.25	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

Table 4-48. USART1/2 characteristics in Synchronous mode(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	f_{PCLK1} = 140 MHz	—	—	17.5	MHz
$t_{SCK(H)}$	SCK clock high time		28.5	—	—	ns
$t_{SCK(L)}$	SCK clock low time		28.5	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

Table 4-49. USART0 characteristics in Smartcard mode(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	f_{PCLK2} = 280 MHz	—	—	140	MHz
$t_{SCK(H)}$	SCK clock high time		3.5	—	—	ns
$t_{SCK(L)}$	SCK clock low time		3.5	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

Table 4-50. USART1/2 characteristics in Smartcard mode(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	f_{PCLK1} = 140 MHz	—	—	70	MHz
$t_{SCK(H)}$	SCK clock high time		7.1	—	—	ns
$t_{SCK(L)}$	SCK clock low time		7.1	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

4.26. CAN characteristics

Refer to *Table 4-29. I/O static characteristics* for more details on the input/output alternate function characteristics (CAN TX and CAN RX).

4.27. EXMC characteristics

Table 4-51. Read timings of asynchronous multiplexed PSRAM/NOR (1)(2)(3)

Symbol	Description	Min	Max	Unit
$t_{W(NE)}$	EXMC_NE low time	24	26	ns
$t_{V(NOE_NE)}$	EXMC_NEx low to EXMC_NOE low	9.71	—	ns
$t_{W(NOE)}$	EXMC_NOE low time	13.29	15.29	ns
$t_{H(NE_NOE)}$	EXMC_NOE high to EXMC_NE high hold time	0	—	ns
$t_{V(A_NE)}$	EXMC_NEx low to EXMC_A valid	0	—	ns
$t_{V(A_NOE)}$	Address hold time after EXMC_NOE high	0	—	ns
$t_{V(BL_NE)}$	EXMC_NEx low to EXMC_BL valid	0	—	ns
$t_{H(BL_NOE)}$	EXMC_BL hold time after EXMC_NOE high	0	—	ns
$t_{SU(DATA_NE)}$	Data to EXMC_NEx high setup time	13.29	—	ns
$t_{SU(DATA_NOE)}$	Data to EXMC_NOEx high setup time	13.29	—	ns
$t_{H(DATA_NOE)}$	Data hold time after EXMC_NOE high	0	—	ns
$t_{H(DATA_NE)}$	Data hold time after EXMC_NEx high	0	—	ns
$t_{V(NADV_NE)}$	EXMC_NEx low to EXMC_NADV low	0	—	ns
$t_{W(NADV)}$	EXMC_NADV low time	2.57	4.57	ns
$t_{H(AD_NADV)}$	EXMC_AD valid hold time after EXMC_NADV high	2.57	4.57	ns

(1) C_L = 30 pF.

(2) Value guaranteed by design, not 100% tested in production.

(3) Based on configure: f_{HCLK} = 280 MHz, AddressSetupTime = 0, AddressHoldTime = 1, DataSetupTime = 1.

Table 4-52. Write timings of asynchronous multiplexed PSRAM/NOR (1)(2)(3)

Symbol	Description	Min	Max	Unit
$t_{W(NE)}$	EXMC_NE low time	16.86	18.86	ns
$t_{V(NWE_NE)}$	EXMC_NEx low to EXMC_NWE low	2.57	—	ns
$t_{W(NWE)}$	EXMC_NWE low time	9.71	11.71	ns
$t_{H(NE_NWE)}$	EXMC_NWE high to EXMC_NE high hold time	2.57	—	ns
$t_{V(A_NE)}$	EXMC_NEx low to EXMC_A valid	0	—	ns
$t_{V(NADV_NE)}$	EXMC_NEx low to EXMC_NADV low	0	—	ns
$t_{W(NADV)}$	EXMC_NADV low time	2.57	4.57	ns
$t_{H(AD_NADV)}$	EXMC_AD valid hold time after EXMC_NADV high	2.57	—	ns
$t_{H(A_NWE)}$	Address hold time after EXMC_NWE high	2.57	—	ns
$t_{H(BL_NWE)}$	EXMC_BL hold time after EXMC_NWE high	2.57	—	ns
$t_{V(BL_NE)}$	EXMC_NEx low to EXMC_BL valid	0	—	ns
$t_{V(DATA_NADV)}$	EXMC_NADV high to DATA valid	2.57	—	ns
$t_{H(DATA_NWE)}$	Data hold time after EXMC_NWE high	2.57	—	ns

(1) C_L = 30 pF.

(2) Value guaranteed by design, not 100% tested in production.

(3) Based on configure: f_{HCLK} = 280 MHz, AddressSetupTime = 0, AddressHoldTime = 1, DataSetupTime =1.

Table 4-53. Read timings of synchronous multiplexed PSRAM/NOR (1)(2)(3)

Symbol	Description	Min	Max	Unit
$t_{W\ (CLK)}$	EXMC_CLK period	14.29	—	ns
$t_{D(CLKL-NExL)}$	EXMC_CLK low to EXMC_NEx low	0	—	ns
$t_{D(CLKH-NExH)}$	EXMC_CLK high to EXMC_NEx high	6.14	—	ns
$t_{D(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	—	ns
$t_{D(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	—	ns
$t_{D(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	0	—	ns
$t_{D(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	6.14	—	ns
$t_{D(CLKL-NOEL)}$	EXMC_CLK low to EXMC_NOE low	0	—	ns
$t_{D(CLKH-NOEH)}$	EXMC_CLK high to EXMC_NOE high	6.14	—	ns
$t_{D(CLKL-ADV)}$	EXMC_CLK low to EXMC_AD valid	0	—	ns
$t_{D(CLKL-ADIV)}$	EXMC_CLK low to EXMC_AD invalid	0	—	ns

(1) C_L = 30 pF.

(2) Value guaranteed by design, not 100% tested in production.

(3) Based on configure: f_{HCLK} = 280 MHz, BurstAccessMode = Enable; Memory Type = PSRAM; WriteBurst = Enable; CLKDivision = 3(EXMC_CLK is 4 divided by HCLK); Data Latency = 1.

Table 4-54. Write timings of synchronous multiplexed PSRAM (1)(2)(3)

Symbol	Description	Min	Max	Unit
$t_{W(CLK)}$	EXMC_CLK period	14.29	—	ns
$t_{D(CLKL-NExL)}$	EXMC_CLK low to EXMC_NEx low	0	—	ns
$t_{D(CLKH-NExH)}$	EXMC_CLK high to EXMC_NEx high	6.14	—	ns
$t_{D(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	—	ns
$t_{D(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	—	ns
$t_{D(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	0	—	ns
$t_{D(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	6.14	—	ns
$t_{D(CLKL-NWEL)}$	EXMC_CLK low to EXMC_NWE low	0	—	ns
$t_{D(CLKH-NWEH)}$	EXMC_CLK high to EXMC_NWE high	6.14	—	ns
$t_{D(CLKL-ADIV)}$	EXMC_CLK low to EXMC_AD invalid	0	—	ns
$t_{D(CLKL-DATA)}$	EXMC_A/D valid data after EXMC_CLK low	0	—	ns
$t_{H(CLKL-NBLH)}$	EXMC_CLK low to EXMC_NBL high	0	—	ns

(1) C_L = 30 pF.

(2) Value guaranteed by design, not 100% tested in production.

(3) Based on configure: f_{HCLK} = 280 MHz, BurstAccessMode = Enable; MemoryType = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); DataLatency = 1.

4.28. TIMER characteristics

Table 4-55. TIMER characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{res}	Timer resolution time	—	1	—	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 280 MHz	3.57	—	ns
f_{EXT}	Timer external clock frequency	—	0	$f_{TIMERxCLK}/2$	MHz
		$f_{TIMERxCLK}$ = 280 MHz	0	140	MHz
RES	Timer resolution	TIMER0 & TIMER2 & TIMER3 & TIMER4& TIMER5 & TIMER6 & TIMER7 & TIMER15 & TIMER16	—	16	bit
		TIMER1	—	32	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	—	1	65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 280 MHz	0.00357	234.06	μs
	32-bit counter clock period when internal clock is	—	1	4294967296	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ =	0.00357	15339168.91	μs

Symbol	Parameter	Conditions	Min	Max	Unit
	selected	280 MHz			
t_{MAX_COUNT}	Maximum possible count (16-bit)	—	—	4294967296	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 280 MHz	—	15.33916891	s
	Maximum possible count (32-bit)	—	—	2.81475E+14	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 280 MHz	—	279.2410483	h

(1) Value guaranteed by design, not 100% tested in production.

4.29. USBFS characteristics

Table 4-56. USBFS start up time(1)

Symbol	Parameter	Max	Unit
$t_{STARTUP}$	USBFS startup time	1	μs

(1) Value guaranteed by design, not 100% tested in production.

Table 4-57. USBFS DC electrical characteristics(1)

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
Input levels	V_{DD}	USBFS operating voltage	—	3.0	—	3.6	V
	V_{DI}	Differential input sensitivity	—	0.2	—	—	
	V_{CM}	Differential common mode range	Includes V_{DI} range	0.8	—	2.5	
	V_{SE}	Single ended receiver threshold	—	0.8	—	2.0	
Output levels	V_{OL}	Static output level low	R_L of 1.5 kΩ to V_{DD}	—	—	0.2	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}	2.8	—	—	
R_{PD}		PA11, PA12(USBFS_DM/DP)	V_{IN} = V_{DD}	14.25	21	24.8	kΩ
R_{PU}		PA12(USBFS_DP)	V_{IN} = V_{SS}	0.9	1.5	1.85	

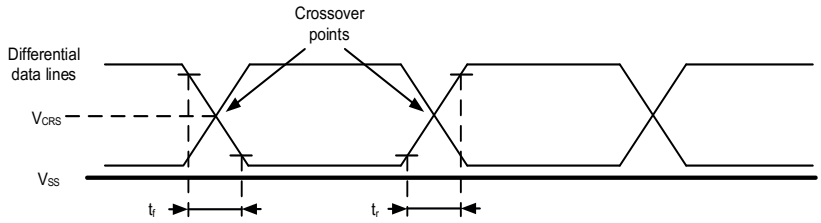
(1) Value guaranteed by design, not 100% tested in production.

Table 4-58. USBFS full speed-electrical characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_R	Rise time	C_L = 50 pF	4	—	20	ns
t_F	Fall time	C_L = 50 pF	4	—	20	ns
t_{RFM}	Rise/ fall time matching	t_R / t_F	90	—	110	%
v_{CRS}	Output signal crossover voltage	—	1.3	—	2.0	V

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-19. USBFS timings: definition of data signal rise and fall time



4.30. WDGT characteristics

Table 4-59. FWDGT min/max timeout period at 40 kHz (IRC40K)(1)

Prescaler divider	PSC[3:0] bits	Min timeout RLD[11:0]= 0x000	Max timeout RLD[11:0]= 0xFFF	Unit
1/4	0000	0.1	409.6	ms
1/8	0001	0.2	819.2	
1/16	0010	0.4	1638.4	
1/32	0011	0.8	3276.8	
1/64	0100	1.6	6553.6	
1/128	0101	3.2	13107.2	
1/256	0110	6.4	26214.4	
1/512	0111	12.8	52,428.8	
1/1024	1000	25.6	104,857.6	
1/2048	1001	51.2	209,715.2	
1/4096	1010	102.4	419,430.4	
1/8192	1011	204.8	838,860.8	
1/16384	1100	409.6	1,677,721.6	
1/32768	1101~1111	819.2	3,355,443.2	

(1) Guaranteed by design, not 100% tested in production

Table 4-60. WWDGT min-max timeout value at 140 MHz (f_{PCLK1})(1)

Prescaler divider	PSC[4:0]	Min timeout value CNT[6:0] = 0x40	Max timeout value CNT[6:0] = 0x7F	Unit
1/1	00000	0.02926	1.8725	ms
1/2	00001	0.05851	3.7450	
1/4	00010	0.11703	7.4898	
1/8	00011	0.23406	14.9796	
1/16	00100	0.46811	29.9593	
1/32	00101	0.93622	59.9186	
1/64	00110	1.8724	119.8372	
1/128	00111	3.7449	239.6745	
1/256	01000	7.4898	479.3490	
1/512	01001	14.9796	958.6980	
1/1024	01010	29.9593	1917.3961	
1/2048	01011	59.9186	3834.7922	
1/4096	01100	119.8372	7669.5844	
1/8192	01101	239.6745	15339.1689	
1/16384	01110	479.3490	30678.3378	
1/32768	01111	958.6980	61356.6756	
1/65536	10000	1917.3961	122713.3513	
1/131072	10001	3834.7922	245426.7026	
1/262144	10010~11111	7669.5844	490853.4052	

(1) Guaranteed by design, not 100% tested in production

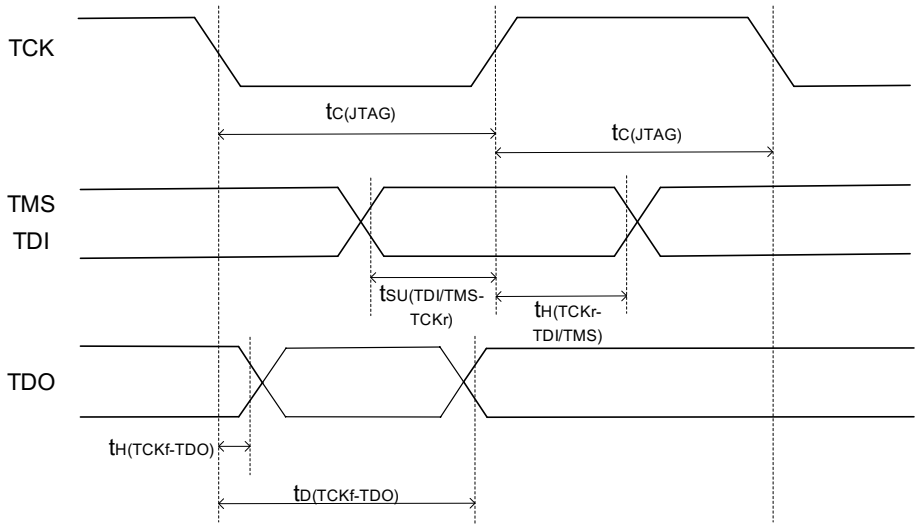
4.31. JTAG Timing

Table 4-61. JTAG Scan Interface Timing (1)

Symbol	Description	Min	Max	Unit
$t_{C(JTAG)}$	Cycle time, JTAG low and high period	20	—	ns
$t_{SU(TDI/TMS - TCKr)}$	Setup time, TDI, TMS before TCK rise (TCKr)	6	—	ns
$t_{H(TCKr -TDI/TMS)}$	Hold time, TDI, TMS after TCKr	1	—	ns
$t_{H(TCKf -TDO)}$	Hold time, TDO after TCKf	1	—	ns
$t_{D(TCKf -TDO)}$	Delay time, TDO valid after TCK fall (TCKf)	—	6	ns

(1) Guaranteed by design, not 100% tested in production

Figure 4-20. JTAG timing diagram



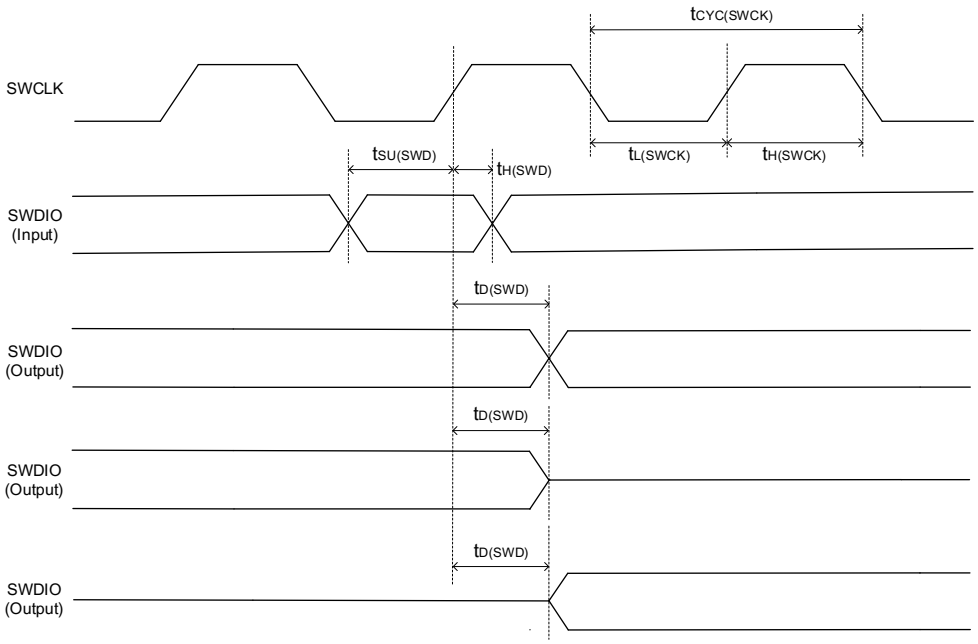
4.32. SWD Timing

Table 4-62. SWD Interface Timing (1)

Symbol	Description	Min	Max	Unit
$t_{CYC(SWCK)}$	SWCLK clock cycle time	20	—	ns
$t_{H(SWCK)}$	SWCLK clock high pulse width	8	—	ns
$t_{L(SWCK)}$	SWCLK clock low pulse width	8	—	ns
$t_{R(SWCK)}$	SWCLK clock rise time	—	1	ns
$t_{F(SWCK)}$	SWCLK clock fall time	—	1	ns
$t_{SU(SWD)}$	SWDIO setup time	6	—	ns
$t_{H(SWD)}$	SWDIO hold time	1	—	ns
$t_{D(SWD)}$	SWDIO data delay time	4	6	ns

(1) Guaranteed by design, not 100% tested in production

Figure 4-21. SWD timing diagram



5. Package information

5.1. LQFP100 package outline dimensions

Figure 5-1. LQFP100 package outline

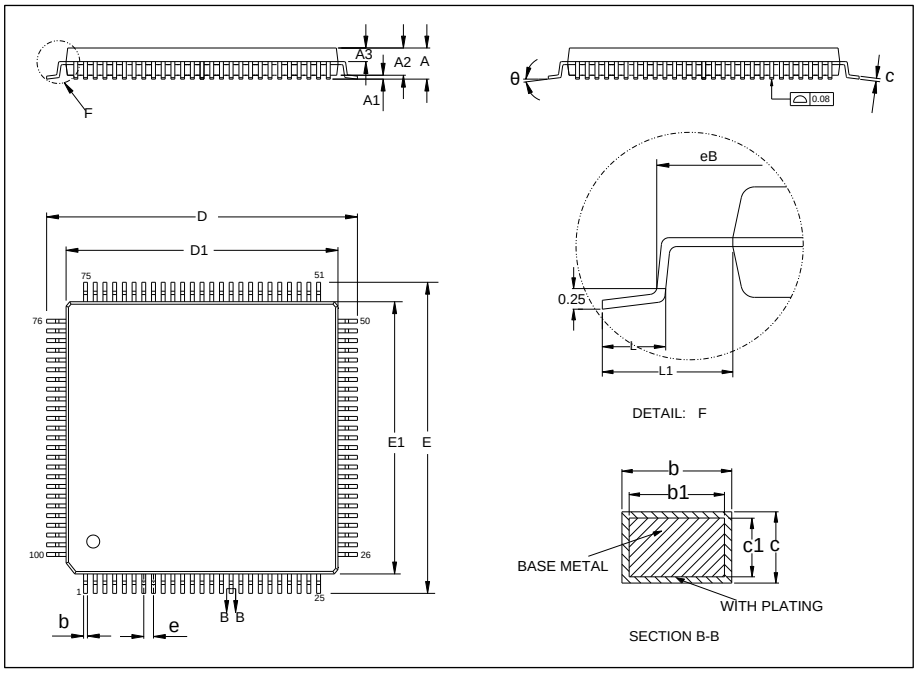
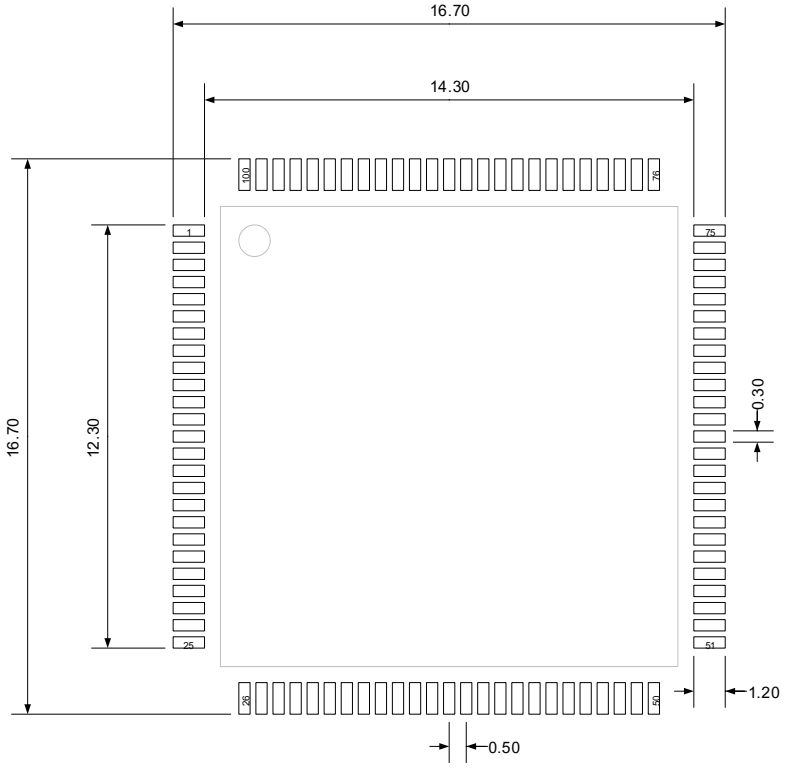


Table 5-1. LQFP100 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
e	—	0.50	—
eB	15.05	—	15.35
L	0.45	—	0.75
L1	—	1.00	—
θ	0°	—	7°

(Original dimensions are in millimeters)

Figure 5-2. LQFP100 recommended footprint



(Original dimensions are in millimeters)

5.2. LQFP64 package outline dimensions

Figure 5-3. LQFP64 package outline

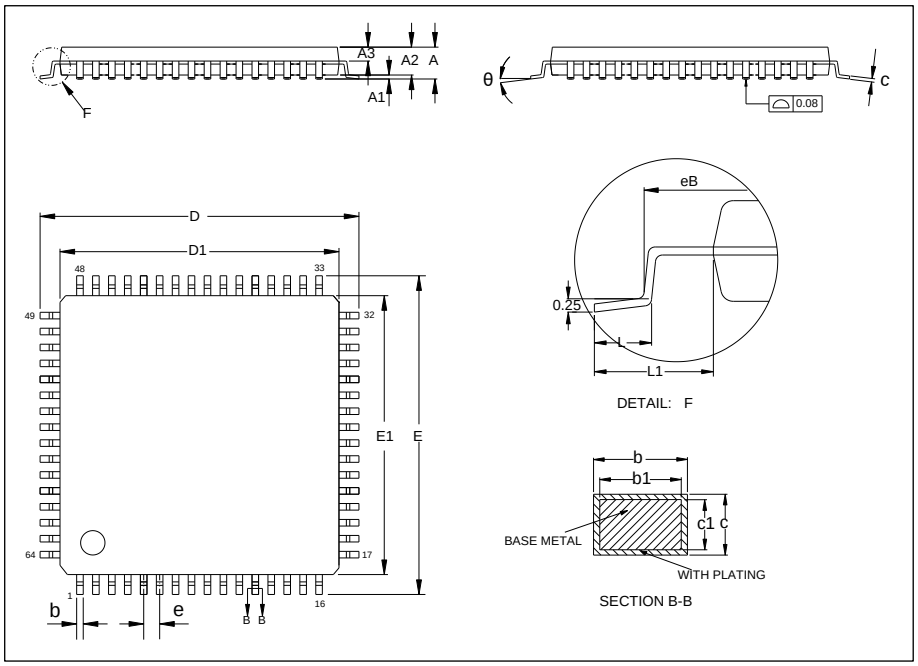
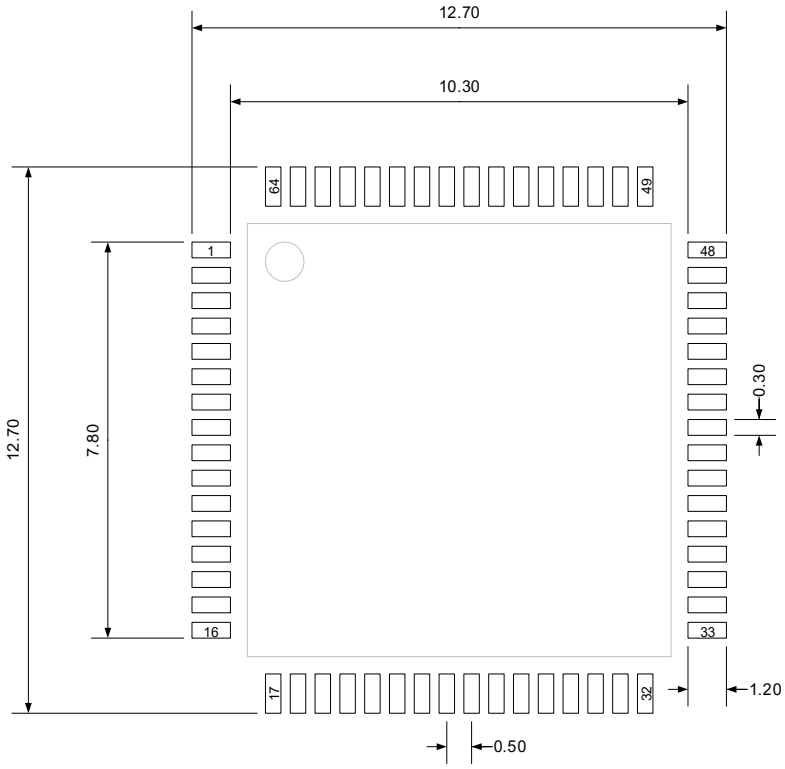


Table 5-2. LQFP64 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	—	0.50	—
eB	11.25	—	11.45
L	0.45	—	0.75
L1	—	1.00	—
θ	0°	—	7°

(Original dimensions are in millimeters)

Figure 5-4. LQFP64 recommended footprint



(Original dimensions are in millimeters)

5.3. QFN64 package outline dimensions

Figure 5-5. QFN64 package outline

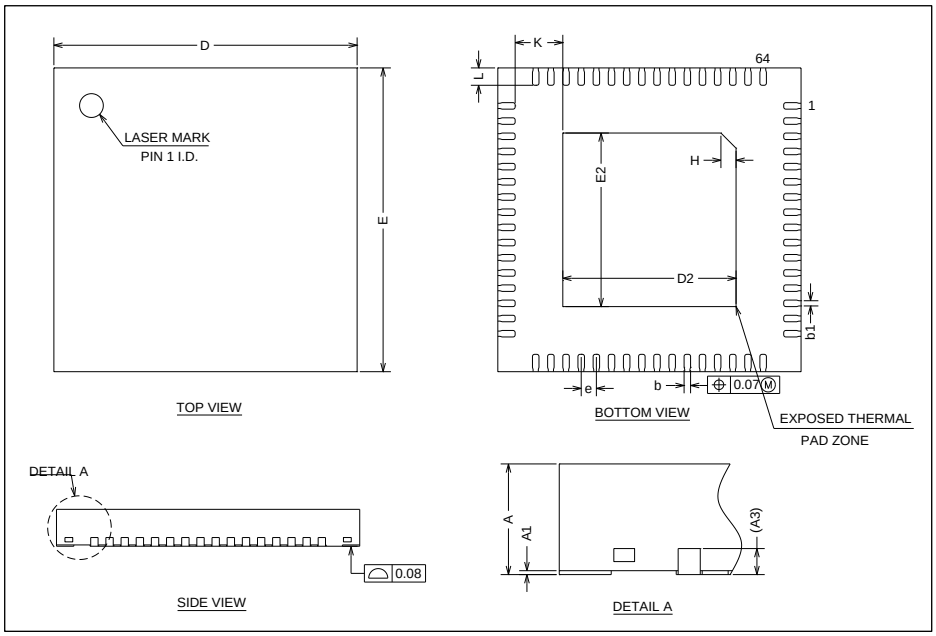
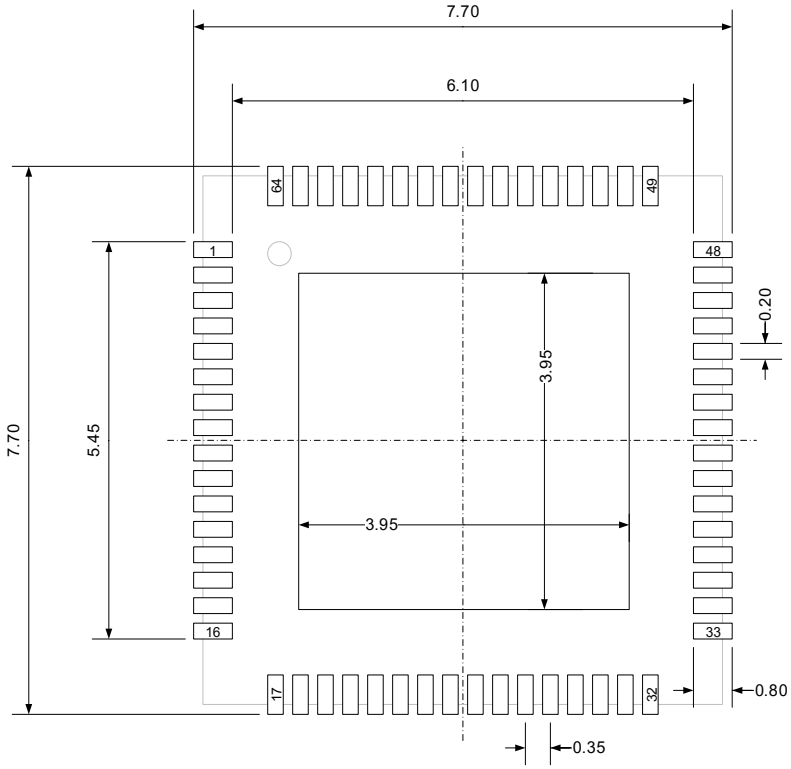


Table 5-3.QFN64 package dimensions

Symbol	Min	Typ	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	—	0.20	—
b	0.05	0.15	0.20
b1	—	0.12	—
D	6.90	7.00	7.10
D2	3.90	4.00	4.10
E	6.90	7.00	7.10
E2	3.90	4.00	4.10
e	—	0.35	—
H	0.30	0.35	0.40
K	—	1.10	—
L	0.30	0.40	0.50

(Original dimensions are in millimeters)

Figure 5-6. QFN64 recommended footprint



(Original dimensions are in millimeters)

5.4. BGA64 package outline dimensions

Figure 5-7. BGA64 package outline

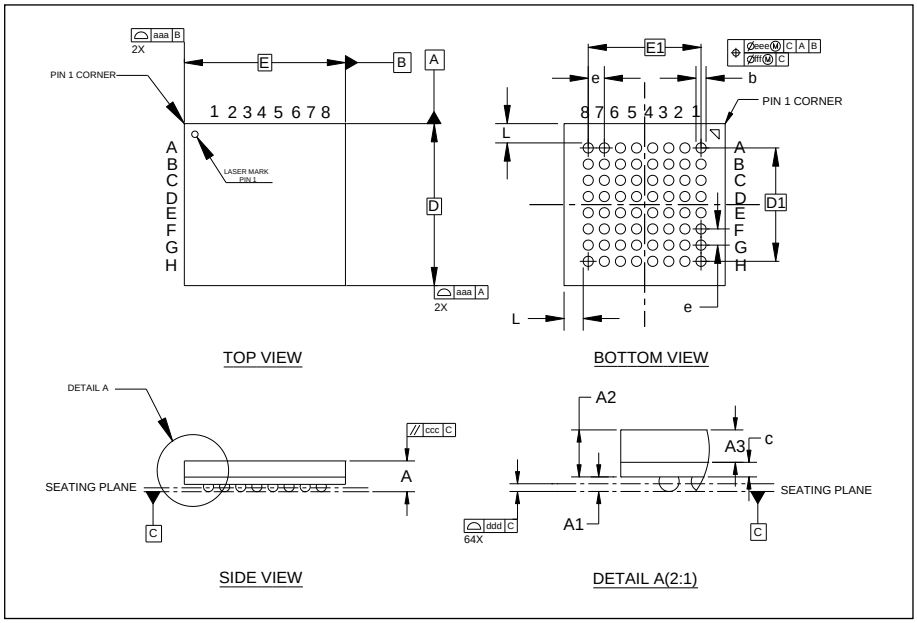
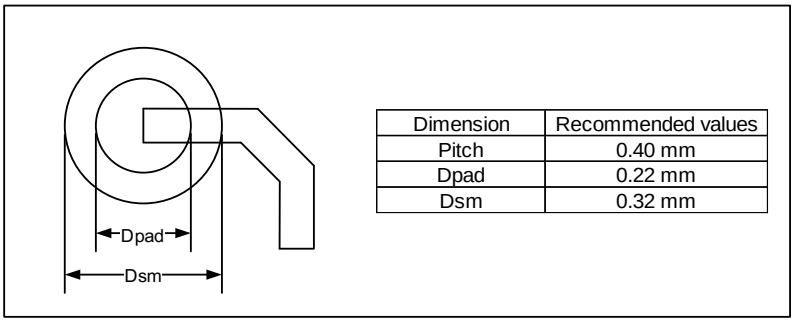


Table 5-4. BGA64 package dimensions

Symbol	Min	Typ	Max
A	0.68	0.76	0.84
A1	0.13	0.18	0.23
A2	0.53	0.58	0.63
A3	—	0.40	—
b	0.20	0.25	0.30
c	0.15	0.18	0.21
D	3.90	4.00	4.10
D1	—	2.80	—
E	3.90	4.00	4.10
E1	—	2.80	—
e	—	0.40	—
L	—	0.475	—
aaa	—	0.10	—
ccc	—	0.10	—
ddd	—	0.08	—
eee	—	0.15	—
fff	—	0.05	—

(Original dimensions are in millimeters)

Figure 5-8. BGA64 recommended footprint



Dimension	Recommended values
Pitch	0.40 mm
Dpad	0.22 mm
Dsm	0.32 mm

(Original dimensions are in millimeters)

5.5. LQFP48 package outline dimensions

Figure 5-9. LQFP48 package outline

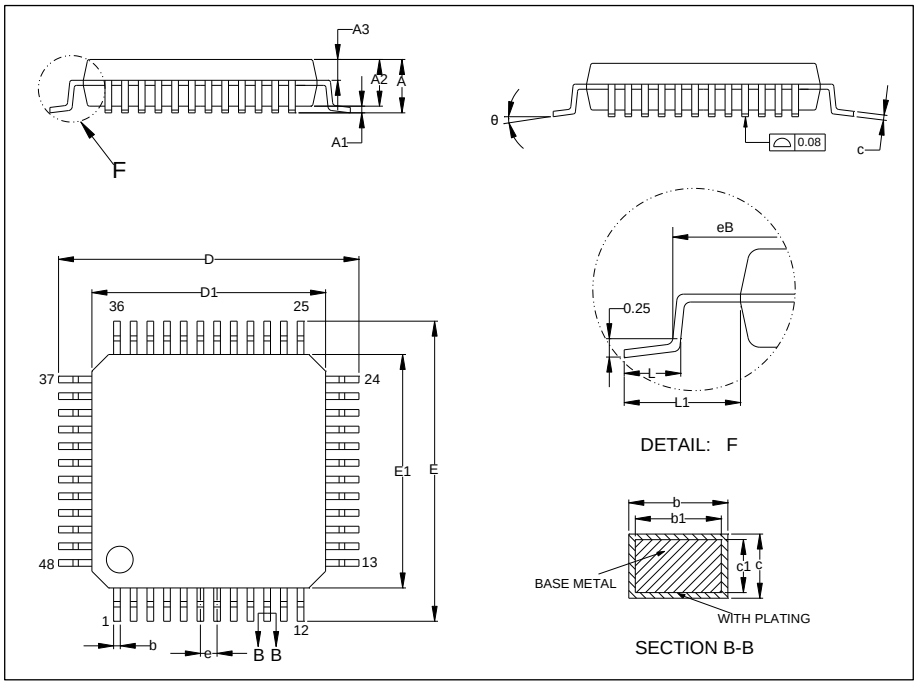
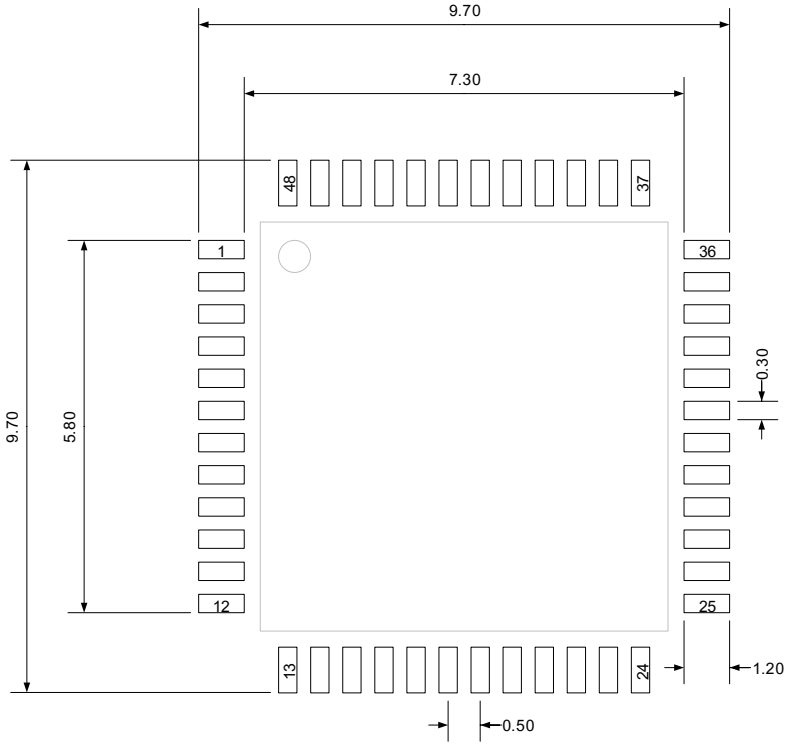


Table 5-5. LQFP48 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	—	0.50	—
eB	8.10	—	8.25
L	0.45	—	0.75
L1	—	1.00	—
θ	0°	—	7°

(Original dimensions are in millimeters)

Figure 5-10. LQFP48 recommended footprint



(Original dimensions are in millimeters)

5.6. QFN48 package outline dimensions

Figure 5-11. QFN48 package outline

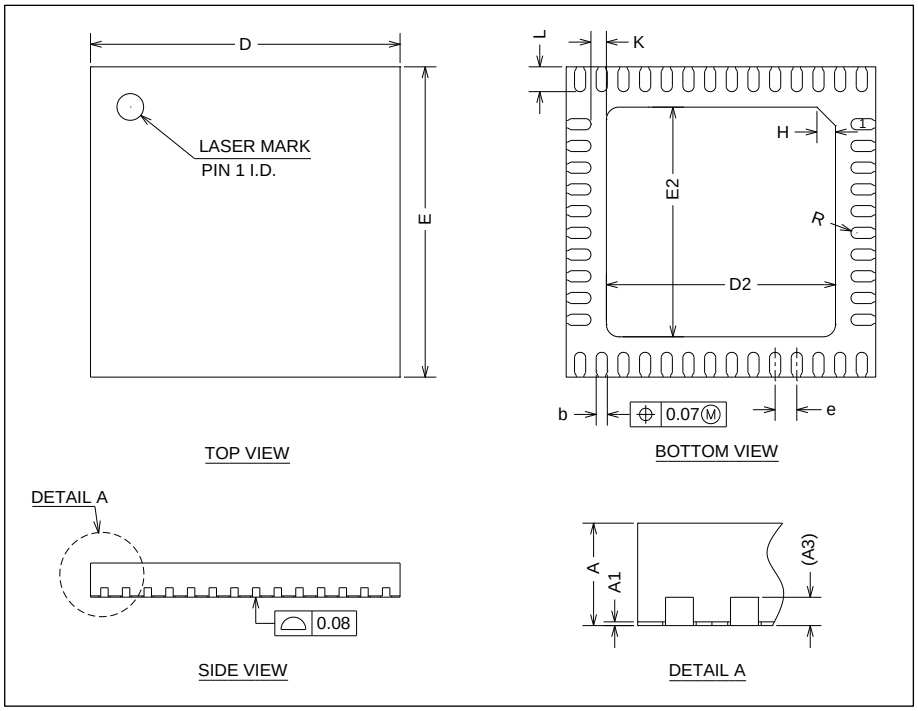
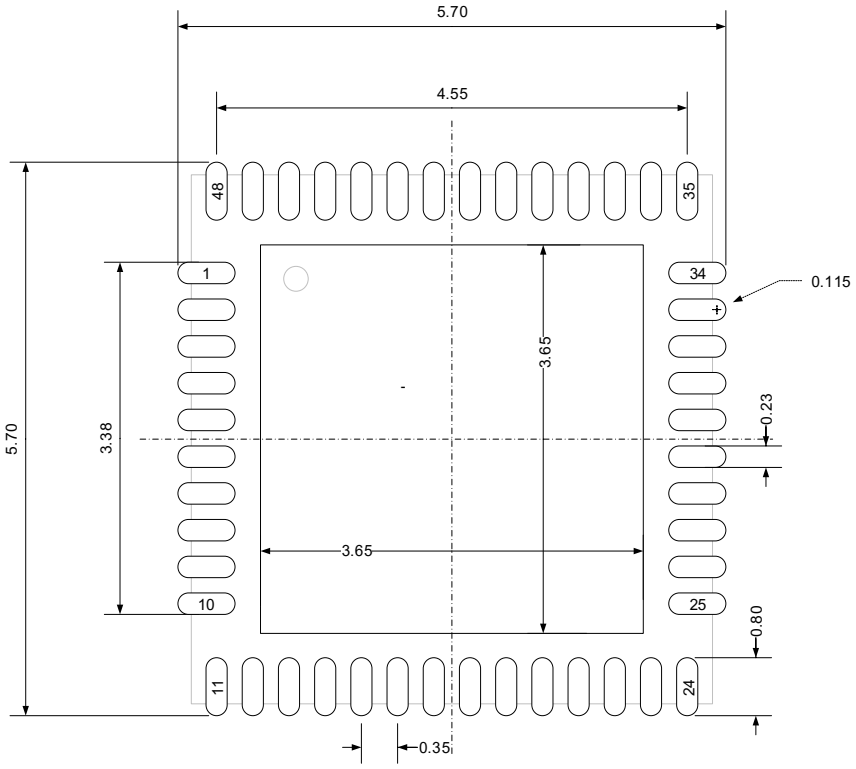


Table 5-6. QFN48 package dimensions

Symbol	Min	Typ	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	—	0.20	—
b	0.13	0.18	0.23
D	4.90	5.00	5.10
D2	3.60	3.70	3.80
E	4.90	5.00	5.10
E2	3.60	3.70	3.80
e	0.25	0.35	0.45
H	—	0.30	—
K	0.15	—	—
L	0.30	0.40	0.50
R	0.07	—	—

(Original dimensions are in millimeters)

Figure 5-12. QFN48 recommended footprint



(Original dimensions are in millimeters)

5.7. Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter "θ". For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

θ_{JA}: Thermal resistance, junction-to-ambient.

θ_{JB}: Thermal resistance, junction-to-board.

θ_{JC}: Thermal resistance, junction-to-case.

Ψ_{JB}: Thermal characterization parameter, junction-to-board.

Ψ_{JT}: Thermal characterization parameter, junction-to-top center.

$$\theta_{JA}=(T_J-T_A)/P_D \quad (5\text{-}1)$$

$$\theta_{JB}=(T_J-T_B)/P_D \quad (5\text{-}2)$$

$$\theta_{JC}=(T_J-T_C)/P_D \quad (5\text{-}3)$$

Where, T_J = Junction temperature.

T_A = Ambient temperature

T_B = Board temperature

T_C = Case temperature which is monitoring on package surface

P_D = Total power dissipation

θ_{JA} represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower θ_{JA} can be considerate as better overall thermal performance.

θ_{JB} is used to measure the heat flow resistance between the chip surface and the PCB board.

θ_{JC} represents the thermal resistance between the chip surface and the package top case. θ_{JC} is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

Table 5-7. Package thermal characteristics(1)

Symbol	Condition	Package	Value	Unit
θ_{JA}	Natural convection, 2S2P PCB	LQFP100	55.78	°C/W
		LQFP64	48.42	
		QFN64	31.01	
		BGA64	78.55	
		LQFP48	55.35	
		QFN48	33.61	

Symbol	Condition	Package	Value	Unit
θ_{JB}	Cold plate, 2S2P PCB	LQFP100	36.73	°C/W
		LQFP64	28.17	
		QFN64	19.06	
		BGA64	42.39	
		LQFP48	32.62	
		QFN48	18.43	
θ_{JC}	Cold plate, 2S2P PCB	LQFP100	21.18	°C/W
		LQFP64	17.56	
		QFN64	20.73	
		BGA64	27.66	
		LQFP48	20.82	
		QFN48	20.32	
Ψ_{JB}	Natural convection, 2S2P PCB	LQFP100	36.16	°C/W
		LQFP64	27.61	
		QFN64	18.51	
		BGA64	36.70	
		LQFP48	31.98	
		QFN48	17.90	
Ψ_{JT}	Natural convection, 2S2P PCB	LQFP100	1.65	°C/W
		LQFP64	1.49	
		QFN64	0.66	
		BGA64	1.33	
		LQFP48	1.60	
		QFN48	0.65	

(1): Thermal characteristics are based on simulation, and meet JEDEC specification.

6. Ordering information

Table 6-1. Part ordering code for GD32F505xx devices

Ordering code	Flash (KB)	Package	Package type	Temperature operating range
GD32F505VGT7	1024	LQFP100	Green	Industrial -40 °C to +105 °C
GD32F505VET7	512	LQFP100	Green	Industrial -40 °C to +105 °C
GD32F505RGT7	1024	LQFP64	Green	Industrial -40 °C to +105 °C
GD32F505RET7	512	LQFP64	Green	Industrial -40 °C to +105 °C
GD32F505RGO7	1024	QFN64	Green	Industrial -40 °C to +105 °C
GD32F505RGL7	1024	BGA64	Green	Industrial -40 °C to +105 °C
GD32F505CGT7	1024	LQFP48	Green	Industrial -40 °C to +105 °C
GD32F505CET7	512	LQFP48	Green	Industrial -40 °C to +105 °C
GD32F505CGO7	1024	QFN48	Green	Industrial -40 °C to +105 °C

7. Revision history

Table 7-1. Revision history

Revision No.	Description	Date
0.9RC1	1. Initial Release	Oct.31, 2025
0.9RC2	1. Modify the CPNs of GD32F505xx series. 2. Modify the function description of pin PC14-OSC32IN, PC15-OSC32OUT, OSCIN-PD0 and OSCOUT-PD1. 3. Change all DAC0_OUT1 to DAC0_OUT0.	Dec.2, 2025
0.9RC3	1. Update ***Figure 2-7. GD32F505Cx QFN48 pinouts***.	Dec.16, 2025
0.9RC4	1. Delete PE2 (TRACECK), PE3 (TRACED0), PE4 (TRACED1), PE5 (TRACED2), PE6 (TRACED3). 2. Change TIMER1_CH0_ETI to TIMER1_CH0 and TIMER1_ETI. 3. Modify description in ***chapter 3.14***. 4. Modify description in ***chapter 4.13***. 5. Delete alternate function EXMC_A0.	Jan.20, 2026
0.9RC5	1. Change the description of notice in ***chapter 3.4***. 2. Modify the parameter VIN in ***Table 4-2.*** 3. Add default function of PA13/PA14/PA15 in ***chapter 2.6***. 4. Add the number of 5VT GPIO in ***chapter 2.1***.	Mar.31, 2026
1.0	1. Added the FMC maximum frequency constraint in ***chapter 2.5***. 2. Updated the parameter name and description from IDDA (PLL) to IDD (PLL) in ***chapter 4.12***. 3. Updated the parameter name and description from IDDA (PLL) to IDD (PLL) in ***chapter 3.3***. 4. Separated the descriptions of VSSA and VDDA in ***chapter 3.4***. 5. Removed Table UART3/4 characteristics in ***chapter 4.25***. 6. Updated the room-temperature accuracy of $Drift_{IRC48M}$ in ***chapter 4.11***. 7. Added t_{ST} and $t_{Standby}$ for FLASH = 192 KB / 128 KB in ***chapter 4.5/4.6***. 8. Updated the description of the first parameter in J_{PLL} from Cycle-to-cycle Jitter to Period Jitter in ***chapter 4.12***.	Sep.1, 2026

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