GigaDevice Semiconductor Inc.

GD32F50x Hardware Development Guide

Application Note
AN278

Revision 1.0

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1. Introduction

This article is specially provided for developers of 32-bit general-purpose MCU GD32F50x series based on Arm® Cortex®-M33 architecture. It provides an overall introduction to the hardware development of GD32F50x series products, such as power, reset, clock, and startup mode settings and download debugging. The purpose of this application note is to allow developers to quickly get started and use GD32F50x series products, and quickly develop and use product hardware, save the time of studying manuals, and speed up product development progress.

This application note is divided into 8 parts to describe:

1. Power supply, mainly introduces the design of GD32F50x series power management, power supply and reset functions.
2. Clock, mainly introduces the functional design of GD32F50x series high and low speed clocks.
3. Boot configuration, mainly introduces the BOOT configuration and design of GD32F50x series.
4. Typical peripheral modules, mainly introduces the hardware design of the main functional modules of the GD32F50x series.
5. Download and debug circuit, mainly introduces the recommended typical download and debug circuit of GD32F50x series.
6. Reference circuit and PCB Layout design, mainly introduces GD32F50x series hardware circuit design and PCB Layout design notes.
7. Steel mesh and soldering: It mainly introduces the selection and usage method of the steel mesh and the reflow soldering temperature curves.
8. Package description, mainly introduces the package forms and names included in the GD32F50x series.

This document also satisfies the minimum system hardware resources used in application development based on GD32F50x series products.

Table 1-1. Applicable Products

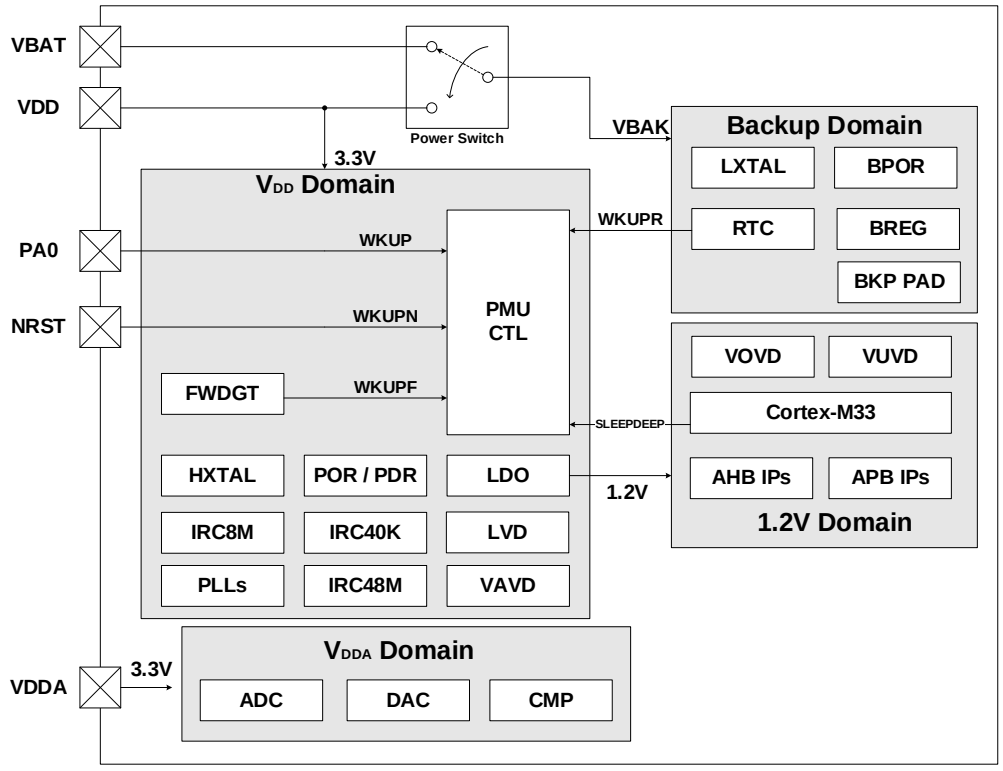
Type	Part Numbers
MCU	GD32F503xx series
	GD32F505xx series

2. Hardware design

2.1. Power supply

The V_{DD} / V_{DDA} operating voltage range of GD32F50x series products is 2.6 V ~ 3.6 V. For GD32F50x series, there are three power domains, including V_{DD} / V_{DDA} domain, 1.2V domain, and Backup domain, as is shown in ***Figure 2-1. GD32F50x Power supply overview***. The V_{DD} / V_{DDA} domain is powered directly by the power supply, and an LDO is embedded in the V_{DD} / V_{DDA} domain to power the 1.2 V domain. The backup domain power supply V_{BAK} can be powered by VDD or VBAT pin through the power switch Power Switch. When the V_{DD} power supply is turned off, the power switch can switch the power supply of the backup domain to the VBAT pin. At this time, the backup domain is powered by the VBAT pin (battery).

Figure 2-1. GD32F50x Power supply overview



LVD: Low Voltage Detector LDO: Voltage Regulator BPOR: V_{BAK} Power On Reset VOVD: $V_{1.2V}$ Over Voltage Detector
POR: Power On Reset PDR: Power Down Reset BREG: Backup registers VUVD: $V_{1.2V}$ Under Voltage Detector

2.1.1. Backup domain

The backup domain supply voltage range is 1.8 V ~ 3.6 V. In order to ensure the content of the Backup domain registers and the RTC supply, when V_{DD} supply is shut down, VBAT pin can be connected to an optional standby voltage supplied by a battery or by another source. But when V_{DD} is connected, even if the V_{BAT} pin is powered by an external battery, etc., V_{BAK}

is still powered by V_{DD}. If no external battery is used in the application, it is recommended to connect V_{BAT} pin externally to V_{DD} pin with a 100 nF external ceramic decoupling capacitor.

Note: If the V_{BAT} pin is left floating, the Power Switch will switch V_{BAK} to V_{DD} after the MCU is powered on, and the internal V_{DD} will directly supply power to the Backup domain.

2.1.2. V_{DD} / V_{DDA} Power domain

V_{DD} / V_{DDA} power domain supplies power to all areas except the backup domain. If V_{DDA} is not equal to V_{DD}, the voltage difference between the two is required to be no more than 300 mV (the internal V_{DDA} and V_{DD} are connected by back-to-back diodes). To avoid noise, V_{DDA} can be connected to V_{DD} through an external filter circuit, and the corresponding V_{SSA} is connected to V_{SS} through a specific circuit (single-point grounding, through 0 Ω resistors or magnetic beads, etc.).

In order to improve the conversion accuracy of the ADC, the independent power supply for V_{DDA} can make the analog circuit achieve better characteristics. Larger packages feature a VREFP ($V_{REFP} \leq V_{DDA}$, $V_{REFN} = V_{SSA}$) pin serving as the voltage reference source for the ADC.

GD32F50x products contain VREFP pin (for packages with at least 100 pins only), which can be powered by an external reference power supply or by being directly connected to VDDA pin.

2.1.3. Power-saving modes

GD32F50x provides three power-saving modes, namely sleep mode, deep sleep mode, and standby mode. Their comparison is listed in ***Table 2-1. Summary of Power-saving Modes***.

Table 2-1. Summary of Power-saving Modes

Mode	Sleep mode	Deep sleep mode	Standby mode
Description	Only the CPU clock is off.	1. Turn off all clocks in the 1.2 V domain. 2. Disable IRC16M, HXTAL, and PLL.	1. Power off the 1.2 V domain. 2. Disable IRC16M, HXTAL, and PLL.
LDO status	On (in normal power consumption and normal drive modes)	On (in normal/low power consumption and normal/low drive modes)	Off
Setting	SLEEPDEEP = 0	SLEEPDEEP = 1 STBMOD = 0	SLEEPDEEP = 1 STBMOD = 1, WURST = 1
Entry command	WFI or WFE	WFI or WFE	WFI or WFE
Wake-up	Wake up MCU from the sleep mode which was entered through WFI by any interrupt.	Wake up MCU from deep sleep mode which was entered through WFI by any interrupt. Wake up MCU from the deep	1. NRST pin 2. WKUP pin 3. FWDGT resetting 4. RTC

Mode	Sleep mode	Deep sleep mode	Standby mode
	Wake up MCU from the sleep mode which was entered through WFE by any event or interrupt in the case that the SEVONPEND bit is set to 1.	sleep mode which was entered through WFE by any event from EXTI or interrupt in the case that the SEVONPEND bit is set to 1.	
Delay in wake-up	None	IRC16M wake-up time The wake-up time shall be extended for LDO if it is in low power mode.	Power-on sequence

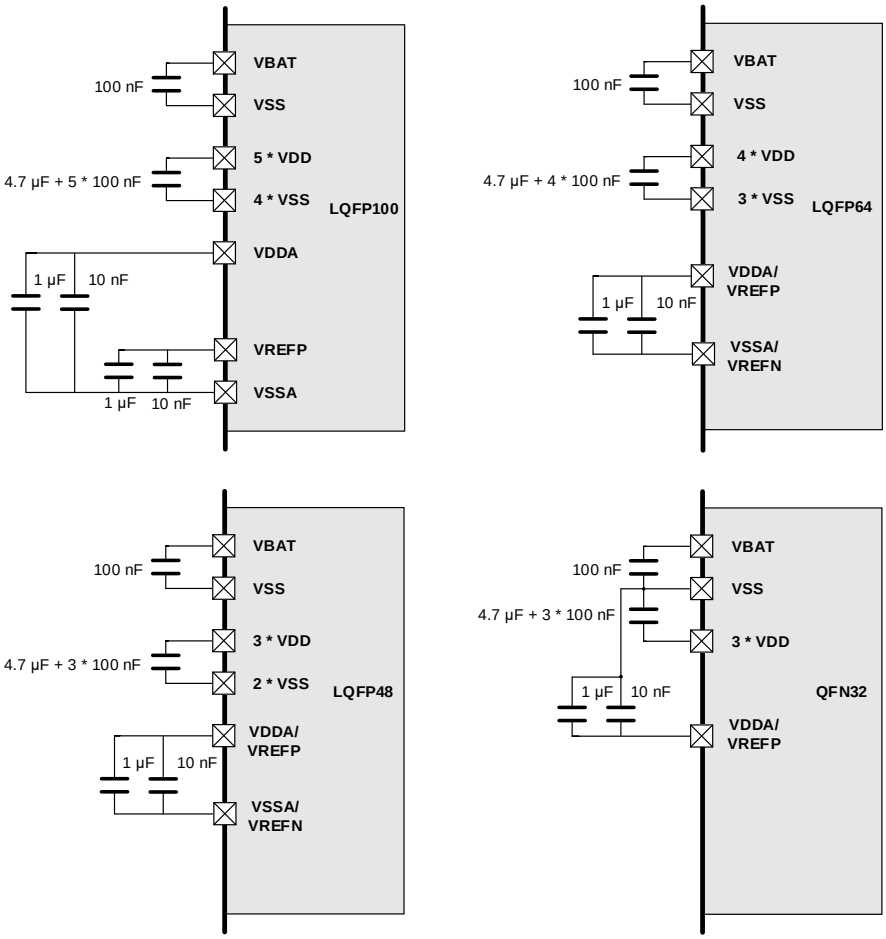
Note: In standby mode, all I/Os are in high impedance state, except NRST pin, PC13 set to function as RTC, PC14 and PC15 used as pins of LXTAL crystal oscillator, and enabled WKUP pin.

2.1.4. Power supply design

The system needs a stable power supply. There are some important things to pay attention to when developing and using:

- VDD pin must be connected to an external capacitor (N * 100 nF ceramic capacitor + not less than 4.7 uF tantalum capacitor, at least one VDD needs to be connected to GND with a capacitor of not less than 4.7 uF, and other VDD pins are connected to 100 nF).
- VDDA pin must be connected with an external capacitor (10 nF + 1 uF ceramic capacitor is recommended).
- VBAT pin must be connected to an external battery (1.8 V ~ 3.6 V). If there is no external battery, it is recommended to connect the VBAT pin to the ground through a 100 nF capacitor and then connect it to the VDD pin
- The VREFP pin voltage be directly connected to the VDDA pin, where 10 nF + 1 uF ceramic capacitors should be connected to GND.

Figure 2-2. GD32F50x Recommend Power Supply Design



Note:

1、 All decoupling capacitors need to be as close as possible to the pins on the PCB board.

2、 When the MCU power supply voltage is unstable or there is a risk of voltage drop, it is recommended to adjust the 4.7 uF capacitor not less than 10 uF.

2.2. Power detection and reset

GD32F50x series reset control includes three resets: power reset, system reset and backup domain reset. A power reset is a cold reset, which resets all systems except the backup domain. System reset works for all parts other than SW-DP controller and backup domain, including processor core and peripheral IPs. Backup domain reset works for backup area.

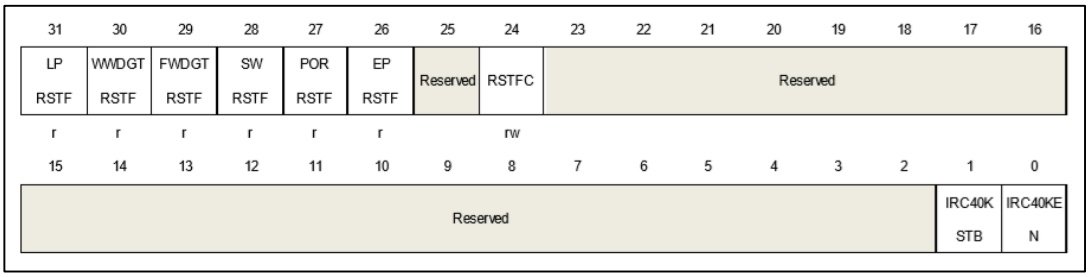
Table 2-2. Reset Contents Under Different Reset Types

Reset mode	Power reset	System reset	Backup domain reset
Reset contents	All systems except the backup domain	All parts other than SW-DP controller and backup domain, including processor core and peripheral IPs	Backup area

During the power and system reset process, NRST will maintain a low level until the reset is over. When the MCU cannot be executed, the NRST pin waveform can be monitored by an oscilloscope to determine whether the chip has been reset.

In addition, the MCU reset source can be judged by querying the register RCU_RSTSCK. This register can only clear the flag bit after a power-on reset. Therefore, during use, after the reset source is obtained, the reset flag can be cleared through the RSTFC control bit. When the watchdog is reset or other reset events, it can be more accurately reflected in the RCU_RSTSCK register.

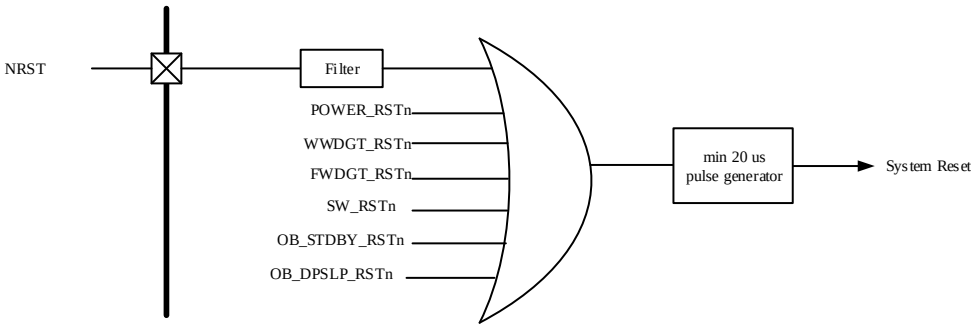
Figure 2-3. RCU_RSTSCK Register



Power supply resets are divided into 2 categories: 1. Power-on/Power-down resets (POR / PDR resets); 2. Resets generated by the internal reset generator after returning from standby mode.

MCU integrates a power-on/power-off reset circuit. When designing an external reset circuit, a capacitor (typical value of 100 nF) must be placed on the NRST pin to ensure that the power on the NRST pin generates a low pulse delay of at least 20us for completing effective power-on reset process.

Figure 2-4. System Reset Circuit



A backup domain reset is generated when one of the following events occurs:

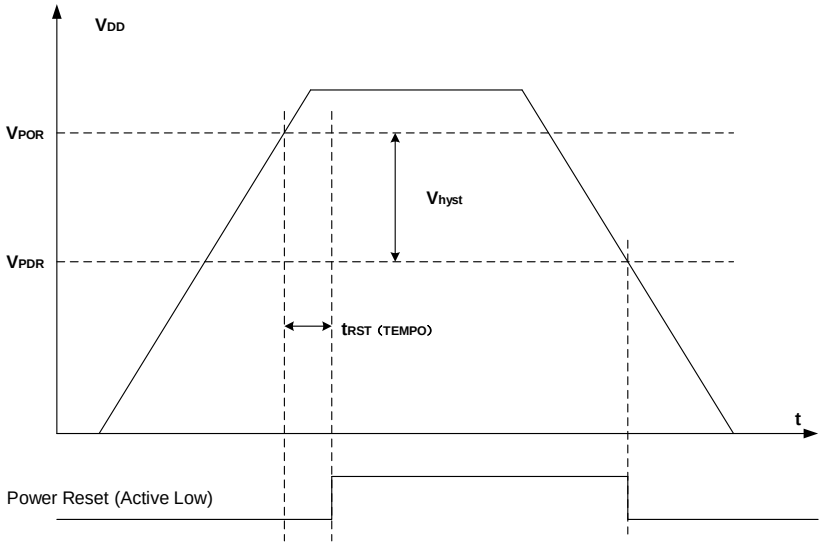
1. The BKPRST bit in the backup domain control register is set to '1';
2. Backup domain power-on reset (when both VDD and VBAT are powered down, and then VDD or VBAT is powered up).

2.2.1. POR / PDR

The chip integrates a POR / PDR (power-on/power-down reset) circuit to detect V_{DD} / V_{DDA} and generate a power reset signal to reset the entire chip except the backup domain when

the voltage is lower than a certain threshold. V_{POR} represents the threshold voltage of power-on reset, V_{PDR} represents the threshold voltage of power-down reset, V_{hyst} represents hysteresis voltage, the values of V_{POR}, V_{PDR}, V_{hyst} are refer to device datasheet.

Figure 2-5. Power-on/Power-down Reset Waveforms

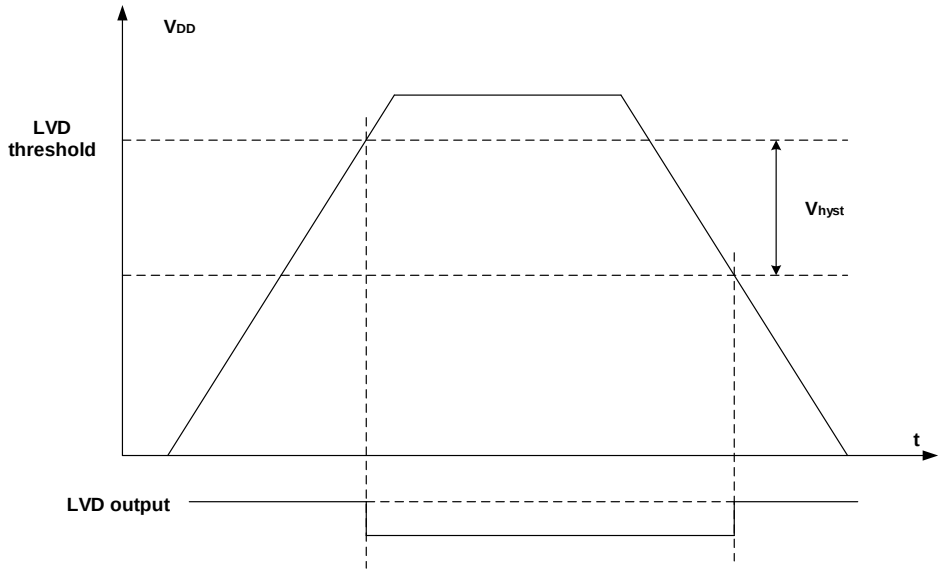


2.2.2. LVD

The function of the LVD is to detect whether the V_{DD}/V_{DDA} supply voltage is lower than the low-voltage detection threshold, which is configured by the LVDT[2:0] bits in the power control register (PMU_CTL). LVD is enabled by LVDEN setting. The LVDF bit in the power status register (PMU_CS) indicates whether a low voltage event occurs. The event is connected to the 16th line of EXTI. The user can configure the 16th line of EXTI to generate a corresponding interrupt. The value of the hysteresis voltage V_{hyst} is refer to device datasheet..

LVD application: When the MCU power supply is subject to external interference, such as a voltage drop, we can set the low voltage detection threshold (the threshold is greater than the PDR value) through LVD. Once it falls to the threshold, the LVD interrupt is turned on, which can be used in the interrupt function. Set operations such as soft reset to avoid other exceptions from the MCU.

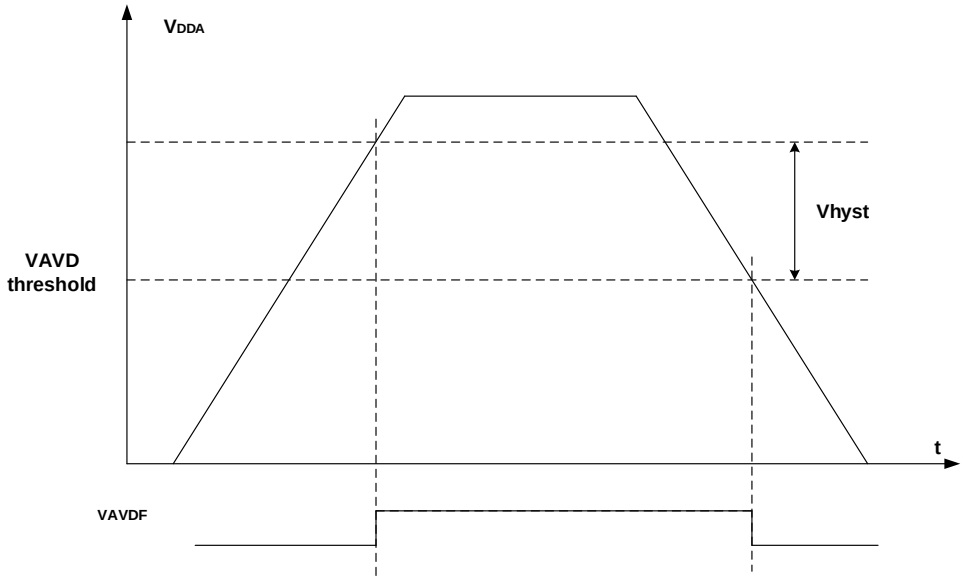
Figure 2-6. LVD Threshold Waveform



2.2.3. VAVD

The V_{DDA} analog voltage detector is used to detect whether the VDDA supply voltage is lower than a programmed threshold selected by the VAVDVC[1:0] bits in the power control register(PMU_CTL0). The VAVD is enabled by setting the VAVDEN bit, and VAVDF bit, which in PMU_CS, indicates if V_{DDA} is higher or lower than the specified VAVD threshold..*Figure 2-7. Waveform of the VAVD threshold* shows the relationship between the VAVD threshold and the VAVDF The hysteresis voltage (Vhyst) please refer to device datasheet.

Figure 2-7. Waveform of the VAVD threshold



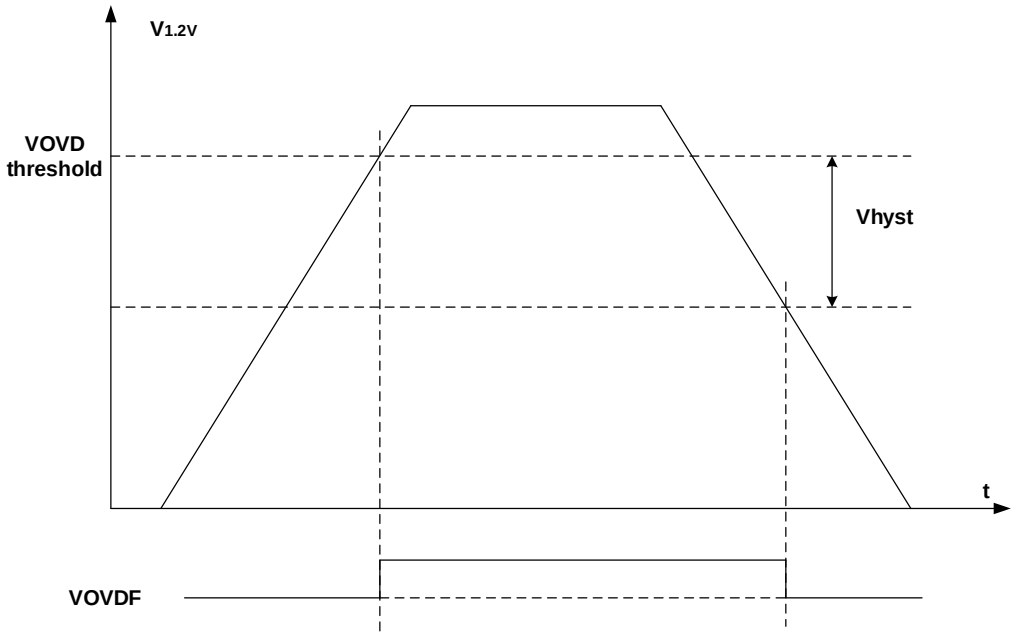
2.2.4. VOVD and VUVD

VUVD ($V_{1.2V}$ Under Voltage Detector) and VOVD($V_{1.2V}$ Over Voltage Detector) are used to

monitor voltage of 1.2 V power domain. Once the 1.2V is powered up, the POR will generate a reset sequence on the 1.2V power domain. If need to enter the expected power saving mode, the associated control bits must be configured. Then, once a WFI (Wait for Interrupt) or WFE (Wait for Event) instruction is executed, the device will enter an expected power saving mode. The voltage of this power domain can be configured by LDOVS[2:0] in the PMU CTL0 register.

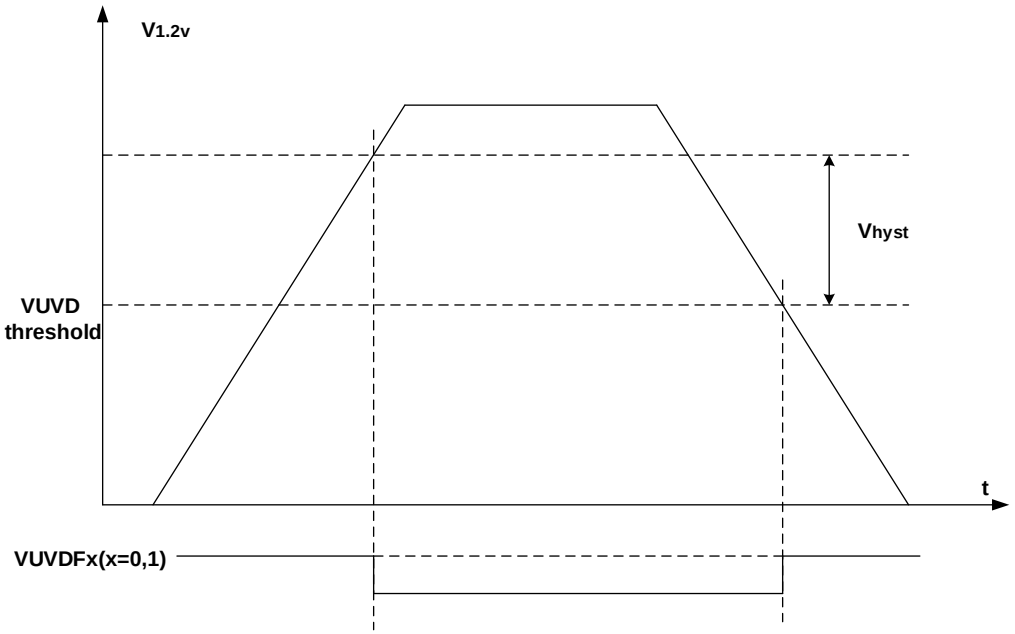
There is an internal 1.2V power over voltage detector, when VOVDEN is 0b1, it means 1.2V power over voltage detector is enabled. Once V1.2V power domain is over than a programmed threshold selected by the VOVDVC[1:0] bits in the power control register(PMU_CTL0), VOVDF0 will be set immediately after two flip-flops synchronization of the analog output. VOVDF1 will be set after digital filter which can be used by configuring the VOVDO_DNF[7:0]bit in PMU_CTL1 register.This allows to suppress spikes with a programmable length of 1 to 255 of 1024* T_{pclk} The hysteresis voltage (Vhyst) please refer to device datasheet.

Figure 2-8. Waveform of VOVD



There is an internal 1.2V power under voltage detector, when VUVDEN is 0b1, it means 1.2V power under voltage detector is enabled. Once $V_{1.2V}$ power domain is lower than a programmed threshold selected by the VUVDVC[1:0] bits in the power control register(PMU_CTL0), VUVDF0 will be set immediately after two flip-flops synchronization of the analog output, VUVDF1 will be set after digital filter which can be used by configuring the VUVDO_DNF[7:0] bits in PMU_CTL1 register.This allows to suppress spikes with a programmable length of 1 to 255 of 1024* T_{pclk} VUVDF1 interrupt is internally connected. The hysteresis voltage (Vhyst) please refer to device datasheet.

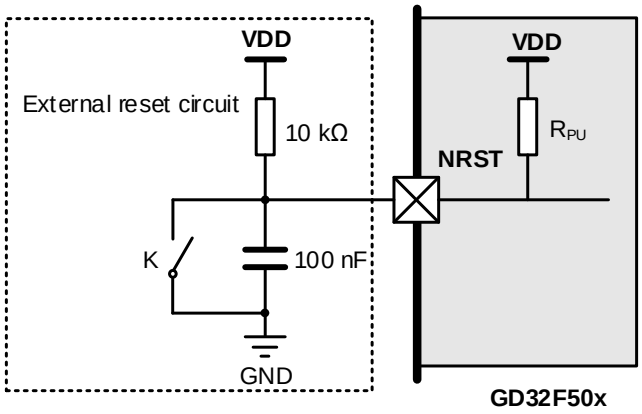
Figure 2-9. Waveform of VUVD



2.2.5. NRST Pin

For the MCU's NRST pin, it is recommended to place a capacitor (typically 100 nF) to prevent accidental reset triggering.

Figure 2-10. Recommend External Reset Circuit



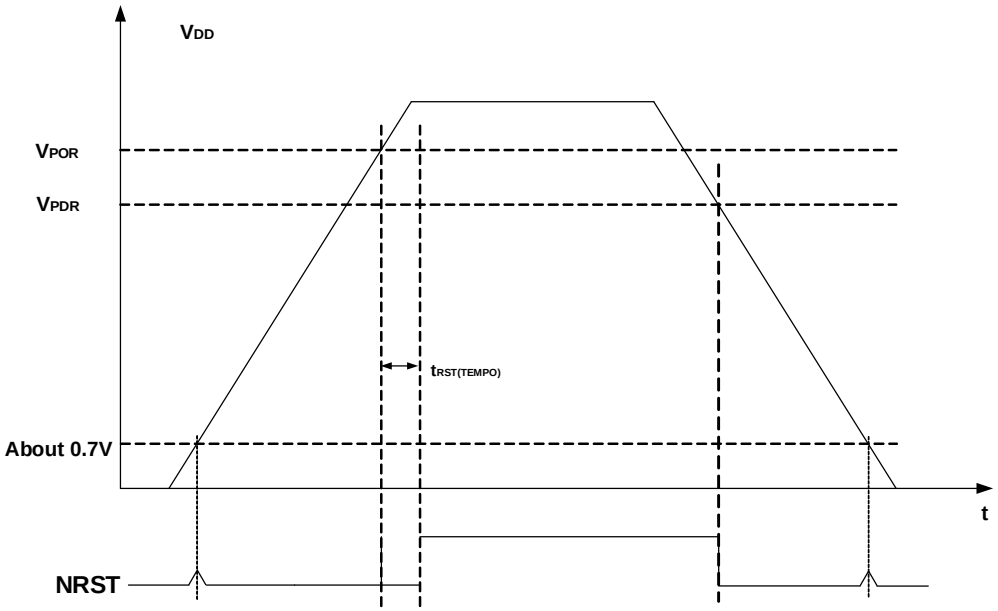
Note:

1. The internal pull-up resistor is 40 kΩ and external pull-up resistor is recommended to be 10 kΩ, so that voltage interference will not cause the chip to work abnormally.
2. If the influence of static electricity is considered, an ESD protection diode can be placed at the NRST pin(For additional hardware protection design guidelines, please refer to the official application note ***AN163 GD32 MCU EMC Hardware Protection Design Reference***).
3. Although there is a hardware POR circuit inside the MCU, it is still recommended to add an external NRST reset resistor-capacitor circuit.

4. If the MCU starts abnormally (due to voltage fluctuations, etc.), the capacitance value of NRST to ground can be appropriately increased, and the MCU reset completion time can be extended to avoid the abnormal power-on sequence area.

Due to the threshold voltage characteristics of the MOS tube, when VDD/VDDA < 0.7V during the chip power-on and power-off process, pulling down the MOS tube inside the chip will not pull down the NRST pin. That is, when VDD/VDDA ≈ 0.7V is used during the chip power-on and power-off process, a tiny pulse will occur, which does not affect the normal operation of the chip, as shown in ***Figure 2-11. NRST Pin Power-on and Power-off MOS Tube Pulse Diagram***.

Figure 2-11. NRST Pin Power-on and Power-off MOS Tube Pulse Diagram



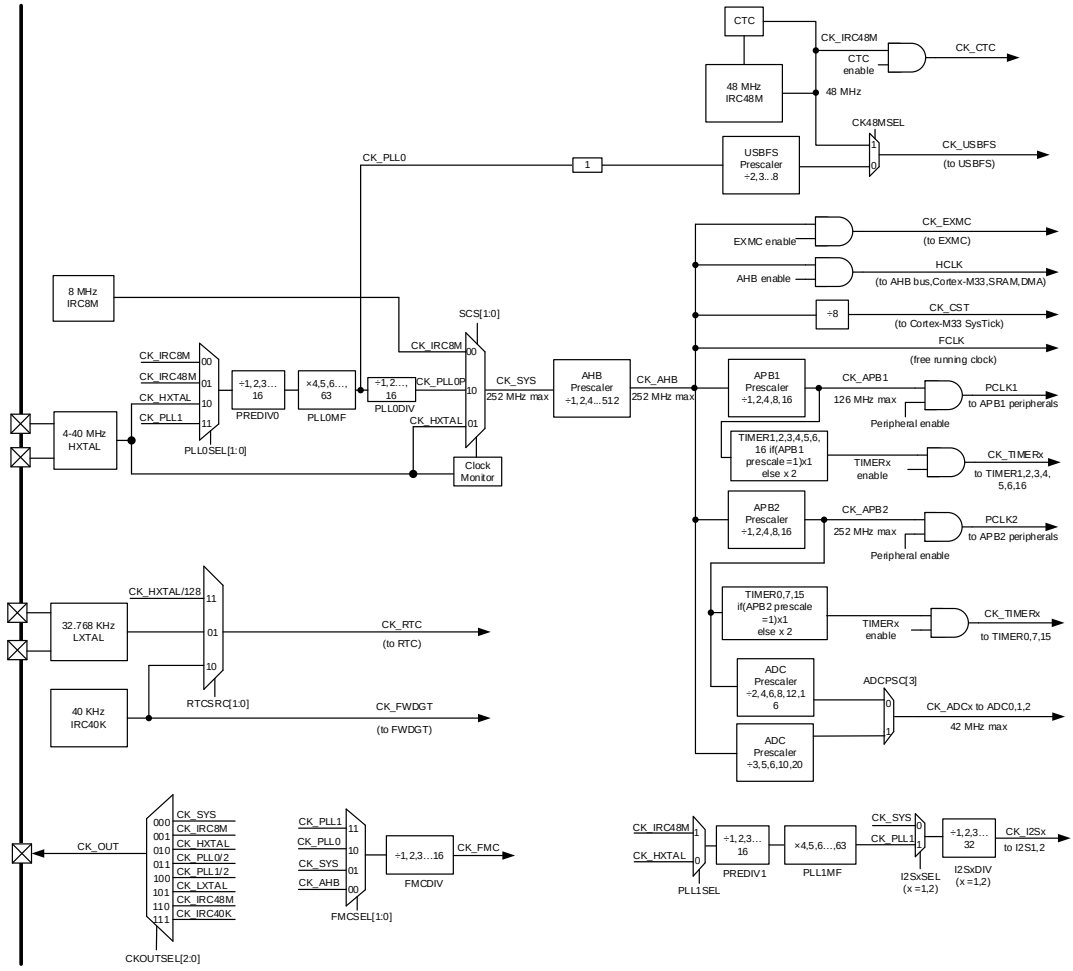
Due to the difference in charging and discharging speed, the pulse duration of the falling edge is longer than that of the rising edge, and the duration of both is ms class.

2.3. Clock

GD32F50x series has a complete clock system inside. You can choose the appropriate clock source according to different applications. The main features of the clock are:

- 4 - 40 MHz external high-speed crystal oscillator (HXTAL)
- 8 MHz internal high-speed RC oscillator (IRC8M)
- 48 MHz internal high-speed RC oscillator (IRC48M)
- 32.768 kHz external low-speed crystal oscillator (LXTAL)
- 40 kHz internal low speed RC oscillator (IRC40K)
- PLL0 clock source can be selected from HXTAL, IRC8M or IRC48M
- HXTAL clock can be monitored
- LXTAL clock can be monitored
- Clock frequency can be monitored

Figure 2-12. GD32F50x Clock Tree



Clock circuit hardware protection design guidelines, please refer to the official application note ***AN163 GD32 MCU EMC Hardware Protection Design Reference***.

2.3.1. External high-speed crystal oscillator clock (HXTAL)

4 - 40 MHz external high-speed crystal oscillator (passive crystal) can provide accurate master clock for the system. The crystal for that specific frequency must be placed close to the HXTAL pin, and the external resistors and matching capacitors connected to the crystal must be adjusted according to the chosen oscillator parameters. HXTAL can also use the bypass input mode to input the clock sourc. When the bypass input is used, the signal is connected to OSC_IN, and OSC_OUT remains floating. The Bypass function of HXTAL needs to be turned on in software (enable the HXTALBPS bit in RCU_CTL).

Figure 2-13. HXTAL External Crystal Circuit

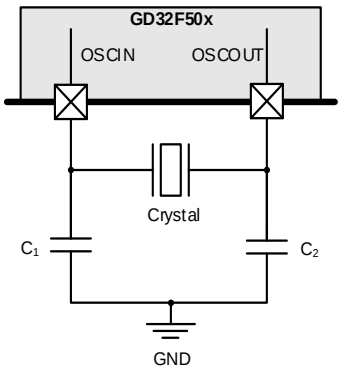
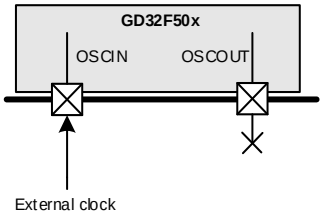


Figure 2-14. HXTAL External Clock Circuit in Bypass Mode



Note:

1. When using the bypass input, the signal is input from OSC_IN, and OSC_OUT remains floating.
2. For the size of the external matching capacitor, please refer to the formula: $C_1 = C_2 = 2*(C_{LOAD} - C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, with a typical value of 10 pF. When it is recommended to use an external high-speed crystal, try to choose a crystal load capacitance of about 20 pF, so that the external matching capacitors C_1 and C_2 can be 20 pF, and the PCB layout should be as close as possible to the crystal pin.
3. C_S is the parasitic capacitance on the PCB board traces and IC pins. The closer the crystal is to the MCU, the smaller the C_S, and vice versa. Therefore, in practical applications, when the crystal is far away from the MCU and causes the crystal to work abnormally, the external matching capacitor can be appropriately reduced.
4. When using an external high-speed crystal, it is recommended to connect a 1 MΩ resistor in parallel at both ends of the crystal to make the crystal easier to vibrate.
5. Accuracy: external active crystal > external passive crystal > internal IRC8M.
6. When the active crystal oscillator is used normally, Bypass will be turned on. At this time, the high level is required to be no less than 0.7 V_{DD}, and the low level is no more than 0.3 V_{DD}.
7. The wires between the resonator and MCU clock pins, namely the wires to OSC_OUT and OSC_IN pins of MCU, may have different lengths due to spatial limit of PCB layout. As a result, the stray capacitance introduced by the two PCB wires will be inconsistent,

resulting in unequal load capacitance values on both sides of the resonator. This difference is required to match the actual PCB. In this case, it is recommended to contact the resonator manufacturer to measure the actual value.

2.3.2. External low-speed crystal oscillator clock (LXTAL)

LXTAL crystal is a 32.768kHz low-speed external crystal, which can provide a low-power and high-precision clock source for RTC. The RTC module of the MCU is equivalent to a counter, and the accuracy will be affected by the crystal performance, matching capacitance and PCB material. If you want to obtain better accuracy, it is recommended to connect PC13 to the timer input capture pin during circuit design. TIMER to calibrate LXTAL, and set the frequency division register of RTC according to the calibration situation. LXTAL can also support bypass clock input (active crystal oscillator, etc.), which can be enabled by configuring the LXTALBPS bit in RCU_BDCTL.

Figure 2-15. LXTAL External Crystal Circuit

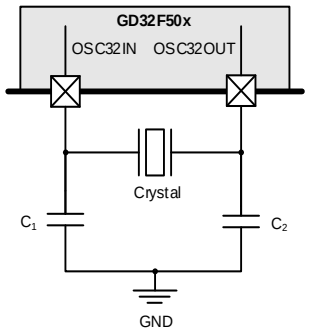
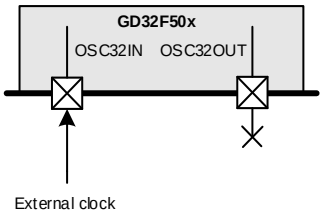


Figure 2-16. LXTAL External Clock Circuit in Bypass Mode



Note:

1. When using the bypass input, the signal is input from OSC32_IN, and OSC32_OUT remains floating.
2. For the size of the external matching capacitor, please refer to the formula: $C_1 = C_2 = 2 * (C_{LOAD} - C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, the empirical value is between 2 pF – 7 pF, and 5 pF is recommended as a reference value calculation. When it is recommended to use an external crystal, try to choose a crystal load capacitance of about 10 pF, so that the externally connected matching capacitors C_1 and

C_2 can be 10 pF, and the PCB layout should be as close to the crystal pin as possible.

3. When the RTC selects IRC40K as the clock source and uses the V_{BAT} external independent power supply, if the MCU is powered off at this time, the RTC will stop counting. After the power is re-energized, the RTC will continue to accumulate the counting value according to the previous count value. If the application needs to use V_{BAT} to power the RTC, the RTC can still time normally, and the RTC must select LXTAL as the clock source.
4. The drive capability of LXTAL can be set in MCU. If it is difficult for an external low-speed crystal to start oscillation during actual debugging, the drive capability of LXTAL can be adjusted to high drive capability.
5. The wires between the resonator and MCU clock pins, namely the wires to OSC_OUT and OSC_IN pins of MCU, may have different lengths due to spatial limit of PCB layout. As a result, the stray capacitance introduced by the two PCB cables will be inconsistent, resulting in unequal load capacitance values on both sides of the resonator. A difference is required to match the actual PCB. In this case, it is recommended to contact the resonator manufacturer to measure the actual value.

2.3.3. Clock output capability (CKOUT)

There are several clock signals can be selected via the CK_OUT clock source selection bits, CKOUTSEL, in the clock configuration register 0 (RCU_CFG0). The corresponding GPIO pin should be configured in the properly alternate function I/O (AFIO) mode to output the selected clock signal.

Table 2-3. Clock output source select

Clock Source Selection bits	Clock Source
000	CK_SYS
001	CK_IRC8M
010	CK_HXTAL
011	CK_PLL0/2
100	CK_PLL1/2
101	CK_LXTAL
110	CK_IRC48M
111	CK_IRC40K

2.3.4. HXTAL Clock monitor (HCKM)

The HXTAL clock monitor function is enabled by the HXTAL clock monitor enable bit, HCKMEN, in the control register (RCU_CTL). This function should be enabled after the HXTAL start-up delay and disabled when the HXTAL is stopped. Once the HXTAL failure is detected, the HXTAL will be automatically disabled. The HXTAL clock stuck interrupt flag, HCKMIF, in the clock interrupt register, RCU_INT, will be set and the HXTAL failure event will be generated. This failure interrupt is connected to the non-maskable interrupt, NMI, of the Cortex®-M33. If the HXTAL is selected as the clock source of CK_SYS, PLL and CK_RTC,

the HXTAL failure will force the CK_SYS source to IRC8M, the PLL will be disabled automatically. If the HXTAL is selected as the clock source of PLL, the HXTAL failure will force the PLL closed automatically. If the HXTAL is selected as the clock source of RTC, the HXTAL failure will reset the RTC clock selection.

2.3.5. LXTAL Clock monitor (LCKM)

A clock monitor on LXTAL can be activated by software writing the LCKMEN bit in the backup domain control register (RCU_BDCTL). LCKMEN can not be enabled before LXTAL is enabled and ready.

The clock monitor on LXTAL is working in all modes except V_{BAT}. If a failure is detected on the external 32 kHz oscillator, an interrupt can be sent to CPU.

The software must then disable the LCKMEN bit, stop the defective external 32 kHz oscillator, and change the RTC clock source, or take any required action to secure the application.

A 4-bits plus one counter will work at IRC40K domain when LCKMD enable. If the LXTAL clock has stuck at 0/1 error or slow down about 20 kHz, the counter will overflow. The LXTAL clock failure will been found. Once the LXTAL failure is detected, the LXTAL clock stuck interrupt flag, LCKMIF, in the clock interrupt register, RCU_INT, will be set and the LXTAL failure event will be generated.

2.3.6. Clock frequency monitor (CKFM)

The clock frequency monitor can use IRC48M to monitor IRC8M, HXTAL, PLL0P and PLL1 clock frequency range. For IRC8M and HXTAL, 1000 IRC48M clock cycle is used as the monitor window. For PLL0P and PLL1, 100 IRC48M clock cycle is used as the monitor window. User can configure the monitoring range of the clock frequency by configuring the RCU_CKFMCFGx (x = 0, 1, 2, 3) register. If the corresponding interrupt is enabled and the clock frequency failure flag is set, the interrupt will be occurred.

When the IRC48M clock is disabled or lost, the clock frequency monitor is invalid.

2.4. Startup Configuration

The GD32F50x devices provide four kinds of boot sources. The boot mode is influenced by Security Protection, NBTSB and BTFOSEL bits in OTP3, and Boot pins. The details are shown in the following table ***Table 2-4. Boot modes***.

The value on the BOOT0 and BOOT1 pins is latched on the 4th rising edge of CK_SYS after a reset. It is up to the user to set the BOOT0 and BOOT1 pins after a power-on reset or a system reset to select the required boot source. Once the two pins have been sampled, they are free and can be used for other purposes.

Table 2-4. Boot modes

Security protection	OTP3		Boot pin		BOOT_MODE[2:0]	Boot Select
	NBTSB	BTFOSEL	BOOT0	BOOT1		
No protection/ Protection level low	0	x	1	1	011	SRAM
No protection/ Protection level low	0	x	1	0	001	BootLoader
No protection/ Protection level low	0	0	0	x	000	Main Flash
No protection/ Protection level low	0	1	0	x	101	OTP1
x	1	0	x	x	000	Main Flash
x	1	1	x	x	101	OTP1
Protection level high	x	0	x	x	000	Main Flash
Protection level high	x	1	x	x	101	OTP1

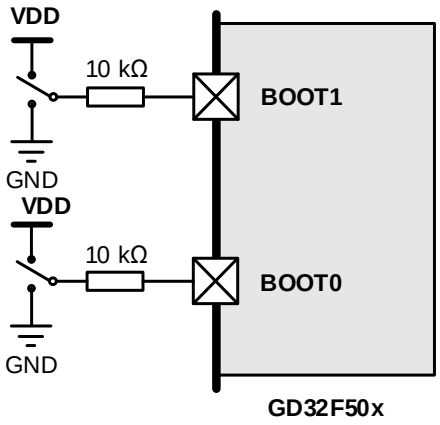
After power-on sequence or a system reset, the Arm® Cortex®-M33 processor fetches the top-of-stack value from address 0x0000 0000 and the base address of boot code from 0x0000 0004 in sequence. Then, it starts executing code from the base address of boot code.

The corresponding memory space of the selected boot source is aliased in the boot memory space which begins at the address 0x0000 0000. When the on-chip SRAM is selected as the boot source, in the application initialization code, you have to relocate the vector table in SRAM using the NVIC exception table and the offset register.

When the main flash memory is selected to be the boot source, the memory space beginning at the address 0x0800 0000 is aliased in the boot memory space. When OTP1 is selected to be the boot source, the memory space beginning at the address 0x1FF0 0000 is aliased in the boot memory space.

The embedded boot loader is located in the System memory, which is used to reprogram the Flash memory.GD32F50x MCU embedded bootloader supports multi interfaces to update the Flash memory. There will be USART port, and standard USB port can be used on GD32F50x line products.

Figure 2-17. Recommend BOOT Circuit Design



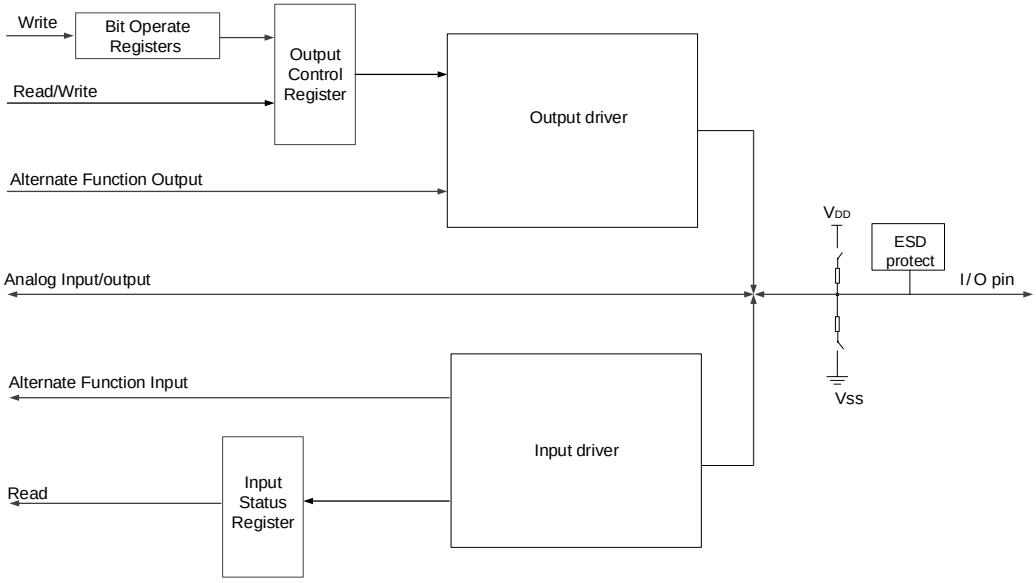
Note: After the MCU is running, if the BOOT status is changed, it will take effect after the system is reset.

2.5. Typical Peripheral Modules

2.5.1. GPIO Circuit

There are up to 80 general purpose I/O pins (GPIO), named PA0 ~ PA15, PB0 ~ PB15, PC0 ~ PC15, PD0 ~ PD15, PE0 ~ PE15 for the device to implement logic input/output functions. Each GPIO port has related control and configuration registers to satisfy the requirements of specific applications. The external interrupt on the GPIO pins of the device have related control and configuration registers in the Interrupt/event Controller Unit (EXIT), the basic structure of GPIO port is shown in ***Figure 2-18. Basic Structure of Standard IO***.

Figure 2-18. Basic Structure of Standard IO



Note:

1. The IO port is divided into 5 V tolerance and non-5 V tolerance. When using, pay attention to distinguish the voltage tolerance of the IO port, see Datasheet for details.
2. When the 5 V-tolerant IO port is directly connected to 5 V, it is recommended that the IO port be configured in open-drain mode and externally pull up to work.
3. During or after the IO port is powered on and reset, the default mode is floating input, and the level characteristics are uncertain. In order to obtain more consistent power consumption, it is recommended that all IO ports be configured as analog inputs and then modified to the corresponding mode according to application requirements (chip Ports that are not exported internally also need to be configured).
4. To improve EMC performance, it is recommended to pull up or pull down the unused IO pins by hardware.
5. The drive capability of the three IO ports PC13, PC14, and PC15 is weak, and the output current capability is limited (about 3 mA). When configured in output mode, the operating speed cannot exceed 2 MHz (the maximum load is 30 pF).
6. The same label PIN in multiple groups can only configure one port as an external interrupt. For example, PA0, PB0, and PC0 only support one of the three IO ports to generate external interrupts, and do not support three external interrupt modes.
7. For 5VT IO, it may introduce sink current when the voltage of the IO is beyong V_{DD}.
8. It is recommended to install ESD protection circuit close to the external end for pins that need to be connected to external devices, switches, or keys.For additional hardware protection design guidelines, please refer to the official application note ***AN163 GD32 MCU EMC Hardware Protection Design Reference***.

2.5.2. USART / UART Circuit

Universal Synchronous Asynchronous Receiver Transmitter (USART) provides a flexible and convenient serial data exchange interface, and data frames can be transmitted in full-duplex or half-duplex, synchronous or asynchronous mode. The USART provides a programmable baud rate generator that divides the system clock to generate the specific frequency required for USART transmission and reception.

USART not only supports the standard asynchronous transceiver mode, but also implements some other types of serial data exchange modes, such as infrared coding specification, SIR, smart card protocol, LIN, and synchronous single-duplex mode. It also supports multiprocessor communication and Modem flow control operation (CTS / RTS). Data frames support transmission from the LSB or MSB. Both the polarity of the data bits and the TX / RX pins can be flexibly configured.

USART supports DMA function to realize high-speed data communication, except UART4.

Table 2-5. USART/UART Important Pin Description

Pin	Type	Description
RX	Input	Receive data
TX	Output	Send data, when USART is enabled, if

Pin	Type	Description
	I/O (Single-Wire Mode/Smart Card Mode)	no data is sent, the default is high level.
CK	Output	Serial clock signal for synchronous communication
nCTS	Input	Hardware flow control mode send enable signal
nRTS	Output	Hardware flow control mode send request signal

See ***Figure 2-19. USART/UART reference circuit without flow*** control, ***Figure 2-20. USART reference circuit with flow control***, ***Figure 2-21. USART reference circuit*** for cross connection of pins when using USART / UART.

Figure 2-19. USART/UART reference circuit without flow control

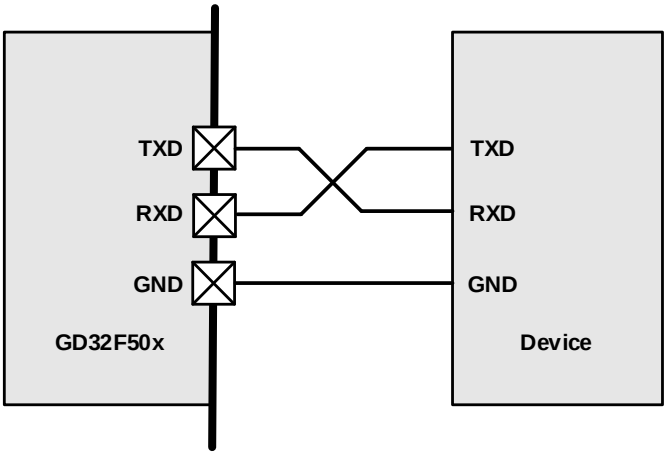


Figure 2-20. USART reference circuit with flow control

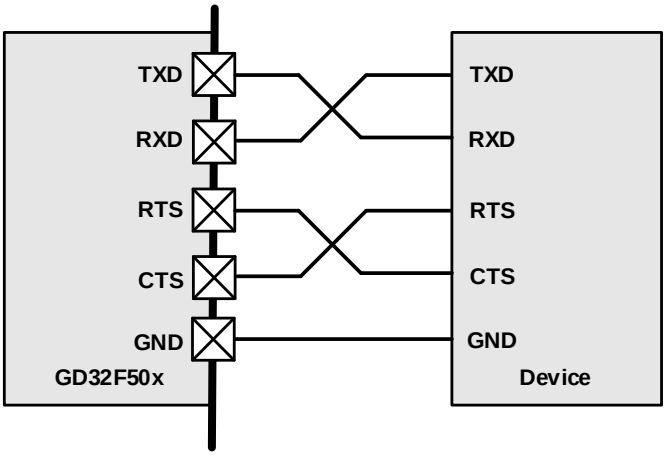
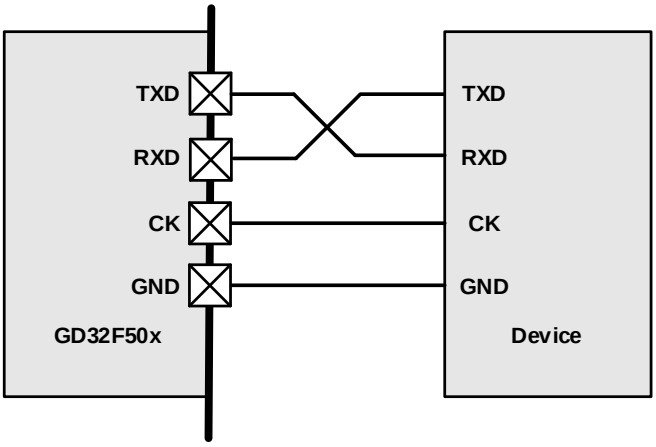


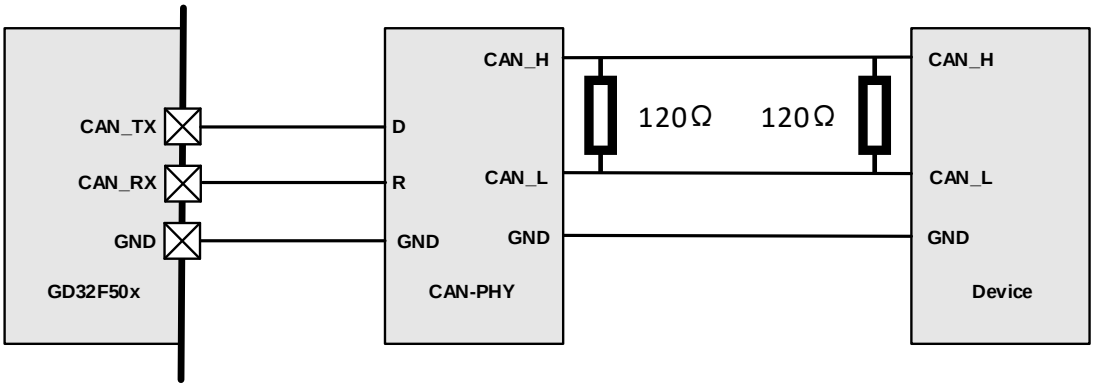
Figure 2-21. USART reference circuit in synchronous mode



2.5.3. CAN circuit

GD32F50x chips provide two CAN communication peripherals (CAN0 and CAN1), as shown in ***Figure 2-22. CAN reference circuit***.

Figure 2-22. CAN reference circuit



For two 120 Ω impedance matching resistors shown in the above figure, their resistance values and whether they are needed can be determined on a case-by-case basis.

The impedance matching resistors exert three functions during CAN communication:

1. Improve the anti-interference capability.
2. Prevent signal reflection for higher signal quality.
3. Ensure that the rising/falling edge is quickly reached for the bus.

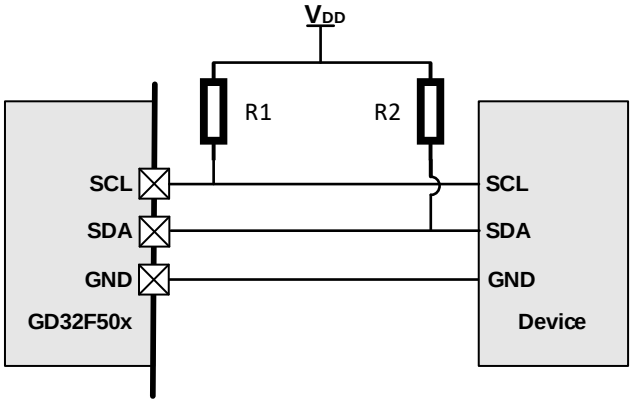
For CAN communication hardware protection design guidelines, please refer to the official application note ***AN163 GD32 MCU EMC Hardware Protection Design Reference***.

2.5.4. I2C circuit

GD32F50x chips provide two I2C peripherals, both supporting the standard I2C protocol with standard mode, fast mode and fast mode plus as well as CRC calculation and checking, SMBus (system management bus), and PMBus (power management bus). As both SDA and

SCL are bidirectional lines, all I2C channels can work in master or slave mode. They can also work in multi-master mode. The I2C interface module can also work in DMA mode, which can effectively alleviate the burden on CPU.

Figure 2-23 I2C reference circuit



For connection to the output pole of the I2C bus device, considering wired-AND, it is required to set a high level when idle.

For the OC / OD circuit, its reaction speed and power consumption depend on the pull-up resistor. The pull-up resistor with small resistance leads to fast reaction and steep signal edge (namely, good signal quality) but high power consumption. On the contrast, the pull-up resistor with large resistance leads to low power consumption but slow circuit reaction and gentle signal edge (namely poor signal quality).

Table 2-6. Reference relation between transmission mode and pull-up resistor

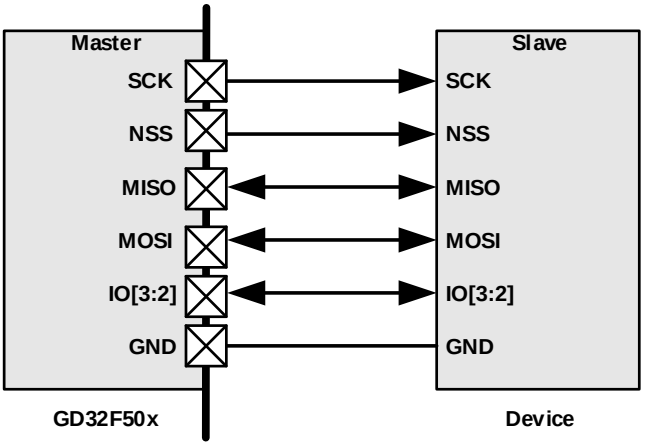
Transmission mode	Pull-up resistor (kΩ)
Standard mode	4.7
Fast mode	2.2
Fast mode plus	1.5

Considering actual wiring of I2C and complex conditions of the circuit board, the resistances of the pull-up resistor listed in ***Table 2-6. Reference relation between transmission mode and pull-up resistor*** are for reference only. In actual use, a series resistor can be added between SDA and SCL to adjust the signal quality.

2.5.5. SPI circuit

GD32F50x chips provide three SPIs. SPI0 can be set through registers and extended to four-wire mode. Except the SPI in four-wire mode, all SPI channels can work in master or slave mode. SPI0 in four-wire mode can only work as a host. It can work as a slave in the mode other than four-wire mode.

Figure 2-24 SPI reference circuit in four-wire mode



The above figure is only for reference when SPI0 works in four-wire mode. At that time, GD32F50x chip can only work as hosts. The following four connection methods in typical work modes are available for general SPI after being properly set through registers. GD32F50x chips can work as masters or slaves in the following work modes.

Figure 2-25 Connection of SPI in typical full duplex mode

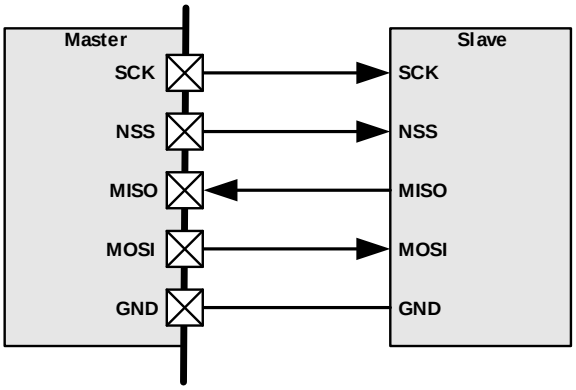


Figure 2-26 Connection of SPI in typical simplex mode (master: receiving; slave: transmitting)

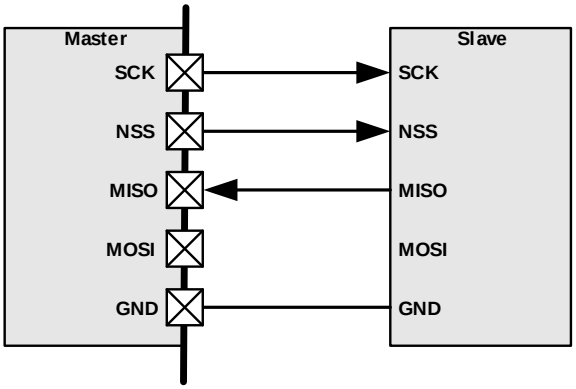


Figure 2-27 Connection of SPI in typical simplex mode (master: transmitting; slave: receiving)

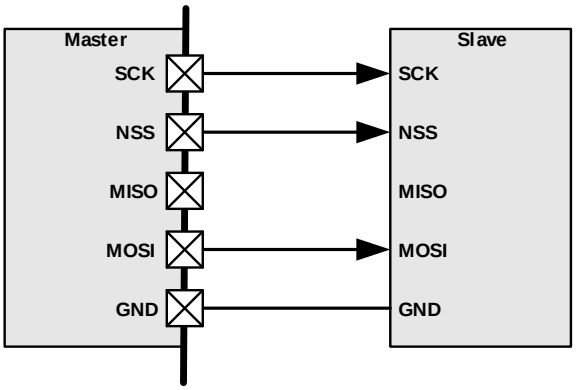
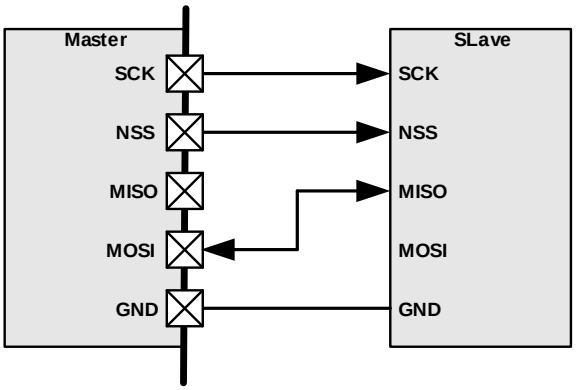


Figure 2-28 Connection of SPI in typical bidirectional line mode



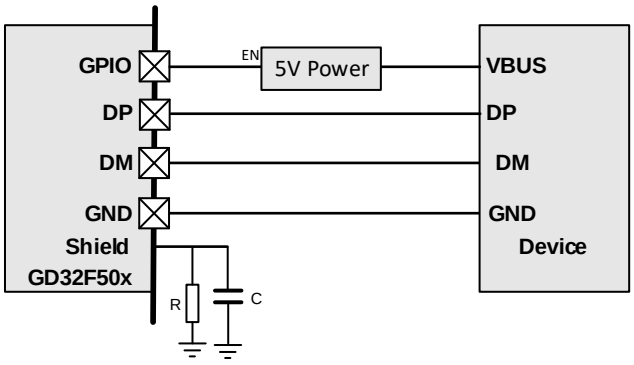
For SPI communication hardware protection design guidelines, please refer to the official application note ***AN163 GD32 MCU EMC Hardware Protection Design Reference***.

2.5.6. USB Circuit

GD32F50x products have a USBFS module. The clock used by the USBFS should be 48 MHz. The 48 MHz USB clock is generated from internal clocks in system, and its source and divider factors are configurable in RCU.

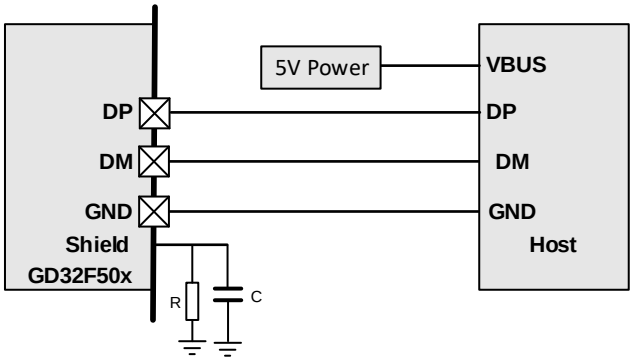
The USB module of GD32F50x can be designed as both USB device and USB host. The recommended circuit when designed as host is shown in ***Figure 2-29. Recommend USB-Host Reference Circuit***; When designing in device mode, the recommended circuit is shown in ***Figure 2-30. Recommend USB- Device Reference*** Circuit.

Figure 2-29. Recommend USB-Host Reference Circuit



Recommendation: R = 1 MΩ, C = 4700 pF

Figure 2-30. Recommend USB- Device Reference Circuit



Recommendation: R = 1 MΩ, C = 4700 pF

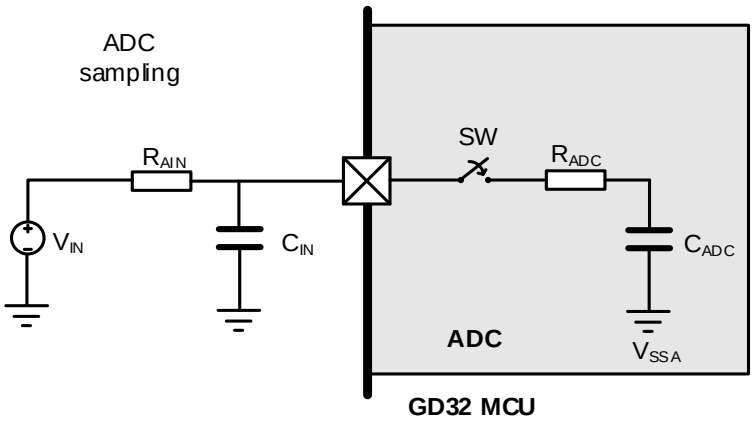
In order to improve the ESD performance of USB, it is recommended to design a resistance-capacitance discharge isolation circuit for the USB case. USB communication hardware protection design guidelines, please refer to the official application note ***AN163 GD32 MCU EMC Hardware Protection Design Reference***.

2.5.7. ADC Circuit

12-bit successive approximation analog-to-digital converter module(ADC) is integrated on GD32F50x series MCU chip. ADC0 has 16 external channels, 2 internal channel (temperature sensor, V_{REFINT} inputs channel), ADC1 has 18 external channels, ADC2 has 17 external channels.

When designing the ADC circuit, it is recommended to place a small capacitor at the ADC input pin. It is recommended to place a small capacitor of 500 pF.

Figure 2-31. ADC Acquisition Circuit Design



When f_{ADC} = 40 MHz, the relationship between Input impedance and Sampling period is shown in ***Table 2-7. fADC = 42 MHz Relationship between Sampling period and External*** input impedance. In order to obtain better conversion results, it is recommended to reduce the frequency of f_{ADC} as much as possible during use, select a larger value for the sampling period, and minimize the input impedance when designing the external circuit. If necessary, use the op amp to follow to reduce the input impedance.

Table 2-7. f_{ADC} = 42 MHz Relationship between Sampling period and External input impedance

T_s (cycles)	t_s (μs)	$R_{AIN\ max}$ (kΩ)
1.5	0.0357	—
7.5	0.1786	1.83
13.5	0.3214	3.70
28.5	0.6786	8.38
41.5	0.9881	12.43
55.5	1.3214	16.80
71.5	1.7024	21.79
239.5	5.7024	74.16

2.5.8. DAC Circuit

The DAC of GD32F50x can convert 12-bit digital data to voltage output on external pins. Data can be in 8-bit or 12-bit mode, left-justified or right-justified. When external triggering is enabled, DMA can be used to update digital data on the input. At the output voltage, the DAC output buffer can be used to obtain higher drive capability. The two DACs can work independently or concurrently.

Table 2-8. DAC Related Pin Description

Name	Description	Signal type
V_{DDA}	Analog power	Input, Analog power
V_{SSA}	Analog power ground	Input, Analog power ground
V_{REFP}	DAC positive reference voltage	Input, Analog positive

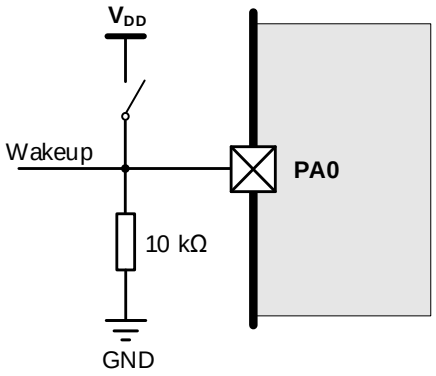
Name	Description	Signal type
	2.6V ≤ V_{REFP} ≤ V_{DDA}	reference voltage
DAC0_OUTx	DACx analog output	Analog output signal

Before enabling the DAC module, the GPIO port (PA4 corresponds to DAC0_OUT0, PA5 corresponds to DAC0_OUT1) should be configured in analog mode.

2.5.9. Standby mode wake-up circuit

The GD32F50x series supports three low-power modes, namely sleep mode, deep-sleep mode and standby mode. The standby mode with the lowest power consumption is the standby mode, which requires the longest wake-up time. Wake-up from Standby mode can be woken up by the rising edge of the WKUP pin. At this time, there is no need to configure the corresponding GPIO, just configure the WUPEN bit in the PMU_CS register. The WKUP wake-up pin reference circuit is designed as follows:

Figure 2-32. Recommend Standby External Wake-up Pin Circuit Design



Note: In this mode, attention should be paid to the circuit design. If there is a series resistance between PA0 and VDD, additional power consumption may be added.

2.5.10. Battery circuit

When V_{DD} is powered down, normal operation of the backup domain of GD32F50x chips can be kept by powering the V_{BAT} pin. The following circuits are for reference when an external battery is used to power the V_{BAT} pin.

Figure 2-33 Non-rechargeable battery reference circuit (1)

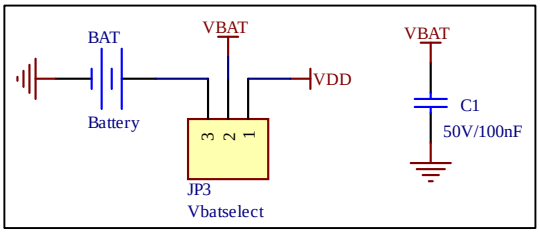


Figure 2-34 Non-rechargeable battery reference circuit (2)

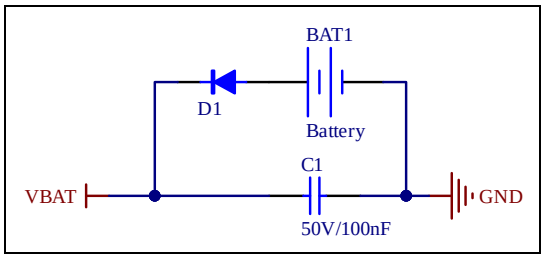
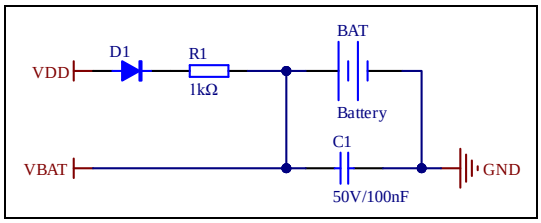


Figure 2-35 Rechargeable battery reference circuit



When referring to the above circuits, pay attention to the battery voltage, voltage drop of the diode, and supply voltage range of the V_{BAT} pin against overvoltage or undervoltage. For the resistor in the rechargeable battery reference circuit, its resistance is selected according to the battery characteristics.

2.6. Download the debug circuit

GD32F50x series cores support JTAG debug interface and SWD interface. The JTAG interface standard is a 20-pin interface, including 5 signal interfaces, and the SWD interface standard is a 5-pin interface, including 2 signal interfaces.

Note: After reset, the debug related ports are in input PU/PD mode, where:
PA15: JTDI is in pull-up mode.
PA14: JTCK/SWCLK in pull-down mode.
PA13: JTMS/SWDIO in pull-up mode.
PB4: NJTRST is in pull-up mode.
PB3: JTDO is floating mode.

Table 2-9. JTAG Download Debug Interface Assignment

Alternate function	GPIO Port
JTMS	PA13
JTCK	PA14
JTDI	PA15
JTDO	PB3
NJTRST	PB4

Figure 2-36. Recommend JTAG Wiring Reference Design

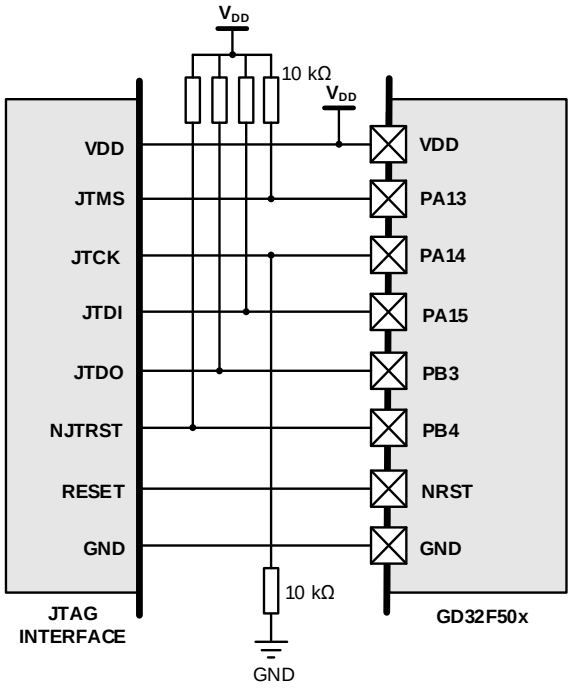
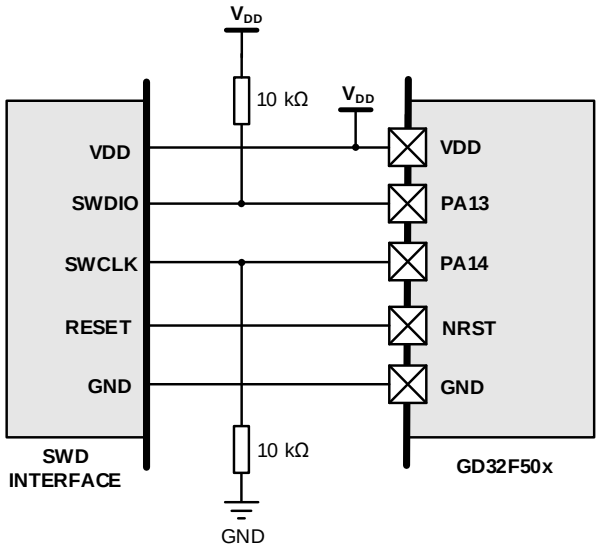


Table 2-10. SWD Download Debug Interface Assignment

Alternate function	GPIO Port
SWDIO	PA13
SWCLK	PA14

Figure 2-37. Recommend SWD Wiring Reference Design



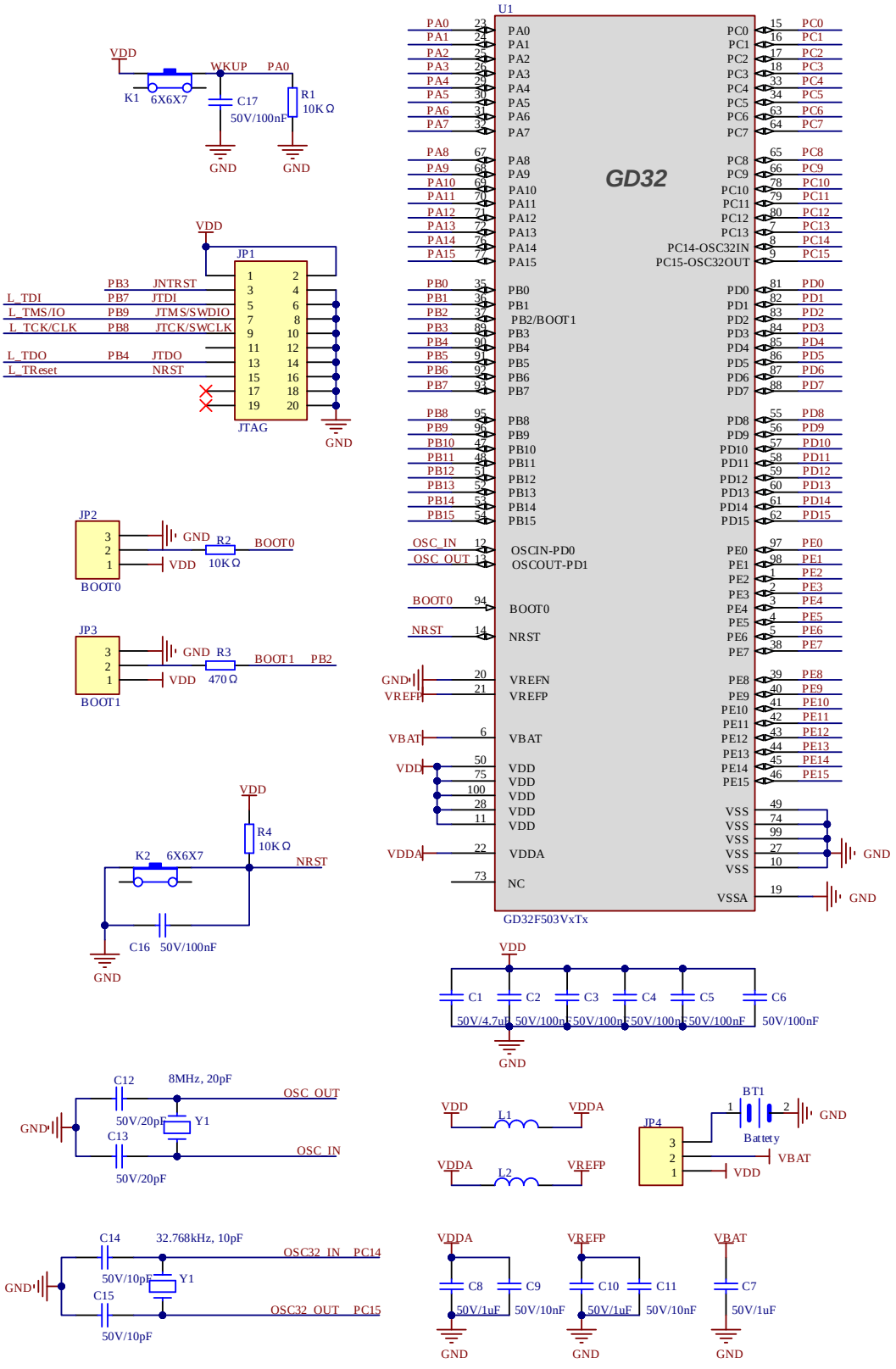
There are several ways to improve the reliability of SWD download and debugging communication and enhance the anti-interference ability of download and debugging.

1. Shorten the length of the two SWD signal lines, preferably within 15 cm.

2. Weave the two SWD wires and the GND wire into a twist and twist them together.
3. Connect separately tens of pF small capacitors in parallel between the two signal lines of the SWD and the ground.
4. Any IO of the two signal lines of SWD is connected in series with a 100 Ω ~ 1 kΩ resistor.

2.7. Reference Schematic Design

Figure 2-38. GD32F50x Recommend Reference Schematic Design



3. PCB Layout Design

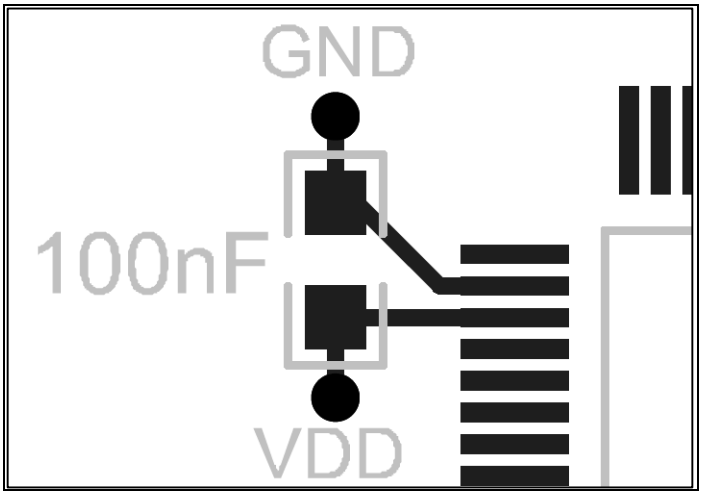
In order to enhance the functional stability and EMC performance of the MCU, it is not only necessary to consider the performance of the supporting peripheral components, but also the PCB Layout. In addition, when conditions permit, try to choose a PCB design scheme with an independent GND layer and an independent power supply layer, which can provide better EMC performance. If conditions do not allow, independent GND layer and power supply layer cannot be provided, then it is also necessary to ensure a good power supply and grounding design, such as making the GND plane under the MCU as complete as possible. For packages with EPAD, it is recommended that EPAD be grounded on the PCB Layout.

In applications with high power or strong interference, it is necessary to consider keeping the MCU away from these strong interference sources. For more layout design references, please see the official document ***AN191 GD32 MCU Hardware Layout Design Reference***.

3.1. Power Supply Decoupling Capacitors

The GD32F50x series power supply has four power supply pins: V_{DD}, V_{DDA}, V_{REFP} and V_{BAT}. The 100 nF decoupling capacitor can be made of ceramic, and it is necessary to ensure that the position is as close to the power supply pin as possible. The power trace should try to make it pass through the capacitor first and then reach the MCU power pin, It is recommended to punch holes near the capacitor pad to connect with GND.

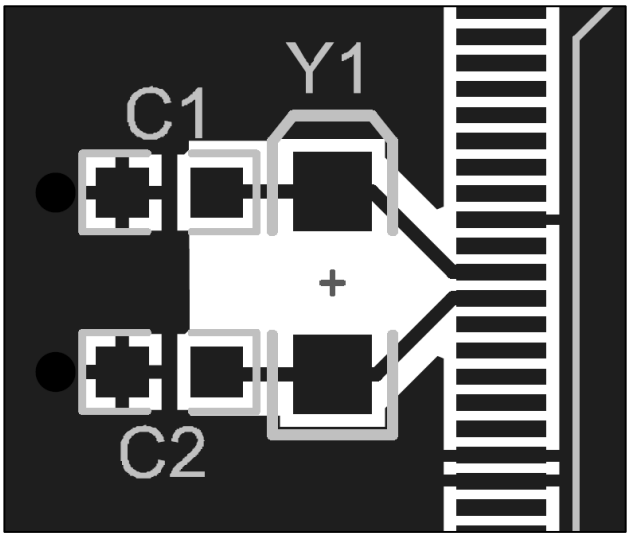
Figure 3-1. Recommend Power Pin Decoupling Layout Design



3.2. Clock Circuit

GD32F50x series clocks have HXTAL and LXTAL, and the clock circuit (including crystal or crystal oscillator and capacitor, etc.) is required to be placed close to the MCU clock pin, and the clock trace should be wrapped by GND as much as possible.

Figure 3-2. Recommend Clock Pin Layout Design (passive crystal)



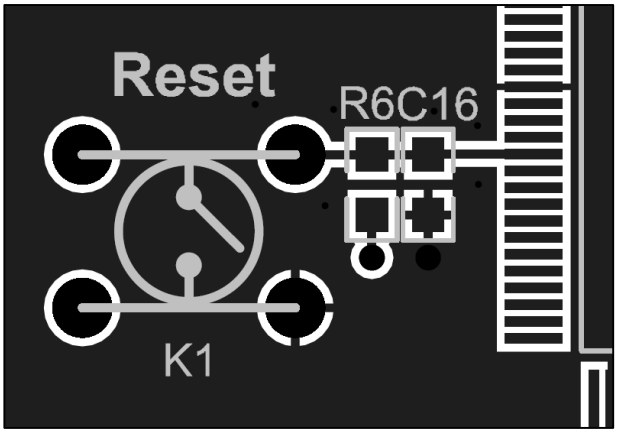
Note:

1. The crystal should be as close to the MCU clock pin as possible, and the matching capacitor should be as close as possible to the crystal.
2. The whole circuit should be on the same layer as the MCU, and the wiring should not go through the layer as much as possible.
3. The PCB area of the clock circuit should be kept as empty as possible, and no traces unrelated to the clock should be taken.
4. High-power, high-interference risk devices and high-speed wiring should be kept away from the clock crystal circuit as far as possible.
5. The clock line is grounded to achieve a shielding effect.

3.3. Reset Circuit

NRST trace PCB Layout reference is as follows:

Figure 3-3. Recommend NRST Trace Layout Design



Note: The resistance and capacitance of the reset circuit should be as close as possible to the NRST pin of the MCU, and the NRST trace should be kept away from devices with strong

interference risk and high-speed traces as far as possible. If conditions permit, it had better to wrap the NRST traces for better shielding effect.

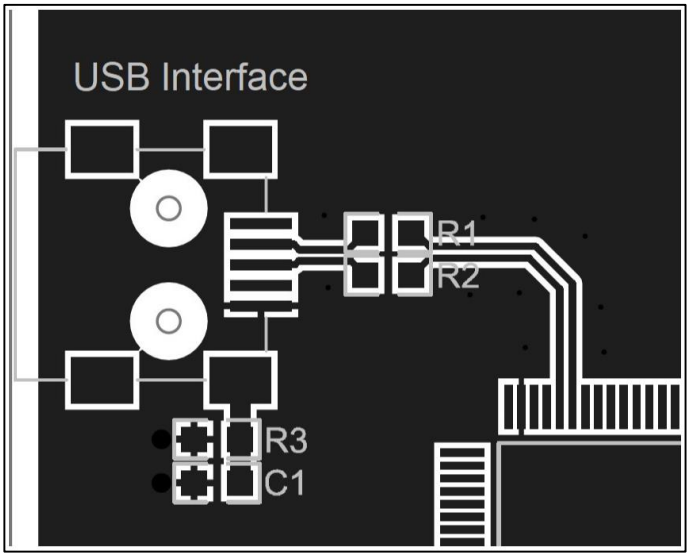
3.4. USB Circuit

The USB module has two differential signal lines, DM and DP. It is recommended that the PCB traces require a characteristic impedance of 90 Ω. The differential traces should be run in strict accordance with the rule of equal length and equal distance, and the traces should be kept as short as possible. If the two differential lines are not equal in length , the short line can be compensated with a serpentine line at the terminal.

Due to impedance matching considerations, the series matching resistance is recommended to be about 50 Ω. When the USB terminal interface is far away from the MCU, the series resistance value needs to be appropriately increased.

The USB differential trace reference is as follows:

Figure 3-4. Recommend USB Differential Trace Layout Design



Recommendation: R1 = R2 = 50 Ω, R3 = 1 MΩ, C = 4700 pF

Note:

1. Reasonable placement during layout to shorten the differential trace distance.
2. Draw differential lines first, try not to exceed two pairs of vias for a pair of differential lines, and place them symmetrically.
3. Symmetrical parallel wiring to ensure that the two lines are tightly coupled, avoiding right-angle, acute-angle, or curved traces.
4. Devices such as resistance-capacitor, EMC connected to the differential traces, or test points should also be symmetrical.

4. Steel mesh and soldering

4.1. Steel mesh

When SMT is applied, the thickness and opening size of the leak of the steel mesh depend on the type of solder paste and the distribution, density, and spacing of pad openings. Overlarge opening of the leak of the steel mesh often leads to distribution of too much solder paste, which is prone to "bridging" during soldering. Too small opening of the leak will lead to application of little solder paste and thus cause insufficient strength of the solder joint or "cold solder".

4.1.1. Recommended thickness of steel mesh

The thickness and opening size of the steel mesh generally follow these rules: The width-to-thickness ratio shall be higher than 1.5 (that is, the opening width of the steel mesh shall be 1.5 times the thickness of the steel mesh or above), and the area ratio shall be higher than 0.66 (that is, the opening area of the steel mesh shall be 0.66 times the lateral area of the opening column or above), which can ensure to the greatest extent that there is proper amount of solder paste on the pad when brushing.

The recommended thickness of the steel mesh of GD32F5xx new products are listed in ***Table 4-1. Recommended thickness of steel mesh of GD32F50x chip***.

Table 4-1. Recommended thickness of steel mesh of GD32F50x chip

Chip package	Thickness (mm)
LQFP100(14x14, 0.5pitch)	0.12
LQFP64(10x10, 0.5pitch)	0.12
BGA64(4x4, 0.4pitch)	0.12
QFN64(7x7, 0.35pitch)	0.12
LQFP48(7x7, 0.5pitch)	0.12
QFN48(5x5, 0.35pitch)	0.12
QFN32(5x5, 0.5pitch)	0.12

In practice, the above table can only be for reference for the thickness of the steel mesh of GD32F50x products. The thickness of the steel mesh of PCB shall be evaluated in combination with the density of PCB devices, pitch value of other chip pins, pad dimensions, and process requirements.

4.1.2. Cleaning and use of steel mesh

Cleaning

- The steel mesh shall be cleaned before use to remove contaminants contacted during transportation or long-term storage.

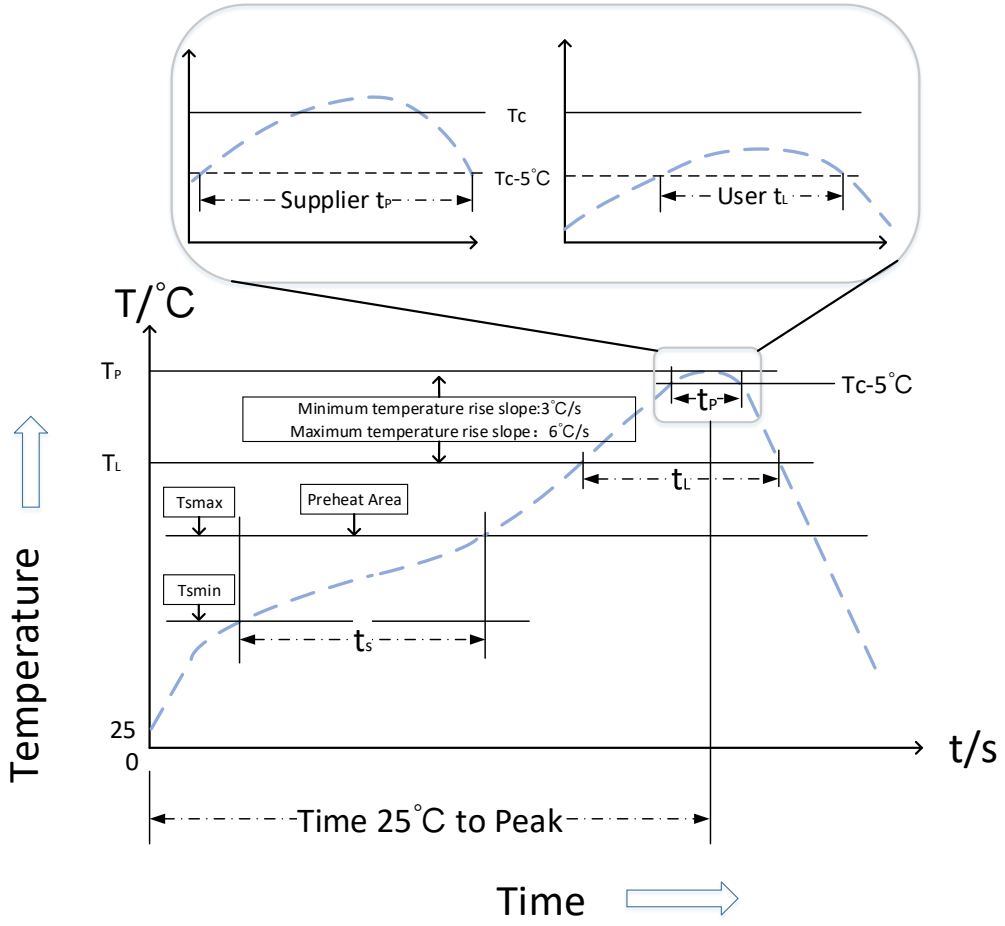
- The steel mesh shall be cleaned in time after use and packed in a special storage position.
- The steel mesh to be cleaned shall not be placed randomly to prevent it from being damaged or bringing other contaminants.
- The steel mesh shall be placed vertically in a special storage position and isolated from each other.

Use

- Solder paste for soldering shall be applied after being heated and stirred evenly to prevent the steel mesh from being blocked.
- The steel mesh shall be gently moved to prevent bumping against hard objects or sharp devices.
- When brushing, the steel mesh shall be kept close to PCB, and attention shall be paid to the adjustment of the pressure on the scraper until there is no residual solder paste on the intact steel mesh.
- The steel mesh shall be lifted for demolding at a proper speed about 3 s after brushing.
- When reaching the service life limit, generally 100,000 times, the steel mesh shall be scrapped.

4.2. Soldering

Figure 4-1 Recommended Reflow Soldering Temperature Curve



During actual processing and production, the reflow soldering temperature curve shall be set with reference to many factors, including component characteristics, PCB material, component distribution density, and solder paste composition. The above soldering temperature curve for GD32F50x chips is introduced below for reference.

Table 4-2. Reflow soldering parameters

Characteristic parameter	Lead-free assembly
Average temperature rise slope from 217 °C to peak temperature	Maximum 3 °C / s
Preheating duration (150 °C to 200 °C)	60 s to 120 s
Duration for keeping the temperature above 217 °C	60 s to 150 s
Peak temperature	260 + 5 / - 0 °C
Duration for true peak temperature of below 5 °C	30 s
Temperature drop slope	Maximum 6 °C / s
Duration for temperature rising from 25 °C to peak temperature	Maximum 8 min

5. Package Description

The GD32F50x series has a total of 4 package types, namely LQFP100, LQFP64, BGA64, QFN64, LQFP48, QFN48, QFN32.

Table 5-1. Package Description

Ordering code	Package
GD32F50xVxT6	LQFP100(14x14, 0.5pitch)
GD32F50xRxT6	LQFP64(10x10, 0.5pitch)
GD32F50xRGL6	BGA64(4x4, 0.4pitch)
GD32F50xREO6	QFN64(7x7, 0.35pitch)
GD32F50xCxT6	LQFP48(7x7, 0.5pitch)
GD32F50xCEO6	QFN48(5x5, 0.35pitch)
GD32F50xKxU6	QFN32(5x5, 0.5pitch)

(Original dimensions are in millimeters)

6. Revision history

Table 6-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Oct. 31, 2025

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