GigaDevice Semiconductor Inc.

GD32W51x_F5HC Series
Software Development Guide

Application Note
AN319

Revision 1.0

(Mar. 2026)

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1. Introduction

This application note is specifically written for the GD32W51x_F5HC series MCUs, aiming to provide functional examples and usage precautions for the peripheral resources of this series of chips, helping users quickly master the software development methods and practices for GD32W51x_F5HC series MCUs. The applicable products are as shown in ***Table 1-1. Applicable product***.

Table 1-1. Applicable product

Type	Model
MCU	GD32W51x_F5HC series

Note: This application note is for reference only. In case of any conflict with the user manual or datasheet, the user manual or datasheet shall prevail.

2. Module usage instructions

2.1. System and memory architecture(SYSTEM)

2.1.1. Boot configuration

At startup, BOOT0 and BOOT1 pins are used to select the boot memory address.

The BOOT0 value may come from the BOOT0 pin or from the value of EFBOOT0 bit in the EFUSE_CTL register to free the GPIO pad if needed.

The BOOT1 value may come from the PA14 pin or from the value of EFBOOT1 bit in the EFUSE_CTL register to free the GPIO pad if needed.

Table 2-1. BOOT0 modes (Only for GD32F5HCxx)

EFUSE_CTL		FMC_OBR1		BOOT0 PC8 pin	BOOT0
SWBOOT0	EFBOOT0	SWBOOT0	nBOOT0		
0	-	1	-	0	0
0	-	1	-	1	1
0	-	0	1	-	0
0	-	0	0	-	1
1	0	-	-	-	0
1	1	-	-	-	1

Table 2-2. BOOT0 modes (Only for GD32W515xx)

SWBOOT0	EFBOOT0	BOOT0 PC8 pin	BOOT0
0	-	0	0
0	-	1	1
1	0	-	0
1	1	-	1

Table 2-3. BOOT1 modes (Only for GD32F5HCxx)

EFUSE_CTL		FMC_OBR1		BOOT1 PA14 pin	BOOT1
SWBOOT1	EFBOOT1	SWBOOT1	nBOOT1		
0	-	1	-	0	0
0	-	1	-	1	1
0	-	0	1	-	0
0	-	0	0	-	1
1	0	-	-	-	0
1	1	-	-	-	1

Table 2-4. BOOT1 modes (Only for GD32W515xx)

SWBOOT1	EFBOOT1	BOOT1 PA14 pin	BOOT1
0	-	0	0

SWBOOT1	EFBOOT1	BOOT1 PA14 pin	BOOT1
0	-	1	1
1	0	-	0
1	1	-	1

Refer to ***Table 2-5. Boot address modes when TrustZone® is disabled, TZEN=0*** and ***Table 2-6. Boot modes when TrustZone® is enabled, TZEN=1*** for boot address when TrustZone® is disabled and enabled respectively. When the EFBOOTLK bit in the EFUSE_CTL register is set, the boot memory address selected according to BOOT1 and BOOT0.

Table 2-5. Boot address modes when TrustZone® is disabled, TZEN=0

EFBOOTLK	BOOT0	BOOT1	Boot address	Boot area
0	0	-	0x08000000	SIP Flash
0	1	0	0x0BF40000	Bootloader / ROM
0	1	1	0x0A000000	SRAM0
1	0	-	0x08000000	SIP Flash
1	1	-	0x0BF40000	Bootloader / ROM

When TrustZone® is enabled by setting the TZEN option bit, the boot space must be in a secure area.

Table 2-6. Boot modes when TrustZone® is enabled, TZEN=1

GSSACMD == 8'hc(1)	EFBOOTLK	BOOT0	BOOT1	EFSB	Boot address	Boot area
0	0	0	-	0	0x0C000000	SIP Flash
0	0	0	-	1	0X0FF84000	secure boot
0	0	1	0	-	0x0FF80000	GSSA
0	0	1	1	-	0x0E000000	SRAM0
-	1	0	-	0	0x0C000000	SIP Flash
-	1	0	-	1	0X0FF84000	secure boot
-	1	1	-	-	0x0FF80000	GSSA
1	0	-	-	-	0x0FF80000	GSSA

Note: (1) When the GSSACMD bitfield is 0x0C, it means 1, otherwise it means 0.

The BOOTx (x=0/1) value (either coming from the pin or the EFBOOTx bit) is latched upon reset release. It is up to the user to set BOOTx values to select the required boot mode. The BOOTx pin or EFBOOTx bit (depending on the EFBOOTLK and SWBOOTx bit value in the EFUSE_CTL register) is also re-sampled when exiting from Standby mode. Consequently, they must be kept in the required Boot mode when in Standby mode. After a startup delay, the selection of the boot area is done before releasing the processor reset.

2.2. Analog-to-digital converter (ADC)

2.2.1. Precautions for the use of ADC

Precautions for the ADC module in the GD32F5HCxx series and GD32W515xx series are as follows:

(1) Increase in the number of external ADC channels

Compared with the GD32W515xx series, the GD32F5HCxx series adds three additional external channels: ADC_IN12, ADC_IN13, and ADC_IN14.

(2) ADC internal channel configuration

In the GD32W515xx series, both ADC channel 9 (temperature sensor) and channel 10 (internal reference voltage) can be enabled simultaneously by configuring the TSVREN bit in the ADC_CCTL register.

Table 2-7. ADC internal channel configuration of the GD32W515xx series

```
/* ADC temperature and vref enable */
adc_internal_channel_config(ADC_CHANNEL_INTERNAL_TEMP_VREF, ENABLE);
…
```

In the GD32F5HCxx series, ADC channel 9 (temperature sensor) can be individually enabled by configuring the TSVEN bit in the ADC_CCTL register, and ADC channel 10 (internal reference voltage) can be individually enabled by configuring the INREFEN bit in the ADC_CCTL register.

Table 2-8. ADC internal channel configuration of the GD32F5HCxx series

```
/* ADC temperature enable */
adc_internal_channel_config(ADC_CHANNEL_INTERNAL_TEMPSENSOR, ENABLE);
/* ADC vref enable */
adc_internal_channel_config(ADC_CHANNEL_INTERNAL_VREFINT, ENABLE);
…
```

(3) ADC inserted sequence DMA function of the GD32F5HCxx series

The GD32F5HCxx series adds the DMA transfer function for the inserted sequence. The DMA request, which is enabled by the IDMA bit of ADC_CTL1 register, is used to transfer data of inserted sequence for conversion of more than one channel. The ADC generates a DMA request at the end of conversion of a inserted channel. When this request is received, the DMA will transfer the converted data from the ADC_IDATA register to the destination location which is specified by the user. The GD32F5HCxx series adds an inserted data register overflow interrupt and the corresponding flag bit.

Table 2-9. DMA transfer configuration for the ADC inserted sequence in GD32F5HCxx series

```
/* ADC DMA function enable */
```

```
adc_dma_mode_enable(ADC_INSERTED_CHANNEL);
…
/* initialize DMA single data mode */
dma_single_data_parameter.periph_addr                = (uint32_t)(&ADC_IDATA);
dma_single_data_parameter.periph_inc                 = DMA_PERIPH_INCREASE_DISABLE;
dma_single_data_parameter.memory0_addr               = (uint32_t)(&adc_value);
dma_single_data_parameter.memory_inc                 = DMA_MEMORY_INCREASE_ENABLE;
dma_single_data_parameter.periph_memory_width        = DMA_PERIPH_WIDTH_16BIT;
dma_single_data_parameter.direction                  = DMA_PERIPH_TO_MEMORY;
dma_single_data_parameter.number                     = 4U;
dma_single_data_parameter.priority                   = DMA_PRIORITY_HIGH;
dma_single_data_mode_init(DMA1, DMA_CH3, &dma_single_data_parameter);
dma_channel_subperipheral_select(DMA1, DMA_CH3, DMA_SUBPERI0);
…
```

(4) ADC conversion data latch function of the GD32F5HCxx series

The ADC has 4 latch data registers, ADC_LDATAx (x=0…3), which can latch the data from a completed conversion in a routine or inserted sequence.

By configuring the SEQSELx (x = 0…3) bits in the ADC_LDCTL register, it can be determined whether the latched data is selected from the routine sequence or the inserted sequence. The COVSELx bits are used to select which conversion result within the chosen sequence is to be latched.

Table 2-10. ADC data latch configuration and reading in GD32F5HCxx series

```
/*   ADC latch data source config */
adc_latch_data_source_configADC_LATCH_DATA_0, ADC_ROUTINE_CHANNEL, 0);
adc_latch_data_source_config(ADC_LATCH_DATA_1, ADC_ROUTINE_CHANNEL, 1);
adc_latch_data_source_config(ADC_LATCH_DATA_2, ADC_INSERTED_CHANNEL, 0);
adc_latch_data_source_config(ADC_LATCH_DATA_3, ADC_INSERTED_CHANNEL, 1);
…
/* get the ADC0 routine channel conversion value */
adc_value[0] = adc_latch_data_read(ADC0, ADC_LATCH_DATA_0);
adc_value[1] = adc_latch_data_read(ADC0, ADC_LATCH_DATA_1);
…
/* get the ADC0 inserted channel conversion value */
adc_value[2] = adc_latch_data_read(ADC0, ADC_LATCH_DATA_2);
adc_value[3] = adc_latch_data_read(ADC0, ADC_LATCH_DATA_3);
…
```

ADC_LDATAx (x=0…3) registers default store inserted sequence xth conversion results.

Table 2-11. ADC latch data register read inserted sequence data by default in GD32F5HCxx series

```
/* read ADC inserted sequence data register */
inserted_data[0] = adc_latch_data_read(ADC_LATCH_DATA_0);
```

```
inserted_data[1] = adc_latch_data_read(ADC_LATCH_DATA_1);
inserted_data[2] = adc_latch_data_read(ADC_LATCH_DATA_2);
inserted_data[3] = adc_latch_data_read(ADC_LATCH_DATA_3);
…
```

2.3. TrustZone protection controller union (TZPCU)

For detailed information, refer to ***AN103 GD32W51x TrustZone Development Guide*** and ***AN300 TrustZone Project Development and Interrupt Introduction in Embedded Builder***.

2.4. Differences between GD32F5HC and GD32W515 products

For detailed information, refer to ***AN299 Differences between GD32F5HC and GD32W515 products***.

3. Revision history

Table 3-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Mar.31, 2026

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