GigaDevice Semiconductor Inc.

Differences between GD32E113/C113 and GD32E103/C103 products

Application Note
AN072

Revision 1.1

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1. Introduction

This application note introduces the characteristic differences between GD32E113/C113 and GD32E103/C103 product series, mainly for electric characteristics and peripheral function characteristics. The differences are described in the following paragraphs.

2. Electric characteristic differences

2.1. Power saving mode wakeup timings

The power saving mode wakeup timings differences are reflected in wakeup timings from sleep mode and deep-sleep mode, which refers to ***Table 2-1. Differences of power saving mode wakeup timings characteristics***.

Table 2-1. Differences of power saving mode wakeup timings characteristics

Part Numbers	Symbol	Parameter	Typ	Unit
GD32C103xx GD32E103xx	t_{Sleep}	Wakeup from Sleep mode	4.3	μs
	$t_{Deep-sleep}$	Wakeup from Deep-sleep mode (LDO On)	18.0	
		Wakeup from Deep-sleep mode (LDO in low power mode)	18.0	
GD32C113xx GD32E113xx	t_{Sleep}	Wakeup from Sleep mode	2	
	$t_{Deep-sleep}$	Wakeup from Deep-sleep mode (LDO On)	34	
		Wakeup from Deep-sleep mode (LDO in low power mode)	34	

Note:

(1) Based on characterization, not tested in production.

(2) The wakeup time is measured from the wakeup event to the point at which the application code reads the first instruction under the below conditions: V_{DD} = V_{DDA} = 3.3 V, IRC8M = System clock = 8 MHz.

2.2. Power consumption

The power consumption differences are reflected in supply current in deep-sleep mode and standby mode, which refers to ***Table 2-2. Differences of power consumption characteristics in deep-sleep mode*** and ***Table 2-3. Differences of Power consumption characteristics in standby mode***.

Table 2-2. Differences of power consumption characteristics in deep-sleep mode

Part Numbers	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
GD32C103xx GD32E103xx	I_{DD}+I_{DDA}	Supply current (Deep-Sleep mode)	V_{DD} = V_{DDA} = 3.3 V, LDO in normal power mode, IRC40K off, RTC off, All GPIOs analog mode	—	41.8	550	μA
			V_{DD} = V_{DDA} = 3.3 V, LDO in low power mode, IRC40K off, RTC off, All GPIOs analog mode	—	31.8	550	μA
GD32C113xx GD32E113xx			V_{DD} = V_{DDA} = 3.3 V, LDO in normal power mode, IRC40K off, RTC off, All GPIOs analog mode	—	125.39	550	μA
			V_{DD} = V_{DDA} = 3.3 V, LDO in low power mode, IRC40K off, RTC off, All GPIOs analog mode	—	107	550	μA

Note:

(1) Based on characterization, not tested in production.

(2) Unless otherwise specified, all values given for TA = 25 °C and test result is mean value.

Table 2-3. Differences of Power consumption characteristics in standby mode

Part Numbers	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
GD32C103xx GD32E103xx	I_{DD}+I_{DDA}	Supply current (Standby mode)	V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC40K on, RTC on	—	2.1	11	μA
			V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC40K on, RTC off	—	2.0	11	μA
			V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC40K off, RTC off	—	1.5	11	μA
GD32C113xx GD32E113xx			V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC40K on, RTC on	—	3.84	11	μA
			V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC40K on, RTC off	—	3.68	11	μA
			V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC40K off, RTC off	—	3.5	11	μA

Note:

(1) Based on characterization, not tested in production.

(2) Unless otherwise specified, all values given for TA = 25 °C and test result is mean value.

2.3. Flash memory

The flash memory characteristics differences are reflected in word programming, page erasing and mass erasing time, which refers to ***Table 2-4. Differences of flash operating time***.

Table 2-4. Differences of flash operating time

Part Numbers	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
GD32C103xx GD32E103xx	t_{PROG}	Word programming time	T_A = -40 °C ~ +85 °C	37	—	44	μs
	t_{ERASE}	Page erase time		3.2	—	4	ms
	t_{MERASE}	Mass erase time		8	—	10	ms
GD32C113xx GD32E113xx	t_{PROG}	Word programming time		80	—	90	μs
	t_{ERASE}	Page erase time		1	—	20	ms
	t_{MERASE}	Mass erase time		8	—	20	ms

Note:

(1) Guaranteed by design, not tested in production.

(2) Word is 32 bits or 64 bits depend on PGW bit in FMC_WS register.

2.4. Analog-to-digital converter (ADC)

The ADC characteristics differences are reflected in maximum operating clock, external input impedance, input sampling capacitance and ADC dynamic accuracy., which refers to ***Table 2-5. Electric characteristic differences of ADC*** and ***Table 2-6. Electric characteristic differences ADC dynamic accuracy***.

Table 2-5. Electric characteristic differences of ADC

Part Numbers	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
GD32C103xx GD32E103xx	f_{ADC}(1)	ADC clock	—	0.1	—	42	MHz
	f_S(1)	Sampling rate	12-bit	0.007	—	3	MSPS
			10-bit	0.008	—	3.5	
			8-bit	0.01	—	4.2	
			6-bit	0.011	—	5.25	
	R_{AIN}(2)	External input impedance	—	—	—	24	kΩ
	C_{ADC}(2)	Input sampling capacitance	No pin/pad capacitance included	—	—	5.5	pF
GD32C113xx GD32E113xx	f_{ADC}(1)	ADC clock	—	0.1	—	40	MHz
	f_S(1)	Sampling rate	12-bit	0.007	—	2.8	MSPS
			10-bit	0.008	—	3.3	
			8-bit	0.01	—	4	
			6-bit	0.011	—	5	
	R_{AIN}(2)	External input impedance	—	—	—	156.57	kΩ
	C_{ADC}(2)	Input sampling capacitance	No pin/pad capacitance included	—	—	4.1	pF

Note:

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Table 2-6. Electric characteristic differences ADC dynamic accuracy

Symbol	Parameter	Parameter	Conditions	Min	Typ	Max	Unit
GD32C103xx GD32E103xx	ENOB	Effective number of bits	f_{ADC} = 14 MHz V_{DDA} = V_{REF+} = 3.3 V Input Frequency = 20 kHz Temperature = 25 °C	—	10.3	—	bits
	SNDR	Signal-to-noise and distortion ratio		—	63.8	—	dB
	SNR	Signal-to-noise ratio		—	64.5	—	
	THD	Total harmonic distortion		—	-67.5	—	
GD32C113xx GD32E113xx	ENOB	Effective number of bits		—	11	—	bits
	SNDR	Signal-to-noise and distortion ratio		—	68	—	dB
	SNR	Signal-to-noise ratio		—	68.5	—	
	THD	Total harmonic distortion		—	-81	—	

Note: Based on characterization, not tested in production.

3. Revision history

Table 3-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Jul.1, 2022
1.1	Update copyright and cover information	Aug.18, 2025

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