GigaDevice Semiconductor Inc.

GD32C231xx
Arm® Cortex®-M23 32-bit MCU

Datasheet

Revision 1.7

(Jun. 2026)

Table of Contents

List of Figures

List of Tables

1. General description

The GD32C231xx device belongs to the value line of GD32 MCU family. It is a new 32-bit general-purpose microcontroller based on the Arm® Cortex®-M23 core. The Cortex-M23 processor is an energy-efficient processor with a very low gate count. It is intended to be used for microcontroller and deeply embedded applications that require an area-optimized processor. The processor delivers high energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier and a 17-cycle divider.

The GD32C231xx device incorporates the Arm® Cortex®-M23 32-bit processor core operating at up to 48 MHz frequency with Flash accesses 0~1 wait states to obtain maximum efficiency. It provides up to 64 KB embedded Flash memory and up to 12 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to one APB bus. The devices offer one 12-bit ADC, two comparators, up to four general 16-bit timers, one 16-bit PWM advanced timer, as well as standard and advanced communication interfaces: up to two SPIs, two I2Cs, three USARTs and an I2S.

The device operates from a 1.8 to 5.5 V power supply and available in –40 to +85 °C temperature range for grade 6 devices, and -40 to 105 °C temperature range for grade 7 devices. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make the GD32C231xx devices suitable for a wide range of applications, especially in areas such as industrial control, motor drives, user interface, power monitor and alarm systems, consumer and handheld equipment, gaming and GPS, E-bike and so on.

2. Device overview

2.1. Device information

Table 2-1. GD32C231xx devices features and peripheral list 1

Part Number		GD32C231xx					
		C6T6	**C8T6**	**C8T7**	**K6U6**	**K8U6**	**K8U7**
FLASH (KB)		32	64	64	32	64	64
SRAM (KB)		12	12	12	12	12	12
Timers	**General timer(16-bit)**	4 (2, 13, 15,16)	4 (2, 13, 15,16)	4 (2, 13, 15,16)	4 (2, 13, 15,16)	4 (2, 13, 15,16)	4 (2, 13, 15,16)
	SysTick	1	1	1	1	1	1
	Advanced timer(16-bit)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)
	Watchdog	2	2	2	2	2	2
	RTC	1	1	1	1	1	1
Connectivity	**USART**	3 (0, 1, 2)	3 (0, 1, 2)	3 (0, 1, 2)	3 (0, 1, 2)	3 (0, 1, 2)	3 (0, 1, 2)
	I2C	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)
	SPI/I2S	2/1 (0-1)/(0)	2/1 (0-1)/(0)	2/1 (0-1)/(0)	2/1 (0-1)/(0)	2/1 (0-1)/(0)	2/1 (0-1)/(0)
GPIO		45	45	45	30	30	30
ADC	**Units**	1	1	1	1	1	1
	Channels (External)	13	13	13	12	12	12
	Channels (Internal)	3	3	3	3	3	3
CMP		2	2	2	2	2	2
Package		LQFP48			QFN32		

Table 2-2. GD32C231xx devices features and peripheral list 2

Part Number		GD32C231xx						
		C6U6	**C8U6**	**K6T6**	**K8T6**	**G6U6TR**	**G8U6TR**	**G8U7TR**
FLASH (KB)		32	64	32	64	32	64	64
SRAM (KB)		12	12	12	12	12	12	12
Timers	**General timer(16-bit)**	4 (2, 13, 15,16)	4 (2, 13, 15,16)	4 (2, 13, 15,16)	4 (2, 13, 15,16)	4 (2, 13, 15,16)	4 (2, 13, 15,16)	4 (2, 13, 15,16)
	SysTick	1	1	1	1	1	1	1
	Advanced timer(16-bit)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)
	Watchdog	2	2	2	2	2	2	2
	RTC	1	1	1	1	1	1	1

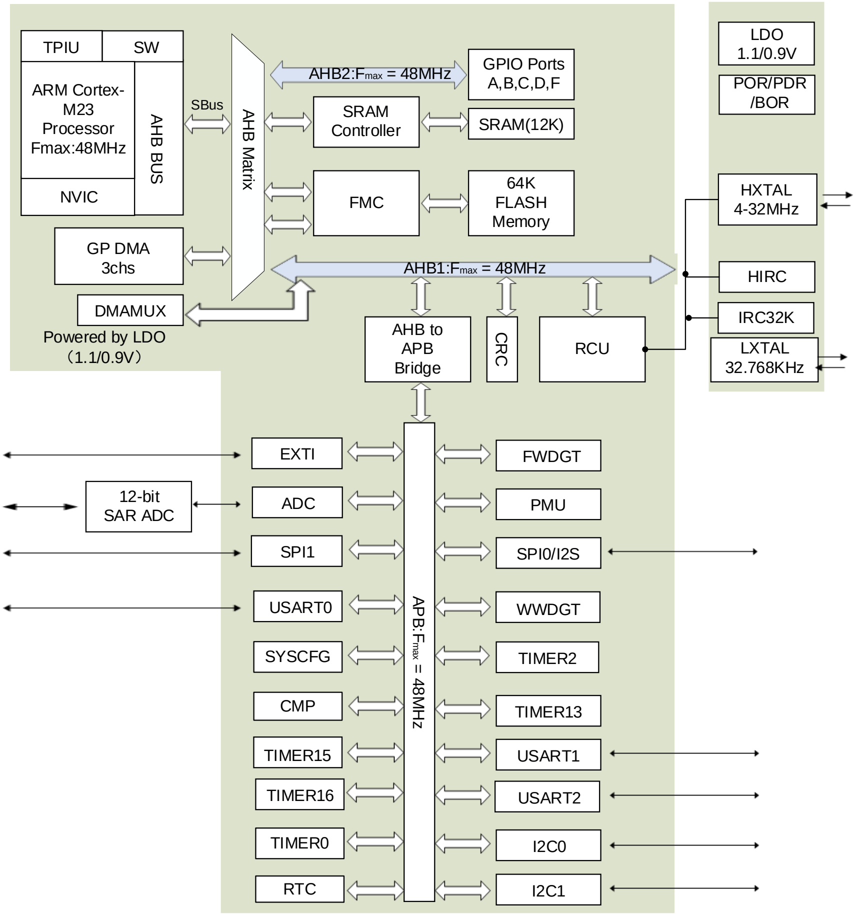
Part Number		GD32C231xx						
		C6U6	C8U6	K6T6	K8T6	G6U6TR	G8U6TR	G8U7TR
Connectivity	USART	3 (0, 1, 2)	3 (0, 1, 2)	3 (0, 1, 2)	3 (0, 1, 2)	2 (0, 1)	2 (0, 1)	2 (0, 1)
	I2C	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)
	SPI/I2S	2/1 (0-1)/(0)	2/1 (0-1)/(0)	2/1 (0-1)/(0)	2/1 (0-1)/(0)	2/1 (0-1)/(0)	2/1 (0-1)/(0)	2/1 (0-1)/(0)
GPIO		45	45	30	30	26	26	26
ADC	Units	1	1	1	1	1	1	1
	Channels (External)	13	13	12	12	11	11	11
	Channels (Internal)	3	3	3	3	3	3	3
CMP		2	2	2	2	2	2	2
Package		QFN48		LQFP32		QFN28		

Table 2-3. GD32C231xx devices features and peripheral list 3

Part Number		GD32C231xx				
		F6P6TR	F8P6TR	F8P7TR	F6V6TR	F8V6TR
FLASH (KB)		32	64	64	32	64
SRAM (KB)		12	12	12	12	12
Timers	General timer(16-bit)	4 (2, 13, 15,16)	4 (2, 13, 15,16)	4 (2, 13, 15,16)	4 (2, 13, 15,16)	4 (2, 13, 15,16)
	SysTick	1	1	1	1	1
	Advanced timer(16-bit)	1 (0)	1 (0)	1 (0)	1 (0)	1 (0)
	Watchdog	2	2	2	2	2
	RTC	1	1	1	1	1
Connectivity	USART	2 (0, 1)	2 (0, 1)	2 (0, 1)	2 (0, 1)	2 (0, 1)
	I2C	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)	2 (0-1)
	SPI/I2S	2/1 (0-1)/(0)	2/1 (0-1)/(0)	2/1 (0-1)/(0)	2/1 (0-1)/(0)	2/1 (0-1)/(0)
GPIO		18	18	18	18	18
ADC	Units	1	1	1	1	1
	Channels (External)	9	9	9	9	9
	Channels (Internal)	3	3	3	3	3
CMP		2	2	2	2	2
Package		TSSOP20			LGA20	

2.2. Block diagram

Figure 2-1. GD32C231xx block diagram



2.3. Pinouts and pin assignment

The figures below all show the package top view.

Figure 2-2. GD32C231Cx LQFP48 pinouts

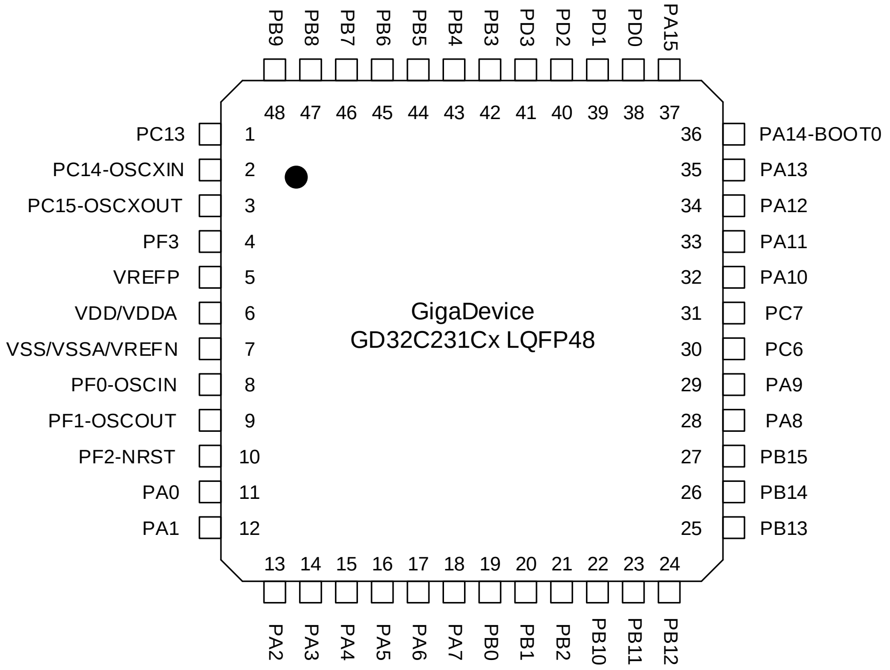


Figure 2-3. GD32C231Cx QFN48 pinouts

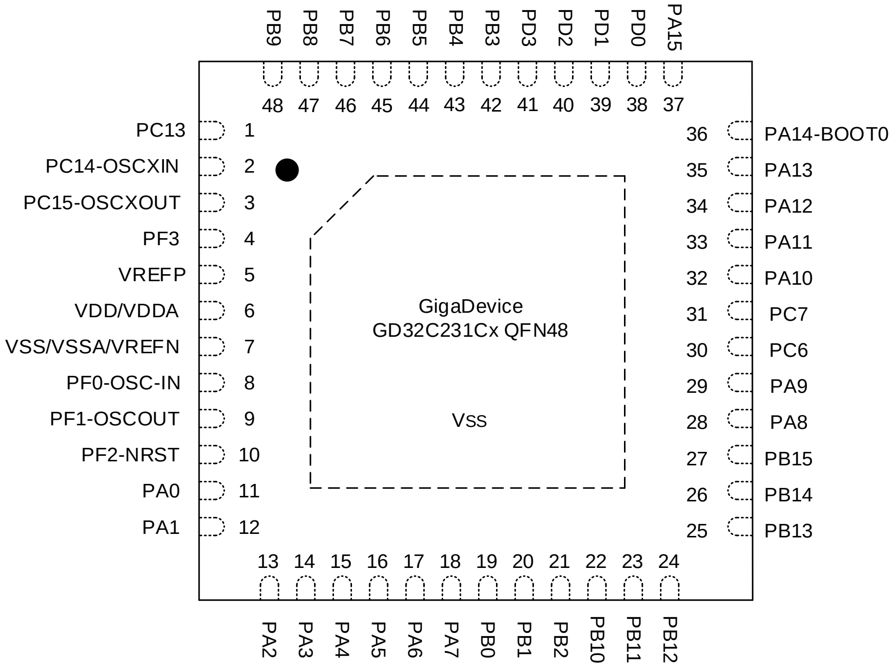


Figure 2-4. GD32C231Kx LQFP32 pinouts

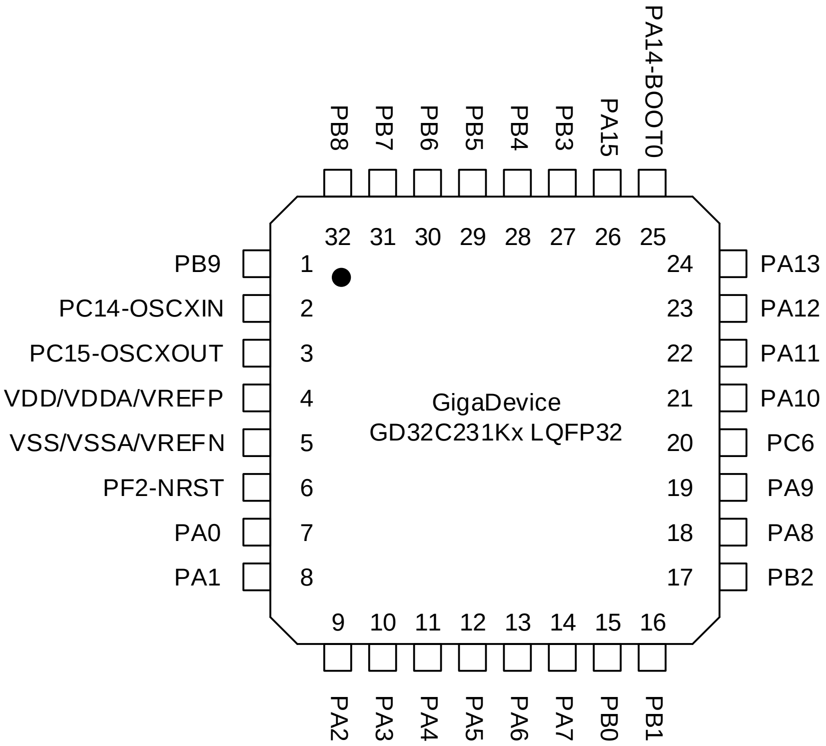


Figure 2-5. GD32C231Kx QFN32 pinouts

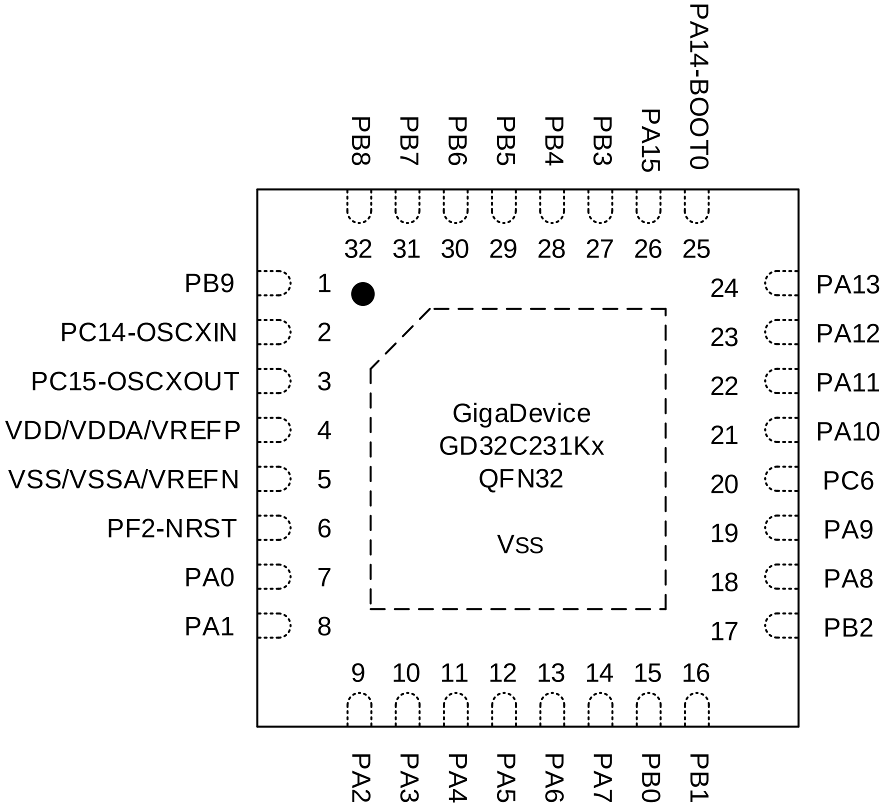


Figure 2-6. GD32C231Gx QFN28 pinouts

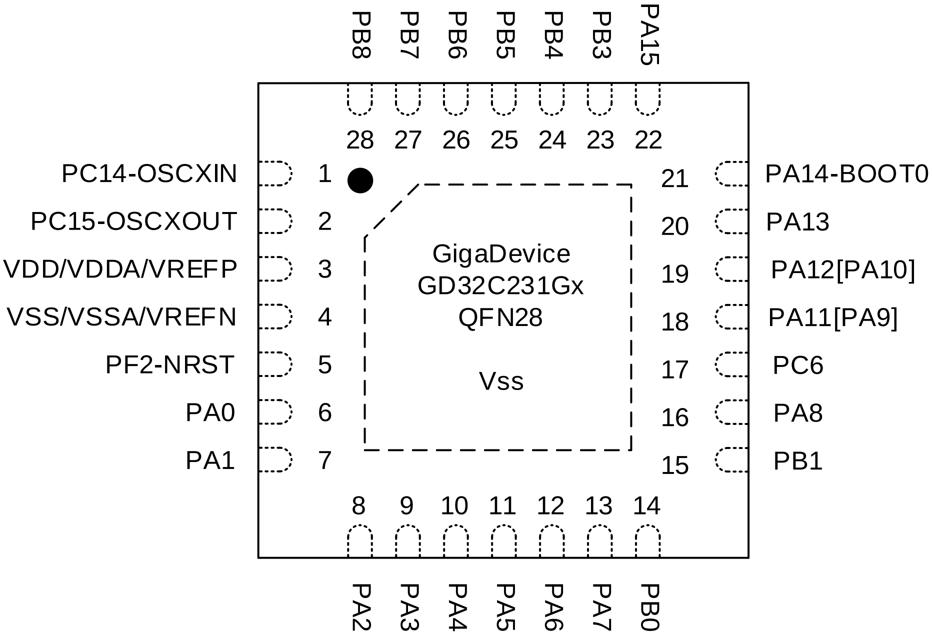


Figure 2-7. GD32C231Fx TSSOP20 pinouts

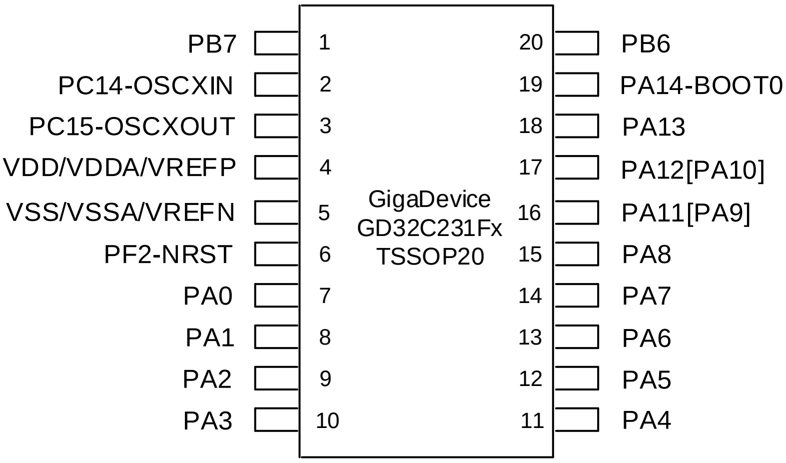
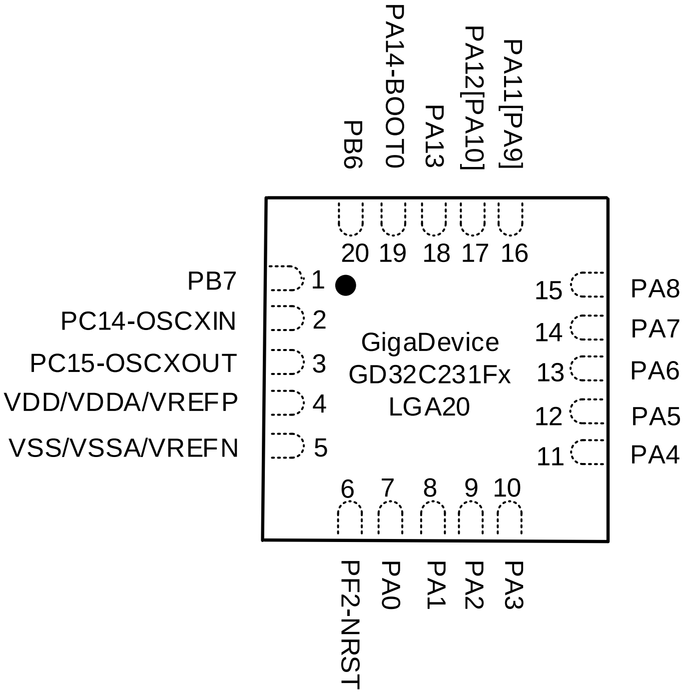


Figure 2-8. GD32C231Fx LGA20 pinouts



2.4. Memory map

Table 2-4. GD32C231xx memory map

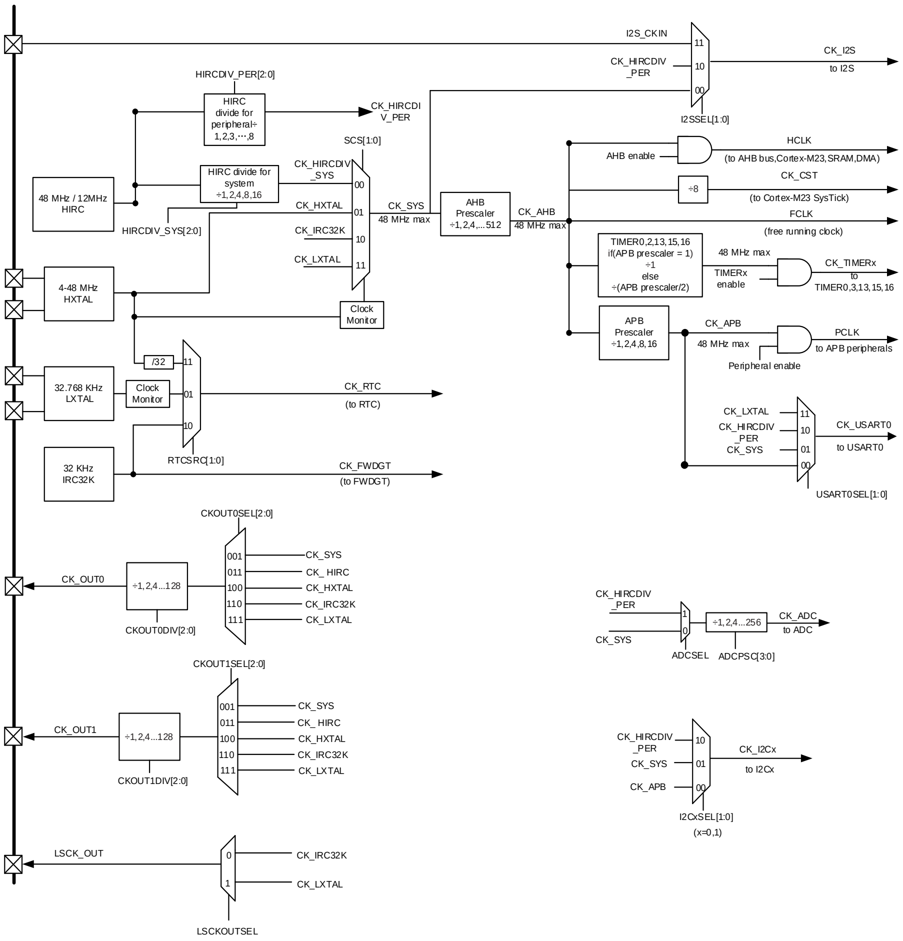
Pre-defined Regions	Bus	ADDRESS	Peripherals
		0xE000 0000 - 0xE00F FFFF	Cortex M23 internal peripherals
External Device		0xA000 0000 - 0xDFFF FFFF	Reserved
External RAM		0x60000000 - 0x9FFFFFFF	Reserved
Peripherals	AHB2	0x5004 0000 - 0x5FFF FFFF	Reserved
		0x5000 0000 - 0x5003 FFFF	Reserved
		0x4800 1800 - 0x4FFF FFFF	Reserved
		0x4800 1400 - 0x4800 17FF	GPIOF
		0x4800 1000 - 0x4800 13FF	Reserved
		0x4800 0C00 - 0x4800 0FFF	GPIOD
		0x4800 0800 - 0x4800 0BFF	GPIOC
		0x4800 0400 - 0x4800 07FF	GPIOB
		0x4800 0000 - 0x4800 03FF	GPIOA
	AHB1	0x4003 8400 - 0x47FF FFFF	Reserved
		0x4003 8000 - 0x4003 83FF	Reserved
		0x4002 4000 - 0x4003 7FFF	Reserved
		0x4002 3400 - 0x4002 3FFF	Reserved
		0x4002 3000 - 0x4002 33FF	CRC
		0x4002 2400 - 0x4002 2FFF	Reserved
		0x4002 2000 - 0x4002 23FF	FMC
		0x4002 1400 - 0x4002 1FFF	Reserved
		0x4002 1000 - 0x4002 13FF	RCU
		0x4002 0C00 - 0x4002 0FFF	Reserved
		0x4002 0800 - 0x4002 0BFF	DMAMUX
		0x4002 0400 - 0x4002 07FF	Reserved
		0x4002 0000 - 0x4002 03FF	DMA
	APB	0x4001 8000 - 0x4001 FFFF	Reserved
		0x4001 7C00 - 0x4001 7FFF	CMP
		0x4001 7800 - 0x4001 7BFF	Reserved
		0x4001 7400 - 0x4001 77FF	Reserved
		0x4001 7000 - 0x4001 73FF	Reserved
		0x4001 6C00 - 0x4001 6FFF	Reserved
		0x4001 6800 - 0x4001 6BFF	Reserved
		0x4001 5C00 - 0x4001 67FF	Reserved
		0x4001 5800 - 0x4001 5BFF	DBG
		0x4001 5400 - 0x4001 57FF	Reserved
		0x4001 5000 - 0x4001 53FF	Reserved
		0x4001 4C00 - 0x4001 4FFF	Reserved
		0x4001 4800 - 0x4001 4BFF	TIMER16

Pre-defined Regions	Bus	ADDRESS	Peripherals
		0x4001 4400 - 0x4001 47FF	TIMER15
		0x4001 3C00 - 0x4001 43FF	Reserved
		0x4001 3800 - 0x4001 3BFF	USART0
		0x4001 3400 - 0x4001 37FF	Reserved
		0x4001 3000 - 0x4001 33FF	SPI0/I2S
		0x4001 2C00 - 0x4001 2FFF	TIMER0
		0x4001 2800 - 0x4001 2BFF	Reserved
		0x4001 2400 - 0x4001 27FF	ADC
		0x4001 2000 - 0x4001 23FF	Reserved
		0x4001 1C00 - 0x4001 1FFF	Reserved
		0x4001 1800 - 0x4001 1BFF	Reserved
		0x4001 1400 - 0x4001 17FF	Reserved
		0x4001 1000 - 0x4001 13FF	Reserved
		0x4001 0C00 - 0x4001 0FFF	Reserved
		0x4001 0800 - 0x4001 23FF	Reserved
		0x4001 0400 - 0x4001 07FF	EXTI
		0x4001 0000 - 0x4001 03FF	SYSCFG
		0x4000 C000 - 0x4000 FFFF	Reserved
		0x4000 7400 - 0x4000 BFFF	Reserved
		0x4000 7000 - 0x4000 73FF	PMU
		0x4000 5C00 - 0x4000 6FFF	Reserved
		0x4000 5800 - 0x4000 5BFF	I2C1
		0x4000 5400 - 0x4000 57FF	I2C0
		0x4000 4C00 - 0x4000 53FF	Reserved
		0x4000 4800 - 0x4000 4BFF	USART2
		0x4000 4400 - 0x4000 47FF	USART1
		0x4000 3C00 - 0x4000 43FF	Reserved
		0x4000 3800 - 0x4000 3BFF	SPI1
		0x4000 3400 - 0x4000 37FF	Reserved
		0x4000 3000 - 0x4000 33FF	FWDGT
		0x4000 2C00 - 0x4000 2FFF	WWDGT
		0x4000 2800 - 0x4000 2BFF	RTC
		0x4000 2400 - 0x4000 27FF	Reserved
		0x4000 2000 - 0x4000 23FF	TIMER13
		0x4000 0800 - 0x4000 1FFF	Reserved
		0x4000 0400 - 0x4000 07FF	TIMER2
		0x4000 0000 - 0x4000 03FF	Reserved
SRAM		0x2000 3000 - 0x3FFF FFFF	Reserved
		0x2000 0000 - 0x2000 2FFF	SRAM(12KB)
Code		0x1FFF 7880 - 0x1FFF FFFF	Reserved
		0x1FFF 7800 - 0x1FFF 787F	Option bytes(128B)
		0x1FFF 7400 - 0x1FFF 77FF	Reserved

Pre-defined Regions	Bus	ADDRESS	Peripherals
		0x1FFF 7000 - 0x1FFF 73FF	OTP bytes(1KB)
		0x1FFF 0C00 - 0x1FFF 6FFF	Reserved
		0x1FFF 0000 - 0x1FFF 0BFF	System memory(3KB)
		0x0801 0000 - 0x1FFE FFFF	Reserved
		0x0800 0000 - 0x0800 FFFF	Flash memory(64KB)
		0x0000 0000 - 0x07FF FFFF	Aliased to Flash or system memory

2.5. Clock tree

Figure 2-9. GD32C231xx clock tree



Legend:

HXTAL: High speed crystal oscillator

LXTAL: Low speed crystal oscillator

HIRC: High speed internal RC oscillator

IRC32K: Internal 32K RC oscillator

2.6. Pin definitions

2.6.1. GD32C231Cx LQFP48 pin definitions

Table 2-5. GD32C231Cx LQFP48 pin definitions

GD32C231Cx LQFP48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PC13	1	I/O		Default: PC13 Alternate: TIMER0_ETI, TIMER0_BRKIN0 Additional: RTC_TS, RTC_OUT0, WKUP1
PC14-OSCXIN	2	I/O		Default: PC14 Alternate: USART0_TX, TIMER0_ETI, TIMER0_BRKIN1, USART1_RTS_DE_CK, TIMER16_CH0, TIMER2_CH1, EVENTOUT Additional: OSC32IN, OSCIN
PC15-OSCXOUT	3	I/O		Default: PC15 Alternate: OSC32EN, OSCEN, TIMER0_ETI, TIMER2_CH2 Additional: OSC32OUT, OSCOUT
PF3	4	I/O		Default: PF3
VREFP	5	P	-	Default: VREFP
VDD/VDDA	6	P	-	Default: VDD/VDDA
VSS/VSSA/VREFN	7	P	-	Default: VSS/VSSA/VREFN
PF0-OSCIN	8	I/O		Default: PF0 Alternate: TIMER13_CH0 Additional: OSCIN
PF1-OSCOUT	9	I/O		Default: PF1 Alternate: OSCEN Additional: OSCOUT
PF2-NRST	10	I/O		Default: NRST Alternate: CK_OUT0, TIMER0_CH3 Additional: PF2(3)
PA0	11	I/O		Default: PA0 Alternate: SPI1_SCK, USART1_CTS, TIMER15_CH0, USART0_TX, TIMER0_CH0, CMP0_OUT Additional: ADC_IN0, WKUP0, CMP0_IM5
PA1	12	I/O	5VT	Default: PA1 Alternate: SPI0_SCK, I2S0_CK, USART1_RTS_DE_CK, TIMER16_CH0, SPI1_IO2, USART0_RX, TIMER0_CH1, I2C0_SMBA, EVENTOUT Additional: ADC_IN1，CMP0_IP
PA2	13	I/O		Default: PA2 Alternate: SPI0_MOSI, I2S0_SD, USART1_TX, TIMER15_CH0_ON, TIMER2_ETI, SPI1_IO3, TIMER0_CH2, USART2_TX, CMP1_OUT

GD32C231Cx LQFP48				
Pin Name	**Pins**	**Pin Type[(1)]**	**I/O Level[(2)]**	**Functions description**
				Additional: ADC_IN2, WKUP3, LSCK_OUT, CMP1_IM5
PA3	14	I/O		Default: PA3 Alternate: SPI1_MISO, USART1_RX, TIMER0_CH0_ON, TIMER0_CH3, USART2_RX, EVENTOUT Additional: ADC_IN3, CMP1_IP
PA4	15	I/O		Default: PA4 Alternate: SPI0_NSS, I2S0_WS, USART1_TX, TIMER0_CH1_ON, SPI1_MOSI, TIMER13_CH0, TIMER16_CH0_ON, EVENTOUT Additional: ADC_IN4, RTC_OUT1， RTC_TS, RTC_OUT0
PA5	16	I/O		Default: PA5 Alternate: SPI0_SCK, I2S0_CK, USART1_RX, TIMER0_CH2_ON, SPI1_IO2, TIMER0_CH0, EVENTOUT Additional: ADC_IN5
PA6	17	I/O		Default: PA6 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, TIMER0_BRKIN0, SPI1_IO3, TIMER15_CH0, USART2_CTS, CMP0_OUT Additional: ADC_IN6
PA7	18	I/O		Default: PA7 Alternate: SPI0_MOSI, I2S0_SD, TIMER2_CH1, TIMER0_CH0_ON, TIMER13_CH0, TIMER16_CH0, USART2_RTS_DE_CK, CMP1_OUT Additional: ADC_IN7
PB0	19	I/O		Default: PB0 Alternate: SPI0_NSS, I2S0_WS, TIMER2_CH2, TIMER0_CH1_ON, CMP0_OUT Additional: ADC_IN8
PB1	20	I/O		Default: PB1 Alternate: TIMER13_CH0, TIMER2_CH3, TIMER0_CH2_ON, TIMER0_CH1_ON, USART2_RTS_DE_CK, EVENTOUT Additional: ADC_IN9, CMP0_IM6
PB2	21	I/O		Default: PB2 Alternate: USART0_RX, SPI1_MISO, CK_OUT1, EVENTOUT Additional: CMP0_IM4, ADC_IN10
PB10	22	I/O	5VT	Default: PB10 Alternate: USART2_RX, SPI1_SCK, I2C1_SCL, CMP0_OUT Additional: ADC_IN11
PB11	23	I/O	5VT	Default: PB11 Alternate: SPI1_MOSI, USART2_TX, I2C1_SDA, CMP1_OUT

GD32C231Cx LQFP48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PB12	24	I/O		Default: PB12 Alternate: SPI1_NSS, TIMER0_BRKIN1, TIMER0_BRKIN0, USART2_RTS_DE_CK, EVENTOUT
PB13	25	I/O		Default: PB13 Alternate: SPI1_SCK, USART2_CTS, TIMER0_CH0_ON, EVENTOUT
PB14	26	I/O		Default: PB14 Alternate: SPI1_MISO, TIMER0_CH1_ON, EVENTOUT
PB15	27	I/O		Default: PB15 Alternate: SPI1_MOSI, TIMER0_CH2_ON, EVENTOUT Additional: RTC_REFIN
PA8	28	I/O		Default: PA8 Alternate: CK_OUT0, USART1_TX, TIMER0_CH0, SPI1_NSS, EVENTOUT, SPI0_NSS, I2S0_WS, TIMER0_CH1_ON, TIMER0_CH2_ON, TIMER2_CH2, TIMER2_CH3, TIMER13_CH0, USART0_RX, CK_OUT1
PA9	29	I/O	5VT	Default: PA9 Alternate: CK_OUT0, USART0_TX, TIMER0_CH1, TIMER2_ETI, SPI1_MISO, I2C0_SCL, EVENTOUT
PC6	30	I/O		Default: PC6 Alternate: TIMER2_CH0
PC7	31	I/O		Default: PC7 Alternate: TIMER2_CH1
PA10	32	I/O	5VT	Default: PA10 Alternate: SPI1_MOSI, USART0_RX, TIMER0_CH2, CK_OUT1, TIMER16_BRKIN0, I2C0_SDA, EVENTOUT
PA11	33	I/O	5VT	Default: PA11 Alternate: SPI0_MISO, I2S0_MCK, USART0_CTS, TIMER0_CH3, SPI1_IO2, TIMER0_BRKIN1, I2C1_SCL, CMP0_OUT
PA12	34	I/O	5VT	Default: PA12 Alternate: SPI0_MOSI, I2S0_SD, USART0_RTS_DE_CK, TIMER0_ETI, SPI1_IO3, I2S_CKIN, I2C1_SDA, CMP1_OUT Additional: ADC_IN12
PA13	35	I/O		Default: PA13, SWDIO Alternate: SWDIO, TIMER2_ETI, USART1_RX, EVENTOUT
PA14-BOOT0	36	I/O		Default: PA14, SWCLK Alternate: SWCLK, USART1_TX, EVENTOUT, SPI0_NSS, I2S0_WS, USART1_RX, TIMER0_CH0, CK_OUT1, USART0_RTS_DE_CK

GD32C231Cx LQFP48

Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Additional: BOOT0
PA15	37	I/O		Default: PA15 Alternate: SPI0_NSS, I2S0_WS, USART1_RX, TIMER0_CH0, CK_OUT1, USART0_RTS_DE_CK, EVENTOUT
PD0	38	I/O		Default: PD0 Alternate: EVENTOUT, SPI1_NSS, TIMER15_CH0
PD1	39	I/O		Default: PD1 Alternate: EVENTOUT, SPI1_SCK, TIMER16_CH0
PD2	40	I/O		Default: PD2 Alternate: TIMER2_ETI, TIMER0_CH0_ON
PD3	41	I/O		Default: PD3 Alternate: USART1_CTS, SPI1_MISO, TIMER0_CH1_ON
PB3	42	I/O		Default: PB3 Alternate: SPI0_SCK, I2S0_CK, TIMER0_CH1, TIMER2_CH1, USART0_RTS_DE_CK, EVENTOUT Additional: CMP1_IM6
PB4	43	I/O		Default: PB4 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, USART0_CTS, TIMER16_BRKIN0, EVENTOUT Additional: CMP1_IM7
PB5	44	I/O	5VT	Default: PB5 Alternate: SPI0_MOSI, I2S0_SD, TIMER2_CH1, TIMER15_BRKIN0, TIMER2_CH2, SPI1_MISO, I2C0_SMBA, CMP1_OUT Additional: WKUP5
PB6	45	I/O	5VT	Default: PB6 Alternate: USART0_TX, TIMER0_CH2, TIMER15_CH0_ON, TIMER2_CH2, USART0_RTS_DE_CK, USART0_CTS, I2C0_SCL, I2C0_SMBA, SPI0_MOSI, I2S0_SD, SPI0_MISO, I2S0_MCK, SPI0_SCK, I2S0_CK, TIMER0_CH1, TIMER2_CH0, TIMER2_CH1, TIMER15_BRKIN0, TIMER16_BRKIN0 Additional: WKUP2, CMP1_IM4
PB7	46	I/O	5VT	Default: PB7 Alternate: USART0_RX, TIMER0_CH3, TIMER16_CH0_ON, TIMER2_CH3, SPI1_MOSI, I2C0_SDA, EVENTOUT, USART1_CTS, TIMER15_CH0, TIMER2_CH0, I2C0_SCL Additional: RTC_REFIN
PB8	47	I/O	5VT	Default: PB8 Alternate: SPI1_SCK, USART1_CTS, TIMER15_CH0, TIMER2_CH0, I2C0_SCL, EVENTOUT
PB9	48	I/O	5VT	Default: PB9

GD32C231Cx LQFP48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: USART1_RTS_DE_CK, TIMER16_CH0, TIMER2_CH1, SPI1_NSS, I2C0_SDA, EVENTOUT

Note:

(1) Type: I = input, O = output, A = analog, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Refer to the description of the NRST_MDSEL[1:0] field in FMC_OBCTL register of GD32C2x1_User_Manual to configure the PF2-NRST pin as a PF2 general GPIO function.

2.6.2. GD32C231Cx QFN48 pin definitions

Table 2-6. GD32C231Cx QFN48 pin definitions

GD32C231Cx QFN48				
Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
PC13	1	I/O		Default: PC13 Alternate: TIMER0_ETI, TIMER0_BRKIN0 Additional: RTC_TS, RTC_OUT0, WKUP1
PC14-OSCXIN	2	I/O		Default: PC14 Alternate: USART0_TX, TIMER0_ETI, TIMER0_BRKIN1, USART1_RTS_DE_CK, TIMER16_CH0, TIMER2_CH1, EVENTOUT Additional: OSC32IN, OSCIN
PC15-OSCXOUT	3	I/O		Default: PC15 Alternate: OSC32EN, OSCEN, TIMER0_ETI, TIMER2_CH2 Additional: OSC32OUT, OSCOUT
PF3	4	I/O		Default: PF3
VREFP	5	P	-	Default: VREFP
VDD/VDDA	6	P	-	Default: VDD/VDDA
VSS/VSSA/VREFN	7	P	-	Default: VSS/VSSA/VREFN
PF0-OSCIN	8	I/O		Default: PF0 Alternate: TIMER13_CH0 Additional: OSCIN
PF1-OSCOUT	9	I/O		Default: PF1 Alternate: OSCEN Additional: OSCOUT
PF2-NRST	10	I/O		Default: NRST Alternate: CK_OUT0, TIMER0_CH3 Additional: PF2[3]
PA0	11	I/O		Default: PA0 Alternate: SPI1_SCK, USART1_CTS, TIMER15_CH0, USART0_TX, TIMER0_CH0, CMP0_OUT Additional: ADC_IN0, WKUP0, CMP0_IM5
PA1	12	I/O	5VT	Default: PA1 Alternate: SPI0_SCK, I2S0_CK, USART1_RTS_DE_CK, TIMER16_CH0, SPI1_IO2, USART0_RX, TIMER0_CH1, I2C0_SMBA, EVENTOUT Additional: ADC_IN1，CMP0_IP
PA2	13	I/O		Default: PA2 Alternate: SPI0_MOSI, I2S0_SD, USART1_TX, TIMER15_CH0_ON, TIMER2_ETI, SPI1_IO3, TIMER0_CH2, USART2_TX, CMP1_OUT Additional: ADC_IN2, WKUP3, LSCK_OUT, CMP1_IM5
PA3	14	I/O		Default: PA3

GD32C231Cx QFN48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: SPI1_MISO, USART1_RX, TIMER0_CH0_ON, TIMER0_CH3, USART2_RX, EVENTOUT Additional: ADC_IN3, CMP1_IP
PA4	15	I/O		Default: PA4 Alternate: SPI0_NSS, I2S0_WS, USART1_TX, TIMER0_CH1_ON, SPI1_MOSI, TIMER13_CH0, TIMER16_CH0_ON, EVENTOUT Additional: ADC_IN4, RTC_OUT1， RTC_TS, RTC_OUT0
PA5	16	I/O		Default: PA5 Alternate: SPI0_SCK, I2S0_CK, USART1_RX, TIMER0_CH2_ON, SPI1_IO2, TIMER0_CH0, EVENTOUT Additional: ADC_IN5
PA6	17	I/O		Default: PA6 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, TIMER0_BRKIN0, SPI1_IO3, TIMER15_CH0, USART2_CTS, CMP0_OUT Additional: ADC_IN6
PA7	18	I/O		Default: PA7 Alternate: SPI0_MOSI, I2S0_SD, TIMER2_CH1, TIMER0_CH0_ON, TIMER13_CH0, TIMER16_CH0, USART2_RTS_DE_CK, CMP1_OUT Additional: ADC_IN7
PB0	19	I/O		Default: PB0 Alternate: SPI0_NSS, I2S0_WS, TIMER2_CH2, TIMER0_CH1_ON, CMP0_OUT Additional: ADC_IN8
PB1	20	I/O		Default: PB1 Alternate: TIMER13_CH0, TIMER2_CH3, TIMER0_CH2_ON, TIMER0_CH1_ON, USART2_RTS_DE_CK, EVENTOUT Additional: ADC_IN9, CMP0_IM6
PB2	21	I/O		Default: PB2 Alternate: USART0_RX, SPI1_MISO, CK_OUT1, EVENTOUT Additional: CMP0_IM4, ADC_IN10
PB10	22	I/O	5VT	Default: PB10 Alternate: USART2_RX, SPI1_SCK, I2C1_SCL, CMP0_OUT Additional: ADC_IN11
PB11	23	I/O	5VT	Default: PB11 Alternate: SPI1_MOSI, USART2_TX, I2C1_SDA, CMP1_OUT
PB12	24	I/O		Default: PB12 Alternate: SPI1_NSS, TIMER0_BRKIN1, TIMER0_BRKIN0, USART2_RTS_DE_CK, EVENTOUT

GD32C231Cx QFN48				
Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
PB13	25	I/O		Default: PB13 Alternate: SPI1_SCK, USART2_CTS, TIMER0_CH0_ON, EVENTOUT
PB14	26	I/O		Default: PB14 Alternate: SPI1_MISO, TIMER0_CH1_ON, EVENTOUT
PB15	27	I/O		Default: PB15 Alternate: SPI1_MOSI, TIMER0_CH2_ON, EVENTOUT Additional: RTC_REFIN
PA8	28	I/O		Default: PA8 Alternate: CK_OUT0, USART1_TX, TIMER0_CH0, SPI1_NSS, EVENTOUT, SPI0_NSS, I2S0_WS, TIMER0_CH1_ON, TIMER0_CH2_ON, TIMER2_CH2, TIMER2_CH3, TIMER13_CH0, USART0_RX, CK_OUT1
PA9	29	I/O	5VT	Default: PA9 Alternate: CK_OUT0, USART0_TX, TIMER0_CH1, TIMER2_ETI, SPI1_MISO, I2C0_SCL, EVENTOUT
PC6	30	I/O		Default: PC6 Alternate: TIMER2_CH0
PC7	31	I/O		Default: PC7 Alternate: TIMER2_CH1
PA10	32	I/O	5VT	Default: PA10 Alternate: SPI1_MOSI, USART0_RX, TIMER0_CH2, CK_OUT1, TIMER16_BRKIN0, I2C0_SDA, EVENTOUT
PA11	33	I/O	5VT	Default: PA11 Alternate: SPI0_MISO, I2S0_MCK, USART0_CTS, TIMER0_CH3, SPI1_IO2, TIMER0_BRKIN1, I2C1_SCL, CMP0_OUT
PA12	34	I/O	5VT	Default: PA12 Alternate: SPI0_MOSI, I2S0_SD, USART0_RTS_DE_CK, TIMER0_ETI, SPI1_IO3, I2S_CKIN, I2C1_SDA, CMP1_OUT Additional: ADC_IN12
PA13	35	I/O		Default: PA13, SWDIO Alternate: SWDIO, TIMER2_ETI, USART1_RX, EVENTOUT
PA14-BOOT0	36	I/O		Default: PA14, SWCLK Alternate: SWCLK, USART1_TX, EVENTOUT, SPI0_NSS, I2S0_WS, USART1_RX, TIMER0_CH0, CK_OUT1, USART0_RTS_DE_CK Additional: BOOT0
PA15	37	I/O		Default: PA15

GD32C231Cx QFN48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: SPI0_NSS, I2S0_WS, USART1_RX, TIMER0_CH0, CK_OUT1, USART0_RTS_DE_CK, EVENTOUT
PD0	38	I/O		Default: PD0 Alternate: EVENTOUT, SPI1_NSS, TIMER15_CH0
PD1	39	I/O		Default: PD1 Alternate: EVENTOUT, SPI1_SCK, TIMER16_CH0
PD2	40	I/O		Default: PD2 Alternate: TIMER2_ETI, TIMER0_CH0_ON
PD3	41	I/O		Default: PD3 Alternate: USART1_CTS, SPI1_MISO, TIMER0_CH1_ON
PB3	42	I/O		Default: PB3 Alternate: SPI0_SCK, I2S0_CK, TIMER0_CH1, TIMER2_CH1, USART0_RTS_DE_CK, EVENTOUT Additional: CMP1_IM6
PB4	43	I/O		Default: PB4 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, USART0_CTS, TIMER16_BRKIN0, EVENTOUT Additional: CMP1_IM7
PB5	44	I/O	5VT	Default: PB5 Alternate: SPI0_MOSI, I2S0_SD, TIMER2_CH1, TIMER15_BRKIN0, TIMER2_CH2, SPI1_MISO, I2C0_SMBA, CMP1_OUT Additional: WKUP5
PB6	45	I/O	5VT	Default: PB6 Alternate: USART0_TX, TIMER0_CH2, TIMER15_CH0_ON, TIMER2_CH2, USART0_RTS_DE_CK, USART0_CTS, I2C0_SCL, I2C0_SMBA, SPI0_MOSI, I2S0_SD, SPI0_MISO, I2S0_MCK, SPI0_SCK, I2S0_CK, TIMER0_CH1, TIMER2_CH0, TIMER2_CH1, TIMER15_BRKIN0, TIMER16_BRKIN0 Additional: WKUP2, CMP1_IM4
PB7	46	I/O	5VT	Default: PB7 Alternate: USART0_RX, TIMER0_CH3, TIMER16_CH0_ON, TIMER2_CH3, SPI1_MOSI, I2C0_SDA, EVENTOUT, USART1_CTS, TIMER15_CH0, TIMER2_CH0, I2C0_SCL Additional: RTC_REFIN
PB8	47	I/O	5VT	Default: PB8 Alternate: SPI1_SCK, USART1_CTS, TIMER15_CH0, TIMER2_CH0, I2C0_SCL, EVENTOUT
PB9	48	I/O	5VT	Default: PB9 Alternate: USART1_RTS_DE_CK, TIMER16_CH0, TIMER2_CH1, SPI1_NSS, I2C0_SDA, EVENTOUT

Note:

(1) Type: I = input, O = output, A = analog, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Refer to the description of the NRST_MDSEL[1:0] field in FMC_OBCTL register of GD32C2x1_User_Manual to configure the PF2-NRST pin as a PF2 general GPIO function.

2.6.3. GD32C231Kx LQFP32 pin definitions

Table 2-7. GD32C231Kx LQFP32 pin definitions

GD32C231Kx LQFP32				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PB9	1	I/O	5VT	Default: PB9 Alternate: USART1_RTS_DE_CK, TIMER16_CH0, TIMER2_CH1, SPI1_NSS, I2C0_SDA, EVENTOUT
PC14-OSCXIN	2	I/O		Default: PC14 Alternate: USART0_TX, TIMER0_ETI, TIMER0_BRKIN1, USART1_RTS_DE_CK, TIMER16_CH0, TIMER2_CH1, EVENTOUT Additional: OSC32IN, OSCIN
PC15-OSCXOUT	3	I/O		Default: PC15 Alternate: OSC32EN, OSCEN, TIMER0_ETI, TIMER2_CH2 Additional: OSC32OUT, OSCOUT
VDD/VDDA/VREFP	4	P	-	Default: VDD/VDDA/VREFP
VSS/VSSA/VREFN	5	P	-	Default: VSS/VSSA/VREFN
PF2-NRST	6	I/O		Default: NRST Alternate: CK_OUT0, TIMER0_CH3 Additional: PF2(3)
PA0	7	I/O		Default: PA0 Alternate: SPI1_SCK, USART1_CTS, TIMER15_CH0, USART0_TX, TIMER0_CH0, CMP0_OUT Additional: ADC_IN0, WKUP0, CMP0_IM5
PA1	8	I/O	5VT	Default: PA1 Alternate: SPI0_SCK, I2S0_CK, USART1_RTS_DE_CK, TIMER16_CH0, SPI1_IO2, USART0_RX, TIMER0_CH1, I2C0_SMBA, EVENTOUT Additional: ADC_IN1，CMP0_IP
PA2	9	I/O		Default: PA2 Alternate: SPI0_MOSI, I2S0_SD, USART1_TX, TIMER15_CH0_ON, TIMER2_ETI, SPI1_IO3, TIMER0_CH2, USART2_TX, CMP1_OUT Additional: ADC_IN2, WKUP3, LSCK_OUT, CMP1_IM5
PA3	10	I/O		Default: PA3 Alternate: SPI1_MISO, USART1_RX, TIMER0_CH0_ON, TIMER0_CH3, USART2_RX, EVENTOUT Additional: ADC_IN3, CMP1_IP
PA4	11	I/O		Default: PA4 Alternate: SPI0_NSS, I2S0_WS, USART1_TX, TIMER0_CH1_ON, SPI1_MOSI, TIMER13_CH0, TIMER16_CH0_ON, EVENTOUT

GD32C231Kx LQFP32				
Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Additional: ADC_IN4, RTC_OUT1， RTC_TS, RTC_OUT0, WKUP1
PA5	12	I/O		Default: PA5 Alternate: SPI0_SCK, I2S0_CK, USART1_RX, TIMER0_CH2_ON, SPI1_IO2, TIMER0_CH0, EVENTOUT Additional: ADC_IN5
PA6	13	I/O		Default: PA6 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, TIMER0_BRKIN0, SPI1_IO3, TIMER15_CH0, USART2_CTS, CMP0_OUT Additional: ADC_IN6
PA7	14	I/O		Default: PA7 Alternate: SPI0_MOSI, I2S0_SD, TIMER2_CH1, TIMER0_CH0_ON, TIMER13_CH0, TIMER16_CH0, USART2_RTS_DE_CK, CMP1_OUT Additional: ADC_IN7
PB0	15	I/O		Default: PB0 Alternate: SPI0_NSS, I2S0_WS, TIMER2_CH2, TIMER0_CH1_ON, CMP0_OUT Additional: ADC_IN8
PB1	16	I/O		Default: PB1 Alternate: TIMER13_CH0, TIMER2_CH3, TIMER0_CH2_ON, TIMER0_CH1_ON, USART2_RTS_DE_CK, EVENTOUT Additional: ADC_IN9, CMP0_IM6
PB2	17	I/O		Default: PB2 Alternate: USART0_RX, SPI1_MISO, CK_OUT1, EVENTOUT Additional: CMP0_IM4, ADC_IN10
PA8	18	I/O		Default: PA8 Alternate: CK_OUT0, USART1_TX, TIMER0_CH0, SPI1_NSS, EVENTOUT, SPI0_NSS, I2S0_WS, TIMER0_CH1_ON, TIMER0_CH2_ON, TIMER2_CH2, TIMER2_CH3, TIMER13_CH0, USART0_RX, CK_OUT1
PA9	19	I/O	5VT	Default: PA9 Alternate: CK_OUT0, USART0_TX, TIMER0_CH1, TIMER2_ETI, SPI1_MISO, I2C0_SCL, EVENTOUT
PC6	20	I/O		Default: PC6 Alternate: TIMER2_CH0
PA10	21	I/O	5VT	Default: PA10 Alternate: SPI1_MOSI, USART0_RX, TIMER0_CH2, CK_OUT1, TIMER16_BRKIN0, I2C0_SDA, EVENTOUT
PA11	22	I/O	5VT	Default: PA11 Alternate: SPI0_MISO, I2S0_MCK, USART0_CTS, T

GD32C231Kx LQFP32				
Pin Name	**Pins**	**Pin Type[(1)]**	**I/O Level[(2)]**	**Functions description**
				IMER0_CH3, SPI1_IO2, TIMER0_BRKIN1, I2C1_SCL, CMP0_OUT
PA12	23	I/O	5VT	Default: PA12 Alternate: SPI0_MOSI, I2S0_SD, USART0_RTS_DE_CK, TIMER0_ETI, SPI1_IO3, I2S_CKIN, I2C1_SDA, CMP1_OUT Additional: ADC_IN12
PA13	24	I/O		Default: PA13, SWDIO Alternate: SWDIO, TIMER2_ETI, USART1_RX, EVENTOUT
PA14-BOOT0	25	I/O		Default: PA14, SWCLK Alternate: SWCLK, USART1_TX, EVENTOUT, SPI0_NSS, I2S0_WS, USART1_RX, TIMER0_CH0, CK_OUT1, USART0_RTS_DE_CK Additional: BOOT0
PA15	26	I/O		Default: PA15 Alternate: SPI0_NSS, I2S0_WS, USART1_RX, TIMER0_CH0, CK_OUT1, USART0_RTS_DE_CK, EVENTOUT
PB3	27	I/O		Default: PB3 Alternate: SPI0_SCK, I2S0_CK, TIMER0_CH1, TIMER2_CH1, USART0_RTS_DE_CK, EVENTOUT Additional: CMP1_IM6
PB4	28	I/O		Default: PB4 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, USART0_CTS, TIMER16_BRKIN0, EVENTOUT Additional: CMP1_IM7
PB5	29	I/O	5VT	Default: PB5 Alternate: SPI0_MOSI, I2S0_SD, TIMER2_CH1, TIMER15_BRKIN0, TIMER2_CH2, SPI1_MISO, I2C0_SMBA, CMP1_OUT Additional: WKUP5
PB6	30	I/O	5VT	Default: PB6 Alternate: USART0_TX, TIMER0_CH2, TIMER15_CH0_ON, TIMER2_CH2, USART0_RTS_DE_CK, USART0_CTS, I2C0_SCL, I2C0_SMBA, SPI0_MOSI, I2S0_SD, SPI0_MISO, I2S0_MCK, SPI0_SCK, I2S0_CK, TIMER0_CH1, TIMER2_CH0, TIMER2_CH1, TIMER15_BRKIN0, TIMER16_BRKIN0 Additional: WKUP2, CMP1_IM4
PB7	31	I/O	5VT	Default: PB7 Alternate: USART0_RX, TIMER0_CH3, TIMER16_CH0_ON, TIMER2_CH3, SPI1_MOSI, I2C0_SDA, EVENTOUT, USART1_CTS, TIMER15_CH0, TIMER2_CH0, I2C0_SCL Additional: RTC_REFIN

GD32C231Kx LQFP32				
Pin Name	**Pins**	**Pin Type[(1)]**	**I/O Level[(2)]**	**Functions description**
PB8	32	I/O	5VT	Default: PB8 Alternate: SPI1_SCK, USART1_CTS, TIMER15_CH0, TIMER2_CH0, I2C0_SCL, EVENTOUT

Note:

(1) Type: I = input, O = output, A = analog, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Refer to the description of the NRST_MDSEL[1:0] field in FMC_OBCTL register of GD32C2x1_User_Manual to configure the PF2-NRST pin as a PF2 general GPIO function.

2.6.4. GD32C231Kx QFN32 definitions

Table 2-8. GD32C231Kx QFN32 pin definitions

GD32C231Kx QFN32				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PB9	1	I/O	5VT	Default: PB9 Alternate: USART1_RTS_DE_CK, TIMER16_CH0, TIMER2_CH1, SPI1_NSS, I2C0_SDA, EVENTOUT
PC14-OSCXIN	2	I/O		Default: PC14 Alternate: USART0_TX, TIMER0_ETI, TIMER0_BRKIN1, USART1_RTS_DE_CK, TIMER16_CH0, TIMER2_CH1, EVENTOUT Additional: OSC32IN, OSCIN
PC15-OSCXOUT	3	I/O		Default: PC15 Alternate: OSC32EN, OSCEN, TIMER0_ETI, TIMER2_CH2 Additional: OSC32OUT, OSCOUT
VDD/VDDA/VREFP	4	P	-	Default: VDD/VDDA/VREFP
VSS/VSSA/VREFN	5	P	-	Default: VSS/VSSA/VREFN
PF2-NRST	6	I/O		Default: NRST Alternate: CK_OUT0, TIMER0_CH3 Additional: PF2(3)
PA0	7	I/O		Default: PA0 Alternate: SPI1_SCK, USART1_CTS, TIMER15_CH0, USART0_TX, TIMER0_CH0, CMP0_OUT Additional: ADC_IN0, WKUP0, CMP0_IM5
PA1	8	I/O	5VT	Default: PA1 Alternate: SPI0_SCK, I2S0_CK, USART1_RTS_DE_CK, TIMER16_CH0, SPI1_IO2, USART0_RX, TIMER0_CH1, I2C0_SMBA, EVENTOUT Additional: ADC_IN1，CMP0_IP
PA2	9	I/O		Default: PA2 Alternate: SPI0_MOSI, I2S0_SD, USART1_TX, TIMER15_CH0_ON, TIMER2_ETI, SPI1_IO3, TIMER0_CH2, USART2_TX, CMP1_OUT Additional: ADC_IN2, WKUP3, LSCK_OUT, CMP1_IM5
PA3	10	I/O		Default: PA3 Alternate: SPI1_MISO, USART1_RX, TIMER0_CH0_ON, TIMER0_CH3, USART2_RX, EVENTOUT Additional: ADC_IN3, CMP1_IP
PA4	11	I/O		Default: PA4 Alternate: SPI0_NSS, I2S0_WS, USART1_TX, TIMER0_CH1_ON, SPI1_MOSI, TIMER13_CH0, TIMER16_CH0_ON, EVENTOUT

GD32C231Kx QFN32				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Additional: ADC_IN4, RTC_OUT1， RTC_TS, RTC_OUT0, WKUP1
PA5	12	I/O		Default: PA5 Alternate: SPI0_SCK, I2S0_CK, USART1_RX, TIMER0_CH2_ON, SPI1_IO2, TIMER0_CH0, EVENTOUT Additional: ADC_IN5
PA6	13	I/O		Default: PA6 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, TIMER0_BRKIN0, SPI1_IO3, TIMER15_CH0, USART2_CTS, CMP0_OUT Additional: ADC_IN6
PA7	14	I/O		Default: PA7 Alternate: SPI0_MOSI, I2S0_SD, TIMER2_CH1, TIMER0_CH0_ON, TIMER13_CH0, TIMER16_CH0, USART2_RTS_DE_CK, CMP1_OUT Additional: ADC_IN7
PB0	15	I/O		Default: PB0 Alternate: SPI0_NSS, I2S0_WS, TIMER2_CH2, TIMER0_CH1_ON, CMP0_OUT Additional: ADC_IN8
PB1	16	I/O		Default: PB1 Alternate: TIMER13_CH0, TIMER2_CH3, TIMER0_CH2_ON, TIMER0_CH1_ON, USART2_RTS_DE_CK, EVENTOUT Additional: ADC_IN9, CMP0_IM6
PB2	17	I/O		Default: PB2 Alternate: USART0_RX, SPI1_MISO, CK_OUT1, EVENTOUT Additional: CMP0_IM4, ADC_IN10
PA8	18	I/O		Default: PA8 Alternate: CK_OUT0, USART1_TX, TIMER0_CH0, SPI1_NSS, EVENTOUT, SPI0_NSS, I2S0_WS, TIMER0_CH1_ON, TIMER0_CH2_ON, TIMER2_CH2, TIMER2_CH3, TIMER13_CH0, USART0_RX, CK_OUT1
PA9	19	I/O	5VT	Default: PA9 Alternate: CK_OUT0, USART0_TX, TIMER0_CH1, TIMER2_ETI, SPI1_MISO, I2C0_SCL, EVENTOUT
PC6	20	I/O		Default: PC6 Alternate: TIMER2_CH0
PA10	21	I/O	5VT	Default: PA10 Alternate: SPI1_MOSI, USART0_RX, TIMER0_CH2, CK_OUT1, TIMER16_BRKIN0, I2C0_SDA, EVENTOUT
PA11	22	I/O	5VT	Default: PA11 Alternate: SPI0_MISO, I2S0_MCK, USART0_CTS, T

GD32C231Kx QFN32				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				IMER0_CH3, SPI1_IO2, TIMER0_BRKIN1, I2C1_SCL, CMP0_OUT
PA12	23	I/O	5VT	Default: PA12 Alternate: SPI0_MOSI, I2S0_SD, USART0_RTS_DE_CK, TIMER0_ETI, SPI1_IO3, I2S_CKIN, I2C1_SDA, CMP1_OUT Additional: ADC_IN12
PA13	24	I/O		Default: PA13, SWDIO Alternate: SWDIO, TIMER2_ETI, USART1_RX, EVENTOUT
PA14-BOOT0	25	I/O		Default: PA14, SWCLK Alternate: SWCLK, USART1_TX, EVENTOUT, SPI0_NSS, I2S0_WS, USART1_RX, TIMER0_CH0, CK_OUT1, USART0_RTS_DE_CK Additional: BOOT0
PA15	26	I/O		Default: PA15 Alternate: SPI0_NSS, I2S0_WS, USART1_RX, TIMER0_CH0, CK_OUT1, USART0_RTS_DE_CK, EVENTOUT
PB3	27	I/O		Default: PB3 Alternate: SPI0_SCK, I2S0_CK, TIMER0_CH1, TIMER2_CH1, USART0_RTS_DE_CK, EVENTOUT Additional: CMP1_IM6
PB4	28	I/O		Default: PB4 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, USART0_CTS, TIMER16_BRKIN0, EVENTOUT Additional: CMP1_IM7
PB5	29	I/O	5VT	Default: PB5 Alternate: SPI0_MOSI, I2S0_SD, TIMER2_CH1, TIMER15_BRKIN0, TIMER2_CH2, SPI1_MISO, I2C0_SMBA, CMP1_OUT Additional: WKUP5
PB6	30	I/O	5VT	Default: PB6 Alternate: USART0_TX, TIMER0_CH2, TIMER15_CH0_ON, TIMER2_CH2, USART0_RTS_DE_CK, USART0_CTS, I2C0_SCL, I2C0_SMBA, SPI0_MOSI, I2S0_SD, SPI0_MISO, I2S0_MCK, SPI0_SCK, I2S0_CK, TIMER0_CH1, TIMER2_CH0, TIMER2_CH1, TIMER15_BRKIN0, TIMER16_BRKIN0 Additional: WKUP2, CMP1_IM4
PB7	31	I/O	5VT	Default: PB7 Alternate: USART0_RX, TIMER0_CH3, TIMER16_CH0_ON, TIMER2_CH3, SPI1_MOSI, I2C0_SDA, EVENTOUT, USART1_CTS, TIMER15_CH0, TIMER2_CH0, I2C0_SCL Additional: RTC_REFIN

GD32C231Kx QFN32				
Pin Name	**Pins**	**Pin Type[(1)]**	**I/O Level[(2)]**	**Functions description**
PB8	32	I/O	5VT	Default: PB8 Alternate: SPI1_SCK, USART1_CTS, TIMER15_CH0, TIMER2_CH0, I2C0_SCL, EVENTOUT

Note:

(1) Type: I = input, O = output, A = analog, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Refer to the description of the NRST_MDSEL[1:0] field in FMC_OBCTL register of GD32C2x1_User_Manual to configure the PF2-NRST pin as a PF2 general GPIO function.

2.6.5. GD32C231Gx QFN28 pin definitions

Table 2-9. GD32C231Gx QFN28 pin definitions

GD32C231Gx QFN28				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PC14-OSCXIN	1	I/O		Default: PC14 Alternate: USART0_TX, TIMER0_ETI, TIMER0_BRKIN1, USART1_RTS_DE_CK, TIMER16_CH0, TIMER2_CH1, EVENTOUT Additional: OSC32IN, OSCIN
PC15-OSCXOUT	2	I/O		Default: PC15 Alternate: OSC32EN, OSCEN, TIMER0_ETI, TIMER2_CH2 Additional: OSC32OUT, OSCOUT
VDD/VDDA/VREFP	3	P	-	Default: VDD/VDDA/VREFP
VSS/VSSA/VREFN	4	P	-	Default: VSS/VSSA/VREFN
PF2-NRST	5	I/O		Default: NRST Alternate: CK_OUT0, TIMER0_CH3 Additional: PF2(3)
PA0	6	I/O		Default: PA0 Alternate: SPI1_SCK, USART1_CTS, TIMER15_CH0, USART0_TX, TIMER0_CH0, CMP0_OUT Additional: ADC_IN0, WKUP0, CMP0_IM5
PA1	7	I/O	5VT	Default: PA1 Alternate: SPI0_SCK, I2S0_CK, USART1_RTS_DE_CK, TIMER16_CH0, SPI1_IO2, USART0_RX, TIMER0_CH1, I2C0_SMBA, EVENTOUT Additional: ADC_IN1，CMP0_IP
PA2	8	I/O		Default: PA2 Alternate: SPI0_MOSI, I2S0_SD, USART1_TX, TIMER15_CH0_ON, TIMER2_ETI, SPI1_IO3, TIMER0_CH2, CMP1_OUT Additional: ADC_IN2, WKUP3, LSCK_OUT, CMP1_IM5
PA3	9	I/O		Default: PA3 Alternate: SPI1_MISO, USART1_RX, TIMER0_CH0_ON, TIMER0_CH3, EVENTOUT Additional: ADC_IN3, CMP1_IP
PA4	10	I/O		Default: PA4 Alternate: SPI0_NSS, I2S0_WS, USART1_TX, TIMER0_CH1_ON, SPI1_MOSI, TIMER13_CH0, TIMER16_CH0_ON, EVENTOUT Additional: ADC_IN4, RTC_OUT1， RTC_TS, RTC_OUT0, WKUP1
PA5	11	I/O		Default: PA5

GD32C231Gx QFN28				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: SPI0_SCK, I2S0_CK, USART1_RX, TIMER0_CH2_ON, SPI1_IO2, TIMER0_CH0, EVENTOUT Additional: ADC_IN5
PA6	12	I/O		Default: PA6 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, TIMER0_BRKIN0, SPI1_IO3, TIMER15_CH0, CMP0_OUT Additional: ADC_IN6
PA7	13	I/O		Default: PA7 Alternate: SPI0_MOSI, I2S0_SD, TIMER2_CH1, TIMER0_CH0_ON, TIMER13_CH0, TIMER16_CH0, CMP1_OUT Additional: ADC_IN7
PB0	14	I/O		Default: PB0 Alternate: SPI0_NSS, I2S0_WS, TIMER2_CH2, TIMER0_CH1_ON, CMP0_OUT Additional: ADC_IN8
PB1	15	I/O		Default: PB1 Alternate: TIMER13_CH0, TIMER2_CH3, TIMER0_CH2_ON, TIMER0_CH1_ON, EVENTOUT Additional: ADC_IN9, CMP0_IM6
PA8	16	I/O		Default: PA8 Alternate: CK_OUT0, USART1_TX, TIMER0_CH0, SPI1_NSS, EVENTOUT, SPI0_NSS, I2S0_WS, TIMER0_CH1_ON, TIMER0_CH2_ON, TIMER2_CH2, TIMER2_CH3, TIMER13_CH0, USART0_RX, CK_OUT1
PC6	17	I/O		Default: PC6 Alternate: TIMER2_CH0
PA11[PA9](4)	18	I/O	5VT	Default: PA11 Alternate: SPI0_MISO, I2S0_MCK, USART0_CTS, TIMER0_CH3, SPI1_IO2, TIMER0_BRKIN1, I2C1_SCL, CMP0_OUT
				Default: PA9 Alternate: CK_OUT0, USART0_TX, TIMER0_CH1, TIMER2_ETI, SPI1_MISO, I2C0_SCL, EVENTOUT
PA12[PA10](4)	19	I/O	5VT	Default: PA12 Alternate: SPI0_MOSI, I2S0_SD, USART0_RTS_DE_CK, TIMER0_ETI, SPI1_IO3, I2S_CKIN, I2C1_SDA, CMP1_OUT Additional: ADC_IN12
				Default: PA10 Alternate: SPI1_MOSI, USART0_RX, TIMER0_CH2, CK_OUT1, TIMER16_BRKIN0, I2C0_SDA, EVENTOUT
PA13	20	I/O		Default: PA13, SWDIO

GD32C231Gx QFN28				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: SWDIO, TIMER2_ETI, USART1_RX, EVENTOUT
PA14-BOOT0	21	I/O		Default: PA14, SWCLK Alternate: SWCLK, USART1_TX, EVENTOUT, SPI0_NSS, I2S0_WS, USART1_RX, TIMER0_CH0, CK_OUT1, USART0_RTS_DE_CK Additional: BOOT0
PA15	22	I/O		Default: PA15 Alternate: SPI0_NSS, I2S0_WS, USART1_RX, TIMER0_CH0, CK_OUT1, USART0_RTS_DE_CK, EVENTOUT
PB3	23	I/O		Default: PB3 Alternate: SPI0_SCK, I2S0_CK, TIMER0_CH1, TIMER2_CH1, EVENTOUT Additional: CMP1_IM6
PB4	24	I/O		Default: PB4 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, USART0_CTS, TIMER16_BRKIN0, EVENTOUT Additional: CMP1_IM7
PB5	25	I/O	5VT	Default: PB5 Alternate: SPI0_MOSI, I2S0_SD, TIMER2_CH1, TIMER15_BRKIN0, TIMER2_CH2, SPI1_MISO, I2C0_SMBA, CMP1_OUT Additional: WKUP5
PB6	26	I/O	5VT	Default: PB6 Alternate: USART0_TX, TIMER0_CH2, TIMER15_CH0_ON, TIMER2_CH2, USART0_RTS_DE_CK, USART0_CTS, I2C0_SCL, I2C0_SMBA, SPI0_MOSI, I2S0_SD, SPI0_MISO, I2S0_MCK, SPI0_SCK, I2S0_CK, TIMER0_CH1, TIMER2_CH0, TIMER2_CH1, TIMER15_BRKIN0, TIMER16_BRKIN0 Additional: WKUP2, CMP1_IM4
PB7	27	I/O	5VT	Default: PB7 Alternate: USART0_RX, TIMER0_CH3, TIMER16_CH0_ON, TIMER2_CH3, SPI1_MOSI, I2C0_SDA, EVENTOUT, USART1_CTS, TIMER15_CH0, TIMER2_CH0, I2C0_SCL Additional: RTC_REFIN
PB8	28	I/O	5VT	Default: PB8 Alternate: SPI1_SCK, USART1_CTS, TIMER15_CH0, TIMER2_CH0, I2C0_SCL, EVENTOUT

Note:

(1) Type: I = input, O = output, A = analog, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Refer to the description of the NRST_MDSEL[1:0] field in FMC_OBCTL register of GD32C2x1_User_Manual to configure the PF2-NRST pin as a PF2 general GPIO

function.

(4) Refer to the description of the PA12_RMP or PA11_RMP field in SYSCFG_CFG0 register of GD32C2x1_User_Manual.

2.6.6. GD32C231Fx TSSOP20 pin definitions

Table 2-10. GD32C231Fx TSSOP20 pin definitions

GD32C231Fx TSSOP20				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PB7	1	I/O	5VT	Default: PB7 Alternate: USART0_RX, TIMER0_CH3, TIMER16_CH0_ON, TIMER2_CH3, SPI1_MOSI, I2C0_SDA, EVENTOUT, USART1_CTS, TIMER15_CH0, TIMER2_CH0, I2C0_SCL Additional: RTC_REFIN
PC14-OSCXIN	2	I/O		Default: PC14 Alternate: USART0_TX, TIMER0_ETI, TIMER0_BRKIN1, USART1_RTS_DE_CK, TIMER16_CH0, TIMER2_CH1, EVENTOUT Additional: OSC32IN, OSCIN
PC15-OSCXOUT	3	I/O		Default: PC15 Alternate: OSC32EN, OSCEN, TIMER0_ETI, TIMER2_CH2 Additional: OSC32OUT, OSCOUT
VDD/VDDA/VREFP	4	P	-	Default: VDD/VDDA/VREFP
VSS/VSSA/VREFN	5	P	-	Default: VSS/VSSA/VREFN
PF2-NRST	6	I/O		Default: NRST Alternate: CK_OUT0, TIMER0_CH3 Additional: PF2(3)
PA0	7	I/O		Default: PA0 Alternate: SPI1_SCK, USART1_CTS, TIMER15_CH0, USART0_TX, TIMER0_CH0, CMP0_OUT Additional: ADC_IN0, WKUP0, CMP0_IM5
PA1	8	I/O	5VT	Default: PA1 Alternate: SPI0_SCK, I2S0_CK, USART1_RTS_DE_CK, TIMER16_CH0, SPI1_IO2, USART0_RX, TIMER0_CH1, I2C0_SMBA, EVENTOUT Additional: ADC_IN1，CMP0_IP
PA2	9	I/O		Default: PA2 Alternate: SPI0_MOSI, I2S0_SD, USART1_TX, TIMER15_CH0_ON, TIMER2_ETI, SPI1_IO3, TIMER0_CH2, CMP1_OUT Additional: ADC_IN2, WKUP3, LSCK_OUT, CMP1_IM5
PA3	10	I/O		Default: PA3 Alternate: SPI1_MISO, USART1_RX, TIMER0_CH0_ON, TIMER0_CH3, EVENTOUT Additional: ADC_IN3, CMP1_IP
PA4	11	I/O		Default: PA4

GD32C231Fx TSSOP20				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: SPI0_NSS, I2S0_WS, USART1_TX, TIMER0_CH1_ON, SPI1_MOSI, TIMER13_CH0, TIMER16_CH0_ON, EVENTOUT Additional: ADC_IN4, RTC_OUT1, RTC_TS, RTC_OUT0, WKUP1
PA5	12	I/O		Default: PA5 Alternate: SPI0_SCK, I2S0_CK, USART1_RX, TIMER0_CH2_ON, SPI1_IO2, TIMER0_CH0, EVENTOUT Additional: ADC_IN5
PA6	13	I/O		Default: PA6 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, TIMER0_BRKIN0, SPI1_IO3, TIMER15_CH0, CMP0_OUT Additional: ADC_IN6
PA7	14	I/O		Default: PA7 Alternate: SPI0_MOSI, I2S0_SD, TIMER2_CH1, TIMER0_CH0_ON, TIMER13_CH0, TIMER16_CH0, CMP1_OUT Additional: ADC_IN7
PA8	15	I/O		Default: PA8 Alternate: CK_OUT0, USART1_TX, TIMER0_CH0, SPI1_NSS, EVENTOUT, SPI0_NSS, I2S0_WS, TIMER0_CH1_ON, TIMER0_CH2_ON, TIMER2_CH2, TIMER2_CH3, TIMER13_CH0, USART0_RX, CK_OUT1
PA11[PA9](4)	16	I/O	5VT	Default: PA11 Alternate: SPI0_MISO, I2S0_MCK, USART0_CTS, TIMER0_CH3, SPI1_IO2, TIMER0_BRKIN1, I2C1_SCL, CMP0_OUT
				Default: PA9 Alternate: CK_OUT0, USART0_TX, TIMER0_CH1, TIMER2_ETI, SPI1_MISO, I2C0_SCL, EVENTOUT
PA12[PA10](4)	17	I/O		Default: PA12 Alternate: SPI0_MOSI, I2S0_SD, USART0_RTS_DE_CK, TIMER0_ETI, SPI1_IO3, I2S_CKIN, I2C1_SDA, CMP1_OUT Additional: ADC_IN12
				Default: PA10 Alternate: SPI1_MOSI, USART0_RX, TIMER0_CH2, CK_OUT1, TIMER16_BRKIN0, I2C0_SDA, EVENTOUT
PA13	18	I/O		Default: PA13, SWDIO Alternate: SWDIO, TIMER2_ETI, USART1_RX, EVENTOUT
PA14-BOOT0	19	I/O		Default: PA14, SWCLK

GD32C231Fx TSSOP20				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: SWCLK, USART1_TX, EVENTOUT, SPI0_NSS, I2S0_WS, USART1_RX, TIMER0_CH0, CK_OUT1, USART0_RTS_DE_CK Additional: BOOT0
PB6	20	I/O	5VT	Default: PB6 Alternate: USART0_TX, TIMER0_CH2, TIMER15_CH0_ON, TIMER2_CH2, USART0_RTS_DE_CK, USART0_CTS, I2C0_SCL, I2C0_SMBA, SPI0_MOSI, I2S0_SD, SPI0_MISO, I2S0_MCK, SPI0_SCK, I2S0_CK, TIMER0_CH1, TIMER2_CH0, TIMER2_CH1, TIMER15_BRKIN0, TIMER16_BRKIN0 Additional: WKUP2, CMP1_IM4

Note:

(1) Type: I = input, O = output, A = analog, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Refer to the description of the NRST_MDSEL[1:0] field in FMC_OBCTL register of GD32C2x1_User_Manual to configure the PF2-NRST pin as a PF2 general GPIO function.

(4) Refer to the description of the PA12_RMP or PA11_RMP field in SYSCFG_CFG0 register of GD32C2x1_User_Manual.

2.6.7. GD32C231Fx LGA20 pin definitions

Table 2-11. GD32C231Fx LGA20 pin definitions

GD32C231Fx LGA20				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PB7	1	I/O	5VT	Default: PB7 Alternate: USART0_RX, TIMER0_CH3, TIMER16_CH0_ON, TIMER2_CH3, SPI1_MOSI, I2C0_SDA, EVENTOUT, USART1_CTS, TIMER15_CH0, TIMER2_CH0, I2C0_SCL Additional: RTC_REFIN
PC14-OSCXIN	2	I/O		Default: PC14 Alternate: USART0_TX, TIMER0_ETI, TIMER0_BRKIN1, USART1_RTS_DE_CK, TIMER16_CH0, TIMER2_CH1, EVENTOUT Additional: OSC32IN, OSCIN
PC15-OSCXOUT	3	I/O		Default: PC15 Alternate: OSC32EN, OSCEN, TIMER0_ETI, TIMER2_CH2 Additional: OSC32OUT, OSCOUT
VDD/VDDA/VREFP	4	P	-	Default: VDD/VDDA/VREFP
VSS/VSSA/VREFN	5	P	-	Default: VSS/VSSA/VREFN
PF2-NRST	6	I/O		Default: NRST Alternate: CK_OUT0, TIMER0_CH3 Additional: PF2[3]
PA0	7	I/O		Default: PA0 Alternate: SPI1_SCK, USART1_CTS, TIMER15_CH0, USART0_TX, TIMER0_CH0, CMP0_OUT Additional: ADC_IN0, WKUP0, CMP0_IM5
PA1	8	I/O	5VT	Default: PA1 Alternate: SPI0_SCK, I2S0_CK, USART1_RTS_DE_CK, TIMER16_CH0, SPI1_IO2, USART0_RX, TIMER0_CH1, I2C0_SMBA, EVENTOUT Additional: ADC_IN1，CMP0_IP
PA2	9	I/O		Default: PA2 Alternate: SPI0_MOSI, I2S0_SD, USART1_TX, TIMER15_CH0_ON, TIMER2_ETI, SPI1_IO3, TIMER0_CH2, CMP1_OUT Additional: ADC_IN2, WKUP3, LSCK_OUT, CMP1_IM5
PA3	10	I/O		Default: PA3 Alternate: SPI1_MISO, USART1_RX, TIMER0_CH0_ON, TIMER0_CH3, EVENTOUT Additional: ADC_IN3, CMP1_IP
PA4	11	I/O		Default: PA4

GD32C231Fx LGA20				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: SPI0_NSS, I2S0_WS, USART1_TX, TIMER0_CH1_ON, SPI1_MOSI, TIMER13_CH0, TIMER16_CH0_ON, EVENTOUT Additional: ADC_IN4, RTC_OUT1， RTC_TS, RTC_OUT0, WKUP1
PA5	12	I/O		Default: PA5 Alternate: SPI0_SCK, I2S0_CK, USART1_RX, TIMER0_CH2_ON, SPI1_IO2, TIMER0_CH0, EVENTOUT Additional: ADC_IN5
PA6	13	I/O		Default: PA6 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, TIMER0_BRKIN0, SPI1_IO3, TIMER15_CH0, CMP0_OUT Additional: ADC_IN6
PA7	14	I/O		Default: PA7 Alternate: SPI0_MOSI, I2S0_SD, TIMER2_CH1, TIMER0_CH0_ON, TIMER13_CH0, TIMER16_CH0, CMP1_OUT Additional: ADC_IN7
PA8	15	I/O		Default: PA8 Alternate: CK_OUT0, USART1_TX, TIMER0_CH0, SPI1_NSS, EVENTOUT, SPI0_NSS, I2S0_WS, TIMER0_CH1_ON, TIMER0_CH2_ON, TIMER2_CH2, TIMER2_CH3, TIMER13_CH0, USART0_RX, CK_OUT1
PA11[PA9](4)	16	I/O	5VT	Default: PA11 Alternate: SPI0_MISO, I2S0_MCK, USART0_CTS, TIMER0_CH3, SPI1_IO2, TIMER0_BRKIN1, I2C1_SCL, CMP0_OUT
				Default: PA9 Alternate: CK_OUT0, USART0_TX, TIMER0_CH1, TIMER2_ETI, SPI1_MISO, I2C0_SCL, EVENTOUT
PA12[PA10](4)	17	I/O		Default: PA12 Alternate: SPI0_MOSI, I2S0_SD, USART0_RTS_DE_CK, TIMER0_ETI, SPI1_IO3, I2S_CKIN, I2C1_SDA, CMP1_OUT Additional: ADC_IN12
				Default: PA10 Alternate: SPI1_MOSI, USART0_RX, TIMER0_CH2, CK_OUT1, TIMER16_BRKIN0, I2C0_SDA, EVENTOUT
PA13	18	I/O		Default: PA13, SWDIO Alternate: SWDIO, TIMER2_ETI, USART1_RX, EVENTOUT
PA14-BOOT0	19	I/O		Default: PA14, SWCLK

GD32C231Fx LGA20				
Pin Name	**Pins**	**Pin Type[1]**	**I/O Level[2]**	**Functions description**
				Alternate: SWCLK, USART1_TX, EVENTOUT, SPI0_NSS, I2S0_WS, USART1_RX, TIMER0_CH0, CK_OUT1, USART0_RTS_DE_CK Additional: BOOT0
PB6	20	I/O	5VT	Default: PB6 Alternate: USART0_TX, TIMER0_CH2, TIMER15_CH0_ON, TIMER2_CH2, USART0_RTS_DE_CK, USART0_CTS, I2C0_SCL, I2C0_SMBA, SPI0_MOSI, I2S0_SD, SPI0_MISO, I2S0_MCK, SPI0_SCK, I2S0_CK, TIMER0_CH1, TIMER2_CH0, TIMER2_CH1, TIMER15_BRKIN0, TIMER16_BRKIN0 Additional: WKUP2, CMP1_IM4

Note:

(1) Type: I = input, O = output, A = analog, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Refer to the description of the NRST_MDSEL[1:0] field in FMC_OBCTL register of GD32C2x1_User_Manual to configure the PF2-NRST pin as a PF2 general GPIO function.

(4) Refer to the description of the PA12_RMP or PA11_RMP field in SYSCFG_CFG0 register of GD32C2x1_User_Manual.

2.6.8. GD32C231xx pin alternate functions

Table 2-12. Port A alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0	SPI1_SCK	USART1_CTS	TIMER15_CH0		USART0_TX	TIMER0_CH0		CMP0_OUT								
PA1	SPI0_SCK/I2S0_CK	USART1_RTS_DE_CK	TIMER16_CH0	SPI1_IO2	USART0_RX	TIMER0_CH1	I2C0_SMBA	EVENTOUT								
PA2	SPI0_MOSI/I2S0_SD	USART1_TX	TIMER15_CH0_ON	TIMER2_ETI	SPI1_IO3	TIMER0_CH2	USART2_TX	CMP1_OUT								
PA3	SPI1_MISO	USART1_RX	TIMER0_CH0_ON			TIMER0_CH3	USART2_RX	EVENTOUT								
PA4	SPI0_NSS/I2S0_WS	USART1_TX	TIMER0_CH1_ON	SPI1_MOSI	TIMER13_CH0	TIMER16_CH0_ON		EVENTOUT								
PA5	SPI0_SCK/I2S0_CK	USART1_RX	TIMER0_CH2_ON	SPI1_IO2		TIMER0_CH0		EVENTOUT								
PA6	SPI0_MISO/I2S0_MCK	TIMER2_CH0	TIMER0_BRKIN0	SPI1_IO3		TIMER15_CH0	USART2_CTS	CMP0_OUT								
PA7	SPI0_MOSI/I2S0_SD	TIMER2_CH1	TIMER0_CH0_ON		TIMER13_CH0	TIMER16_CH0	USART2_RTS_DE_CK	CMP1_OUT								
PA8	CK_OUT0	USART1_TX	TIMER0_CH0	SPI1_NSS				EVENTOUT	SPI0_NSS/I2S0_WS	TIMER0_CH1_ON	TIMER0_CH2_ON	TIMER2_CH2	TIMER2_CH3	TIMER13_CH0	USART0_RX	CK_OUT1
PA9	CK_OUT0	USART0_TX	TIMER0_CH1	TIMER2_ETI	SPI1_MISO		I2C0_SCL	EVENTOUT								
PA10	SPI1_MOSI	USART0_RX	TIMER0_CH2	CK_OUT1		TIMER16_BRKIN0	I2C0_SDA	EVENTOUT								
PA11	SPI0_MISO/I2S0_MCK	USART0_CTS	TIMER0_CH3	SPI1_IO2		TIMER0_BRKIN1	I2C1_SCL	CMP0_OUT								
PA12	SPI0_MOSI/I2S0_SD	USART0_RTS_DE_CK	TIMER0_ETI	SPI1_IO3		I2S_CKIN	I2C1_SDA	CMP1_OUT								
PA13	SWDIO			TIMER2_ETI	USART1_RX			EVENTOUT								
PA14	SWCLK	USART1_TX						EVENTOUT	SPI0_NSS/I2S0_WS	USART1_RX	TIMER0_CH0	CK_OUT1	USART0_RTS_DE_CK			

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA15	SPI0_NSS/I2S0_WS	USART1_RX	TIMER0_CH0	CK_OUT1	USART0_RTS_DE_CK			EVENTOUT								

Table 2-13. Port B alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB0	SPI0_NSS/I2S0_WS	TIMER2_CH2	TIMER0_CH1_ON					CMP0_OUT								
PB1	TIMER13_CH0	TIMER2_CH3	TIMER0_CH2_ON			TIMER0_CH1_ON	USART2_RTS_DE_CK	EVENTOUT								
PB2	USART0_RX	SPI1_MISO		CK_OUT1				EVENTOUT								
PB3	SPI0_SCK/I2S0_CK	TIMER0_CH1		TIMER2_CH1	USART0_RTS_DE_CK			EVENTOUT								
PB4	SPI0_MISO/I2S0_MCK	TIMER2_CH0			USART0_CTS	TIMER16_BRKIN0		EVENTOUT								
PB5	SPI0_MOSI/I2S0_SD	TIMER2_CH1	TIMER15_BRKIN0	TIMER2_CH2	SPI1_MISO		I2C0_SMBA	CMP1_OUT								
PB6	USART0_TX	TIMER0_CH2	TIMER15_CH0_ON	TIMER2_CH2	USART0_RTS_DE_CK	USART0_CTS	I2C0_SCL	I2C0_SMBA	SPI0_MOSI/I2S0_SD	SPI0_MISO/I2S0_MCK	SPI0_SCK/I2S0_CK	TIMER0_CH1	TIMER2_CH0	TIMER2_CH1	TIMER15_BRKIN0	TIMER16_BRKIN0
PB7	USART0_RX	TIMER0_CH3	TIMER16_CH0_ON	TIMER2_CH3	SPI1_MOSI		I2C0_SDA	EVENTOUT		USART1_CTS	TIMER15_CH0	TIMER2_CH0			I2C0_SCL	
PB8	SPI1_SCK	USART1_CTS	TIMER15_CH0	TIMER2_CH0			I2C0_SCL	EVENTOUT								
PB9		USART1_RTS_DE_CK	TIMER16_CH0	TIMER2_CH1		SPI1_NSS	I2C0_SDA	EVENTOUT								
PB10		USART2_RX				SPI1_SCK	I2C1_SCL	CMP0_OUT								
PB11	SPI1_MOSI	USART2_TX					I2C1_SDA	CMP1_OUT								
PB12	SPI1_NSS	TIMER0_BRKIN1	TIMER0_BRKIN0	USART2_RTS_DE_CK				EVENTOUT								
PB13	SPI1_SCK	USART2_CTS	TIMER0_CH0_ON					EVENTOUT								

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB14	SPI1_MISO		TIMER0_CH1_ON					EVENTOUT								
PB15	SPI1_MOSI		TIMER0_CH2_ON					EVENTOUT								

Table 2-14. Port C alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC6		TIMER2_CH0														
PC7		TIMER2_CH1														
PC13		TIMER0_ETI	TIMER0_BRKIN0													
PC14	USART0_TX	TIMER0_ETI	TIMER0_BRKIN1							USART1_RTS_DE_CK	TIMER16_CH0	TIMER2_CH1				EVENTOUT
PC15	OSC32EN	OSCEN	TIMER0_ETI	TIMER2_CH2												

Table 2-15. Port D alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PD0	EVENTOUT	SPI1_NSS	TIMER15_CH0													
PD1	EVENTOUT	SPI1_SCK	TIMER16_CH0													
PD2		TIMER2_ETI	TIMER0_CH0_ON													
PD3	USART1_CTS	SPI1_MISO	TIMER0_CH1_ON													

Table 2-16. Port F alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PF0			TIMER13_CH0													
PF1	OSCEN															
PF2	CK_OUT0	TIMER0_CH3														
PF3																

3. Functional description

3.1. Arm® Cortex®-M23 core

The Cortex-M23 processor is an energy-efficient processor with a very low gate count. It is intended to be used for microcontroller and deeply embedded applications that require an area-optimized processor. The processor is highly configurable enabling a wide range of implementations from those requiring memory protection and powerful trace technology to cost sensitive devices requiring minimal area, while delivering outstanding computational performance and an advanced system response to interrupts.

32-bit Arm® Cortex®-M23 processor core

- Up to 48 MHz operation frequency.
- Single-cycle multiplication and 17-cycle hardware divider.
- Ultra-low power, energy-efficient operation.
- Excellent code density.
- Integrated Nested Vectored Interrupt Controller (NVIC).
- 24-bit SysTick timer.

The Cortex®-M23 processor is based on the ARMv8-M architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M23:

- Internal Bus Matrix connected with AHB master, Serial Wire Debug Port and Single-cycle IO port.
- Nested Vectored Interrupt Controller (NVIC).
- Breakpoint Unit(BPU).
- Data Watchpoint and Trace (DWT).
- Serial Wire Debug Port.

3.2. Embedded memory

- Up to 64 Kbytes of Flash memory.
- Up to 12 Kbytes of SRAM with ECC.
- Support Flash ECC

64 Kbytes of inner Flash memory, and 12 Kbytes of inner SRAM at most is available for storing programs and data, and Flash is accessed (read) at CPU clock speed with 0~1 wait states. ***Table 2-4. GD32C231xx memory map*** shows the memory map of the GD32C231xx series of devices, including code, SRAM, peripheral, and other pre-defined regions.

3.3. Clock, reset and supply management

- External 4 to 48 MHz crystal oscillator.
- Internal 48 / 12MHz factory-trimmed RC.
- Internal 32 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator.
- 1.8 to 5.5 V application supply and I/Os.
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset).

The Clock Control Unit (CCTL) provides a range of oscillator and clock functions. These include speed internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and APB domains. The maximum frequency of the AHB, APB domains is 48 MHz/48 MHz. See ***Figure 2-9. GD32C231xx clock tree*** for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from 1.633 V and down to 1.593V. The device remains in reset mode when V_{DD} is below a specified threshold.

Power supply schemes:

- V_{DD}/V_{DDA} range: 1.8 to 5.5 V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD}/V_{DDA} pins, external analog power supplies for ADC, reset blocks, RCs.
- V_{SS} is 0 V.

3.4. Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main Flash memory (default).
- Boot from system memory.
- Boot from on-chip SRAM.

In default condition, boot from main Flash memory is selected. The boot loader is located in the internal boot ROM memory (system memory). It is used to reprogram the Flash memory by using USART0 (PA9/PA10 and PA11/PA12) or USART1 (PA2 and PA3) or I2C0 (PB6 and PB7).

Note: When booting from system memory, the USART RX pins (PA10/PA12, PA3) are in input level detection mode. Therefore, unused USART RX pins (PA10/PA12, PA3) need to be kept at a stable logic level to prevent false triggering.

3.5. Power saving modes

The MCU supports six kinds of power saving modes to achieve even lower power consumption. They are Run1, Sleep, Sleep1, Deep-sleep, Deep-sleep 1, and Standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Run1 mode**

  When in Run1 mode, the NPLDO is off and LPLDO is on, the system clock source should be IRC32K.

- **Sleep mode**

  The Sleep mode is corresponding to the SLEEPING mode of the Cortex®-M23. In Sleep mode, only clock of Cortex®-M23 is off. To enter the Sleep mode, it is only necessary to clear the SLEEPDEEP bit in the Cortex®-M23 System Control Register, and execute a WFI or WFE instruction. If the Sleep mode is entered by executing a WFI instruction, any interrupt can wake up the system. If it is entered by executing a WFE instruction, any wakeup event can wake up the system (If SEVONPEND is 1, any interrupt can wake up the system, refer to Cortex®-M23 Technical Reference Manual). The mode offers the lowest wakeup time as no time is wasted in interrupt entry or exit.

- **Sleep1 mode**

  The Sleep1 mode is corresponding to the SLEEPING mode of the Cortex®-M23 When in Run1 mode. In this mode the NPLDO is off and LPLDO is on, the system clock source is IRC32K.

- **Deep-sleep mode**

  The Deep-sleep mode is based on the SLEEPDEEP mode of the Cortex®-M23. In Deep-sleep mode, all clocks in the V_{CORE_RUN} domain are off, and all of HIRC, HXTAL are disabled. The contents of SRAM and registers are preserved. The NPLDO is on. Before entering the Deep-sleep mode, it is necessary to set the SLEEPDEEP bit in the Cortex®-M23 System Control Register, and set LPMOD bits to “00” in the PMU_CTL0 register. Then, the device enters the Deep-sleep mode after a WFI or WFE instruction is executed. If the Deep-sleep mode is entered by executing a WFI instruction, any interrupt from EXTI lines can wake up the system. If it is entered by executing a WFE instruction, any wakeup event from EXTI lines can wake up the system (If SEVONPEND is 1, any interrupt from EXTI lines can wake up the system, refer to Cortex®-M23 Technical Reference Manual). When exiting the Deep-sleep mode, theHIRC is selected as the system clock.

- **Deep-sleep 1 mode**

  The Deep-sleep1 mode is based on the SLEEPDEEP mode of the Cortex®-M23. In Deep-sleep1 mode, all clocks in the V_{CORE_RUN} domain are off, and all of HIRC, HXTAL are disabled. The contents of SRAM and registers are preserved. The NPLDO is off and LPLDO is on. Before entering the Deep-sleep1 mode, it is necessary to set the SLEEPDEEP bit in the Cortex®-M23 System Control Register, and set LPMOD bits to “01” in the PMU_CTL0 register. Then, the device enters the Deep-sleep1 mode after a WFI or WFE instruction is executed. If the Deep-sleep1 mode is entered by executing a WFI instruction, any interrupt from EXTI lines can wake up the system. If it is entered by executing a WFE instruction, any wakeup event from EXTI lines can wake up the system (If SEVONPEND is 1, any interrupt from EXTI lines can wake up the system, refer to Cortex®-M23 Technical Reference Manual). When exiting the Deep-sleep1 mode, the

HIRC is selected as the system clock.

- **Standby mode**

  The Standby mode is based on the SLEEPDEEP mode of the Cortex®-M23. In Standby mode, the whole V_{CORE_RUN} domain is power off, the NPLDO is shut down, and all of HIRC, HXTAL are disabled. Before entering the Standby mode, it is necessary to set the LPMOD bits to “11” in the PMU_CTL0 register, and clear WUF bit in the PMU_CS register, and set the SLEEPDEEP bit in the Cortex®-M23 System Control Register. Then, the device enters the Standby mode after a WFI or WFE instruction is executed, and the STBF status flag in the PMU_CS register indicates that the MCU has been in Standby mode. There are four wakeup sources for the Standby mode, including the external reset from NRST pin, the RTC alarm, the FWDGT reset, LXTAL clock failure detedtion and the rising edge on WKUPx pins. The Standby mode achieves the lowest power consumption, but spends longest time to wake up. Besides, the contents of SRAM and registers in V_{CORE_RUN} power domain are lost in Standby mode. When exiting from the Standby mode, a power-on reset occurs and the Cortex®-M23 will execute instruction code from the 0x00000000 address.

3.6. General-purpose inputs/outputs (GPIOs)

- Up to 45 fast GPIOs, all mappable on 16 external interrupt lines.
- Analog input/output configurable.
- Alternate function input/output configurable.

There are up to 45 general purpose I/O pins (GPIO) in GD32C231xx, named PA0 ~ PA15, PB0 ~ PB15, PC6, PC7, PC13~PC15, PD0~PD3, PF0~ PF3 to implement logic input/output functions. Each GPIO port has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt/Event Controller Unit (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins.

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), input, peripheral alternate function or analog mode. Most of the GPIO pins are shared with digital or analog alternate functions.

3.7. CRC calculation unit (CRC)

- Supports 7/8/16/32 bit data input.
- For 7(8)/16/32 bit input data length, the calculation cycles are 1/2/4 AHB clock cycles.
- Free 8-bit register is unrelated to calculation and can be used for any other goals by any other peripheral devices.
- User configurable polynomial value and size.

A cyclic redundancy check (CRC) is an error-detecting code commonly used in digital networks and storage devices to detect accidental changes to raw data. This CRC calculation unit can be used to calculate 7/8/16/32 bit CRC code within user configurable polynomial.

3.8. Direct memory access controller (DMA)

- 3 channels for DMA controller.
- DMA request from DMAMUX: peripherals (Timers, ADC, SPIs, I2Cs and USARTs) and request generator.

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby increasing system performance by off-loading the MCU from copying large amounts of data and avoiding frequent interrupts to serve peripherals needing more data or having available data. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory.

Each channel is connected to flexible hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

3.9. DMA request multiplexer (DMAMUX)

- 3 channels for DMAMUX request multiplexer.
- 4 channels for DMAMUX request generator.
- Support 24 trigger inputs and 24 synchronization inputs.

DMAMUX is a transmission scheduler for DMA requests. The DMAMUX request multiplexer is used for routing a DMA request line between the peripherals / generated DMA request (from the DMAMUX request generator) and the DMA controller. Each DMAMUX request multiplexer channel selects a unique DMA request line, unconditionally or synchronously with events from its DMAMUX synchronization inputs. The DMA request is pending until it is served by the DMA controller which generates a DMA acknowledge signal (the DMA request signal is de-asserted).

3.10. Analog to digital converter (ADC)

- 12-bit SAR ADC's conversion rate is up to 1.60 MSPS.
- Hardware oversampling ratio adjustable from 2x to 256x improves resolution to 16-bit.
- Input voltage range: V_{REFN} to V_{REFP}.
- Temperature sensor.

A 12-bit multi-channel ADC is integrated in the device. It has a total of 16 multiplexed channels: up to 13 external channels, 1 channel for internal temperature sensor (V_{SENSE}), 1 channel for internal reference voltage (V_{REFINT}) and 1 channel for positive reference voltage (V_{REFP}). An on-chip hardware oversampling scheme improves performance while off-loading the related computational burden from the CPU. The analog watchdog allows the application to detect whether the input voltage goes outside the user-defined higher or lower thresholds. A configurable channel management block can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced use.

The ADC can be triggered from the events generated by the general level 0 timer (TIMER2) and the advanced timers (TIMER0) with internal connection. The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally connected to the ADC_IN13 input channel which is used to convert the sensor output voltage in a digital value.

To ensure a high accuracy on ADC, the independent power supply V_{DDA} is implemented to achieve better performance of analog circuits. V_{DDA} can be externally connected to V_{DD} through the external filtering circuit that avoids noise on V_{DDA}. According to the different packages, VREFP pin can be connected to VDDA pin, or external reference voltage. For packages without VREFP and VREFN pins, V_{REFP} is internally connected to V_{DDA}, and V_{REFN} is internally connected to V_{SSA}.

3.11. Real time clock (RTC)

- Independent binary-coded decimal (BCD) format timer/counter with four 32-bit backup registers.
- Calendar with sub-second, second, minute, hour, week day, day, month and year automatically correction.
- Alarm function with wake up from deep-sleep and standby mode capability.
- On-the-fly correction for synchronization with master clock. Digital calibration with 0.95 ppm resolution for compensation of quartz crystal inaccuracy.

The real time clock is an independent timer which provides a set of continuously running counters in backup registers to provide a real calendar function, and provides an alarm interrupt or an expected interrupt. It is not reset by a system or power reset, or when the device wakes up from standby mode. In the RTC unit, there are two prescalers used for implementing the calendar and other functions. One prescaler is a 7-bit asynchronous prescaler and the other is a 15-bit synchronous prescaler.

3.12. Timers and PWM generation

- Up to four 16-bit general timers (TIMER2 TIMER13, TIMER15, TIMER16), and one 16-bit advanced timer (TIMER0).
- Up to 4 independent channels of PWM, output compare or input capture for each general timer and external trigger input.
- Encoder interface controller with two inputs using quadrature decoder.
- 24-bit SysTick timers down counter.
- 2 watchdog timers (free watchdog timer and window watchdog timer).

The advanced timer (TIMER0) can be used as a three-phase PWM multiplexed on 4 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general timer. The 4 independent channels can be used for input capture, output compare, PWM generation (edge-aligned or center-aligned counting modes) and single pulse mode output. If configured as a general 16-bit timer, it has the same functions as the TIMERx timer. It can be synchronized with external signals or to interconnect with other general timers together which have the same architecture and features.

The general timer can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TIMER2 is based on a 16-bit auto-reload up/down/center-aligned counter and a 16-bit prescaler. TIMER13, TIMER15 and TIMER16 is based on a 16-bit auto-reload up counter and a 16-bit prescaler.

The TIMER0 and TIMER2 also support an encoder interface with two inputs using quadrature decoder.

The GD32C231xx have two watchdog peripherals, free watchdog timer and window watchdog timer. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-stage prescaler. It is clocked from an independent 32 KHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wakeup interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. The features are shown below:

- A 24-bit down counter.
- Auto reload capability.
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source.

3.13. Universal synchronous/asynchronous receiver transmitter (USART/UART)

- Up to three USARTs with operating frequency up to 6 MBits/s.
- Supports both asynchronous and clocked synchronous serial communication modes.
- IrDA SIR encoder and decoder support for USART0.

- LIN break generation and detection for USART0.
- ISO 7816-3 compliant smart card interface for USART0.
- Dual clock domain for USART0.
- Wake up from Deep-sleep mode USART0.

The USART (USART0, USART1, USART2) are used to translate data between serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART transmitter and receiver. The USART also supports DMA function for high speed data communication.

3.14. Inter-integrated circuit (I2C)

- Supports standard mode (up to 100 kHz) and fast mode (up to 400 kHz).
- The I2C0 supports fast mode plus (up to 1MHz).
- Both master and slave functions with the same interface.
- Provide arbitration function, optional PEC (packet error checking) generation and checking.
- Supports 7-bit and 10-bit addressing mode and general call addressing mode.
- Multiple 7-bit slave addresses (2 addresses with configurable mask).
- Wakeup from Deep-sleep / Deep-sleep1 mode on I2C address match.

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two lines serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides different data transfer rates: up to 100 KHz in standard mode, up to 400 KHz in the fast mode and up to 1 MHz in the fast mode plus. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

3.15. Serial peripheral interface (SPI)

- Master or slave operation with full-duplex or simplex mode
- Support both master and slave mode.
- Hardware CRC calculation and transmit automatic CRC error checking.
- Separate transmit and receive buffer, 16 bits wide (only in SPI0).
- Separate transmission and reception 32-bit FIFO (only in SPI1)
- Data frame size can be 8 or 16 bits (only in SPI0).
- Data frame size can be 4 to 16 bits (only in SPI1).
- Transmission and reception using DMA.
- SPI TI mode supported.
- SPI NSS pulse mode supported.

- Quad-SPI configuration available in master mode (only in SPI1).

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). All SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking. Quad-SPI master mode is also supported in SPI1.

3.16. Inter-IC sound (I2S)

- Sampling frequency from 8 KHz to 192 KHz.
- Support either master or slave mode.

The Inter-IC sound (I2S) bus provides a standard communication interface for digital audio applications by 3-wire serial lines. GD32C231xx contain an I2S-bus interface that can be operated with 16/32 bit resolution in master or slave mode, pin multiplexed with SPI0. The audio sampling frequency from 8 KHz to 192 KHz is supported.

3.17. Comparators (CMP)

- Two fast rail-to-rail low-power comparators with software configurable.
- Programmable reference voltage (internal or external I/O).

Two Comparators (CMP) is implemented within the device. It can wake up from low-power mode to generate interrupts and also can be combined as a window comparator.

3.18. Debug mode

- Serial wire debug port (SW-DP).

Debug capabilities can be accessed by a debug tool via Serial Wire (SW - Debug Port).

3.19. Package and operation temperature

- LQFP48 (GD32C231CxTx), QFN48 (GD32C231CxUx), LQFP32 (GD32C231KxTx), QFN32 (GD32C231KxUx), QFN28 (GD32C231GxUxTR), TSSOP20 (GD32C231FxPxTR), LGA20 (GD32C231FxVxTR).
- Operation temperature range: -40°C to +85°C (industrial level) for grade 6 devices, and -40°C to +105°C (industrial level) for grade 7 devices.

4 Electrical characteristics

4.1. Parameter introduction

- Parameter conditions: Unless otherwise specified, all values given for V_{DD}/V_{DDA} = 5 V, T_A = 25°C, and all voltages are referenced to V_{SS}.
- Value guaranteed by design, not 100% tested in production indicates that the value is derived from design or simulation and/or process characteristics.
- Value guaranteed by characterization, not 100% tested in production indicates that the value is derived from random test.
- Value guaranteed by sample, not 100% tested in production indicates that the value is derived from testing parameters with a small sample size.
- If the value is not specially indicated, it means the value guaranteed by 100% tested in production.

See the following table for some abbreviation terms and their descriptions in this chapter.

Table 4-1. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
DMA	Direct Memory Access
GPIO	General Purpose Input/Output
SPI/I2S	Serial Peripheral Interface / Inter-IC Sound
I2C	Inter-Integrated Circuit Interface
USART	Universal Synchronous / Asynchronous Receiver / Transmitter
FWDGT	Free Watchdog Timer
WWDGT	Window Watchdog Timer

4.2. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly beyond the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-2. Absolute maximum ratings (1)

Symbol	Description	Min	Max	Unit
V_{DD}/V_{DDA}	Supply voltage range	V_{SS} - 0.3	V_{SS} + 5.9	V
V_{IN}	Input voltage on 5V tolerant pin	V_{SS} - 0.3	V_{SS} + 5.9	V
	Input voltage on other I/O	V_{SS} - 0.3	V_{DD}/V_{DDA} + 0.3	V
I_{IO}	Maximum current for GPIO pins	—	20	mA
$\sum I_{IO}$	Maximum current sunk/sourced by all GPIO pin	—	80	
$I_{DD/DDA}$	Maximum current into VDD/VDDA pin	—	100	
$I_{SS/SSA}$	Maximum current into VSS/VSSA pin	—	100	
T_{STG}	Storage temperature range	-65	150	°C
T_J	Maximum junction temperature	—	125	°C

(1) Value guaranteed by design, not 100% tested in production.

4.3. General operating conditions

Table 4-3. General operating conditions (1)

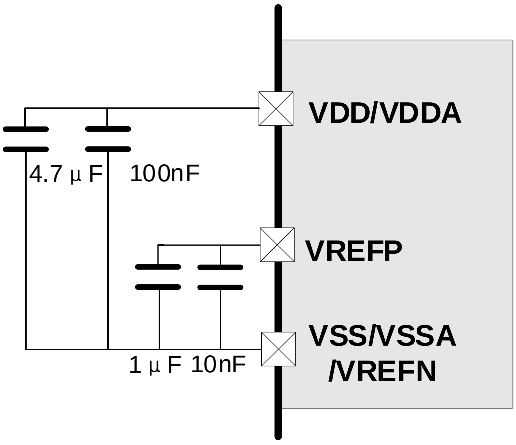
Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DD}/V_{DDA}	Supply voltage	ADC/COMP not used	1.8	—	5.5	V
		ADC used	2	—	5.5	
		COMP used	2.2	—	5.5	
V_{CORE}	Core logic supply voltage powered by internal voltage regulator	NPLDO	—	1.2	—	V
		LPLDO	—	1.0	—	
f_{CPU}	Core clock frequency	—	—	—	48	MHz
f_{HCLK}	AHB1 clock frequency	—	0	—	48	MHz
f_{PCLK}	APB clock frequency	—	0	—	48	MHz
P_D(3)	Power dissipation at T_A = 85°C of LQFP48	—	—	—	359	mW
	Power dissipation at T_A = 105°C of LQFP48		—	—	72	
	Power dissipation at T_A = 85°C of QFN48(		—	—	874	
	Power dissipation at T_A = 85°C of LQFP32		—	—	378	
	Power dissipation at T_A = 85°C of QFN32		—	—	515	
	Power dissipation at T_A = 105°C of QFN32		—	—	103	
	Power dissipation at T_A = 85°C of QFN28		—	—	378	
	Power dissipation at T_A = 105°C of QFN28		—	—	76	
	Power dissipation at T_A = 85°C of TSSOP20		—	—	346	
	Power dissipation at T_A = 105°C of TSSOP20		—	—	69	
	Power dissipation at T_A = 85°C of LGA20		—	—	260	
T_A	Operating temperature range for grade 6 device	—	-40	—	85	°C
	Operating temperature range for grade 7 device	—	-40	—	105	
T_J(2)	Junction temperature	—	-40	—	110	°C

(1) Value guaranteed by design, not 100% tested in production.

(2) The device junction temperature must be kept below maximum T_J, otherwise it may cause permanent damage to the device.

(3) For grade 6 devices, the parameter of T_A=85°C, For grade 7 devices, the parameter of T_A=105°C.

Figure 4-1. Recommended power supply decoupling capacitors (1)



(1) All decoupling capacitors need to be as close as possible to the pins on the PCB board.

4.4. Power supply requirement characteristics

Table 4-4. Power supply requirement characteristics(1)

Symbol	Description	Conditions	Min	Max	Unit
$t_{VDD/VDDA}$	V_{DD}/V_{DDA} rise time rate	—	0	∞	μs/V
	V_{DD}/V_{DDA} fall time rate	—	50	∞	

(1) Value guaranteed by design, not 100% tested in production.

4.5. Start-up timings of Operating conditions

Table 4-5. Start-up timings of Operating conditions (1)(2)(3)

Symbol	Description	Conditions	Typ	Unit
t_{ST}	Start-up time	Clock source from IRC48M	54	μs

(1) Value guaranteed by sample, not 100% tested in production.

(2) After power-up, the start-up time is the time between the rising edge of NRST high and the first I/O instruction conversion in SystemInit function.

(3) Excluding the time to initialize SRAM during startup.

4.6. Wake-up times from power saving modes

Table 4-6. Wake-up times from power saving modes (1)(2)

Symbol	Description	Conditions	Typ	Unit
t_{Sleep}	Wakeup from Sleep mode to Run mode	Transiting to Run mode executing from EFLASH, EFLASH power on during Sleep mode	254	ns
	Wakeup from Sleep 1 mode to Run 1 mode(3)	Transiting to Run 1 mode executing from SRAM, EFLASH power on during Sleep 1 mode	394.67	μs
		Transiting to Run 1 mode executing from	393.33	

Symbol	Description	Conditions	Typ	Unit
		SRAM, EFLASH power off during Sleep 1 mode		
$t_{Deep\text{-}sleep}$	Wakeup from Deep-sleep mode to Run mode	Transiting to Run mode executing from EFLASH, EFLASH power on during Deep-sleep mode	25.49	µs
		Transiting to Run mode executing from EFLASH, EFLASH power off during Deep-sleep mode	39.52	
		Transiting to Run mode executing from SRAM, EFLASH power off	2.54	
	Wakeup from Deep-sleep 1 mode to Run mode	Transiting to Run mode executing from EFLASH, EFLASH power on during Deep-sleep 1 mode	29.59	µs
		Transiting to Run mode executing from EFLASH, EFLASH power off during Deep-sleep 1 mode	43.67	
		Transiting to Run mode executing from SRAM, EFLASH power off	6.74	
$t_{Standby}$(3)	Wakeup from Standby mode to Run mode	Transiting to Run mode	80	µs

(1) Value guaranteed by sample, not 100% tested in production.

(2) The wakeup time is measured from the wakeup event to the point at which the application code reads the first instruction under the below conditions except sleep 1 mode: V_{DD}/V_{DDA} = 5 V, System clock = HXTAL = 8 MHz.

(3) V_{DD}/V_{DDA} = 5 V, System clock = IRC32K = 32 kHz.

4.7. Power consumption

The power consumption is measured as described in ***Figure 4-2. Power consumption measurement diagram***. The current consumption values are derived from the tests powered by V_{DD}/V_{DDA}, while the current is $I_{DD/DDA}$. Unless otherwise stated, V_{DD}/V_{DDA} = 5 V is applied to supply pins in typical current consumption columns.

The MCU is configured under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- Configure the WSCNT bits in the FMC_WS register correctly depend on the AHB clock frequency (refer to the table “The relation between WSCNT and AHB clock frequency” available in the GD32C2x1_User_Manual).
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$

Figure 4-2. Power consumption measurement diagram

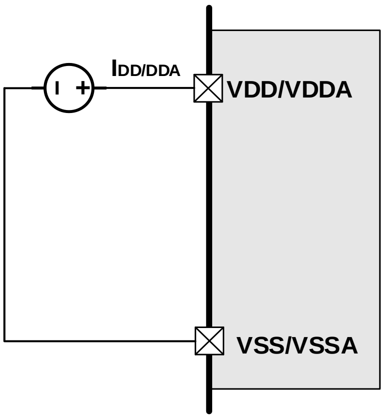


Table 4-7. Power consumption in Run mode executing from flash memory (1)(2)(4)

Symbol	Description	Conditions			Typ	Unit
		Execute from	General	f_{HCLK}		
$I_{DD/DDA}$	Supply current from VDD/VDDA (Run mode)	EFLASH	HXTAL bypass, System clock = f_{HXTAL_bypass} = f_{HCLK} ($f_{HCLK} \geq 4$ MHz), System clock = f_{HXTAL_bypass} = 4MHz ($f_{HCLK} < 4$ MHz); LXTAL bypass, System clock = f_{LXTAL_bypass} = 32.768kHz (f_{HCLK} = 32.768kHz)	48MHz(3)	4.05	mA
				48MHz	2.49	
				32MHz	1.84	
				24MHz	1.51	
				16MHz	1.18	
				8MHz	0.86	
				4MHz	0.70	
				2MHz	0.63	
				1MHz	0.59	
				500kHz	0.58	
				32.768kHz	0.53	
			IRC48M = 48 MHz, System clock = $f_{IRC48MDIV\_SYS}$ = f_{HCLK} ($f_{HCLK} \geq 375$kHz); IRC32K = 32 kHz, System clock = f_{IRC32K} = f_{HCLK} (f_{HCLK} = 32kHz)	48MHz(3)	3.95	
				48MHz	2.43	
				24MHz	1.47	
				12MHz	0.99	
				6MHz	0.75	
				3MHz	0.63	
				1.5MHz	0.57	
				750kHz	0.54	
				375kHz	0.53	
				32kHz	0.53	

(1) Value guaranteed by sample, not 100% tested in production.

(2) During power consumption test, GPIO needs to be configure as analog Input mode.

(3) All peripherals are enabled, and f_{PCLK} = f_{HCLK}.

(4) The Flash memory access time is adjusted with the correctly wait states number.

Table 4-8. Power consumption in Run mode executing from SRAM (1)(2)(4)

Symbol	Description	Conditions			Typ	Unit
		Execute from	General	f_{HCLK}		
$I_{DD/DDA}$	Supply current from VDD/VDDA (Run mode)	SRAM	HXTAL bypass, System clock = f_{HXTAL_bypass} = f_{HCLK} ($f_{HCLK} \geq 4$ MHz), System clock = f_{HXTAL_bypass} = 4MHz ($f_{HCLK} < 4$ MHz); LXTAL bypass, System clock = f_{LXTAL_bypass} = 32.768kHz (f_{HCLK} = 32.768kHz)	48MHz(3)	4.21	mA
				48MHz	2.28	
				32MHz	1.69	
				24MHz	1.40	
				16MHz	1.11	
				8MHz	0.82	
				4MHz	0.67	
				2MHz	0.61	
				1MHz	0.58	
				500kHz	0.56	

Symbol	Description	Conditions			Typ	Unit
		Execute from	General	f_{HCLK}		
				32.768kHz	0.53	
			IRC48M = 48 MHz, System clock = $f_{IRC48MDIV\_SYS}$ = f_{HCLK} (f_{HCLK} ≥ 375kHz); IRC32K = 32 kHz, System clock = f_{IRC32K} = f_{HCLK} (f_{HCLK} = 32kHz)	48MHz(3)	4.07	
				48MHz	2.14	
				24MHz	1.32	
				12MHz	0.91	
				6MHz	0.71	
				3MHz	0.61	
				1.5MHz	0.56	
				750kHz	0.53	
				375kHz	0.52	
				32kHz	0.52	

(1) Value guaranteed by sample, not 100% tested in production.

(2) During power consumption test, GPIO needs to be configure as Analog Input mode.

(3) All peripherals are enabled, and f_{PCLK} = f_{HCLK}.

(4) EFLASH power on in Run mode when executing from SRAM.

Table 4-9. Power consumption in Run mode with different codes(1)(2)(3)

Symbol	Description	Conditions			Typ	Unit	Typ	Unit
		Execute from	General	Code				
$I_{DD/DDA}$	Supply current from VDD/VDDA (Run mode)	EFLASH	HXTAL bypass, System clock = f_{HXTAL_bypass} = f_{HCLK} = 48 MHz	Coremark	3.81	mA	79.38	µA /MHz
				Dhrystone 2.1	4.55		94.79	
				While (1)(5)	2.49		51.88	
			HXTAL bypass, System clock = f_{HXTAL_bypass} = f_{HCLK} = 16 MHz	Coremark	1.80		112.50	
				Dhrystone 2.1	2.13		133.13	
				While (1)(5)	1.18		73.75	
			HXTAL bypass, System clock = f_{HXTAL_bypass} = 4 MHz, f_{HCLK} = 2 MHz	Coremark	0.74		370.00	
				Dhrystone 2.1	0.82		410.00	
				While (1)(5)	0.63		315.00	
			IRC48M = 48 MHz, System clock = $f_{IRC48MDIV\_SYS}$ =	Coremark	4.00		83.33	
				Dhrystone 2.1	4.70		97.92	
				While (1)(5)	2.43		50.63	

Symbol	Description	Conditions			Typ	Unit	Typ	Unit
		Execute from	General	Code				
			f_{HCLK} = 48 MHz					
			IRC48M = 48 MHz, System clock = $f_{IRC48MDIV\_SYS}$ = f_{HCLK} = 12 MHz	Coremark	1.48		123.33	
				Dhrystone 2.1	1.76		146.67	
				While (1) (5)	0.99		82.50	
			IRC48M = 48 MHz, System clock = $f_{IRC48MDIV\_SYS}$ = f_{HCLK} = 3 MHz	Coremark	0.79		263.33	
				Dhrystone 2.1	0.88		293.33	
				While (1) (5)	0.63		210.00	
		SRAM(4)	HXTAL bypass, System clock = f_{HXTAL_bypass} = f_{HCLK} = 48 MHz	Coremark	3.03		63.13	
				Dhrystone 2.1	3.01		62.71	
				While (1) (5)	2.28		47.50	
			HXTAL bypass, System clock = f_{HXTAL_bypass} = f_{HCLK} = 16 MHz	Coremark	1.43		89.38	
				Dhrystone 2.1	1.35		84.38	
				While (1)(5)	1.11		69.38	
			HXTAL bypass, System clock = f_{HXTAL_bypass} = 4 MHz, f_{HCLK} = 2 MHz	Coremark	0.65		325.00	
				Dhrystone 2.1	0.65		325.00	
				While (1) (5)	0.67		335.00	
			IRC48M = 48 MHz, System clock = $f_{IRC48MDIV\_SYS}$ = f_{HCLK} = 48 MHz	Coremark	3.25		67.71	
				Dhrystone 2.1	3.22		67.08	
				While (1) (5)	2.14		44.58	
			IRC48M = 48 MHz, System clock = $f_{IRC48MDIV\_SYS}$ =	Coremark	1.21		100.83	
				Dhrystone 2.1	1.19		99.17	
				While (1) (5)	0.91		75.83	

Symbol	Description	Conditions			Typ	Unit	Typ	Unit
		Execute from	General	Code				
			f_{HCLK} = 12 MHz					
			IRC48M = 48 MHz, System clock = $f_{IRC48MDIV\_SYS}$ = f_{HCLK} = 3 MHz	Coremark	0.71		236.67	
				Dhrystone 2.1	0.68		226.67	
				While (1) (5)	0.61		203.33	

(1) Value guaranteed by sample, not 100% tested in production.
(2) During power consumption test, GPIO needs to be configure as Analog Input mode.
(3) All peripherals disabled.
(4) EFLASH power on in Run mode when executing from SRAM.
(5) The code of While (1) used for results provided in ***Table 4-7*** and ***Table 4-8***.

Table 4-10. Power consumption in Run 1 mode executing from SRAM (1)(2)(3)

Symbol	Description	Conditions			Typ	Unit
		Peripherals	General	f_{HCLK}		
$I_{DD/DDA}$	Supply current from VDD/VDDA (Run 1 mode)	All disabled	IRC32K = 32 kHz, System clock = f_{IRC32K} = f_{HCLK}	32kHz	480.5	μA
			IRC32K = 32 kHz, System clock = f_{IRC32K} = f_{HCLK}, EFLASH power off	32kHz	407.0	
		All enabled	IRC32K = 32 kHz, System clock = f_{IRC32K} = f_{HCLK}	32kHz	488.8	
			IRC32K = 32 kHz, System clock = f_{IRC32K} = f_{HCLK}, EFLASH power off	32kHz	415.3	

(1) Value guaranteed by sample, not 100% tested in production.
(2) During power consumption test, GPIO needs to be configure as Analog Input mode.
(3) When the peripherals are enabled, f_{PCLK} = f_{HCLK}.

Table 4-11. Power consumption in Sleep mode (1)(2)

Symbol	Description	Conditions			Typ	Unit
		EFLASH power	General	f_{HCLK}		
$I_{DD/DDA}$	Supply current from VDD/VDDA (Sleep mode)	EFLASH power on	HXTAL bypass, System clock = f_{HXTAL_bypass} = f_{HCLK} (f_{HCLK} ≥ 4 MHz), System clock = f_{HXTAL_bypass} =	48MHz(3)	3.49	mA
				48MHz	1.54	
				32MHz	1.20	
				24MHz	1.03	
				16MHz	0.86	

Symbol	Description	Conditions			Typ	Unit
		EFLASH power	General	f_{HCLK}		
			4MHz (f_{HCLK} < 4 MHz); LXTAL bypass, System clock = f_{LXTAL_bypass} = 32.768kHz (f_{HCLK} = 32.768kHz)	8MHz	0.69	
				4MHz	0.61	
				2MHz	0.58	
				1MHz	0.57	
				500kHz	0.56	
				32.768kHz	0.53	
			IRC48M = 48 MHz, System clock = $f_{IRC48MDIV\_SYS}$ = f_{HCLK} (f_{HCLK} ≥ 375kHz); IRC32K = 32 kHz, System clock = f_{IRC32K} = f_{HCLK} (f_{HCLK} = 32kHz)	48MHz(3)	3.35	
				48MHz	1.40	
				24MHz	0.95	
				12MHz	0.73	
				6MHz	0.62	
				3MHz	0.56	
				1.5MHz	0.54	
				750kHz	0.52	
				375kHz	0.51	
				32kHz	0.53	
		EFLASH power off(4)	HXTAL bypass, System clock = f_{HXTAL_bypass} = f_{HCLK} (f_{HCLK} ≥ 4 MHz), System clock = f_{HXTAL_bypass} = 4MHz (f_{HCLK} < 4 MHz); LXTAL bypass, System clock = f_{LXTAL_bypass} = 32.768kHz (f_{HCLK} = 32.768kHz), EFLASH power off	48MHz	1.55	
				32MHz	1.19	
				24MHz	1.00	
				16MHz	0.82	
				8MHz	0.64	
				4MHz	0.54	
				2MHz	0.51	
				1MHz	0.50	
				500kHz	0.49	
				32.768kHz	0.45	
			IRC48M = 48 MHz, System clock = $f_{IRC48MDIV\_SYS}$ = f_{HCLK} (f_{HCLK} ≥ 375kHz); IRC32K = 32 kHz, System clock = f_{IRC32K} = f_{HCLK} (f_{HCLK} = 32kHz), EFLASH power off	48MHz	1.42	
				24MHz	0.92	
				12MHz	0.68	
				6MHz	0.56	
				3MHz	0.50	
				1.5MHz	0.46	
				750kHz	0.45	
				375kHz	0.44	
				32kHz	0.45	

(1) Value guaranteed by sample, not 100% tested in production.

(2) During power consumption test, GPIO needs to be configure as Analog Input mode.

(3) All peripherals are enabled, and f_{PCLK} = f_{HCLK}.

(4) Executing from SRAM When EFLASH power off.

Table 4-12. Power consumption in Sleep 1 mode(1)(2)(3)

Symbol	Description	Conditions			Typ	Unit
		Peripherals	General	f_{HCLK}		
$I_{DD/DDA}$	Supply current from VDD/VDDA (Sleep 1 mode)	All disabled	IRC32k = 32 kHz, System clock = f_{IRC32K} = f_{HCLK}	32kHz	480.5	μA
			IRC32k = 32 kHz, System clock = f_{IRC32K} = f_{HCLK}, EFLASH power off	32kHz	407.1	
		All enabled	IRC32k = 32 kHz, System clock = f_{IRC32K} = f_{HCLK}	32kHz	488.8	

(1) Value guaranteed by sample, not 100% tested in production.

(2) During power consumption test, GPIO needs to be configure as Analog Input mode.

(3) When the peripherals are enabled, f_{PCLK} = f_{HCLK}.

Table 4-13. Power consumption in Deep-sleep mode(1)(2)

Symbol	Description	Conditions		Typ	Unit
		General	V_{DD}/V_{DDA}		
$I_{DD/DDA}$	Supply current from VDD/VDDA (Deep-sleep mode)	All clocks off, V_{CORE} set to 1.0 V (PMU_CTL0->DSMODVS[1:0] = 01)	1.8V	57.02	μA
			3.3V	57.67	
			5V	58.31	
			5.5V	59.13	
		All clocks off, V_{CORE} set to 1.1 V (PMU_CTL0->DSMODVS[1:0] = 10)	1.8V	58.62	
			3.3V	59.27	
			5V	59.90	
			5.5V	60.70	
		All clocks off, V_{CORE} set to 1.2 V (PMU_CTL0->DSMODVS[1:0] = 11)	1.8V	61.16	
			3.3V	61.79	
			5V	62.41	
			5.5V	63.21	
		All clocks off, EFLASH power off, V_{CORE} set to 1.0V (PMU_CTL0->DSMODVS[1:0] = 01)	1.8V	50.69	
			3.3V	51.33	
			5V	52.02	
			5.5V	52.76	
		All clocks off, EFLASH power off, V_{CORE} set to 1.1V (PMU_CTL0->DSMODVS[1:0] = 10)	1.8V	52.03	
			3.3V	52.66	
			5V	53.29	
			5.5V	54.03	
		All clocks off, EFLASH power off, V_{CORE} set to 1.2V (PMU_CTL0->DSMODVS[1:0] = 11)	1.8V	54.15	
			3.3V	54.79	
			5V	55.39	
			5.5V	56.11	

Symbol	Description	Conditions		Typ	Unit
		General	V_{DD}/V_{DDA}		
		IRC32K off, LXTAL bypass, RTC on, RTC supplied with LXTAL bypass (32.768kHz)	1.8V	57.10	
			3.3V	57.75	
			5V	58.40	
			5.5V	59.24	
		IRC32K off, LXTAL bypass, RTC on, RTC supplied with LXTAL bypass (32.768kHz), EFLASH power off	1.8V	50.78	
			3.3V	51.39	
			5V	52.06	
			5.5V	52.83	

(1) Value guaranteed by sample, not 100% tested in production.

(2) During power consumption test, GPIO needs to be configure as Analog Input mode.

Table 4-14. Power consumption in Deep-sleep 1 mode(1)(2)

Symbol	Description	Conditions		Typ	Unit
		General	V_{DD}/V_{DDA}		
$I_{DD/DDA}$	Supply current from VDD/VDDA (Deep-sleep 1 mode)	All clocks off, V_{CORE} set to 0.9 V (PMU_CTL0->DSMODVS[1:0] = 00)	1.8V	13.05	μA
			3.3V	13.19	
			5V	13.33	
			5.5V	13.47	
		All clocks off, V_{CORE} set to 1.0 V (PMU_CTL0->DSMODVS[1:0] = 01)	1.8V	14.10	
			3.3V	14.23	
			5V	14.39	
			5.5V	14.53	
		All clocks off, V_{CORE} set to 1.1 V (PMU_CTL0->DSMODVS[1:0] = 10)	1.8V	15.79	
			3.3V	15.90	
			5V	16.05	
			5.5V	16.19	
		All clocks off, V_{CORE} set to 1.2 V (PMU_CTL0->DSMODVS[1:0] = 11)	1.8V	18.26	
			3.3V	18.38	
			5V	18.57	
			5.5V	18.70	
		All clocks off, EFLASH power off, V_{CORE} set to 0.9 V (PMU_CTL0->DSMODVS[1:0] = 00)	1.8V	3.98	
			3.3V	4.09	
			5V	4.23	
			5.5V	4.29	
		All clocks off, EFLASH power off, V_{CORE} set to 1.0V (PMU_CTL0->DSMODVS[1:0] = 01)	1.8V	4.85	
			3.3V	4.95	
			5V	5.09	
			5.5V	5.18	
		All clocks off, EFLASH power off, V_{CORE} set to 1.1V (PMU_CTL0->DSMODVS[1:0] = 10)	1.8V	6.23	
			3.3V	6.35	
			5V	6.48	
			5.5V	6.56	
			1.8V	8.30	

Symbol	Description	Conditions		Typ	Unit
		General	V_{DD}/V_{DDA}		
		All clocks off, EFLASH power off, V_{CORE} set to 1.2V (PMU_CTL0->DSMODVS[1:0] = 11)	3.3V	8.39	
			5V	8.56	
			5.5V	8.62	
		IRC32K off, LXTAL bypass, RTC on, RTC supplied with LXTAL bypass (32.768kHz)	1.8V	14.19	
			3.3V	14.28	
			5V	14.45	
			5.5V	14.57	
		IRC32K off, LXTAL bypass, RTC on, RTC supplied with LXTAL bypass (32.768kHz), EFLASH power off	1.8V	4.93	
			3.3V	5.02	
			5V	5.15	
			5.5V	5.22	
		IRC32K off, LXTAL on, RTC on, RTC supplied with LXTAL (32.768kHz)	1.8V	14.67	
			3.3V	14.93	
			5V	15.43	
			5.5V	15.71	
		IRC32K off, LXTAL on, RTC on, RTC supplied with LXTAL (32.768kHz), EFLASH power off	1.8V	5.42	
			3.3V	5.68	
			5V	6.30	
			5.5V	6.93	
		IRC32K on, LXTAL off, RTC on, RTC supplied with IRC32K	1.8V	14.27	
			3.3V	14.51	
			5V	14.93	
			5.5V	15.12	
		IRC32K on, LXTAL off, RTC on, RTC supplied with IRC32K, EFLASH power off	1.8V	5.02	
			3.3V	5.27	
			5V	5.75	
			5.5V	6.36	

(1) Value guaranteed by sample, not 100% tested in production.

(2) During power consumption test, GPIO needs to be configure as Analog Input mode.

Table 4-15. Power consumption in Standby mode(1)

Symbol	Description	Conditions		Typ	Unit
		General	V_{DD}/V_{DDA}		
I_{SUM}	Sum of supply current from VDD/VDDA (Standby mode)	All clocks off	1.8V	2.52	μA
			3.3V	2.63	
			5V	2.76	
			5.5V	2.82	
		LXTAL bypass, IRC32K off, RTC on, RTC clocked by LXTAL bypass (32.768 kHz)	1.8V	2.59	
			3.3V	2.65	
			5V	2.82	
			5.5V	2.87	
		LXTAL off, IRC32K on, RTC on, RTC clocked by IRC32K	1.8V	2.98	
			3.3V	3.15	

Symbol	Description	Conditions		Typ	Unit
		General	V_{DD}/V_{DDA}		
			5V	3.33	
			5.5V	3.44	
		LXTAL off, IRC32K on, RTC off, FWDGT on, FWDGT clocked by IRC32K	1.8V	2.96	
			3.3V	3.11	
			5V	3.33	
			5.5V	3.44	

(1) Value guaranteed by sample, not 100% tested in production.

The current consumption of the on-chip peripherals is given in the following table. To avoid adding the CPU dynamic power consumption to the peripheral power consumption, the MCU needs to enter sleep mode to stop the CPU operation during current measurement. The MCU is configured under the following conditions:

- All I/O pins are in analog input mode
- The given value is in the table calculated by measuring the difference of the current consumptions:
  - -- The target peripheral is clocked on and enters sleep mode
  - -- All peripherals are clocked off and enter sleep mode

The power consumption of the digital part of the on-chip peripherals is given in the following table. The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

Table 4-16. Peripheral current consumption characteristics(1)

Bus	Peripherals	Typical consumption	Unit
AHB1	DMAMUX	0.96	μA/MHz
	DMA	1.13	
	CRC	0.28	
	FMC	7.37	
AHB2	GPIOA	0.50	
	GPIOB	0.46	
	GPIOC	0.22	
	GPIOD	0.21	
	GPIOF	0.21	
APB	PMU	0.30	
	I2C1	2.41	
	I2C0	3.15	
	USART2	1.22	
	TIMER16	1.85	
	TIMER15	1.82	
	TIMER13	0.86	
	USART1	1.21	
	USART0	3.84	
	SPI1	0.66	
	SPI0	1.09	
	TIMER2	2.71	
	TIMER0	5.03	
	ADC	2.37	
	WWDGT	0.21	
	CMP	0.09	
	SYSCFG	0.28	

(1) Value guaranteed by sample, not 100% tested in production.

4.8. EMC characteristics

System level ESD (Electrostatic discharge, according to IEC 61000-4-2) and EFT (Electrical Fast Transient/burst, according to IEC 61000-4-4) testing result is given in the ***Table 4-17. System level ESD and EFT characteristics*** (1). System level ESD is for end-customer operation, it includes ESD field events on system level occur in an unprotected area (outside EPA). System level ESD protection necessary to satisfy higher ESD levels.

Table 4-17. System level ESD and EFT characteristics (1)

Symbol	Description	Conditions	Max	Unit	Level
V_{ESD}	Contact / Air mode high voltage stressed on few special I/O pins	V_{DD}/V_{DDA} = 5 V, T_A = 25 °C LQFP48, f_{HCLK} = 48 MHz IEC 61000-4-2	CD 8k AD 15k	V	4A
V_{EFT}	Fast transient high voltage burst stressed on Power and GND	V_{DD}/V_{DDA} = 5 V, T_A = 25 °C LQFP48, f_{HCLK} = 48 MHz IEC 61000-4-4	4k	V	4A

(1) Value guaranteed by characterization, not 100% tested in production.

EMI (Electromagnetic Interference) emission test result is given in the ***Table 4-18. EMI characteristics*** (1), The electromagnetic field emitted by the device are monitored while an application, executing EEMBC code, is running. The test is compliant with SAE J1752-3:2017 standard which specifies the test board and the pin loading.

Table 4-18. EMI characteristics (1)

Symbol	Description	Conditions	Package	Max vs. [f_{HXTAL}/f_{HCLK}] 8/48 MHz			Unit
				0.1-30MHz	30-130MHz	130MHz-1GHz	
S_{EMI}	Peak level	V_{DD}/V_{DDA} = 5.5 V, T_J = +25 °C, f_{HCLK} = 48 MHz, conforms to SAE J1752-3:2017	LQFP48	-7.75	2.21	4.40	dBμV

(1) Value guaranteed by characterization, not 100% tested in production.

Component level ESD include HBM (Human body model, according to ANSI/ESDA/JEDEC JS-001) and CDM (ANSI/ESDA/JEDEC JS-002), that ESD field events during manufacturing in an ESD protected area, such as PCB assembly/repair, IC assembly/test and Fab environment. The ESD protected area (EPA) has many measures, for instance ESD protective packaging, grounding person wrist strap to ground (or flooring/footwear), grounded work surface and ionizer.

Static latch-up (LU, according to JEDEC78) test is based on the two measurement methods, I/O current injection value (I-test) and power supply over-voltage value.

Table 4-19. Component level ESD characteristics latch-up characteristics (1)

Symbol	Description	Conditions	Package	Max	Unit	Level
V_{HBM}	Human body model electrostatic discharge voltage (Any pin combination)	T_A = 25 °C; JS-001	LQFP48	4000	V	3A
V_{CDM}	Charge device model electrostatic discharge voltage (All pins)	T_A = 25 °C; JS-002	LQFP48	1000	V	C3
LU	I-test	T_A = 125 °C; JESD78	LQFP48	200	mA	Class II Level A
	V_{supply} over voltage			8.25	V	

(1) Value guaranteed by characterization, not 100% tested in production.

4.9. Power supply supervisor characteristics

Table 4-20. Power supply supervisor characteristics

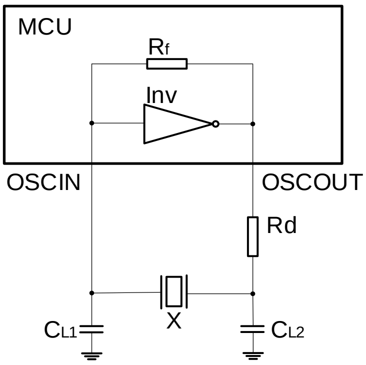
Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{POR}	Power on reset threshold	—	—	1.633(1)	1.71(2)	V
V_{PDR}	Power down reset threshold	—	1.55(2)	1.593(1)	—	
V_{BOR1}(1)	Brown-out reset threshold 1	rising edge	—	2.1	—	V
		falling edge	—	2.0	—	
V_{BOR2}(1)	Brown-out reset threshold 2	rising edge	—	2.3	—	V
		falling edge	—	2.2	—	
V_{BOR3}(1)	Brown-out reset threshold 3	rising edge	—	2.6	—	V
		falling edge	—	2.5	—	
V_{BOR4}(1)	Brown-out reset threshold 4	rising edge	—	2.9	—	V
		falling edge	—	2.8	—	
$V_{HYST(POR\_PDR)}$ (1)	Hysteresis of POR and PDR	—	—	40	—	mV
$V_{HYST(BOR)}$ (1)	BOR hysteresis	—	—	100	—	mV
$t_{RST(TEMPO)}$ (1)	Reset temporization	—	—	544	—	μs

(1) Value guaranteed by design, not 100% tested in production.

(2) Value guaranteed by characterization, not 100% tested in production.

4.10. External clock characteristics

Figure 4-3. Internal structure diagram of OSCIN and OSCOUT pin



It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine which load capacitors will best tune their resonator/crystal to the microcontroller device for optimum start-up and operation over temperature/voltage extremes.

Table 4-21. High speed external clock (HXTAL) generated from a crystal/ceramic characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{HXTAL}	Crystal or ceramic frequency	1.8 V ≤V_{DD}/V_{DDA} ≤ 5.5 V	4	8	48	MHz
R_F	Feedback resistor	1.8 V ≤V_{DD}/V_{DDA} ≤ 5.5 V	—	400	—	kΩ
C_{HXTAL}(2)	Recommended matching capacitance on OSCIN and OSCOUT	—	—	20	30	pF
$Duty_{HXTAL}$	Crystal or ceramic duty cycle	—	30	50	70	%
g_m	Oscillator transconductance	Startup	—	30	—	mA/V
$I_{DD(HXTAL)}$	Crystal or ceramic operating current	V_{DD}/V_{DDA} = 5 V, R_m = 30 Ω, C_L = 10 pF, HXTAL = 8 MHz	—	3.2	—	mA
$t_{ST(HXTAL)}$	Crystal or ceramic startup time	V_{DD}/V_{DDA} = 5 V HXTAL = 8 MHz	—	1.5	—	ms

(1) Value guaranteed by design, not 100% tested in production.

(2) C_{HXTAL1} = C_{HXTAL2} = 2*(C_{LOAD} - C_S), For C_{HXTAL1} and C_{HXTAL2}, it is recommended matching capacitance on OSCIN and OSCOUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

(3) More details about g_m could be found in ***AN052 GD32 MCU Resonator-Based Clock Circuits.***

Table 4-22. High speed external user clock characteristics (HXTAL in bypass mode) (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
$f_{HXTAL(EXT)}$	External clock source or oscillator frequency	1.8 V ≤V_{DD}/V_{DDA} ≤ 5.5 V	1	—	50	MHz
$V_{H(HXTAL)}$	OSCIN input pin high level voltage	1.8 V ≤V_{DD}/V_{DDA} ≤ 5.5 V	0.7V_{DD}/V_{DDA}	—	V_{DD}/V_{DDA}	V
$V_{L(HXTAL)}$	OSCIN input pin low level voltage		V_{SS}	—	0.3V_{DD}/V_{DDA}	

Symbol	Description	Conditions	Min	Typ	Max	Unit
$t_{H/L(HXTAL)}$	OSCIN high or low time	—	5	—	—	ns
$t_{R/F(HXTAL)}$	OSCIN rise or fall time	—	—	—	5	
C_{IN}	OSCIN input capacitance	—	—	5	—	pF
$Duty_{HXTAL}$	Duty cycle	—	40	—	60	%

(1) Value guaranteed by design, not 100% tested in production.

Table 4-23. Low speed external clock (LXTAL) generated from a crystal/ceramic characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{LXTAL}	Crystal or ceramic frequency	1.8 V $\leq V_{DD}/V_{DDA} \leq$ 5.5 V	—	32.768	—	kHz
C_{LXTAL}(2)	Recommended matching capacitance on OSC32IN and OSC32OUT	—	—	10	—	pF
$Duty_{LXTAL}$	Crystal or ceramic duty cycle	—	30	—	70	%
g_m(3)	Oscillator transconductance	LXTALDRI= 0	—	6.8	—	μA/V
		LXTALDRI= 1	—	13.7	—	
$I_{DD(LXTAL)}$	Crystal or ceramic operating current	LXTALDRI= 0	—	0.8	—	uA
		LXTALDRI= 1	—	1.15	—	
$t_{ST(LXTAL)}$(4)	Crystal or ceramic startup time	LXTALDRI= 0	—	0.7	—	s
		LXTALDRI= 1	—	0.35	—	

(1) Value guaranteed by design, not 100% tested in production.

(2) $C_{LXTAL1} = C_{LXTAL2} = 2*(C_{LOAD} - C_S)$, For C_{LXTAL1} and C_{LXTAL2}, it is recommended matching capacitance on OSC32IN and OSC32OUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

(3) More details about g_m could be found in ***AN052 GD32 MCU Resonator-Based Clock Circuits.***

(4) $t_{ST\ (LXTAL)}$ is the startup time measured from the moment it is enabled (by software) to the 32.768 kHz oscillator stabilization flags is SET. This value varies significantly with the crystal manufacturer.

Table 4-24. Low speed external user clock characteristics (LXTAL in bypass mode) (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
$f_{LXTAL(EXT)}$	External clock source or oscillator frequency	1.8 V $\leq V_{DD}/V_{DDA} \leq$ 5.5 V	—	32.768	1000	kHz
$V_{H(LXTAL)}$	OSC32IN input pin high level voltage	1.8 V $\leq V_{DD}/V_{DDA} \leq$ 5.5 V	0.7 V_{DD}/V_{DDA}	—	V_{DD}/V_{DDA}	V
$V_{L(LXTAL)}$	OSC32IN input pin low level voltage		V_{SS}	—	0.3 V_{DD}/V_{DDA}	
$t_{H/L(LXTAL)}$	OSC32IN high or low time	—	250	—	—	ns
$t_{R/F(LXTAL)}$	OSC32IN rise or fall time	—	—	—	50	
C_{IN}	OSC32IN input capacitance	—	—	5	—	pF
$Duty_{LXTAL}$	Duty cycle	—	30	—	70	%

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-4. Recommended external OSCIN and OSCOUT pins circuit for crystal

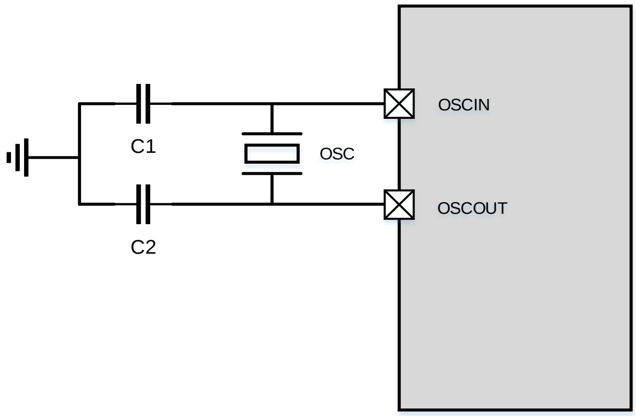
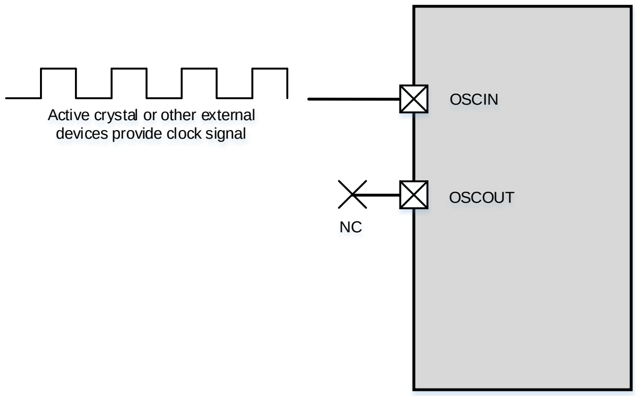


Figure 4-5. Recommended external OSCIN and OSCOUT pins circuit for oscillator



4.11. Internal clock characteristics

Table 4-25. High speed internal clock (IRC48M) characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{IRC48M}	High Speed Internal Oscillator (IRC48M) frequency	V_{DD}/V_{DDA} = 5V, T_A = 25 °C	47.76	48	48.24	MHz
$Drift_{IRC48M}$	IRC48M oscillator Frequency Drift, Factory-trimmed(1)	V_{DD}/V_{DDA} = 5V, T_A = -40 °C ~ +85 °C	-3	—	2	%
		V_{DD}/V_{DDA} = 5V, T_A = -40 °C ~ +105 °C	-3	—	2	%
	IRC48M oscillator Frequency accuracy, User trimming step(2)	—	—	0.3	—	%
$Duty_{IRC48M}$(2)	IRC48M oscillator duty cycle	—	45	50	55	%
$I_{DDA(IRC48M)}$(2)	IRC48M oscillator operating current	f_{IRC48M} = 48 MHz	—	250	—	μA
$t_{ST(IRC48M)}$(2)	IRC48M oscillator startup time	f_{IRC48M} = 48 MHz	—	2.2	—	μs

(1) Value guaranteed by characterization, not 100% tested in production.
(2) Value guaranteed by design, not 100% tested in production.

Table 4-26. High speed internal clock (IRC12M) characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{IRC12M}	High Speed Internal Oscillator (IRC12M) frequency	V_{DD}/V_{DDA} = 5V, T_A = 25 °C	11.94	12	12.06	MHz
$Drift_{IRC12M}$	IRC12M oscillator Frequency Drift, Factory-trimmed(1)	V_{DD}/V_{DDA} = 5V, T_A = -40 °C ~ +85 °C	-3	—	2	%
		V_{DD}/V_{DDA} = 5V, T_A = -40 °C ~ +105 °C	-3	—	2	%
	IRC12M oscillator Frequency accuracy, User trimming step(2)	—	—	0.3	—	%
$Duty_{IRC12M}$(2)	IRC12M oscillator duty cycle	—	45	50	55	%
$I_{DDA(IRC12M)}$(2)	IRC12M oscillator operating current	f_{IRC12M} = 12 MHz	—	50	—	μA
$t_{ST(IRC12M)}$(2)	IRC12M oscillator startup time	f_{IRC12M} = 12 MHz	—	4	—	μs

(1) Value guaranteed by characterization, not 100% tested in production.
(2) Value guaranteed by design, not 100% tested in production.

Table 4-27. Low speed internal clock (IRC32K) characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{IRC32K}	Low Speed Internal oscillator (IRC32K) frequency	V_{DD}/V_{DDA} = 5V, T_A = 25 °C	31	32	33	kHz
		V_{DD}/V_{DDA} = 5V, T_A = -40 °C ~ 85 °C(1)	29	—	35	
		V_{DD}/V_{DDA} = 5V, T_A = -40 °C ~ 105 °C(1)	29	—	35	
$I_{DDA(IRC32K)}$(2)	IRC32K oscillator operating current	—	—	650	—	nA
$t_{ST(IRC32K)}$(2)	IRC32K oscillator startup time	—	—	40	—	μs

(1) Value guaranteed by characterization, not 100% tested in production.

(2) Value guaranteed by design, not 100% tested in production.

4.12. Memory characteristics

Table 4-28. Flash memory characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
$I_{DD/DDA(FLASH)}$	Average supply current from V_{DD}/V_{DDA} during FLASH operation	Erasing	—	0.5	—	mA
		Programming	—	0.7	—	mA
PE_{CYC}(2)	Number of guaranteed program /erase cycles before failure (Endurance)	T_A range(4)	100	—	—	kcycles
t_{RET}(2)	Data retention time	T_A = 105°C after up to 0 kcycle(3)	4	—	—	years
		T_A = 85°C after up to 10 kcycles(3)	15	—	—	
		T_A = 55°C after up to 10 kcycles(3)	30	—	—	
N_{WS}	Flash wait state counter during read operation	f_{HCLK} ≤ 24MHz	—	0	—	HCLK cycles
		24MHz < f_{HCLK} ≤ 48MHz	—	1	—	
t_{PROG}	Double Word programming time	T_A = -40 °C ~ + 105 °C	—	85	—	μs
t_{PROG_ROW}	Row (8 double word) programming time	Normal programming	—	0.68	—	ms
		Fast programming	—	0.4	—	
t_{PROG_PAGE}	Page (1 Kbyte) programming time	Normal programming	—	10.88	—	ms
		Fast programming	—	6.4	—	
t_{ERASE}	Page erase time	T_A = -40 °C ~ + 105 °C	4	—	6	ms
t_{MERASE}	Mass erase time	T_A = -40 °C ~ + 105°C	30	—	40	ms

(1) Value guaranteed by design, not 100% tested in production.

(2) Value guaranteed by characterization, not 100% tested in production.

(3) Cycling performed over the whole temperature range.

(4) For grade 6 devices, T_A range = -40°C ~+85°C. For grade 7 devices, T_A range = -40°C ~+105°C.

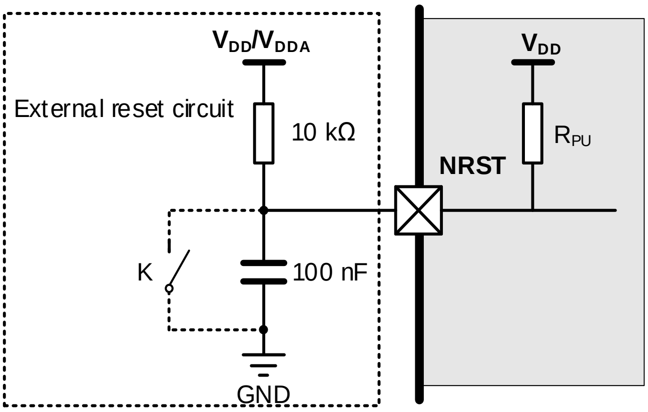
4.13. NRST pin characteristics

Table 4-29. NRST pin characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST Input low level voltage	—	—	—	0.3 V_{DD}/V_{DDA}	V
$V_{IH(NRST)}$	NRST Input high level voltage	—	0.7 V_{DD}/V_{DDA}	—	—	
V_{HYST}	Schmidt trigger Voltage hysteresis	V_{DD}/V_{DDA} = 1.8 V	—	330	—	mV
		V_{DD}/V_{DDA} = 3.3 V	—	380	—	
		V_{DD}/V_{DDA} = 5.0 V	—	460	—	
		V_{DD}/V_{DDA} = 5.5 V	—	480	—	
R_{PU}	Pull-up equivalent resistor	—	—	40	—	kΩ
$t_{F(NRST)}$	NRST input filtered pulse	1.8V < V_{DD}/V_{DDA} < 5.5 V	—	—	79.7	ns
$t_{NF(NRST)}$	NRST input not filtered pulse	1.8V < V_{DD}/V_{DDA} < 5.5 V	324	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-6. Recommended external NRST pin circuit (1)



(1) Unless the voltage on NRST pin go below $V_{IL(NRST)}$ level, the device would not generate a reliable reset.

4.14. GPIO characteristics

More details about GPIO could be found in ***AN092 GD32 MCU GPIO structure and precautions.***

Table 4-30. I/O static characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{IL}(1)	CMOS Low level input voltage	1.8 V ≤ V_{DD}/V_{DDA} ≤ 5.5 V	—	—	0.3V_{DD}/V_{DDA}	V
	TTL Low level input voltage	2.7 V ≤ V_{DD}/V_{DDA} ≤ 3.6 V	—	—	0.8	
V_{IH}(1)	CMOS High level input voltage	1.8 V ≤V_{DD}/V_{DDA} ≤ 5.5 V	0.7V_{DD}/V_{DDA}	—	—	V

Symbol	Description	Conditions	Min	Typ	Max	Unit
		V				
	TTL High level input voltage	2.7 V ≤V_{DD}/V_{DDA}≤ 3.6 V	2	—	—	
V_{HYS}(1)	Input hysteresis	1.8 V ≤V_{DD}/V_{DDA}≤ 5.5 V	—	340	—	mV
I_{LEAK}(2)	IO input leakage current	V_{SS} ≤ V_{IN} ≤V_{DD}/V_{DDA}	-2	—	2	μA
R_{PU}(1)	Weak pull-up equivalent resistor	$V_{IN} = V_{SS}$	—	40	—	kΩ
R_{PD}(1)	Weak pull-down equivalent resistor	$V_{IN} = V_{DD}/V_{DDA}$	—	40	—	kΩ

(1) Value guaranteed by design, not 100% tested in production.

(2) Value guaranteed by characterization, not 100% tested in production.

Table 4-31. Output voltage characteristics for all I/Os (1)

Symbol	Description	Conditions	Typ	Unit
V_{OL} (GPIO_OSPD = 0)	Low level output voltage for an IO Pin (I_{IO} = +1 mA)	V_{DD}/V_{DDA} = 1.8 V	0.244	V
		V_{DD}/V_{DDA} = 3.3 V	0.111	
		V_{DD}/V_{DDA} = 5 V	0.079	
		V_{DD}/V_{DDA} = 5.5 V	0.076	
V_{OH} (GPIO_OSPD = 0)	High level output voltage for an IO Pin (I_{IO} = +1 mA)	V_{DD}/V_{DDA} = 1.8 V	1.509	
		V_{DD}/V_{DDA} = 3.3 V	3.159	
		V_{DD}/V_{DDA} = 5 V	4.897	
		V_{DD}/V_{DDA} = 5.5 V	5.403	
V_{OL} (GPIO_OSPD = 1)	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD}/V_{DDA} = 1.8 V	0.307	
		V_{DD}/V_{DDA} = 3.3 V	0.143	
		V_{DD}/V_{DDA} = 5 V	0.107	
		V_{DD}/V_{DDA} = 5.5 V	0.102	
	Low level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD}/V_{DDA} = 2.7 V	0.496	
		V_{DD}/V_{DDA} = 3.3 V	0.388	
		V_{DD}/V_{DDA} = 5 V	0.277	
		V_{DD}/V_{DDA} = 5.5 V	0.262	
	Output low level voltage for an FT I/O pin in FM+ mode(2) (I_{IO} = +20 mA)	V_{DD}/V_{DDA} = 2.7 V	0.247	
		V_{DD}/V_{DDA} = 3.3 V	0.207	
		V_{DD}/V_{DDA} = 5 V	0.155	
		V_{DD}/V_{DDA} = 5.5 V	0.149	
V_{OH} (GPIO_OSPD = 1)	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD}/V_{DDA} = 1.8 V	1.448	
		V_{DD}/V_{DDA} = 3.3 V	3.125	
		V_{DD}/V_{DDA} = 5 V	4.870	
		V_{DD}/V_{DDA} = 5.5 V	5.365	
	High level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD}/V_{DDA} = 2.7 V	2.111	
		V_{DD}/V_{DDA} = 3.3 V	2.829	
		V_{DD}/V_{DDA} = 5 V	4.660	
		V_{DD}/V_{DDA} = 5.5 V	5.180	

(1) Value guaranteed by sample, not 100% tested in production.

(2) Only applicable to pin PA9/PA10/PB6/PB7/PB8/PB9

Table 4-32. I/O port AC characteristics (1)(2)(3)(4)

Speed	Symbol	Description	Conditions	Max	Unit
0	t_R/t_F	Output high to low level fall time and output low to high level rise time	1.8 V ≤V_{DD}/V_{DDA} ≤ 5.5 V, C_L = 10 pF, Fmax=2MHz	53	ns
			1.8 V ≤V_{DD}/V_{DDA} ≤ 5.5 V, C_L = 30 pF, Fmax=2Mz	84	
1	t_R/t_F	Output high to low level fall time and output low to high level rise time	2.70 V ≤V_{DD}/V_{DDA} ≤ 5.5 V, C_L = 30 pF, Fmax=50MHz	4.5	ns
			1.8 V ≤V_{DD}/V_{DDA} ≤ 5.5 V, C_L = 10 pF, Fmax=40MHz	4.4	
			2.70 V ≤V_{DD}/V_{DDA} ≤ 5.5 V, C_L = 50 pF, Fmax=30MHz	6.6	
			1.8 V ≤V_{DD}/V_{DDA} ≤ 5.5 V, C_L = 30 pF, Fmax=30MHz	7.6	

(1) The maximum frequency is defined with the following conditions: (tr+tf) ≤ 2/3 T Skew ≤ 1/20 T 45% < Duty cycle < 55%.

(2) The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.

(3) Value guaranteed by design, not 100% tested in production.

(4) The data is for reference only, and the specific values are related to PCB Layout.

4.15. Internal reference voltage characteristics

Table 4-33. Internal reference voltage characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	T_A = -40°C ~ +105 °C	1.16	1.2	1.24	V
$t_{S\_VREFINT}$(2)	ADC sampling time when reading the internal reference voltage	—	5	—	—	μs
$t_{STA\_VREFINT}$	Start time of reference voltage buffer when ADC is enable	—	—	8	10	μs
$I_{DD/DDA(VREFINT\_BUF)}$	V_{REFINT} buffer consumption from V_{DD}/V_{DDA} when converted by ADC	—	—	12.5	15	μA
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	—	—	5.7	12.4	mV

(1) Value guaranteed by design, not 100% tested in production.

(2) The shortest sampling time can be determined in the application by multiple iterations.

Table 4-34. Internal reference voltage calibration values

Symbol	Test conditions	Memory address
V_{REFINT}(1)	V_{DD}/V_{DDA} = 5 V (± 4.5mV),	0x1FFF 0BFC-0x1FFF 0BFD

Symbol	Test conditions	Memory address
	Temperature = 25 °C (± 4 °C)	

(1) V_{REFINT} is internally connected to the ADC_IN14 input channel.

4.16. ADC characteristics

Table 4-35. ADC characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DD}/V_{DDA}	Operating voltage	—	2	5	5.5	V
V_{REFP}(2)	Positive Reference Voltage	—	2	—	V_{DD}/V_{DDA}	V
V_{IN}	ADC input voltage range	—	0	—	V_{REFP}	V
f_{ADC}	ADC clock	—	—	—	24	MHz
f_S	Sampling rate	12-bit	—	—	1.60	MSPS
		10-bit	—	—	1.84	
		8-bit	—	—	2.18	
		6-bit	—	—	2.66	
R_{AIN}	External input impedance	See ***Equation 1***	—	—	136.12	kΩ
R_{ADC}	Input sampling switch resistance	—	—	—	0.7	kΩ
C_{ADC}	Input capacitance	No pin/pad capacitance included	—	2.9	—	pF
t_S	Sampling time	f_{ADC} = 24 MHz	0.1	—	10.6	μs
t_{CONV}	Total conversion time(including sampling time)	12-bit	—	15	—	1/ f_{ADC}
		10-bit	—	13	—	
		8-bit	—	11	—	
		6-bit	—	9	—	
$I_{DD/DDA(ADC)}$	ADC consumption from V_{DD}/V_{DDA} and V_{REFP}	V_{DD}/V_{DDA} = V_{REFP} = 5 V	—	1030	—	μA
$t_{ST(ADC)}$	Startup time	—	—	1	—	μs

(1) Value guaranteed by design, not 100% tested in production.

(2) V_{REFP} should always be equal to or less than V_{DD}/V_{DDA}, especially during power up.

Equation 1: R_{AIN} max formula $R_{AIN} < \frac{T_S}{f_{ADC}*C_{ADC}*\ln(2^{N+2})} - R_{ADC}$

The formula above (***Equation 1***) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 4-36. ADC RAIN max for f_{ADC} = 24 MHz (1)(2)

Resolution	Sampling cycles	t_S (μs)	R_{AIN} max (kΩ)
12 bits	2.5	0.104	0.441
	3.5	0.146	0.979
	7.5	0.313	3.125
	12.5	0.521	5.809
	19.5	0.813	9.566

Resolution	Sampling cycles	t_S (μs)	R_{AIN} max (kΩ)
	39.5	1.656	20.300
	79.5	3.313	41.769
	160.5	6.688	85.243
10 bits	2.5	0.104	0.665
	3.5	0.146	1.292
	7.5	0.313	3.796
	12.5	0.521	6.927
	19.5	0.813	11.310
	39.5	1.656	23.833
	79.5	3.313	48.880
	160.5	6.688	99.600
8 bits	2.5	0.104	0.979
	3.5	0.146	1.730
	7.5	0.313	4.736
	12.5	0.521	8.493
	19.5	0.813	13.752
	39.5	1.656	28.780
	79.5	3.313	58.836
	160.5	6.688	119.700
6 bits	2.5	0.104	1.448
	3.5	0.146	2.387
	7.5	0.313	6.144
	12.5	0.521	10.840
	19.5	0.813	17.415
	39.5	1.656	36.200
	79.5	3.313	73.770
	160.5	6.688	149.850

(1) Value guaranteed by design, not 100% tested in production.

(2) The R_{AIN} value was calculated by theory and stray capacitance of actual pcb has not been taken into account.

Table 4-37. ADC accuracy at f_{ADC} = 12 MHz (1)(2)(3)

Symbol	Description	Test conditions	Typ	Unit
EO	Offset error	$V_{DD}/V_{DDA} = V_{REFP}$ = 3.3 V, f_{ADC} = 12 MHz, f_S = 0.8 MSPS, T_A = 25 °C	±0.6	LSB
DNL	Differential linearity error		±0.5	
INL	Integral linearity error		±0.8	
ENOB	Effective number of bits		10.5	Bits
SNDR	Signal-to-noise and distortion ratio		65	dB
SNR	Signal-to-noise ratio		65	
THD	Total harmonic distortion		-80	

(1) Value guaranteed by sample, not 100% tested in production.

(2) Some guidance is provided to improve the sampling accuracy of ADC. Refer to AN059 Methods to improve ADC sampling accuracy.

(3) Guaranteed by sample results for LQFP48 packages.

Table 4-38. ADC accuracy at f_{ADC} = 24 MHz (1)(2)(3)

Symbol	Description	Test conditions	Typ	Unit
EO	Offset error	$V_{DD}/V_{DDA} = V_{REFP} = 5$ V, f_{ADC} = 24MHz, f_S = 1.6 MSPS, T_A = 25 °C	±0.95	LSB
DNL	Differential linearity error		±0.5	
INL	Integral linearity error		±0.7	
ENOB	Effective number of bits		10.8	Bits
SNDR	Signal-to-noise and distortion ratio		67.13	dB
SNR	Signal-to-noise ratio		67.25	
THD	Total harmonic distortion		-81.9	

(1) Value guaranteed by sample, not 100% tested in production.

(2) Some guidance is provided to improve the sampling accuracy of ADC. Refer to AN059 Methods to improve ADC sampling accuracy.

(3) Guaranteed by sample results for LQFP48 packages.

Figure 4-7. Differential linearity error

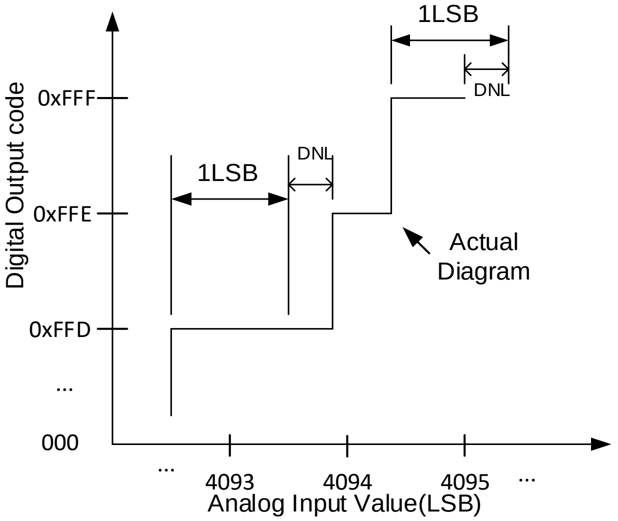
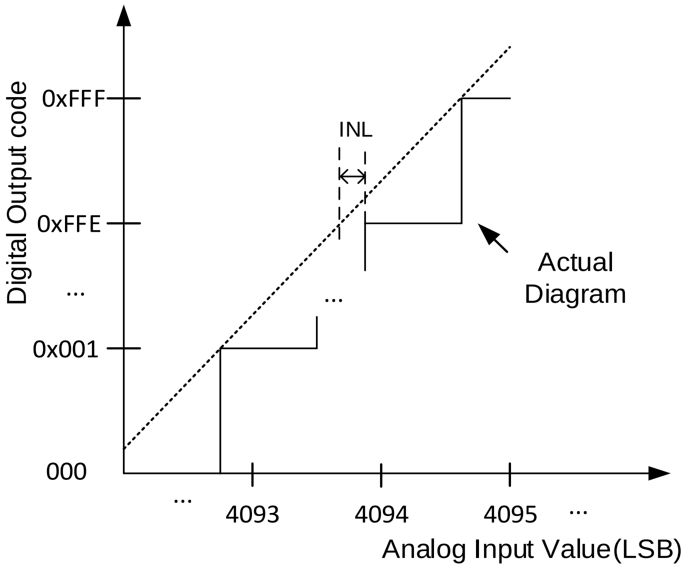


Figure 4-8. Integral linearity error



4.17. Temperature sensor characteristics

Table 4-39. Temperature sensor characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{25}(1)	Voltage at T_A = 25 °C (± 4 °C)	V_{DD}/V_{DDA} = 5 V (± 4.5 mV)	904	924	944	mV
Avg_Slope(2)	Average slope	—	—	2.52	—	mV/°C
T_L(2)	V_{SENSE} linearity with temperature	T_J = -40 °C to 125 °C	—	-2.2~0.2	—	°C
$t_{ST(TS)}$	Start up time	—	—	8	—	μs
t_{S_temp}(2)	ADC sampling time when reading the temperature	—	5	—	—	μs

(1) The V_{25} ADC conversion result is stored in the TS_CAL1 byte.

(2) Value guaranteed by design, not 100% tested in production.

(3) Shortest sampling time can be determined in the application by multiple iterations.

Table 4-40. Temperature sensor calibration values

Symbol	Description	Memory address
TS_CAL1	Temperature sensor raw data acquired value at 25 °C (±4 °C), V_{DD}/V_{DDA} = 5V (±4.5 mV)	0x1FFF 0BF8-0x1FFF 0BF9

4.18. Comparators characteristics

Table 4-41. CMP characteristics (1)

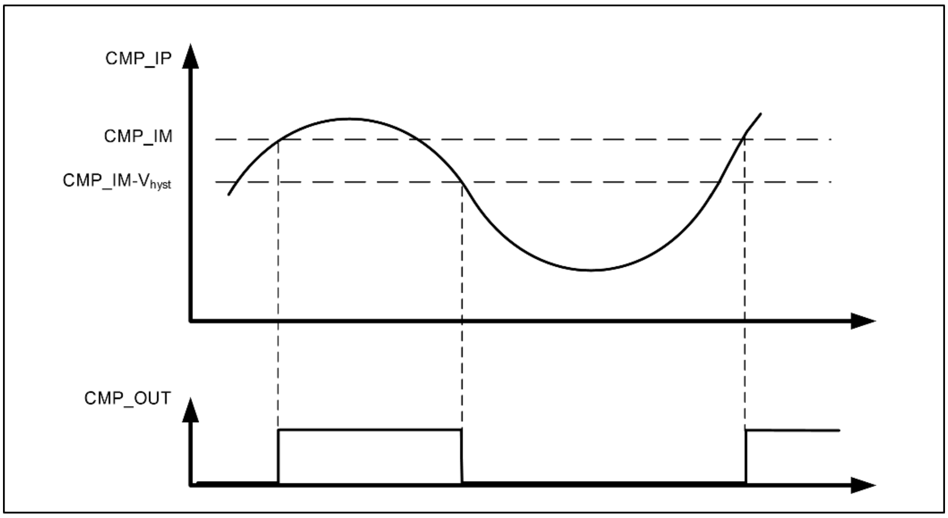
Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DD}/V_{DDA}	Operating voltage	—	2.2	5	5.5	V

Symbol	Description	Conditions		Min	Typ	Max	Unit
V_{IN}	Input voltage range	—		0	—	V_{DD}/V_{DDA}	V
V_{BG}	Scaler input voltage	—		—	1.2	—	V
V_{SC}	Scaler offset voltage	—		—	±5	—	mV
$I_{DD/DDA(SCALER)}$	Scaler static consumption from V_{DD}/V_{DDA}	BEN=0 (bridge disable)		—	0.3	—	μA
		BEN=1 (bridge enable)		—	3.3	—	
$t_{ST(SCALER)}$	Scaler startup time	—		—	15	—	μs
t_D	Propagation delay for 200mV step with 100 mV overdrive	Very-low speed / ultra-low power mode		—	680	—	ns
		Low speed / low power mode		—	290	—	ns
		Medium speed / medium power mode		—	110	—	ns
		High speed / full power mode		—	30	—	ns
	Propagation delay for step > 200 mV with 100 mV overdrive only on positive inputs	Very-low speed / ultra-low power mode		—	930	—	ns
		Low speed / low power mode		—	400	—	ns
		Medium speed / medium power mode		—	155	—	ns
		High speed / full power mode		—	40	—	ns
$t_{ST(CMP)}$	Comparator startup time to reach propagation delay specification	Very-low speed / ultra-low power mode		—	6.3	—	μs
		Low speed / low power mode		—	4.3	—	
		Medium speed / medium power mode		—	1.25	—	
		High speed / full power mode		—	0.27	—	
$I_{DD/DDA(CMP)}$	Current consumption from V_{DD}/V_{DDA}	Very-low speed / ultra-low power mode	Static	—	5.6	9.9	μA
			With 50 kHz ±100 mV overdrive square signal	—	11.3	—	
		Low speed / low power mode	Static	—	7	11	μA
			With 50 kHz ±100 mV overdrive square signal	—	9.7	—	
		Medium speed / medium power mode	Static	—	12	16	μA
			With 50 kHz ±100 mV overdrive square signal	—	12.8	—	
		High speed / full power mode	Static	—	60	64	μA
			With 50 kHz ±100 mV	—	56.5	—	

Symbol	Description	Conditions	Min	Typ	Max	Unit
		overdrive square signal				
V_{OFFSET}	Offset error	—	—	±5	—	mV
V_{HYST}	Hysteresis Voltage	No Hysteresis	—	0	—	mV
		Low Hysteresis	—	15	—	
		Medium Hysteresis	—	30	—	
		High Hysteresis	—	45	—	

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-9. CMP hysteresis



4.19. TIMER characteristics

Table 4-42. TIMER characteristics (1)

Symbol	Description	Conditions	Min	Max	Unit
t_{RES}	Timer resolution time	—	1	—	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 48 MHz	20.833	—	ns
f_{EXT}	Timer external clock frequency	—	0	$f_{TIMERxCLK}$ /4	MHz
		$f_{TIMERxCLK}$ = 48 MHz	0	12	MHz
RES	Timer resolution	—	—	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	—	1	65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 48 MHz	0.0208	1365	μs
t_{MAX_COUNT}	Maximum possible count	—	—	65536 x 65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 48 MHz	—	89.48	s

(1) Value guaranteed by design, not 100% tested in production.

4.20. I2C characteristics

Table 4-43. I2C characteristics (1)(2)

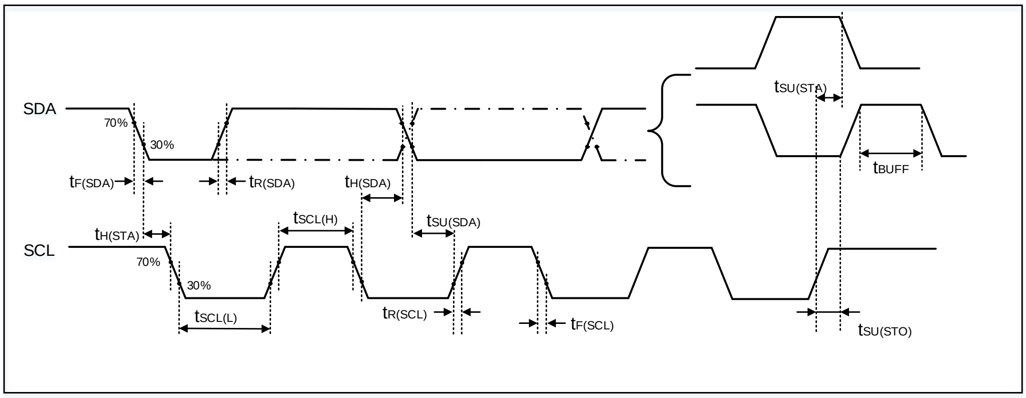
Symbol	Description	Conditions	Standard mode		Fast mode		Fast mode plus		Unit
			Min	Max	Min	Max	Min	Max	
$t_{SCL(H)}$	SCL clock high time	—	4.0	—	0.6	—	0.2	—	μs
$t_{SCL(L)}$	SCL clock low time	—	4.7	—	1.3	—	0.5	—	μs
$t_{SU(SDA)}$	SDA setup time	—	250	—	100	—	50	—	ns
$t_{H(SDA)}$	SDA data hold time	—	0 (3)	3450	0	900	0	450	ns
$t_{R(SDA/SCL)}$	SDA and SCL rise time	—	—	1000	—	300	—	120	ns
$t_{F(SDA/SCL)}$	SDA and SCL fall time	—	—	300	—	300	—	120	ns
$t_{H(STA)}$	Start condition hold time	—	4.0	—	0.6	—	0.26	—	μs
$t_{SU(STA)}$	Repeated Start condition setup time	—	4.7	—	0.6	—	0.26	—	μs
$t_{SU(STO)}$	Stop condition setup time	—	4.0	—	0.6	—	0.26	—	μs
t_{BUFF}	Stop to Start condition time (bus free)	—	4.7	—	1.3	—	0.5	—	μs

(1) Value guaranteed by design, not 100% tested in production.

(2) To ensure the standard mode I2C frequency, f_{PCLK} must be at least 2 MHz. To ensure the fast mode I2C frequency, f_{PCLK} must be at least 4 MHz. To ensure the fast mode plus I2C frequency, f_{PCLK1} must be at least a multiple of 10 MHz.

(3) The device should provide a data hold time of 300 ns at least in order to bridge the undefined region of the falling edge of SCL.

Figure 4-10. I2C bus timing diagram



4.21. SPI characteristics

Table 4-44. Standard SPI characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	$V_{DD}/V_{DDA} > 2$ V	—	—	24	MHz
		1.8V ≤ V_{DD}/V_{DDA} ≤ 2 V	—	—	12	
$t_{SCK(H)}$	SCK clock high time	Master mode, f_{PCLK} = 48 MHz, presc = 2	—	20	—	ns
$t_{SCK (L)}$	SCK clock low time	Master mode, f_{PCLK} = 48 MHz, presc = 2	—	20	—	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time	—	—	—	10	ns
$t_{SU(MI)}$	Data input setup time	—	1	—	—	ns
$t_{H(MI)}$	Data input hold time	—	0	—	—	ns
SPI slave mode						
$t_{SU(NSS)}$	NSS enable setup time	—	0	—	—	ns
$t_{H(NSS)}$	NSS enable hold time	—	1	—	—	ns
$t_{A(SO)}$	Data output access time	—	—	8	—	ns
$t_{DIS(SO)}$	Data output disable time	—	—	9	—	ns
$t_{V(SO)}$	Data output valid time	—	—	9	—	ns
$t_{SU(SI)}$	Data input setup time	—	0	—	—	ns
$t_{H(SI)}$	Data input hold time	—	1	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-11. SPI timing diagram - master mode

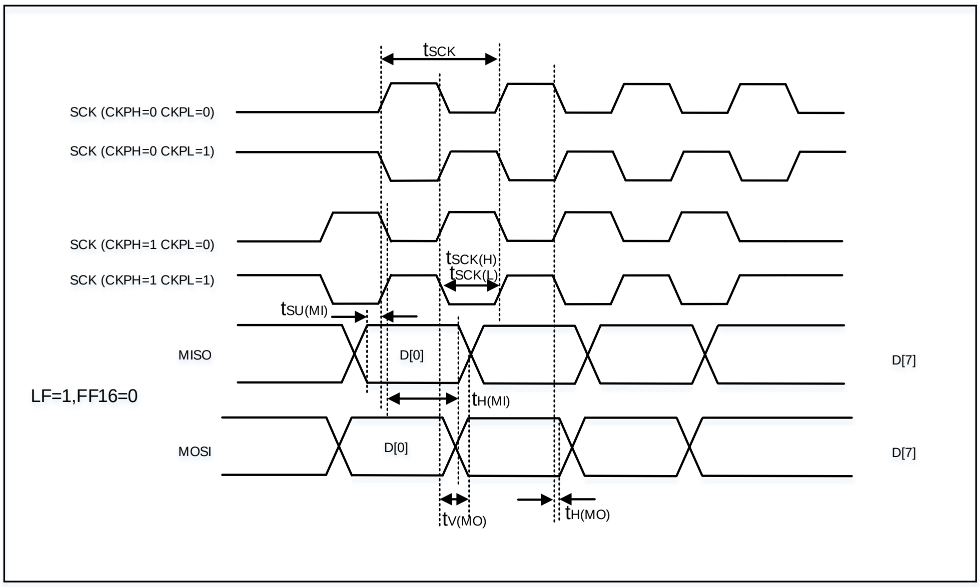


Figure 4-12. SPI timing diagram - slave mode (CKPH=0)

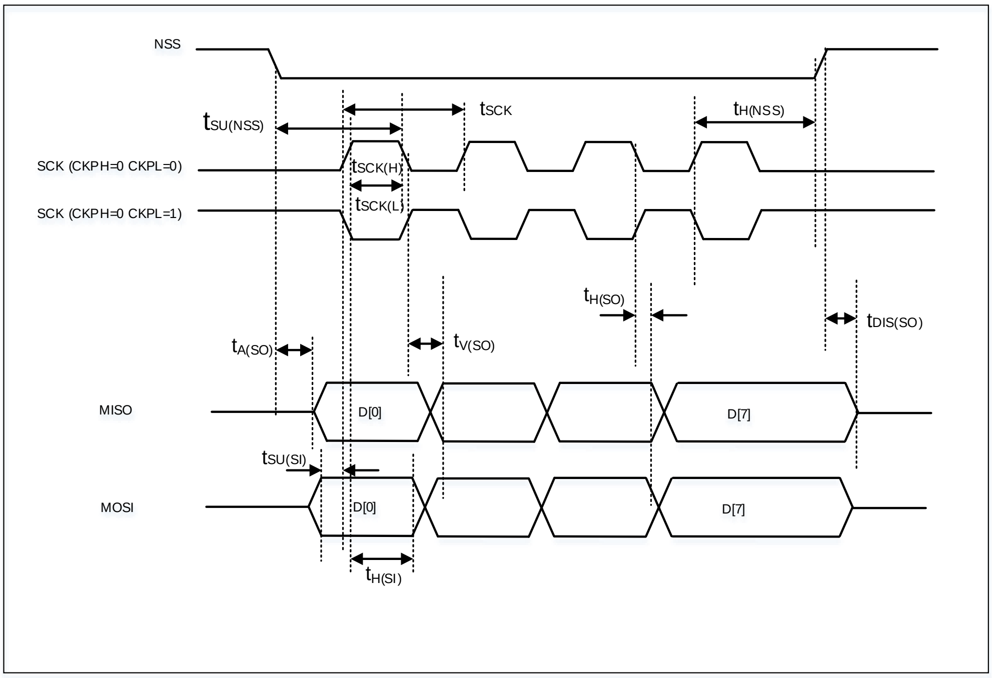
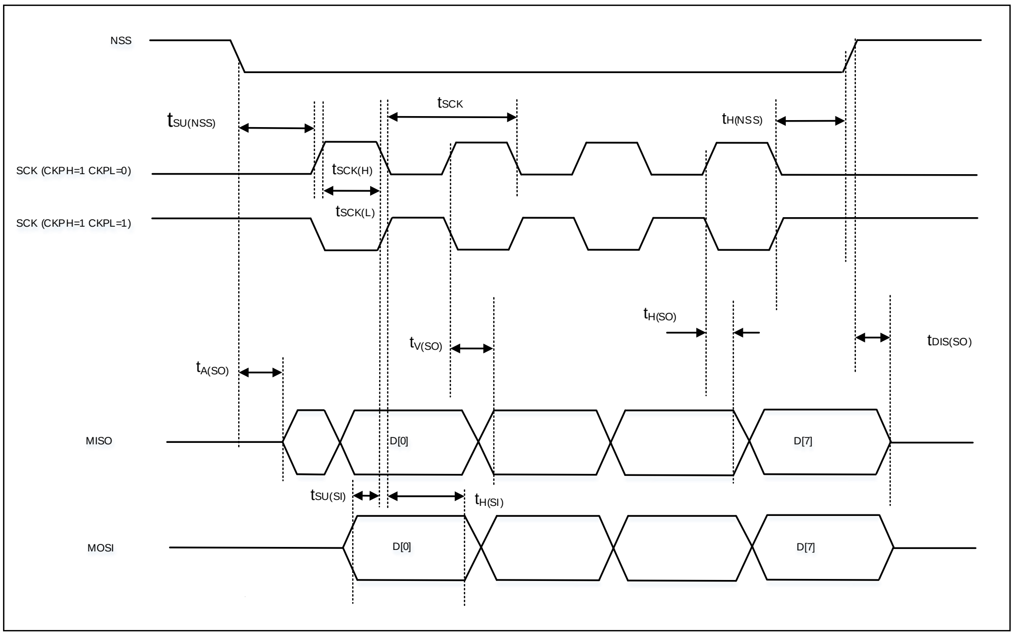


Figure 4-13. SPI timing diagram - slave mode (CKPH=1)



4.22. I2S characteristics

Table 4-45. I2S characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{CK}	Clock frequency	Master mode (data: 16 bits, Audio frequency = 96 kHz)	—	6.25	—	MHz
		Slave mode	—	—	12.5	
t_H	Clock high time	—	—	80	—	ns
t_L	Clock low time		—	80	—	ns
$t_{V(WS)}$	WS valid time	Master mode	—	3	—	ns
$t_{H(WS)}$	WS hold time	Master mode	—	3	—	ns
$t_{SU(WS)}$	WS setup time	Slave mode	0	—	—	ns
$t_{H(WS)}$	WS hold time	Slave mode	3	—	—	ns
$Duty_{(SCK)}$	I2S slave input clock duty cycle	Slave mode	—	50	—	%
$t_{SU(SD\_MR)}$	Data input setup time	Master mode	1	—	—	ns
$t_{SU(SD\_SR)}$	Data input setup time	Slave mode	0	—	—	ns
$t_{H(SD\_MR)}$	Data input hold time	Master receiver	0	—	—	ns
$t_{H(SD\_SR)}$		Slave receiver	1	—	—	ns
$t_{V(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	—	—	10	ns
$t_{H(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	3	—	—	ns
$t_{V(SD\_MT)}$	Data output valid time	Master transmitter (after enable edge)	—	—	10	ns

Symbol	Description	Conditions	Min	Typ	Max	Unit
$t_{H(SD\_MT)}$	Data output hold time	Master transmitter (after enable edge)	0	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-14. I2S timing diagram - master mode

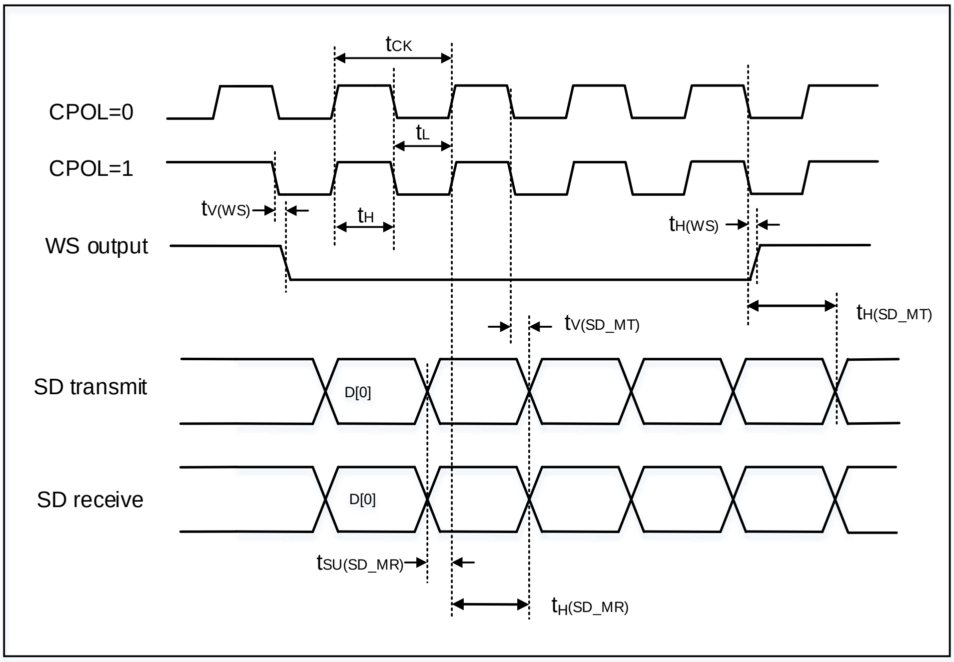
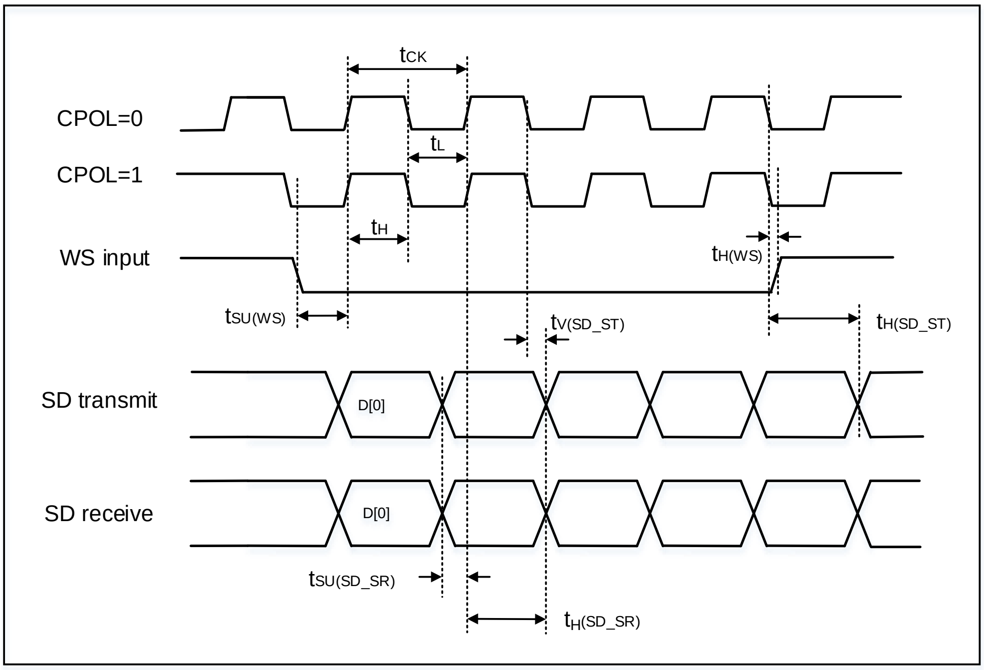


Figure 4-15. I2S timing diagram - slave mode



4.23. USART characteristics

Table 4-46. USART characteristics in Synchronous mode (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	Master mode	—	—	6	MHz
$t_{H(SCK)}$	SCK clock high time	Master mode	82.3	—	—	ns
$t_{L(SCK)}$	SCK clock low time	Master mode	82.3	—	—	ns
$t_{V(TX)}$	Data output valid time	Master mode	—	1	2	ns
$t_{H(TX)}$	Data output hold time	Master mode	0	—	—	

(1) Guaranteed by design, not 100% tested in production.

4.24. WDGT characteristics

Table 4-47. FWDGT min/max timeout period at 32 kHz (IRC32K) (1)

Prescaler divider	PSC[2:0] bits	Min timeout RLD[11:0]= 0x000	Max timeout RLD[11:0]= 0xFFF	Unit
1/4	000	0.03125	511.90625	ms
1/8	001	0.03125	1023.78125	
1/16	010	0.03125	2047.53125	
1/32	011	0.03125	4095.03125	
1/64	100	0.03125	8190.03125	
1/128	101	0.03125	16380.03125	
1/256	110 or 111	0.03125	32760.03125	

(1) Value guaranteed by design, not 100% tested in production.

Table 4-48. WWDGT min-max timeout value at 48 MHz (f_{PCLK}) (1)

Prescaler divider	PSC[3:0]	Min timeout value CNT[6:0] = 0x40	Unit	Max timeout value CNT[6:0] = 0x7F	Unit
1/1	0000	85.33	μs	5.461	ms
1/2	0001	170.67		10.923	
1/4	0010	341.33		21.845	
1/8	0011	682.67		43.691	
1/16	0100	1.365	ms	87.382	
1/32	0101	2.731		174.764	
1/64	0110	5.461		349.528	
1/128	0111	10.922		699.056	
1/256	1000	21.854		1398.112	
1/512	1001	43.691		2796.224	
1/1024	1010	87.381		5592.448	
1/2048	1011	174.763		11184.896	
1/4096	1100	349.525		22369.792	
1/8192	1101	699.051		44739.584	
1/1	1110	85.33	μs	5.461	
1/1	1111	85.33		5.461	

(1) Value guaranteed by design, not 100% tested in production.

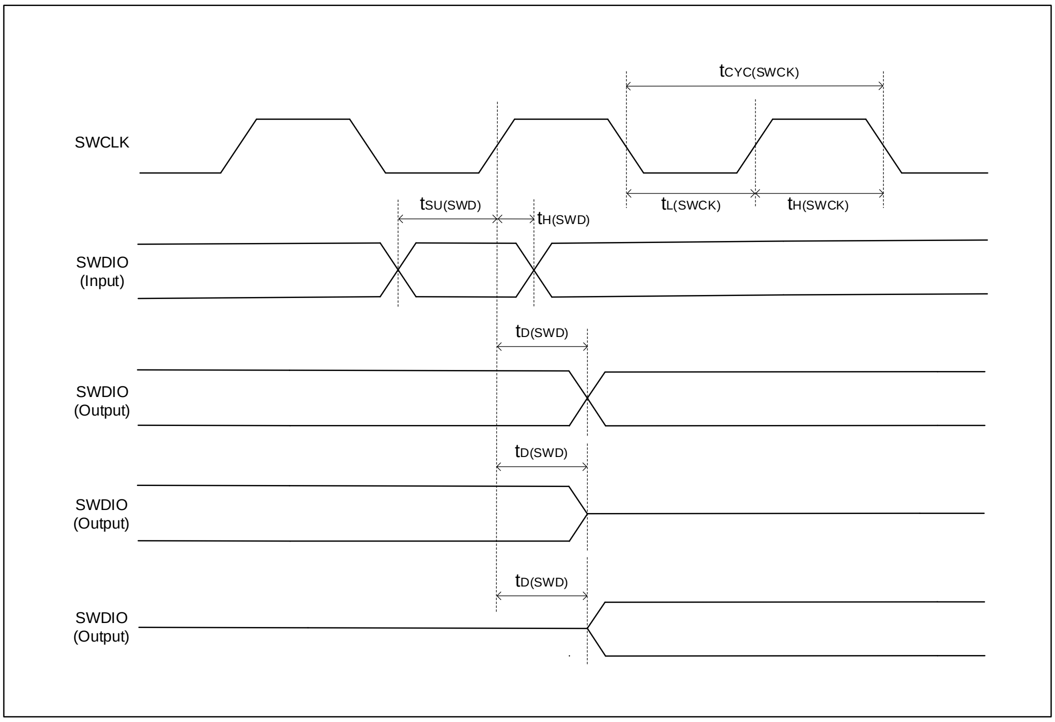
4.25. SWD Timing

Table 4-49. SWD Interface Timing (1)

Symbol	Description	Min	Max	Unit
$t_{CYC(SWCK)}$	SWCLK clock cycle time	40	—	ns
$t_{H(SWCK)}$	SWCLK clock high pulse width	17	—	ns
$t_{L(SWCK)}$	SWCLK clock low pulse width	17	—	ns
$t_{R(SWCK)}$	SWCLK clock rise time	—	1	ns
$t_{F(SWCK)}$	SWCLK clock fall time	—	1	ns
$t_{SU(SWD)}$	SWDIO setup time	15	—	ns
$t_{H(SWD)}$	SWDIO hold time	1	—	ns
$t_{D(SWD)}$	SWDIO data delay time	10	12	ns

(1) Guaranteed by design, not 100% tested in production

Figure 4-16. SWD SWCLK Timings



5 Package information

5.1 LQFP48 package outline dimensions

Figure 5-1. LQFP48 package outline

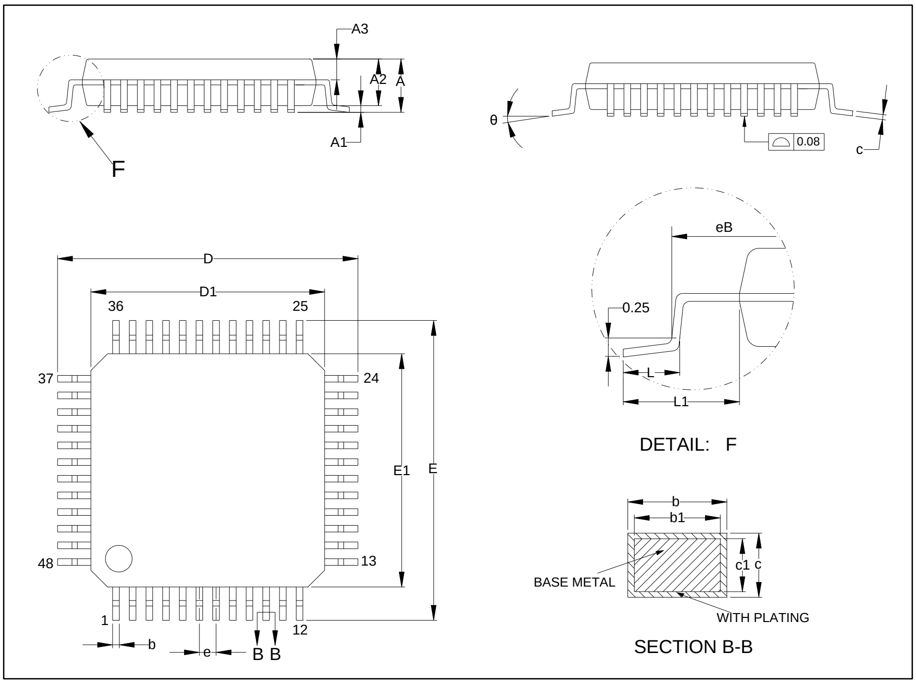
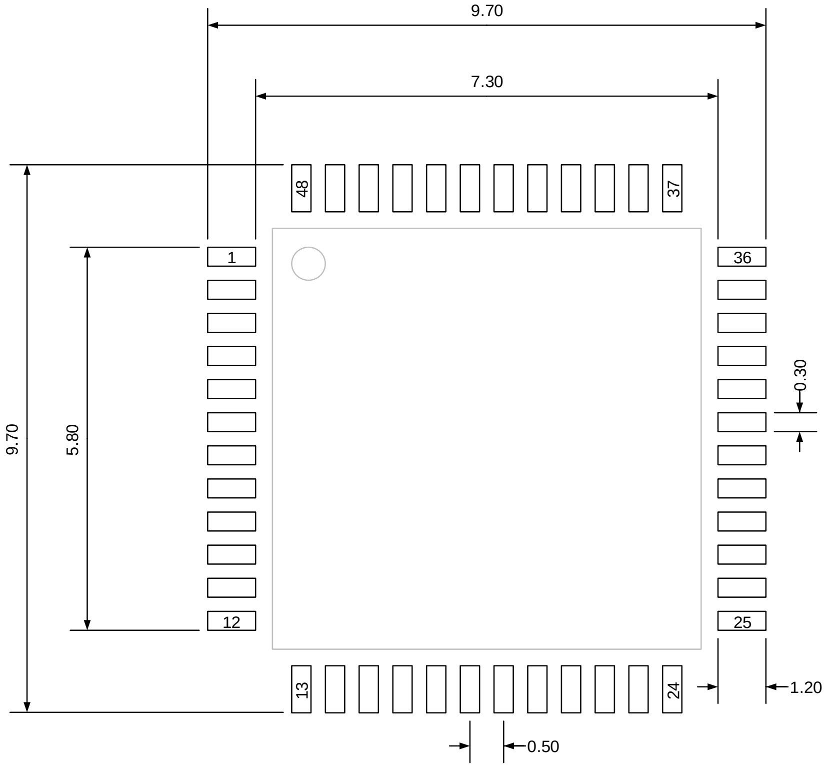


Table 5-1. LQFP48 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	—	0.50	—
eB	8.10	—	8.25
L	0.45	—	0.75
L1	—	1.00	—
θ	0°	—	7°

(Original dimensions are in millimeters)

Figure 5-2. LQFP48 recommended footprint



(Original dimensions are in millimeters)

5.2 QFN48 package outline dimensions

Figure 5-3. QFN48 package outline

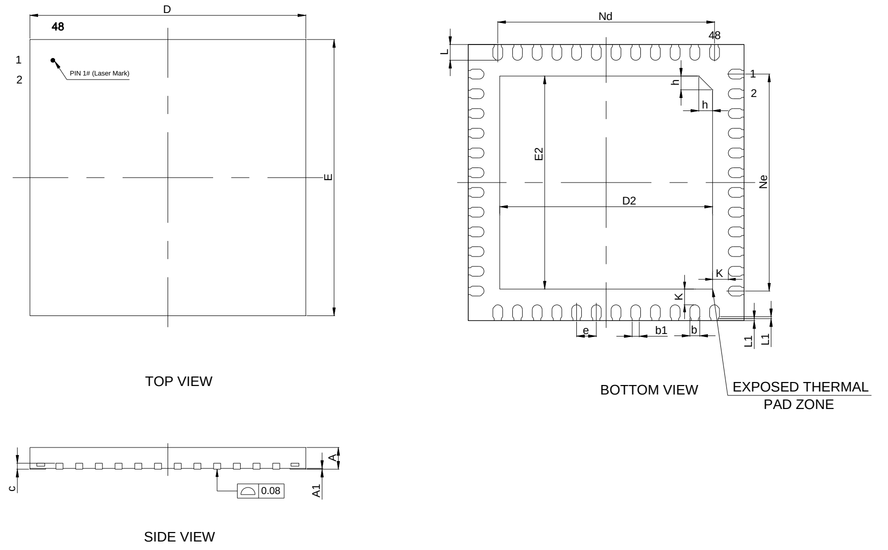
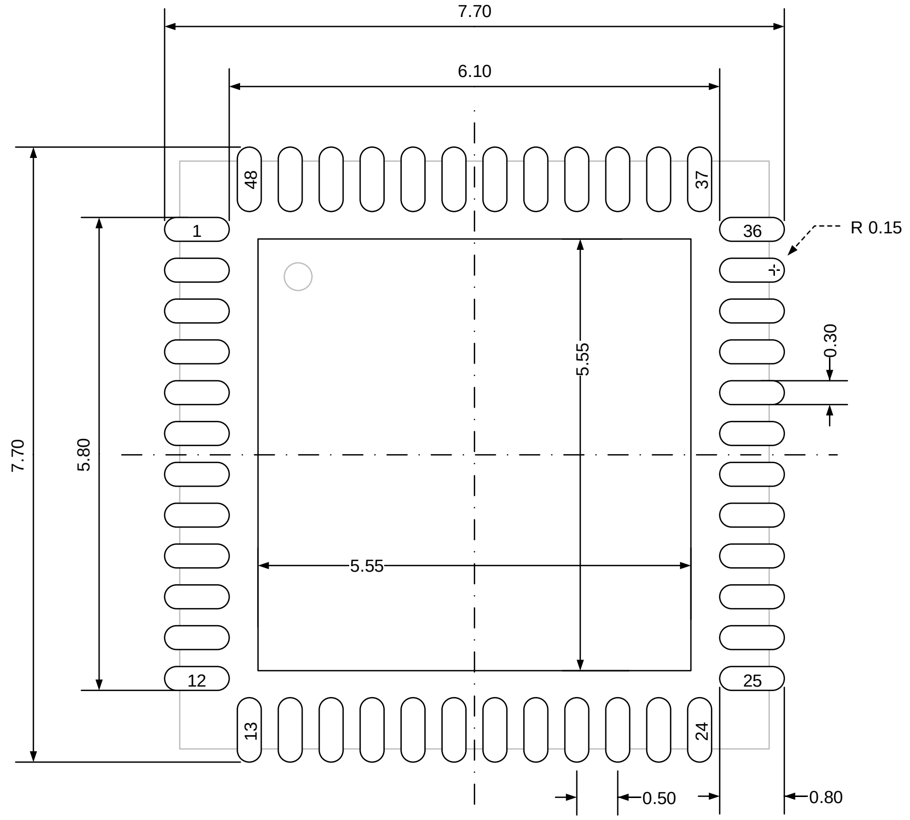


Table 5-2. QFN48 package dimensions

Symbol	Min	Typ	Max
A	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1	—	0.18	—
c	—	0.152	—
D	6.90	7.00	7.10
D2	5.50	5.60	5.70
E	6.90	7.00	7.10
E2	5.50	5.60	5.70
e	—	0.50	—
K	—	0.30	—
L	0.35	0.40	0.45
L1	0	0.05	0.10
h	0.30	0.35	0.40
Nd	—	5.50	—
Ne	—	5.50	—

(Original dimensions are in millimeters)

Figure 5-4. QFN48 recommended footprint



(Original dimensions are in millimeters)

5.3 LQFP32 package outline dimensions

Figure 5-5. LQFP32 package outline

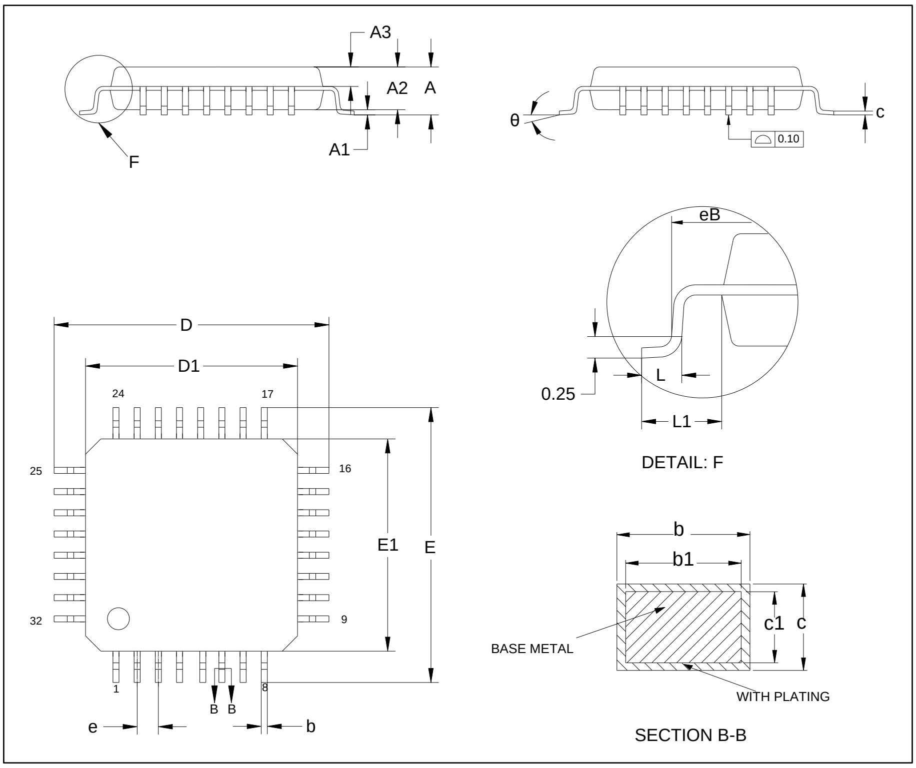
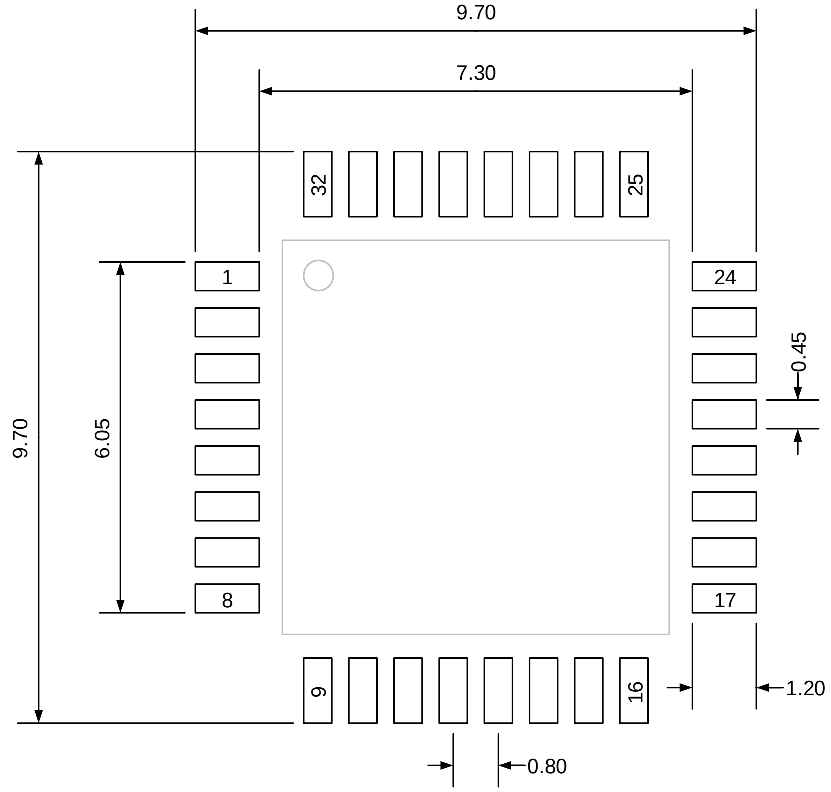


Table 5-3. LQFP32 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.33	—	0.41
b1	0.32	0.35	0.38
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	—	0.80	—
eB	8.10	—	8.25
L	0.45	—	0.75
L1	—	1.00	—
θ	0°	—	7°

(Original dimensions are in millimeters)

Figure 5-6. LQFP32 recommended footprint



(Original dimensions are in millimeters)

5.4 QFN32 package outline dimensions

Figure 5-7. QFN32 package outline

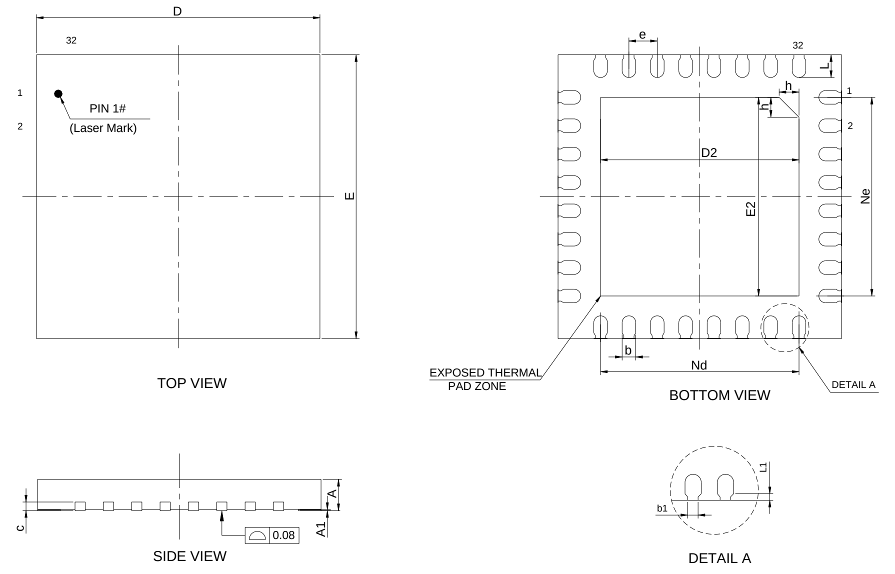
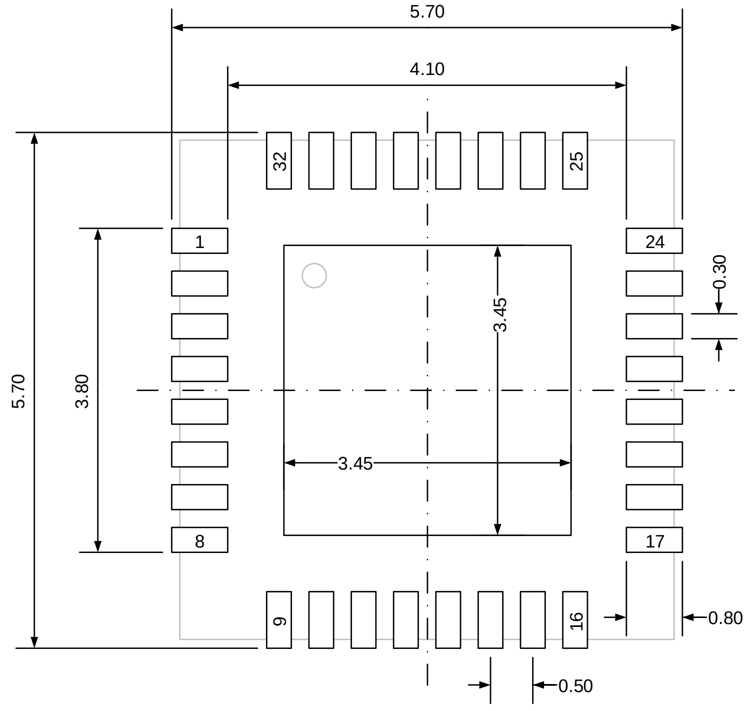


Table 5-4. QFN32 package dimensions

Symbol	Min	Typ	Max
A	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.18	0.25	0.30
b1	—	0.16	—
c	—	0.152	—
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
e	—	0.50	—
h	0.30	0.35	0.40
L	0.35	0.40	0.45
L1	—	0.10	—
Nd	—	3.50	—
Ne	—	3.50	—

(Original dimensions are in millimeters)

Figure 5-8. QFN32 recommended footprint



(Original dimensions are in millimeters)

5.5 QFN28 package outline dimensions

Figure 5-9. QFN28 package outline

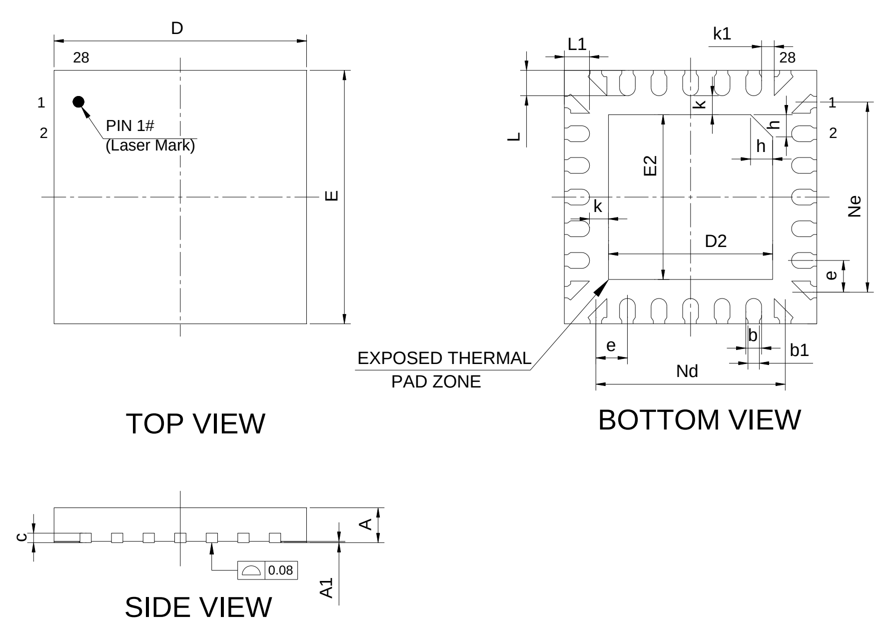
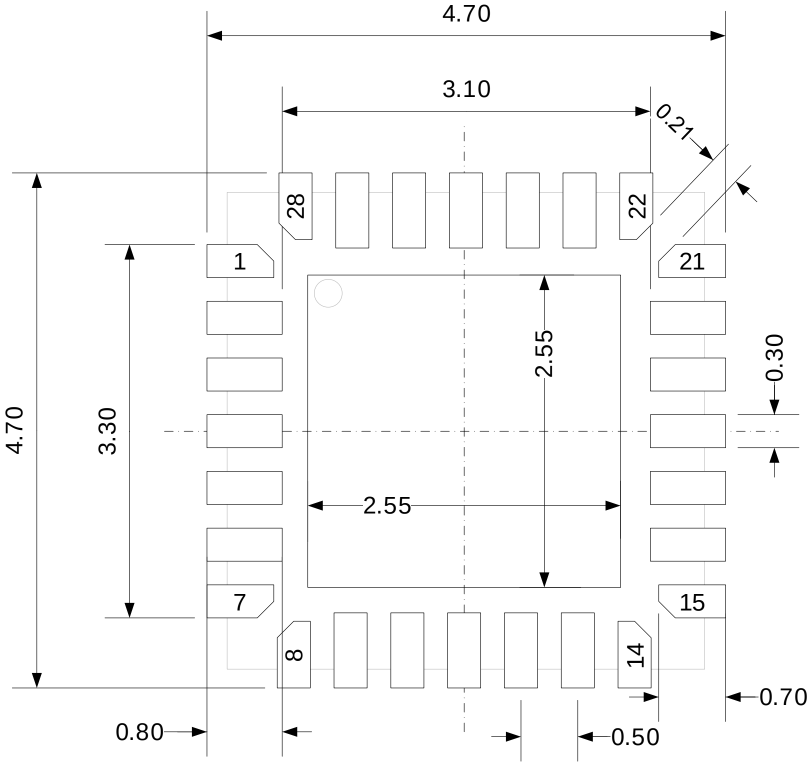


Table 5-5. QFN28 package dimensions

Symbol	Min	Typ	Max
A	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1	—	0.18	—
c	—	0.152	—
D	3.90	4.00	4.10
D2	2.50	2.60	2.70
E	3.90	4.00	4.10
E2	2.50	2.60	2.70
e	—	0.50	—
h	0.30	0.35	0.40
L	0.35	0.40	0.45
L1	—	0.35	—
k	—	0.30	—
k1	—	0.20	—
Nd	—	3.00	—
Ne	—	3.00	—

(Original dimensions are in millimeters)

Figure 5-10. QFN28 recommended footprint



(Original dimensions are in millimeters)

5.6 TSSOP20 package outline dimensions

Figure 5-11. TSSOP20 package outline

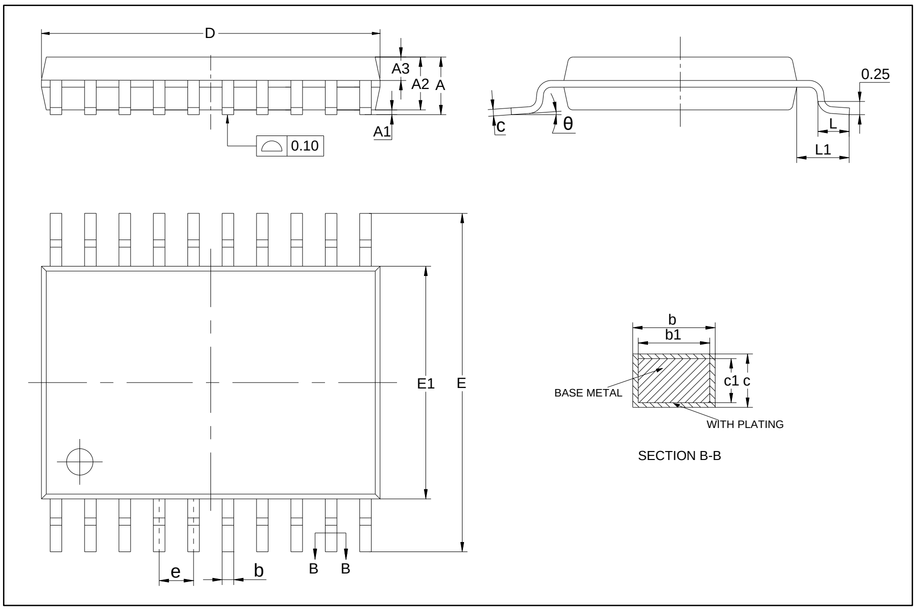
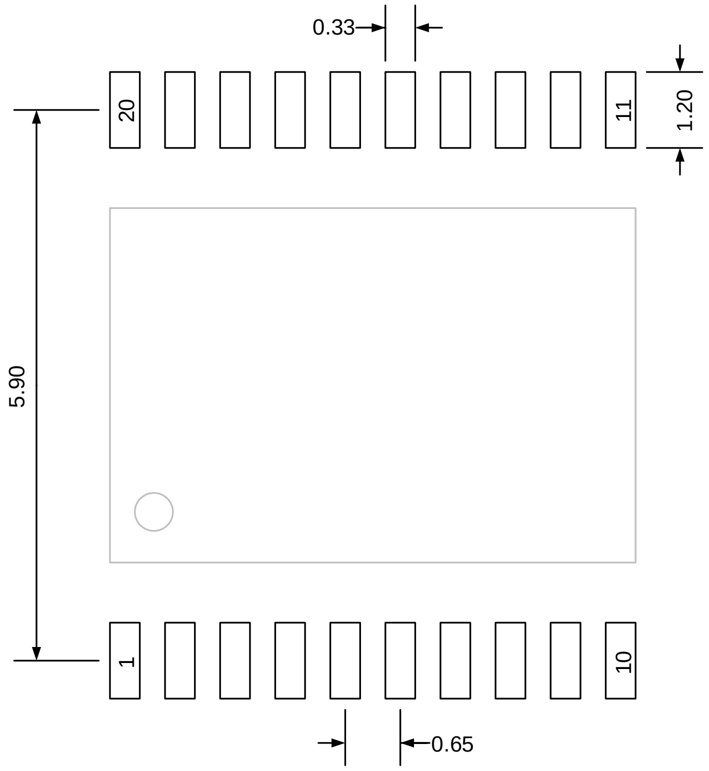


Table 5-6. TSSOP20 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.28
b1	0.19	0.22	0.25
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	—	0.65	—
L	0.45	0.60	0.75
L1	—	1.00	—
θ	0°	—	8°

(Original dimensions are in millimeters)

Figure 5-12. TSSOP20 recommended footprint



(Original dimensions are in millimeters)

5.7 LGA20 package outline dimensions

Figure 5-13. LGA20 package outline

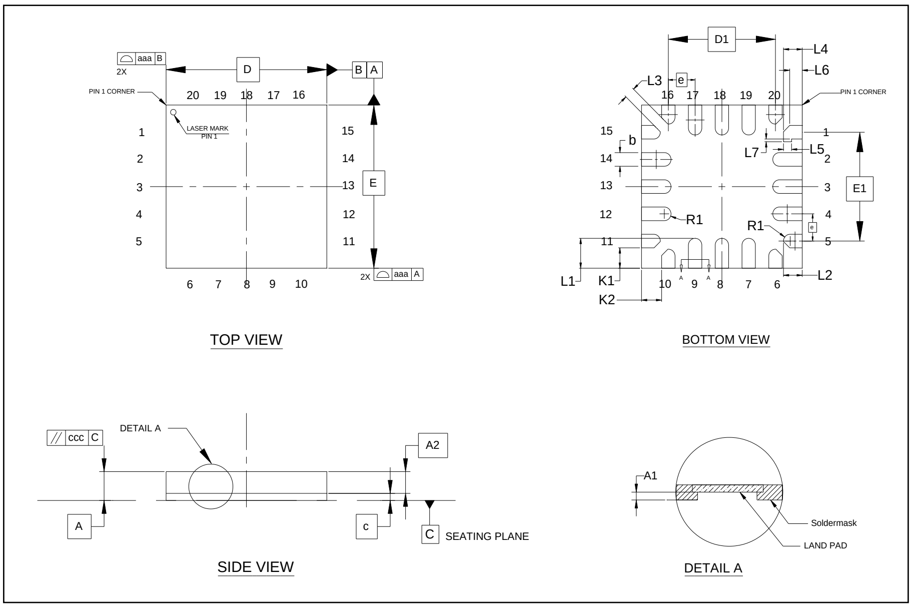
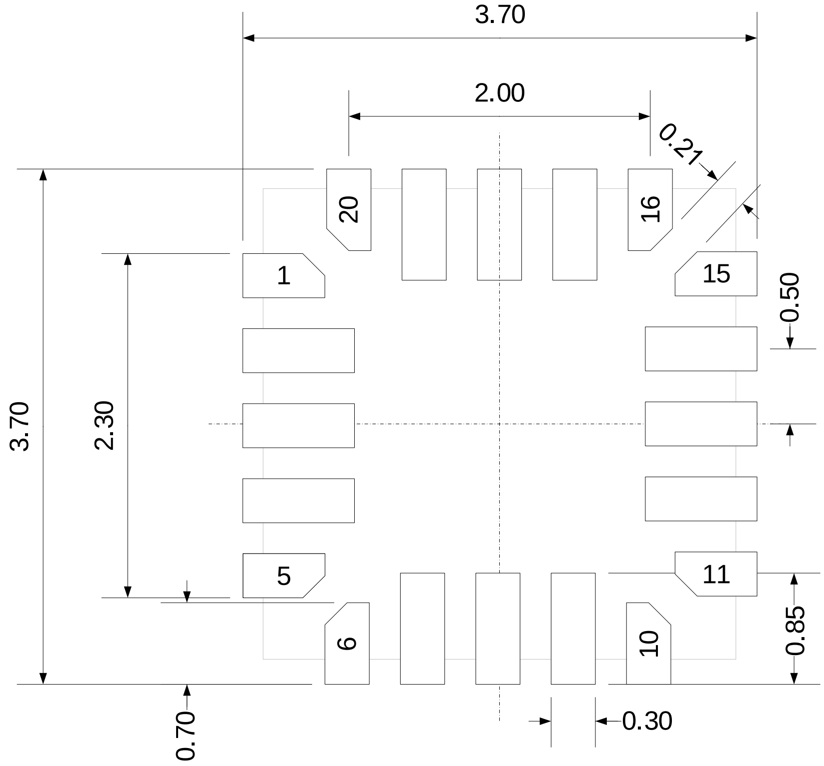


Table 5-7. LGA20 package dimensions

Symbol	Min	Typ	Max
A	0.51	0.56	0.61
A1	—	0.015	0.022
A2	0.35	0.40	0.45
b	0.20	0.25	0.30
c	0.13	0.16	0.19
D	2.90	3.00	3.10
D1	1.95	2.00	2.05
E	2.90	3.00	3.10
E1	1.95	2.00	2.05
e	—	0.50	—
K1	—	0.375	—
K2	—	0.375	—
L1	0.50	0.55	0.60
L2	0.30	0.35	0.40
L3	—	0.20	—
L4	0.30	0.35	0.40
L5	—	0.125	—
L6	—	0.234	—
L7	—	0.05	—
R1	—	0.125	—
aaa	—	0.10	—
ccc	—	0.08	—

(Original dimensions are in millimeters)

Figure 5-14. LGA20 recommended footprint



(Original dimensions are in millimeters)

5.8 Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter “θ”. For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

θ_{JA}: Thermal resistance, junction-to-ambient.

θ_{JB}: Thermal resistance, junction-to-board.

θ_{JC}: Thermal resistance, junction-to-case.

Ψ_{JB}: Thermal characterization parameter, junction-to-board.

Ψ_{JT}: Thermal characterization parameter, junction-to-top center.

$$\theta_{JA}=(T_J-T_A)/P_D \tag{5-1}$$

$$\theta_{JB}=(T_J-T_B)/P_D \tag{5-2}$$

$$\theta_{JC}=(T_J-T_C)/P_D \tag{5-3}$$

Where, T_J = Junction temperature.

T_A = Ambient temperature

T_B = Board temperature

T_C = Case temperature which is monitoring on package surface

P_D = Total power dissipation

θ_{JA} represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower θ_{JA} can be considerate as better overall thermal performance. θ_{JA} is generally used to estimate junction temperature.

θ_{JB} is used to measure the heat flow resistance between the chip surface and the PCB board.

θ_{JC} represents the thermal resistance between the chip surface and the package top case. θ_{JC} is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

Table 5-8. Package thermal characteristics(1)

Symbol	Condition	Package	Value	Unit
θ_{JA}	Natural convection, 2S2P PCB	LQFP48	69.64	°C/W
		QFN48	28.60	
		LQFP32	66.11	
		QFN32	48.50	
		QFN28	66.07	
		TSSOP20	72.35	
		LGA20	96.08	

Symbol	Condition	Package	Value	Unit
θ_{JB}	Cold plate, 2S2P PCB	LQFP48	43.16	°C/W
		QFN48	6.10	
		LQFP32	42.66	
		QFN32	28.32	
		QFN28	32.52	
		TSSOP20	53.01	
		LGA20	58.46	
θ_{JC}	Cold plate, 2S2P PCB	LQFP48	25.36	°C/W
		QFN48	5.62	
		LQFP32	30.06	
		QFN32	24.07	
		QFN28	30.58	
		TSSOP20	25.05	
		LGA20	31.54	
Ψ_{JB}	Natural convection, 2S2P PCB	LQFP48	47.75	°C/W
		QFN48	5.95	
		LQFP32	43.18	
		QFN32	28.93	
		QFN28	32.55	
		TSSOP20	53.15	
		LGA20	58.61	
Ψ_{JT}	Natural convection, 2S2P PCB	LQFP48	2.45	°C/W
		QFN48	0.17	
		LQFP32	4.56	
		QFN32	3.33	
		QFN28	3.27	
		TSSOP20	1.93	
		LGA20	1.83	

(1) Thermal characteristics are based on simulation, and meet JEDEC specification.

6 Ordering information

Table 6-1. Part ordering code for GD32C231xx devices

Ordering code	Flash (KB)	Package	Package type	Temperature operating range
GD32C231C8T6	64	LQFP48	Green	Industrial -40°C to +85°C
GD32C231C8T7	64	LQFP48	Green	Industrial -40°C to +105°C
GD32C231C6T6	32	LQFP48	Green	Industrial -40°C to +85°C
GD32C231C8U6	64	QFN48	Green	Industrial -40°C to +85°C
GD32C231C6U6	32	QFN48	Green	Industrial -40°C to +85°C
GD32C231K8T6	64	LQFP32	Green	Industrial -40°C to +85°C
GD32C231K6T6	32	LQFP32	Green	Industrial -40°C to +85°C
GD32C231K8U6	64	QFN32	Green	Industrial -40°C to +85°C
GD32C231K8U7	64	QFN32	Green	Industrial -40°C to +105°C
GD32C231K6U6	32	QFN32	Green	Industrial -40°C to +85°C
GD32C231G8U6TR	64	QFN28	Green	Industrial -40°C to +85°C
GD32C231G8U7TR	64	QFN28	Green	Industrial -40°C to +105°C
GD32C231G6U6TR	32	QFN28	Green	Industrial -40°C to +85°C
GD32C231F8P6TR	64	TSSOP20	Green	Industrial -40°C to +85°C
GD32C231F8P7TR	64	TSSOP20	Green	Industrial -40°C to +105°C
GD32C231F6P6TR	32	TSSOP20	Green	Industrial -40°C to +85°C
GD32C231F8V6TR	64	LGA20	Green	Industrial -40°C to +85°C
GD32C231F6V6TR	32	LGA20	Green	Industrial -40°C to +85°C

7 Revision history

Table 7-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Apr.30, 2025
1.1	1. Change TIMER0_BRKIN2 to TIMER0_BRKIN1 in chaper ***2.6. Pin definition***. 2. Update ***Table 4-36. ADC accuracy at fADC = 24 MHz(1)(2)(3)***. 3. Add description of peripheral power consumption testing methods before ***Table 4-16. Peripheral current consumption characteristics(1)***.	Jun.03, 2025
1.2	1. Add GD32C231K8U7. 2. Update the ***Table 4-27.Flash memory characteristics(1)*** to add data at 105°C. 3. Change the maximum temperature of T_A in V_{REFINT} condition to 105°C in ***Table 4-32. Internal reference voltage characteristics(1)***. 4. Update ***Table 4-3. General operating conditions(1)***.	Jul.08, 2025
1.3	1. Add GD32C231C8T7 and GD32F8P7TR. 2. Modify the description of t_{PROG} from "Word programming time" to "Double Word programming time" in ***Table 4-27. Flash memory characteristics(1)***.	Jul.24, 2025
1.4	1. Update ***Table 4-3. General operating conditions (1)***. 2. Update ***Table 4-4. Power supply requirement characteristics (1)***. 3. Add note for ***Table 4-6. Wake-up times from power saving modes (1)(2)***. 4. Update ***Table 4-19. Component level ESD characteristics latch-up characteristics (1)***. 5. Update ***Table 4-33. Internal reference voltage calibration values***.	Dec.24, 2025
1.5	1. Update ***Table 4-3. General operating conditions (1)***. 2. Update ***Table 4-25. High speed internal clock (IRC48M) characteristics***. 3. Update ***Table 4-26. Low speed internal clock (IRC32K) characteristics***. 4. Update ***Table 4-27. Flash memory characteristics (1)***. 5. Update ***Table 6-1. Part ordering code for GD32C231xx devices***.	Jan.07, 2026
1.6	1. Modify the function description of PB6 in ***Table 2-10. GD32C231Fx TSSOP20 pin definitions*** and ***Table 2-11.***	Jan.23, 2026

Revision No.	Description	Date
	GD32C231Fx LGA20 pin definitions.	
1.7	1. Update ***Figure 2-1. GD32C231xx block diagram*** and ***Figure 2-9 GD32C231xx Clock Tree***. 2. Add the I2S0_MCK function in Section ***2.6. Pin definitions***. 3. Add support for the Flash ECC feature in Section ***3.2. Embedded memory***. 4. Change VDD_min from 2.3 V to 1.8 V and update corresponding voltages in Chapter 4. When using ADC, VDD_min = 2 V; when using COMP, VDD_min = 2.2 V. 5. In ***Table 4-4. Power supply requirement characteristics(1)***, remove the power up rate requirement for voltages below 2.3 V. 6. In ***Table 4-5. Start-up timings of Operating conditions(1)(2)(3)***, remove the start up time of HXTAL as clock source and update data for IRC48M as system clock. 7. In ***Table 4-6. Wake-up times from power saving modes (1)(2)***, update parameters for sleep mode wake up time. 8. Update parameters in Section ***4.7. Power consumption***. 9. In ***Table 4-19. Component level ESD characteristics latch-up characteristics (1)***, update LU temperature and grading. 10. In ***Table 4-21. High speed external clock (HXTAL) generated from a crystal/ceramic characteristics (1)***, change IDD(HXTAL) current from 2.2 mA to 3.2 mA. 11. In ***Table 4-26. Low speed internal clock (IRC32K) characteristics***, add information for IRC12M. 12. Modify GPIO low speed mode to 2 MHz and enhance high drive capability. 13. Update all I/O output voltage characteristics in ***Table 4-31. Output voltage characteristics for all I/Os (1)***. 14. Update I/O port AC characteristics in ***Table 4-32. I/O port AC characteristics (1)(2)(3)(4)***. 15. In ***Table 4-38. ADC accuracy at fADC = 24 MHz (1)(2)(3)***, add static and dynamic performance data for 5.5 V and 24 MHz. 16. In Table 4-44. ***Standard SPI Characteristics (1)***, update the relationship between SPI clock frequency and supply voltage.	Jun.15, 2026

Important Notice

This document is the property of GigaDevice Semiconductor Inc. and its subsidiaries (the "Company"). This document, including any product of the Company described in this document (the “Product”), is owned by the Company according to the laws of the People’s Republic of China and other applicable laws. The Company reserves all rights under such laws and no Intellectual Property Rights are transferred (either wholly or partially) or licensed by the Company (either expressly or impliedly) herein. The names and brands of third party referred thereto (if any) are the property of their respective owner and referred to for identification purposes only.

To the maximum extent permitted by applicable law, the Company makes no representations or warranties of any kind, express or implied, with regard to the merchantability and the fitness for a particular purpose of the Product, nor does the Company assume any liability arising out of the application or use of any Product. Any information provided in this document is provided only for reference purposes. It is the sole responsibility of the user of this document to determine whether the Product is suitable and fit for its applications and products planned, and properly design, program, and test the functionality and safety of its applications and products planned using the Product. The Product is designed, developed, and/or manufactured for ordinary business, industrial, personal, and/or household applications only, and the Product is not designed or intended for use in (i) safety critical applications such as weapons systems, nuclear facilities, atomic energy controller, combustion controller, aeronautic or aerospace applications, traffic signal instruments, pollution control or hazardous substance management; (ii) life-support systems, other medical equipment or systems (including life support equipment and surgical implants); (iii) automotive applications or environments, including but not limited to applications for active and passive safety of automobiles (regardless of front market or aftermarket), for example, EPS, braking, ADAS (camera/fusion), EMS, TCU, BMS, BSG, TPMS, Airbag, Suspension, DMS, ICMS, Domain, ESC, DCDC, e-clutch, advanced-lighting, etc.. Automobile herein means a vehicle propelled by a self-contained motor, engine or the like, such as, without limitation, cars, trucks, motorcycles, electric cars, and other transportation devices; and/or (iv) other uses where the failure of the device or the Product can reasonably be expected to result in personal injury, death, or severe property or environmental damage (collectively "Unintended Uses"). Customers shall take any and all actions to ensure the Product meets the applicable laws and regulations. The Company is not liable for, in whole or in part, and customers shall hereby release the Company as well as its suppliers and/or distributors from, any claim, damage, or other liability arising from or related to all Unintended Uses of the Product. Customers shall indemnify and hold the Company, and its officers, employees, subsidiaries, affiliates as well as its suppliers and/or distributors harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of the Product.

Information in this document is provided solely in connection with the Product. The Company reserves the right to make changes, corrections, modifications or improvements to this document and the Product described herein at any time without notice. The Company shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. Information in this document supersedes and replaces information previously supplied in any prior versions of this document.