GigaDevice Semiconductor Inc.

GD32C2x1 Hardware Development Guide

Application Note

AN240

Revision 1.2

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1. Introduction

The article is specially provided for developers of 32-bit general-purpose MCU GD32C2x1 series based on Arm® Cortex®-M23 architecture. It provides an overall introduction to the hardware development of GD32C2x1 series products, such as power supply, reset, clock, boot mode settings and download debugging. The purpose of this application notes is to allow developers to quickly get started and use GD32C2x1 series products, and quickly develop and use product hardware, save the time of studying manuals, and speed up product development progress.

This application note is divided into seven parts to describe:

1. Power supply, mainly introduces the design of GD32C2x1 series power management, power supply and reset functions.
2. Power Detection and Reset, Mainly introduces the functional design of power detection and reset in the GD32C2x1 series.
3. Clock, mainly introduces the functional design of GD32C2x1 series high and low speed clocks.
4. Boot configuration, mainly introduces the BOOT configuration and design of GD32C2x1 series.
5. Typical peripheral modules, mainly introduces the hardware design of the main functional modules of the GD32C2x1 series.
6. Download and debug circuit, mainly introduces the recommended typical download and debug circuit of GD32C2x1 series.
7. Reference circuit and PCB Layout design, mainly introduces GD32C2x1 series hardware circuit design and PCB Layout design notes.
8. Package description, mainly introduces the package forms and names included in the GD32C2x1 series.

This document also satisfies the minimum system hardware resources used in application development based on GD32C2x1 series products.

Table 1-1. Applicable Products

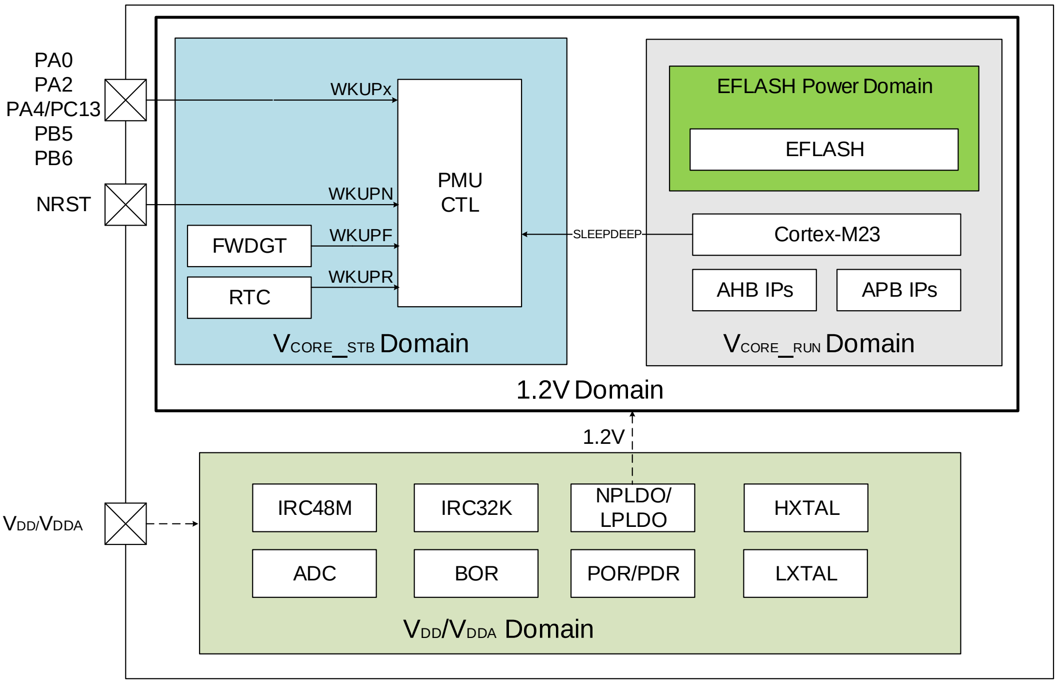
Type	Part Numbers
MCU	GD32C231xx series
	GD32C221xx series
	GD32C211xx series

2. Hardware design

2.1. Power supply

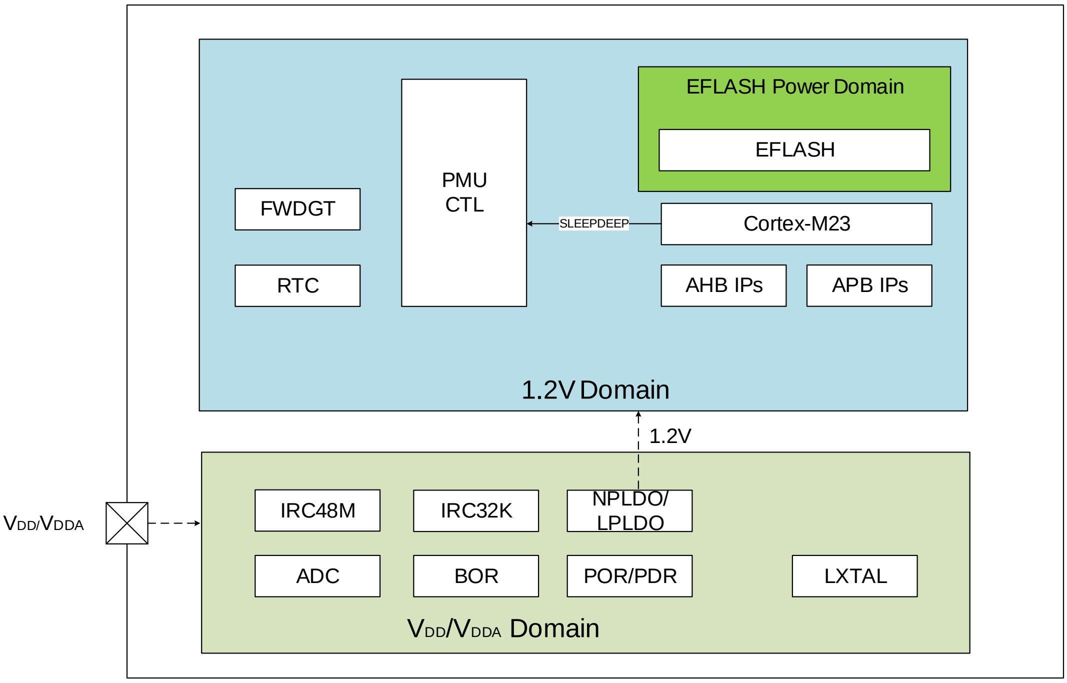
The V_{DD} / V_{DDA} operating voltage range of GD32C2x1 series products is 2.3 V ~ 5.5V. For GD32C2x1 series, there are three power domains, including V_{DD} / V_{DDA} domain, 1.2V domain, and Backup domain, as is shown in ***Figure 2-1. GD32C231 / GD32C221 Power supply overview*** and ***Figure 2-2. GD32C211 Power supply overview***. There are two power domains, including V_{DD}/V_{DDA} domain and 1.2V domain. The power of the V_{DD}/V_{DDA} domain is supplied directly. An embedded LDO in the V_{DD}/V_{DDA} domain is used to supply the 1.2V domain power.

Figure 2-1. GD32C231 / GD32C221 Power supply overview



POR: Power On Reset PDR: Power Down Reset BOR: Brownout Reset
NPLDO: Normal power Voltage Regulator LPLDO: Low power Voltage Regulator

Figure 2-2. GD32C211 Power supply overview



POR: Power On Reset PDR: Power Down Reset

NPLDO: Normal power Voltage Regulator LPLDO: Low power Voltage Regulator

2.1.1. V_{DD}/V_{DDA} domain

V_{DD} / V_{DDA} domain includes HXTAL (high speed crystal oscillator. The GD32C211 devices only supports external high-speed clock input.), LXTAL (low speed crystal oscillator), NPLDO, LPLDO, POR/PDR (power on/down Reset), BOR (Brownout Reset), ADC (A/D converter), IRC48M (internal 48MHz RC oscillator), IRC32K (internal 32KHz RC oscillator) etc.

In order to improve the conversion accuracy of the ADC, the VREFP pin is individually brought out on the 48-pin package to provide a reference power supply for the ADC.

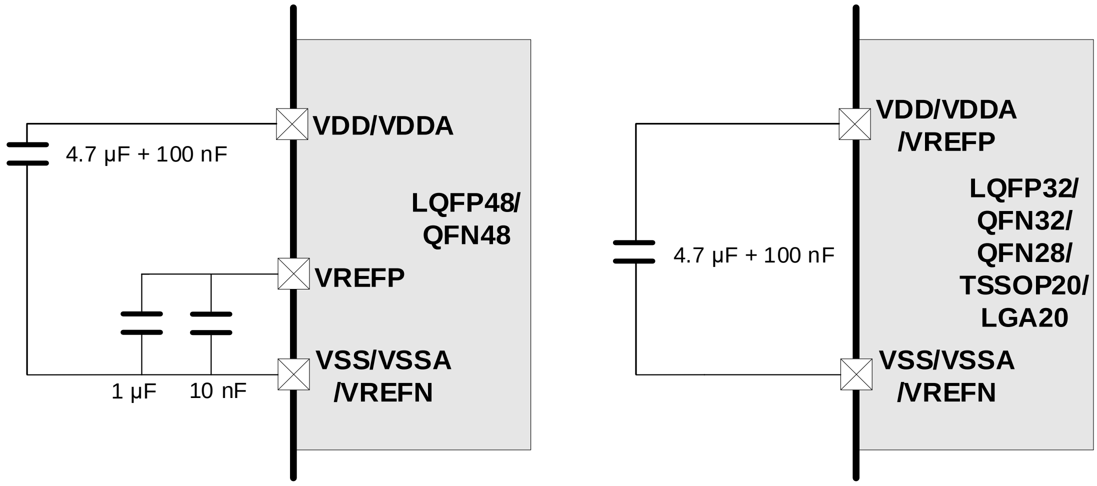
- The package chip with 48 pins contains VREFP, and V_{REFP} can use an external reference power supply, or can be directly connected to V_{DD}/V_{DDA}.
- The package chip less than 48 pins has no VREFP pin, V_{REFP} is internally connected directly to V_{DD}/V_{DDA}.

2.1.2. Power supply design

The system needs a stable power supply. There are some important things to pay attention to when developing and using:

- The VDD/VDDA pin must be connected with an external capacitor (100nF ceramic capacitor + not less than 4.7uF tantalum capacitor).
- The VREFP pin can be generated internally or directly connected to VDD/VDDA, and a 10nF+1uF ceramic capacitor should be connected between the VREFP pin and ground.

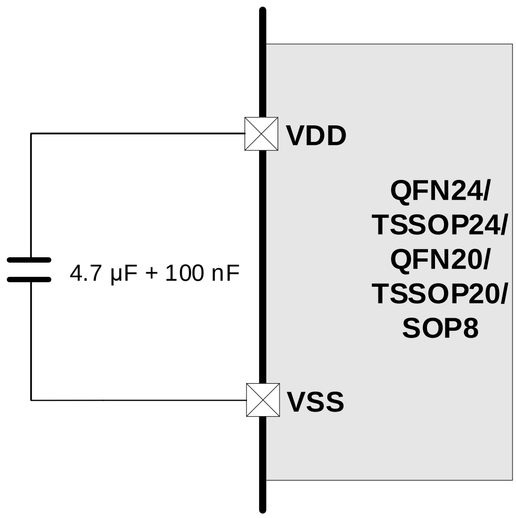
Figure 2-3. GD32C231 / GD32C221 Recommended Power Supply Design



Note:

1. All decoupling capacitors need to be as close as possible to the pins on the PCB board.
2. When the MCU power supply voltage is unstable or there is a risk of voltage drop, it is recommended to adjust the 4.7uF capacitor not less than 10uF.
3. LQFP48: VSS, VSSA, VREFN are connected internally, VDD and VDDA are connected internally.
4. QFN48: VSS, VSSA, VREFN are connected with EPAD internally, VDD and VDDA are connected internally.
5. LQFP32: VSS, VSSA, VREFN are connected internally, VREFP, VDD and VDDA are connected internally.
6. QFN32: VSS, VSSA, VREFN are connected with EPAD internally, VREFP, VDD and VDDA are connected internally.
7. TSSOP20: VSS, VSSA, VREFN are connected internally, VREFP and VDDA are connected internally.
8. LGA20: VSS, VSSA, VREFN are connected internally, VREFP and VDDA are connected internally.

Figure 2-4. GD32C211 Recommended Power Supply Design



Note:

1. All decoupling capacitors need to be as close as possible to the pins on the PCB board.
2. When the MCU power supply voltage is unstable or there is a risk of voltage drop, it is recommended to adjust the 4.7uF capacitor not less than 10uF.
3. QFN24: VSS and VREFN are connected with EPAD internally, VDD and VREFP are connected internally.
4. TSSOP24: VSS and VREFN are connected internally, VDD and VREFP are connected internally.
5. QFN20: VSS and VREFN are connected internally, VDD and VREFP are connected internally.
6. TSSOP20: VSS and VREFN are connected internally, VDD and VREFP are connected internally.
7. SOP8: VSS and VREFN are connected internally, VDD and VREFP are connected internally.

2.2. Power supply detection and reset

The reset control of the GD32C231xx / GD32C221xx series includes three types of resets: power-on reset, system reset, and backup register reset. The reset control of the GD32C211xx series includes three control methods: power-on reset, system reset, and RTC reset. The power-on reset is a cold reset. For the GD32C231xx / GD32C221xx series, the power-on reset resets all registers except those in the backup domain, while for the GD32C211 series, the power-on reset resets all registers. During the power-on and system reset process, the NRST pin remains at a low level until the reset is complete. If the MCU fails to execute properly, the waveform of the NRST pin can be monitored using an oscilloscope to determine whether the chip is continuously experiencing reset events.

In addition, the MCU reset source can be searched by the register RCU_RSTSCK (0x40021024). This register can only clear the flag bit after power-on reset. Therefore, during use, after the reset source is obtained, the reset flag can be cleared through the RSTFC control bit, so that a watchdog reset or other reset events can be more accurately reflected in the RCU_RSTSCK register:

Figure 2-5. RCU_RSTSCK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LPRSTF	WWDGTRSTF	FWDGTRSTF	SWRSTF	PORRSTF	EPRSTF	BORRSTF	RSTFC	OBLRSTF	保留						
r	r	r	r	r	r	r	rw	r							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
保留														IRC32KSTB	IRC32KEN
														r	rw

MCU integrates a power-up / power-down reset circuit, when a reset occurs, the system reset pulse generator ensures that each reset source (external or internal) can have a low level pulse delay of at least 20μs. To prevent a false trigger reset, the NRST pin is recommended to place a capacitor (typically 100nF).

Figure 2-6. System Reset Circuit of GD32C231xx / GD32C221xx Series

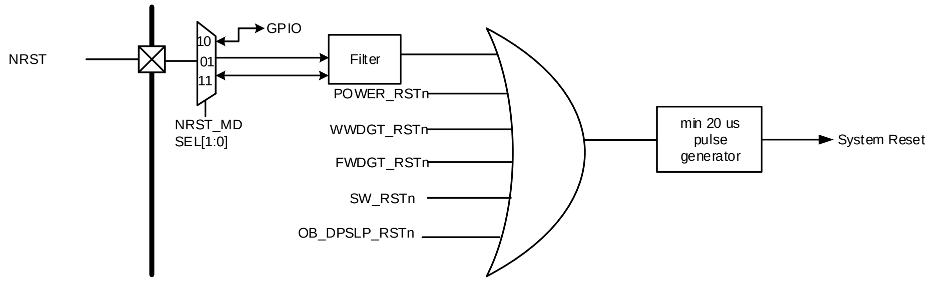
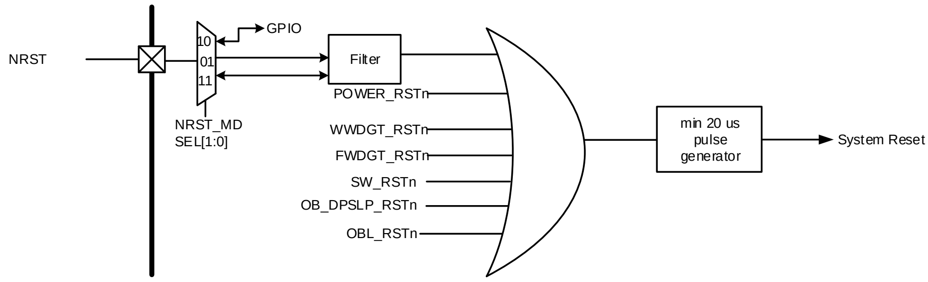


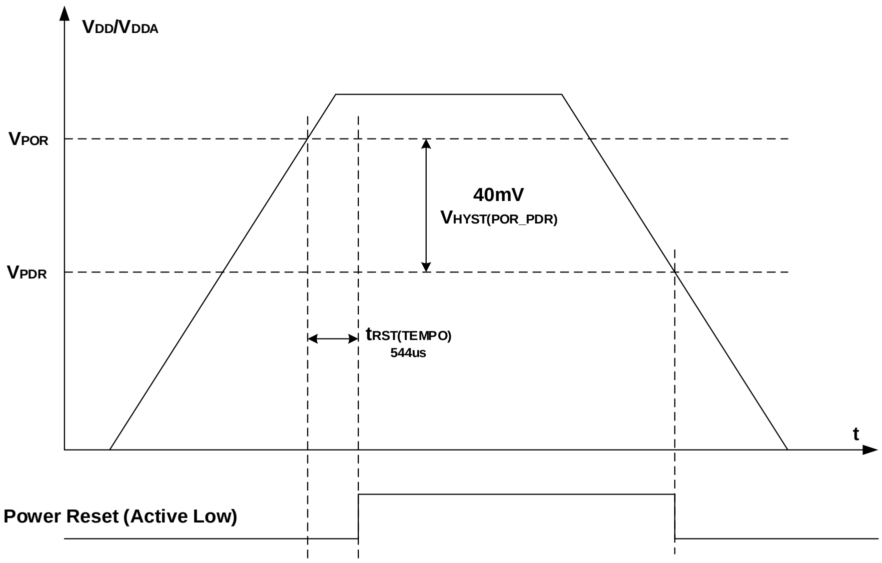
Figure 2-7. System Reset Circuit of GD32C211xx Series



2.2.1. POR / PDR

The chip integrates a POR/PDR (power-on/power-down reset) circuit to detect V_{DD}/V_{DDA} and generate a power reset signal to reset the entire chip except the V_{CORE_STB} domain when the voltage is lower than a certain threshold. V_{POR} is the threshold voltage of power-on reset. V_{PDR} is the threshold voltage of power-down reset. The value of the hysteresis voltage $V_{HYST(POR\_PDR)}$ of the GD32 C2x1 series is about 40 mV.

Figure 2-8. Power-on/power-down reset waveforms



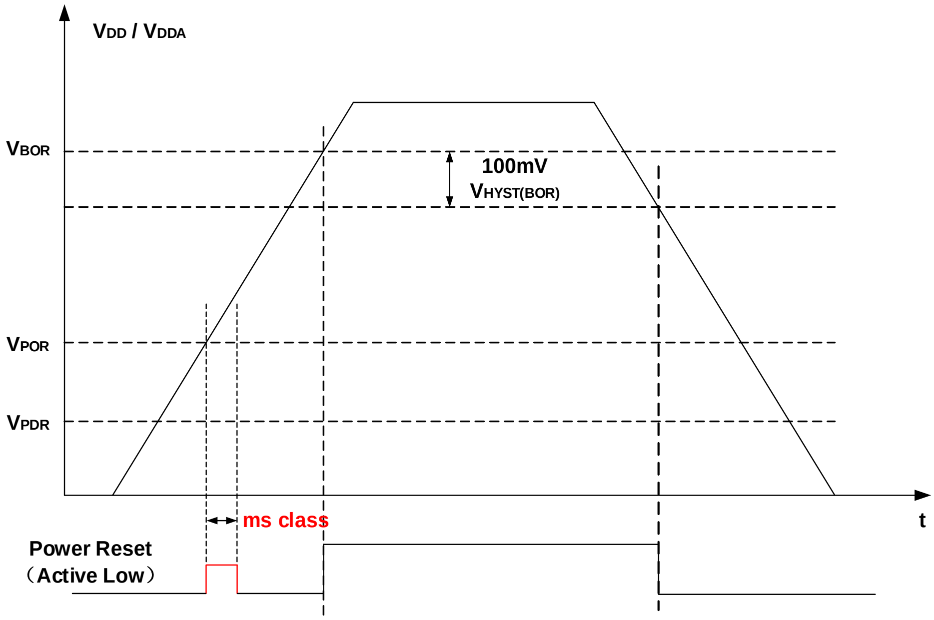
During system power-on, when V_{DD} rises to V_{POR}, a power reset is triggered after a delay of $t_{RST(TEMPO)}$. Before the power reset releases to high, V_{DD} must rise to V_{DD_MIN} to ensure proper system operation. During system power off, when V_{DD} drops to V_{PDR}, the power reset is asserted and held low.

Since V_{DD_MIN} (2.3V) and $V_{POR/VPDR}$ (Approximately1.6V) have a wide voltage gap, the system may enter an undefined state if V_{DD} falls between V_{POR} / V_{PDR} and V_{DD_MIN} with NRST high. To avoid this risk, users can enable BOR by configuring the option byte BORST_EN and set the BOR threshold near V_{DD_MIN}.

2.2.2. BOR

The GD32C2x1 series MCU also integrates a BOR circuit. The BOR circuit is used to detect V_{DD}/V_{DDA} and generate the power reset signal which resets the whole chip except the V_{CORE_STB} domain when the supply voltage is lower than the specified threshold which defined in the BOR_TH bits in option bytes. Notice that the POR/PDR circuit is always implemented. BOR is enabled by setting BORST_EN bit in option bytes. ***Figure 2-9. BOR Threshold Waveform*** shows the relationship between the supply voltage and the BOR reset signal. V_{BORR} and V_{BORF} indicates the threshold of BOR on reset, which defined in the BORR_TH and BORF_TH bits in option bytes. The value of the hysteresis voltage $V_{HYST(BOR)}$ is 100mV.

Figure 2-9. BOR Threshold Waveform



The BOR threshold is set through the option byte BORR_TH and BORF_TH, and can set four different levels. Additionally, the voltage fluctuation reset can be disabled through BORST_EN configuration. In this case, the power-on reset is defined by the POR/PDR level. Refer to the following table for the corresponding relationship.

Table 2-1. V_{BOR} Threshold Voltage Setting

Symbol	Conditions	Typ	
		GD32C231 GD32C231	GD32C211
BORF_TH=BORR_TH =11(BOR level4)	Rising edge	2.90 V	2.90 V
	Falling edge	2.80 V	2.80 V
BORF_TH=BORR_TH =10(BOR level3)	Rising edge	2.60 V	2.60 V
	Falling edge	2.50 V	2.50 V
BORF_TH=BORR_TH =01(BOR level2)	Rising edge	2.30 V	2.30 V
	Falling edge	2.20 V	2.20 V
BORF_TH=BORR_TH=00(BOR level1)	Rising edge	2.10 V	2.10 V
	Falling edge	2.00 V	2.00 V
BORST_EN =0 (BOR off, POR and PDR)	Rising edge	1.633 V	1.62 V
	Falling edge	1.593 V	1.58 V

Regardless of whether BOR is enabled or not, the POR/PDR (power-on/power-off reset) circuit is always in the detection state. Therefore, the power reset level will be pulled high once V_{DD}/V_{DDA} rises to VPOR. After loading the option bytes to enable BOR, the power reset will be quickly pulled low until V_{DD}/V_{DDA} rises to VBOR set by the option byte BORR_TH, at which point the power reset level will be pulled high again.

That is, when V_{DD}/V_{DDA} rises the edge, the NRST pin voltage will have a pulse when V_{DD}/V_{DDA} reaches VPOR. The duration of the pulse is ms class. The pulse will not affect the normal operation of the chip, which is shown in the red pulse in the waveform diagram of the ***Figure***

2-9. BOR Threshold Waveform.

2.2.3. NRST Pin

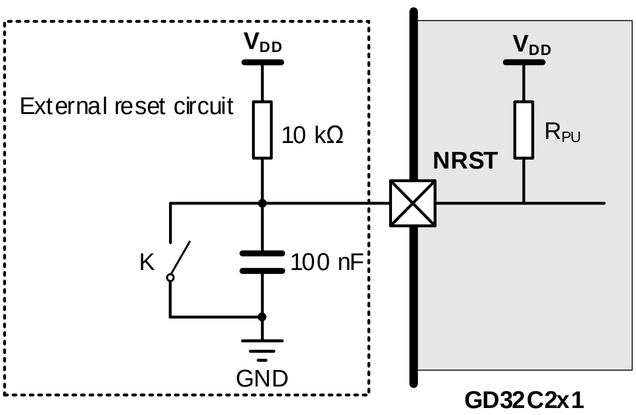
The NRST pin has three modes, which can be selected through the NRST_MDSEL[1:0] bits in the FMC_OBCTL option byte control register.

1. Input/output mode(default mode): the GPIO function of the NRST pin is not available in this mode. The reset signal can be transferred from the NRST pin to the device, causing the device to reset, the reset pulse signal can be reflected through the NRST pin, and the minimum reset pulse duration is 20 μs.
2. Input mode: the GPIO function of the NRST pin is not available in this mode, the reset signal can be transferred from the NRST pin to the device, causing the device to reset, but the internal reset of the device is not visible at the NRST pin.
3. GPIO mode: NRST pin can only function as standard GPIO, reset function is not available, reset signal is only inside the device, not reflected in NRST pin.

The option bytes are reloaded and take effect on every power-on reset or when the OBRLD bit in the FMC_CTL register is set to 1. Before the option bytes are loaded and take effect, the NRST pin functions in its default NRST reset mode. If the NRST pin is configured as a GPIO input, the user should avoid applying an external low-level signal to this pin before the option bytes are loaded and take effect; otherwise, the system will remain in reset state and fail to operate normally.

For the NRST pin of the MCU, it is recommended to place a capacitor (typically 100 nF) in the NRST pins to prevent a false trigger reset.

Figure 2-10. Recommend External Reset Circuit



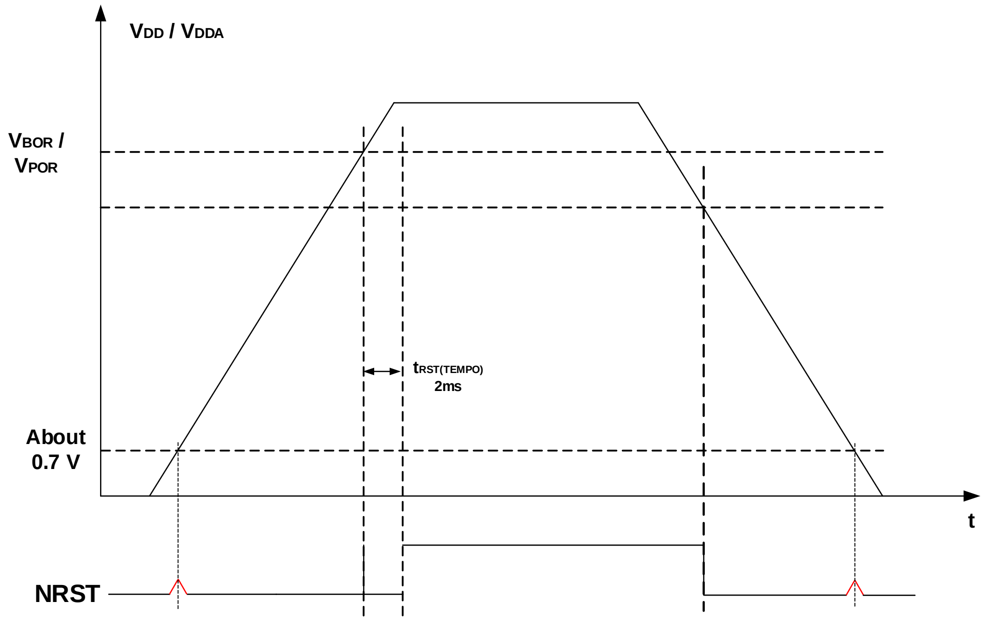
Note:

1. The pull-up resistor is recommended to be 10kΩ, so that voltage interference will not cause the chip to work abnormally.
2. If the influence of static electricity is considered, an ESD protection diode can be placed at the NRST pin.
3. Although there is a hardware POR circuit inside the MCU, it is still recommended to add an external NRST reset resistor-capacitor circuit.

4. If the MCU starts abnormally (due to voltage fluctuations, etc.), the capacitance value of NRST to ground can be appropriately increased, and the MCU reset completion time can be extended to avoid the abnormal power-on sequence area.
5. For the GD32C211 series in SOP8 package, the four I/O pads (PA0, PA1, PA2, and NRST-PC2) are simultaneously bonded to Pin 4, which is configured for NRST function by factory default. Users can configure Pin 4 for other I/O functions by setting the option byte FMC_OBCTL NRST_MDSEL[1:0] = 10 and then configuring SYSCFG_CFG3_PINMUX1. Before the option bytes are loaded and take effect, the user should avoid applying an external low-level signal to Pin 4. Otherwise, the chip will remain in reset state and fail to operate normally.

Due to the threshold voltage characteristics of MOS transistors, during the power-up and power-down process of the chip, when V_{DD}/V_{DDA} is less than 0.7V, the internal pull-down MOS transistor of the chip will not pull the NRST pin low. In other words, during the power-up and power-down process, when V_{DD}/V_{DDA} is approximately 0.7V, a small pulse may occur, which does not affect the normal operation of the chip. This is illustrated by the red pulse shown in *Figure 2-11. NRST Pin Power-On/Power-Down MOSFET Pulse Diagram*.

Figure 2-11. NRST Pin Power-On/Power-Down MOSFET Pulse Diagram



Due to the difference in charging and discharging speeds, the duration of the pulse on the falling edge is slightly longer than on the rising edge, with both durations being in the millisecond range.

2.3. Clock

GD32C2x1 series has a complete clock system inside, and you can choose a suitable clock source according to different applications. The main features of the clock for GD32C231/ GD32C221 Series:

- 4-48 MHz external high-speed crystal oscillator (HXTAL)
- Internal 48 MHz RC oscillator (IRC48M)
- 32.768 kHz external low-speed crystal oscillator (LXTAL)
- Internal 32 kHz RC oscillator (IRC32K)
- HXTAL and LXTAL clock monitor

Due to the multiplexing of the PC14-OSC32IN/OSCEXTIN pin functions in the GD32C211 series, OSCEXTIN and LXTAL cannot be used simultaneously. Main Features of Clock for GD32C211 Series:

- 4-48 MHz external high-speed driven clock (OSCEXTIN)
- Internal 48 MHz RC oscillator (IRC48M)
- 32.768 kHz external low-speed crystal oscillator (LXTAL)
- Internal 32 kHz RC oscillator (IRC32K)
- HXTAL and LXTAL clock monitor

Figure 2-12. Clock tree of GD32C231 / GD32C221 devices

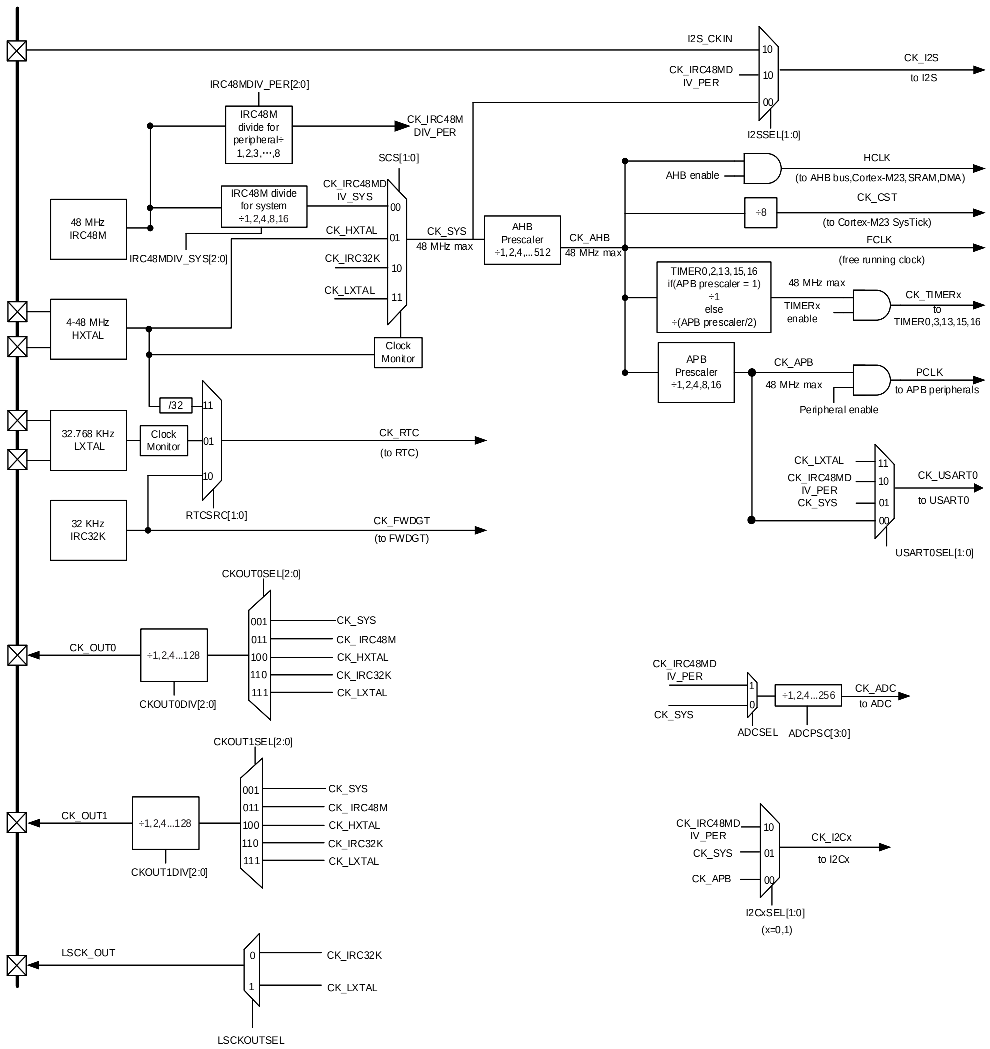
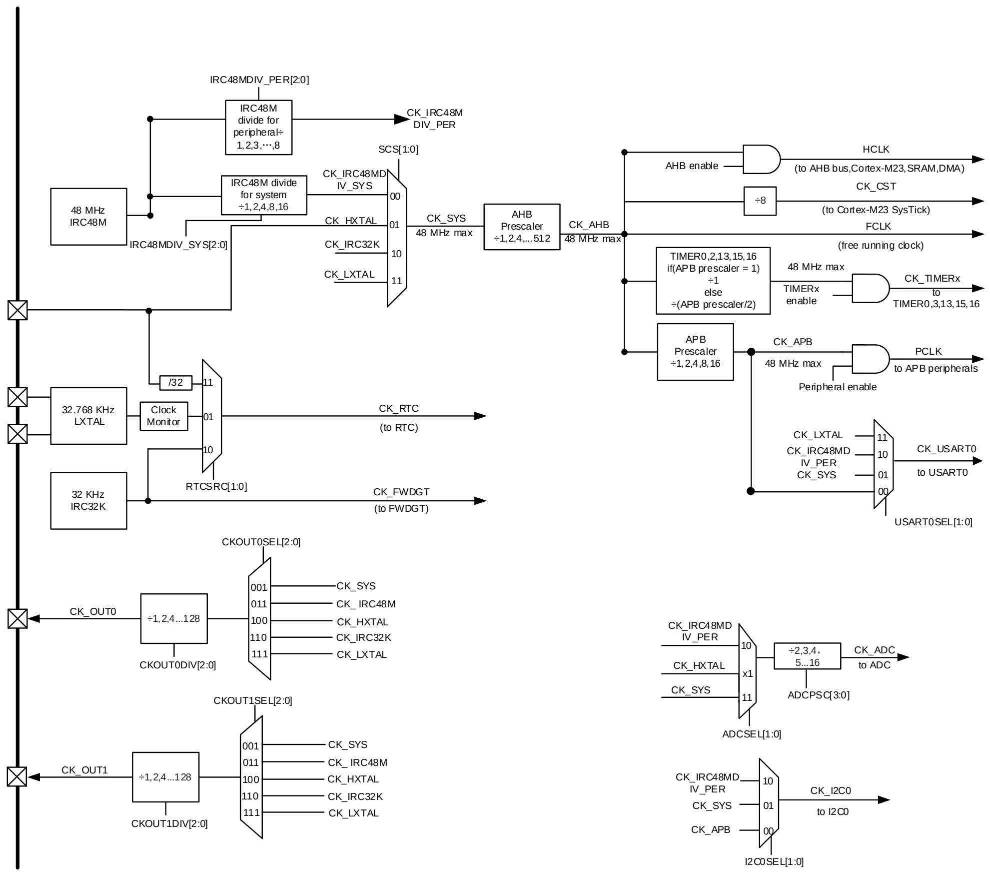


Figure 2-13. Clock tree of GD32C211 devices



2.3.1. External high-speed crystal oscillator clock (HXTAL)

For the GD32C231/GD32C221 devices, a 4-48MHz external high-speed crystal oscillator (passive crystal) can provide an accurate main clock for the system. For the GD32C211 series, only external high-speed clock input is supported, such as receiving an input clock from the host as a slave device or using an active crystal oscillator as the clock source. The following description applies only to the GD32C231/GD32C221 devices.

The crystal of a specific frequency must be placed close to the HXTAL pins, and the external resistors and matching capacitors connected to the crystal must be adjusted based on the oscillator parameters selected. HXTAL can also operate in bypass input mode to accept a clock source (such as a 1-50MHz active crystal oscillator). In bypass input mode, the clock signal is input through the OSCIN pin, and the software needs to configure the HXTALBPS bit in the RCU_CTL register to enable the bypass function of HXTAL. When HXTAL operates in bypass mode, the OSCOUT pin can either be left floating or configured as GPIO or OSCEN functionality. The OSCEN functionality can provide a clock enable signal to the external clock source, allowing the MCU to request the external clock source to stop when entering low-power mode, thereby reducing system power consumption.

For those packages that lead out the PF0-OSCIN and PF1-OSCOUT pins, the HXTAL clock source defaults to using the PF0-OSCIN and PF1-OSCOUT pins. It can also be remapped to the PC14-OSCXIN and PC15-OSCXOUT pins by setting the HXTAL_REMAP bit in the FMC_OBCTL option byte control register to 0, enabling the HXTAL remapping function. For those packages that do not lead out the PF0-OSCIN and PF1-OSCOUT pins, the HXTAL clock source defaults to using the PC14-OSCXIN and PC15-OSCXOUT pins. As a result, the PC14-OSCXIN and PC15-OSCXOUT pins are shared between HXTAL and LXTAL clock sources, meaning the two clock sources can not be used simultaneously.

Figure 2-14. HXTAL External Crystal Circuit

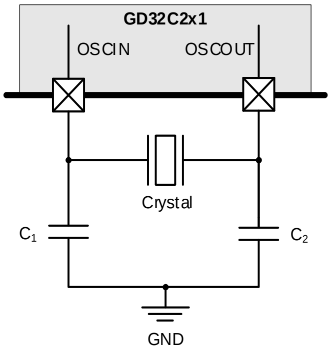
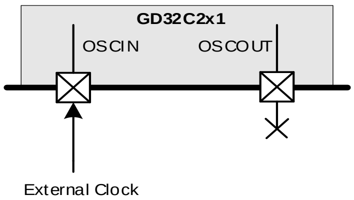


Figure 2-15. HXTAL External Clock Circuit



Note:

1. When using the bypass input, the signal is input from OSCIN, and OSCOUT remains floating.
2. For the size of the external matching capacitor, please refer to the formula: $C_1 = C_2 = 2*(C_{LOAD} - C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, with a typical value of 10pF. When it is recommended to use an external high-speed crystal, try to choose a crystal load capacitance of about 20pF, so that the external matching capacitors C_1 and C_2 can be 20pF, and the PCB layout should be as close to the crystal pin as possible.
3. C_S is the parasitic capacitance on the PCB board traces and IC pins. The closer the crystal is to the MCU, the smaller the C_S, and vice versa. Therefore, in practical applications, when the crystal is far away from the MCU, causing the crystal to work abnormally, the external matching capacitor can be appropriately reduced.
4. When using an external high-speed crystal, it is recommended to connect a 1MΩ resistor in parallel at both ends of the crystal to make the crystal easier to vibrate.
5. Accuracy: external active crystal oscillator > external passive crystal > internal IRC16M.
6. When the active crystal oscillator is used normally, Bypass will be turned on. At this time, the high level is required to be no less than 0.7 V_{DD}/V_{DDA}, and the low level is no more than 0.3 V_{DD}/V_{DDA}.

7. The traces connecting the resonator to the MCU clock pins may cause inconsistent lengths of the traces connected to the OSCOUT and OSCIN pins due to the space constraints of the PCB layout. This will make the stray capacitances introduced by the two PCB traces inconsistent, so that the load capacitances on both sides of the resonator cannot be equal in value, and there needs to be a difference to match the actual PCB board. In this case, it is recommended to contact the resonator manufacturer to calculate the actual value.

2.3.2. External low-speed crystal oscillator clock (LXTAL)

LXTAL crystal is a 32.768 kHz low-speed external crystal (passive crystal), which can provide a low-power and high-precision clock source for RTC. The RTC module of the MCU is equivalent to a counter. The accuracy will be affected by the crystal performance, matching capacitance and PCB material. If you want to obtain better accuracy, it is recommended to connect PC13 to the timer input capture pin during circuit design. TIMER to calibrate LXTAL, and set the frequency division register of RTC according to the calibration situation. LXTAL can also support bypass clock input (active crystal oscillator, etc.), which can be enabled by configuring the LXTALBPS bit in RCU_CTL1. When LXTAL operates in bypass mode, the OSC32OUT pin can be left floating, configured as GPIO, or set to the OSC32EN functionality. The OSC32EN functionality provides a clock enable signal to the external clock source, allowing the MCU to request the external clock source to stop when entering low-power mode, thereby reducing system power consumption.

Figure 2-16. LXTAL External Crystal Circuit

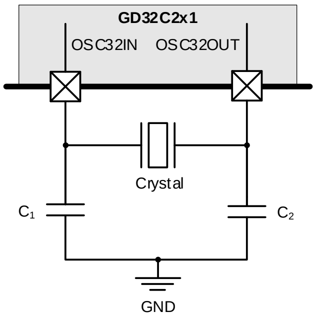
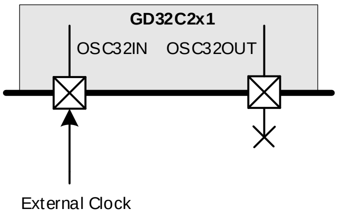


Figure 2-17. LXTAL External Clock Circuit



Note:

1. When using the bypass input, the signal is input from OSC32IN, and OSC32OUT remains floating.

2. For the size of the external matching capacitor, please refer to the formula: $C_1 = C_2 = 2*(C_{LOAD} - C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, the empirical value is between 2pF-7pF, and 5pF is recommended as a reference value calculation. When it is recommended to use an external crystal, try to choose a crystal load capacitance of about 10pF, so that the externally connected matching capacitors C_1 and C_2 can be 10pF, and the PCB layout should be as close to the crystal pin as possible.
3. The MCU can set the drive capability of LXTAL. If it is found that the external low-speed crystal is difficult to vibrate during the actual debugging process, you can try to adjust the drive capability of LXTAL to high drive capability.
4. The traces connecting the resonator to the MCU clock pins may cause inconsistent lengths of the traces connected to the two crystal pins of the MCU due to the space constraints of the PCB layout. This will make the stray capacitances introduced by the two PCB traces inconsistent, so that the load capacitances on both sides of the resonator cannot be equal in value, and there needs to be a difference to match the actual PCB board. In this case, it is recommended to contact the resonator manufacturer to calculate the actual value.

2.3.3. Clock Output Capability (CKOUT)

GD32C2x1 series MCUs can output clocks from 32kHz to 48MHz. There are several clock signals can be selected via the CK_OUT clock source selection bits, CKOUTSEL, in the configuration register 0 (RCU_CFG0). The corresponding GPIO pin should be configured in the properly alternate function I/O (AFIO) mode to output the selected clock signal.

Table 2-2. CKOUT0SEL[1:0] Control Bits

CKOUTSEL[2:0]	Clock source	
	GD32C231 GD32C232	GD32C211
000	No Clock	No Clock
001	CK_SYS	CK_SYS
010	Reserved	Reserved
011	CK_IRC48M	CK_IRC48M
100	CK_HXTAL	CK_HXTAL（OSCEXTIN）
101	Reserved	Reserved
110	CK_IRC32K	CK_IRC32K
111	CK_LXTAL	CK_LXTAL

2.3.4. HXTAL Clock Monitor (CKM)

The HXTAL clock monitor function is enabled by the HXTAL clock monitor enable bit, CKMEN, in the control register, RCU_CTL0. This function should be enabled after the HXTAL start-up delay and disabled when the HXTAL is stopped. Once the HXTAL failure is detected, the HXTAL will be automatically disabled. The HXTAL Clock Stuck Flag, CKMIF, in the interrupt register, RCU_INT, will be set and the HXTAL failure event will be generated. This failure interrupt is connected to the Non-Maskable Interrupt, NMI, of the Cortex-M23. If the HXTAL is selected as the clock source of CK_SYS, the HXTAL failure will force the CK_SYS source to IRC48MDIV_SYS.

Note: CKM is only for GD32C231xx / GD32C221xx devices. If the HXTAL is selected as the clock source of CK_SYS or PLL, the HXTAL failure will force the CK_SYS source to IRC48M.

2.3.5. LXTAL Clock Monitor (LCKM)

A clock monitor on LXTAL can be activated by software writing the LCKMEN bit in the control register 1(RCU_CTL1). LCKMEN can not be enabled before LXTAL and IRC32K are enabled and ready.

For GD32C231xx / GD32C221xx devices, the clock monitor on LXTAL is working in all modes except V_{CORE_STB}. For GD32C211xx devices, the clock monitor on LXTAL is working in all modes. If a failure is detected on the external 32 KHz oscillator, an interrupt can be sent to CPU. This failure interrupt is connected to the Non-Maskable Interrupt, NMI, of the Cortex-M23. If the LXTAL is selected as the clock source of CK_SYS, the LXTAL failure will force the CK_SYS source to IRC32K.

The software must then disable the LCKMEN bit, stop the defective 32 KHz oscillator, and change the RTC clock source, or take any required action to secure the application.

A 4-bits plus one counter will work at IRC32K domain when LCKMEN enable. If the LXTAL clock has stuck at 0 / 1 error or slow down about 20KHz, the counter will overflow. The LXTAL clock failure will been found.

2.4. Startup Configuration

The GD32C2x1 series microcontroller provides three boot sources, which can be selected using the BOOT0 pin and the boot mode configuration bits (BOOTLK, nBOOT1, SWBT0, nBOOT0) in the user option byte. When the SWBT0 bit is configured to 0, the logic level of the BOOT0 pin is latched on the rising edge of the fourth CK_SYS (system clock) after reset. After sampling the BOOT0 pin level, the pin can be released and used for other purposes. When the SWBT0 bit is configured to 1, the desired boot source is selected using the boot mode configuration bits (BOOTLK, nBOOT1, nBOOT0), and the BOOT0 pin level is invalid.

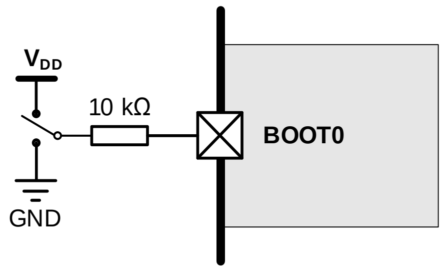
The embedded Bootloader is stored in the system memory and is used to reprogram the FLASH memory. The Bootloader can interact with external devices through USART0/1 and I2C0.

Regardless of how other modes are configured, forced booting can be achieved from the main Flash memory's single entry point by setting the BOOTLK bit.

Table 2-3. BOOT mode

Selected boot area	Boot mode configuration				
	BOOTLK	nBOOT1 bit	BOOT0 pin	SWBT0 bit	nBOOT0 bit
Main Flash memory	0	x	0	0	x
System memory	0	1	1	0	x
Embedded SRAM	0	0	1	0	x
Main Flash memory	0	x	x	1	1
System memory	0	1	x	1	0
Embedded SRAM	0	0	x	1	0
Main Flash memory	1	x	x	x	x

Figure 2-18. Recommend BOOT Circuit Design



Note:

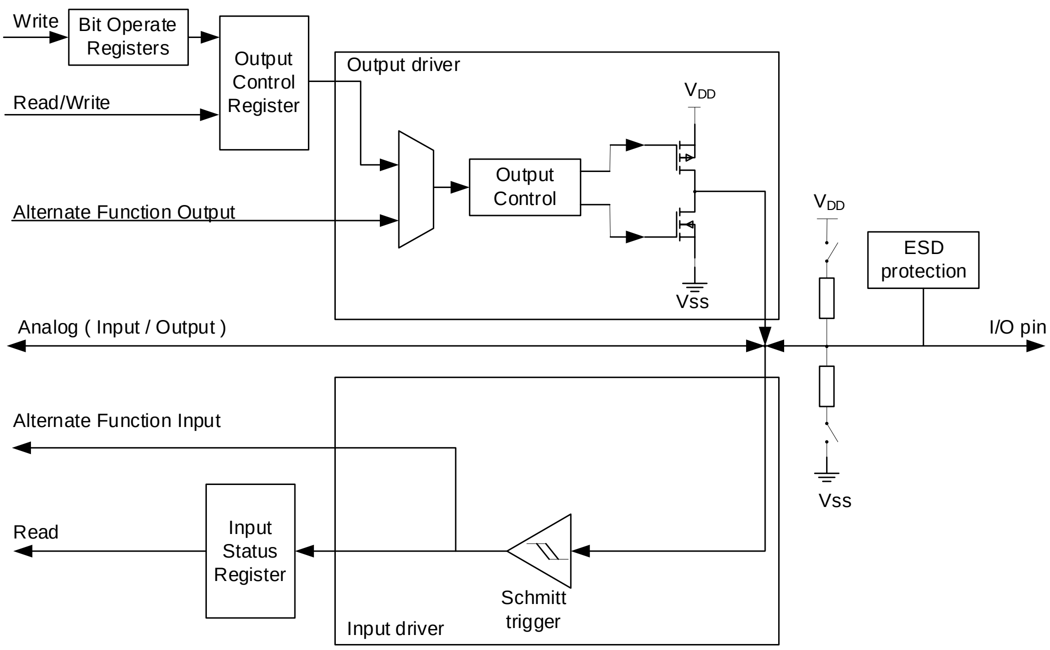
1. After the MCU is running, if the BOOT state is changed, it will take effect after the system is reset. MCU.
2. Once the BOOT0 pin state is sampled, it can be released for other purposes.

2.5. Typical Peripheral Modules

2.5.1. GPIO Circuit

GD32C2x1 can support up to 45 general-purpose I/O pins (GPIO), which are PA0 ~ PA15, PB0 ~ PB15, PC6 ~ PC7, PC13 ~ PC15, PD0 ~ PD3, PF0 ~ PF3; each pin can be independently configured through registers, the basic structure of the GPIO port is shown in the following figure:

Figure 2-19. Basic structure of standard IO



Note:

1. GPIO ports are divided into two types: N5T and 5VT. For N5T GPIOs, the input voltage V_{IN} must meet the condition $V_{IN} \leq V_{DD}/V_{DDA} + 0.3V$. For 5VT GPIOs, the input voltage V_{IN} is allowed to exceed V_{DD}/V_{DDA}, but it must meet the condition $V_{IN} \leq 5.5V$.
2. When 5VT GPIO ports are configured in open-drain mode, external pull-up is required for operation.
3. The GPIOs of GD32C2x1 comply with CMOS and TTL standards. When communicating with devices that support TTL levels, V_{DD}/V_{DDA} must satisfy the condition $2.7V \leq V_{DD}/V_{DDA} \leq 3.6V$.
4. After the IO port is powered on and reset, the default mode is floating input, and the level characteristics are uncertain. In order to obtain more consistent power consumption, it is recommended that all IO ports be configured as analog inputs and then modified to the corresponding mode according to application requirements (chip Ports that are not exported internally also need to be configured).
5. To improve EMC performance, it is recommended to pull up or pull down the unused IO pins by hardware.
6. The same label PIN in multiple groups can only configure one port as an external interrupt. For example, PA0, PB0, and PC0 only support one of the three IO ports to generate external interrupts, and do not support three external interrupt modes.
7. For the GD32C211 series in SOP8 package, multiple I/O pads can be connected to the same pin. Users can configure the target pin for GPIO function through SYSCFG_CFG3. Specifically, Pin 4 has four I/O pads (PA0, PA1, PA2, and NRST-PC2) simultaneously bonded to it, and Pin 4 is configured for NRST function by factory default. Users can configure Pin 4 for other I/O functions by setting the option byte FMC_OBCTL NRST_MDSEL[1:0] = 10 and then configuring SYSCFG_CFG3_PINMUX1. Before the option bytes are loaded and take effect, the user should avoid applying an external low-

level signal to Pin 4; otherwise, the chip will remain in reset state and fail to operate normally.

2.5.2. ADC Circuit

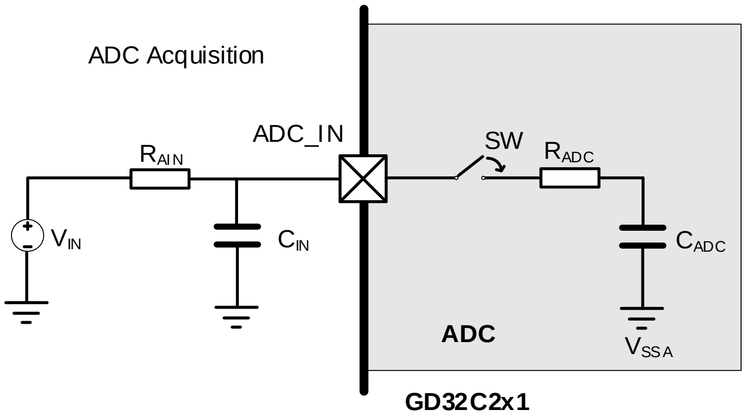
The GD32C2x1 integrates a 12-bit SAR ADC internally. The GD32C231/GD32C221 devices support up to 16 channels, capable of measuring 13 external and 3 internal signal sources. The internal signals include the temperature sensor V_{SENSE} channel (ADC_CH13), the internal reference voltage V_{REFINT} input channel (ADC_CH14), and the ADC positive reference voltage VREFP input channel (ADC_CH15). The GD32C211 devices supports up to 11 channels, capable of measuring 9 external and 2 internal signal sources. The internal signals include the temperature sensor V_{SENSE} channel (ADC_CH9) and the internal reference voltage V_{REFINT} input channel (ADC_CH10).

The temperature sensor reflects the change in temperature and is not suitable for measuring absolute temperature. If accurate temperature measurement is required, an external temperature sensor must be used. The internal reference voltage V_{REFINT} provides a regulated voltage output (1.2V) to the ADC.

If the ADC collects the external input voltage during use, if the sampled data fluctuates greatly, it may be due to the interference caused by power supply fluctuations. You can calibrate by sampling the internal V_{REFINT} and then calculate the externally sampled voltage.

When designing the ADC circuit, it is recommended to place a small capacitor at the ADC input pin. It is recommended to place a small capacitor of 500pF.

Figure 2-20. ADC Acquisition Circuit Design



When f_{ADC} = 24MHz, the relationship between the input impedance and the sampling period is as follows. In order to obtain better conversion results, it is recommended to reduce the frequency of f_{ADC} as much as possible during use, and select a larger value for the sampling period. When designing external circuits, try to reduce the input Impedance, if necessary, use the op amp to follow to reduce the input impedance.

Table 2-4. Relationship between sampling period and external input impedance

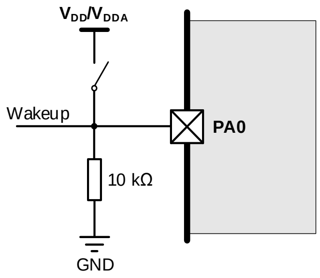
Resolution	Sampling cycles	GD32C231 GD32C232		GD32C211	
		f_{ADC} =24MHz		f_{ADC} =16MHz	
		t_S (μs)	R_{AIN} max (kΩ)	t_S (μs)	R_{AIN} max (kΩ)
12 bits	2.5	0.104	0.441	/	/
	3.5	0.146	0.979	0.219	1.61
	7.5	0.313	3.125	0.469	4.83
	12.5	0.521	5.809	0.781	8.86
	19.5	0.813	9.566	1.219	14.49
	39.5	1.656	20.300	2.469	30.6
	79.5	3.313	41.769	4.968	62.8
	160.5	6.688	85.243	10.03	128
10 bits	2.5	0.104	0.665	/	/
	3.5	0.146	1.292	0.219	2.08
	7.5	0.313	3.796	0.469	5.84
	12.5	0.521	6.927	0.781	10.5
	19.5	0.813	11.310	1.219	17.11
	39.5	1.656	23.833	2.469	35.9
	79.5	3.313	48.880	4.968	73.47
	160.5	6.688	99.600	10.03	149.55
8 bits	2.5	0.104	0.979	/	/
	3.5	0.146	1.730	0.219	2.74
	7.5	0.313	4.736	0.469	7.25
	12.5	0.521	8.493	0.781	12.88
	19.5	0.813	13.752	1.219	20.77
	39.5	1.656	28.780	2.469	43.32
	79.5	3.313	58.836	4.968	88.4
	160.5	6.688	119.700	10.03	179.7
6 bits	2.5	0.104	1.448	/	/
	3.5	0.146	2.387	0.219	3.73
	7.5	0.313	6.144	0.469	9.36
	12.5	0.521	10.840	0.781	16.41
	19.5	0.813	17.415	1.219	26.27
	39.5	1.656	36.200	2.469	54.45
	79.5	3.313	73.770	4.968	110.8
	160.5	6.688	149.850	10.03	224.9

2.5.3. Standby mode wake-up circuit

The power consumption is regarded as one of the most important issues for the devices of

GD32C2x1 series. The GD32C2x1 series products feature six power-saving modes to achieve lower power consumption, including Run1, Sleep, Sleep1, Deep-sleep, Deep-sleep 1, and Standby mode. The lowest power consumption is the standby mode, which requires the longest wake-up time. Wake-up from Standby mode can be woken up by the rising edge of the WKUP pin. At this time, there is no need to configure the corresponding GPIO, just configure the WUPENx bit in the PMU_CS register. The reference circuit design corresponding to the WKUP wake-up pin is as follows.

Figure 2-21. Recommend Standby external wake-up pin circuit design



Note:

1. In this mode, attention should be paid to the circuit design. If there is a series resistance between the WKUP pin and V_{DD}/V_{DDA}, additional power consumption may be added.
2. If WUPEN0 is set before entering the power saving mode, a rising edge on the WKUP pin0 wakes up the system from the power saving mode. As the WKUP pin0 is active high, the WKUP pin0 is internally configured to input pull down mode. And set this bit will trigger a wakup event when the input is aready high.As the same with other WKUP bit. Learing more can refer to use manual.

2.6. Download the debug circuit

The GD32C2x1 series cores only support SWD debug interface. The SWD interface standard is a 5-pin interface, of which 2 are signal interfaces.

Note:

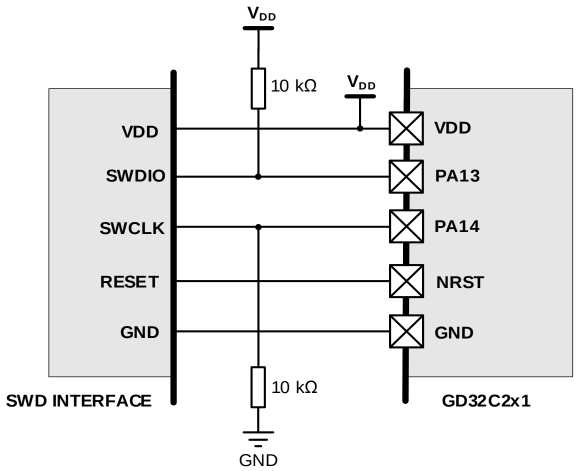
1. SWCLK shares a GPIO (PA14) with BOOT0. The factory default setting for the SWBT0 bit in the user option bytes is 1, making the BOOT0 pin level invalid. The boot mode can be selected through the boot mode configuration bits (BOOTLK bit, nBOOT1 bit, nBOOT0 bit) in the user option bytes. After reset, the default function of the PA14 pin is SWCLK, and the debug-related ports are set to input mode with pull-up/pull-down configurations, where:
   PA13: SWDIO in pull-up mode
   PA14: SWCLK in pull-down mode
2. When the SWBT0 bit in the user option bytes is configured to 0, the logic level of the BOOT0 pin is latched on the rising edge of the fourth CK_SYS (system clock) after reset. After latching, the pin is released for other uses, with its default function set to SWCLK. Before the logic level of the BOOT0 pin is latched, the debug-related ports are not

configured as input with pull-up/pull-down mode.

Table 2-5. SWD Download Debug Interface Assignment

Alternate function	GPIO port
SWDIO	PA13
SWCLK	PA14

Figure 2-22. Recommend SWD Wiring Reference Design



There are several ways to improve the reliability of SWD download and debugging communication and enhance the anti-interference ability of download and debugging.

1. Shorten the length of the two SWD signal lines, preferably within 15cm.
2. Weave the two SWD wires and the GND wire into a twist and twist them together.
3. Connect separately tens of pF small capacitors in parallel between the two signal lines of the SWD and the ground.
4. Any IO of the two signal lines of SWD is connected in series with a 100Ω~1kΩ resistor.

2.7. Reference Schematic Design

Figure 2-23. GD32C231 / GD32C221 Recommend Reference Schematic Design

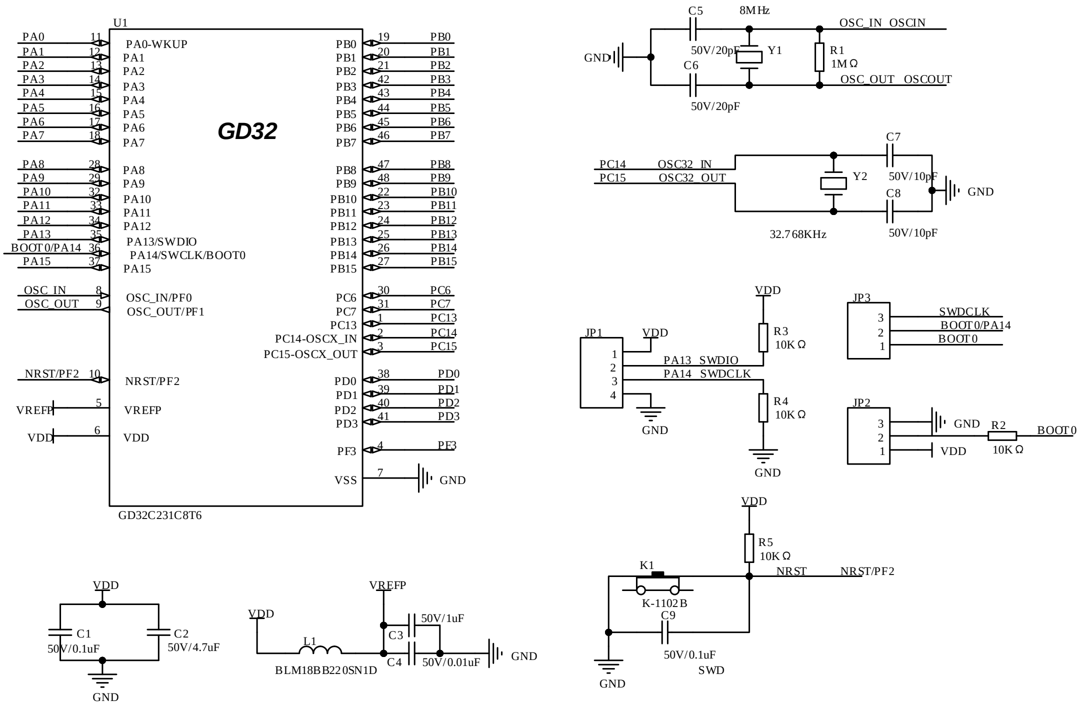
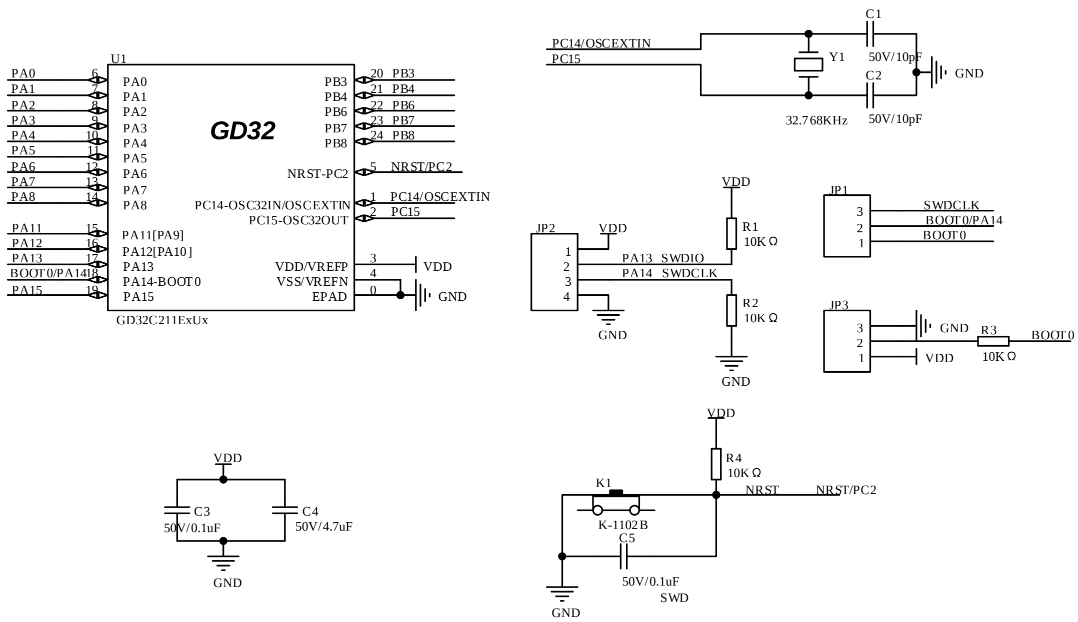


Figure 2-24. GD32C211 Recommend Reference Schematic Design



3. PCB Layout Design

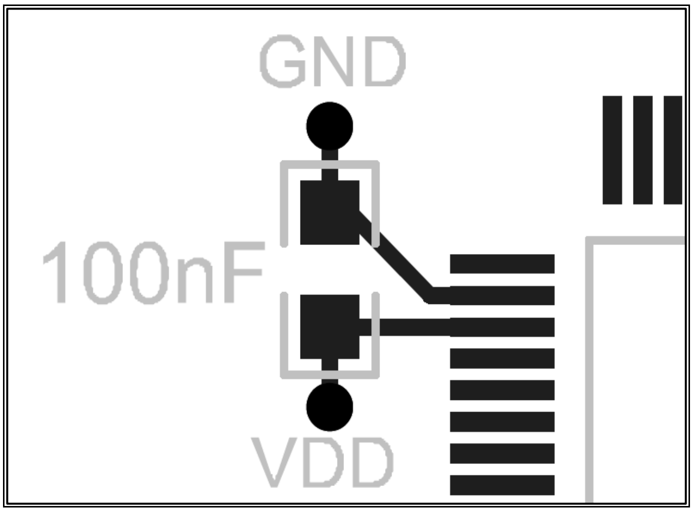
In order to enhance the functional stability and EMC performance of the MCU, it is not only necessary to consider the performance of the supporting peripheral components, but also the PCB Layout. In addition, when conditions permit, try to choose a PCB design solution with an independent GND layer and an independent power supply layer, which can provide better EMC performance. If conditions do not allow, independent GND layer and power supply layer cannot be provided, then it is also necessary to ensure a good power supply and grounding design, such as making the GND plane under the MCU as complete as possible. For packages with EPAD, it is recommended that EPAD be grounded on the PCB Layout.

In applications with high power or strong interference, it is necessary to consider keeping the MCU away from these strong interference sources.

3.1. Power Supply Decoupling Capacitors

The GD32C2x1 series power supply has three power supply pins: V_{DD}/V_{DDA} and V_{REFP}. The 100nF decoupling capacitor can be made of ceramic, and it is necessary to ensure that the position is as close to the power supply pin as possible. The power trace should try to make it pass through the capacitor first and then reach the MCU power pin, It is recommended to punch holes near the capacitor pad to connect with GND.

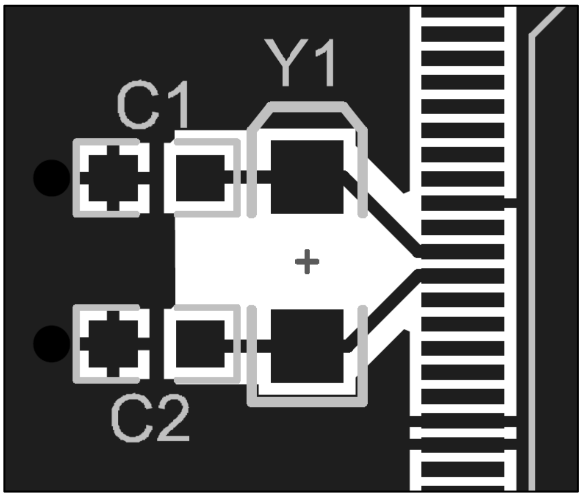
Figure 3-1. Recommend Power Pin Decoupling Layout Design



3.2. Clock Circuit

GD32C2x1 series clocks have HXTAL and LXTAL, and the clock circuit (including crystal or crystal oscillator and capacitor, etc.) is required to be placed close to the MCU clock pin, and the clock trace should be wrapped by GND as much as possible.

Figure 3-2. Recommend Clock Pin Layout Design (passive crystal)



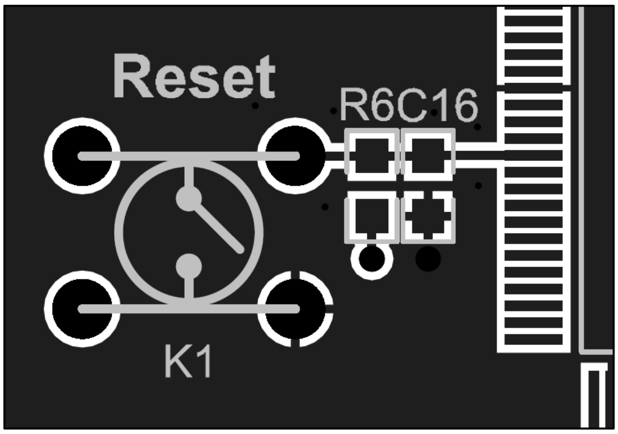
Note:

1. The crystal should be as close to the MCU clock pin as possible, and the matching capacitor should be as close as possible to the crystal.
2. The whole circuit should be on the same layer as the MCU, and the wiring should not go through the layer as much as possible.
3. The PCB area of the clock circuit should be kept as empty as possible, and no traces unrelated to the clock should be taken.
4. High-power, high-interference risk devices and high-speed wiring should be kept away from the clock crystal circuit as far as possible.
5. The clock line is grounded to achieve a shielding effect.

3.3. Reset Circuit

NRST trace PCB Layout reference is as follows:

Figure 3-3. Recommend NRST Trace Layout Design



Note: The resistance and capacitance of the reset circuit should be as close as possible to the NRST pin of the MCU, and the NRST trace should be kept away from devices with strong interference risk and high-speed traces as far as possible. If conditions permit, it had better to wrap the NRST traces for better shielding effect.

4. Package Description

GD32C231 series has a total of 7 package types, namely LQFP48, QFN48, LQFP32, QFN32, QFN28, TSSOP20 and LGA20.

GD32C221 series has a total of 3 package types, namely LQFP48, QFN32, and TSSOP20.

GD32C211 series has a total of 5 package types, namely QFN24, TSSOP24, QFN20, TSSOP20 and SOP8.

Table 4-1. Package Description

Ordering code	Package
GD32C231CxTx	LQFP48(7X7, 0.5pitch)
GD32C231CxUx	QFN48(7X7, 0.5pitch)
GD32C231KxTx	LQFP32(7X7, 0.8pitch)
GD32C231KxUx	QFN32(5X5, 0.5pitch)
GD32C231GxUx	QFN28(4X4, 0.5pitch)
GD32C231FxPx	TSSOP20(6.4X4.4, 0.65pitch)
GD32C231FxVx	LGA20(5X5, 0.5pitch)
GD32C221CxTx	LQFP48(7X7, 0.5pitch)
GD32C221KxUx	QFN32(5X5, 0.5pitch)
GD32C221FxPx	TSSOP20(6.5X4.4, 0.65pitch)
GD32C211E6U6TR	QFN24(4X4, 0.5pitch)
GD32C211E6P6TR	TSSOP24(7.8X4.4, 0.65pitch)
GD32C211F6U6TR	QFN20(3X3, 0.5pitch)
GD32C211F6P6TR	TSSOP20(6.5X4.4, 0.65pitch)
GD32C211J6M6TR	SOP8(4.9X3.9, 1.27pitch)

(Original dimensions are in millimeters)

5. Revision history

Table 5-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Jun.03, 2025
1.1	Added GD32C221/GD32C211 content.	Sept.08, 2025
1.2	Add configuration instructions for BOR, NRST and GPIO.	Apr.23, 2026

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