GigaDevice Semiconductor Inc.

Differences between GD32E51x and GD32E50x Products

Application Note
AN205

Revision 1.2

(Dec. 2025)

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1. Introduction

This application note introduces the characteristic differences between GD32E51x and GD32E50x product series, mainly for electric characteristics and peripheral function characteristics, the differences are described in the following paragraphs. The applicable products are as shown in ***Table 1-1. GD32E51x and GD32E50x products***.

Table 1-1. GD32E51x and GD32E50x products

Part Numbers	Products
GD32E50x	GD32E503xx
	GD32E505xx
	GD32E507xx
	GD32E508xx
	GD32EPRTxx
GD32E51x	GD32E513xx
	GD32E517xx
	GD32E518xx
	GD32EPRTxxA

Note: This application note is for reference only. In case of any conflict with the user manual or datasheet, the user manual or datasheet shall prevail.

2. Electric characteristic differences

2.1. DC operating conditions

DC operating conditions differences are reflected in supply voltage, which refers to ***Table 2-1. Differences of DC operating conditions***.

Table 2-1. Differences of DC operating conditions

Part Numbers	Symbol	Parameter	Conditions	Min(1)	Unit
GD32E50x	V_{DD}	Supply voltage	-	1.71	V
	V_{DDA}	Analog supply voltage, f_{ADCMAX} = 14 MHz	-	1.71	
	V_{BAT}	Battery supply voltage	-	1.71(2)	
GD32E51x	V_{DD}	Supply voltage	-	1.62	
	V_{DDA}	Analog supply voltage, f_{ADCMAX} = 14 MHz	-	1.62	
	V_{BAT}	Battery supply voltage	-	1.62(2)	

Note:

(1) Based on characterization, not tested in production.

(2) In the application which V_{BAT} supply the backup domains, if the VBAT voltage drops below the minimum value, when V_{DD} is powered on again, it is necessary to refresh the registers of backup domains and enable LXTAL again.

2.2. Start-up timings of operating conditions

Start-up timings of operating conditions differences are reflected in the start time when the system clock source is HXTAL or IRC8M, which refers to ***Table 2-2. Differences of start-up timings of operating conditions***.

Table 2-2. Differences of start-up timings of operating conditions

Part Numbers	Symbol	Parameter	Conditions	Typ	Unit
GD32E50x	$t_{start-up}$	Start-up time	Clock source from HXTAL	608	μs
			Clock source from IRC8M	74	
GD32E51x			Clock source from HXTAL	2270	
			Clock source from IRC8M	104.8	

Note:

(1) Based on characterization, not tested in production.

(2) After power-up, the start-up time is the time between the rising edge of NRST high and the first I/O instruction conversion in SystemInit function.

(3) PLL is off.

2.3. Power saving mode wakeup timings characteristics

Power saving mode wakeup timings characteristics differences are reflected in wakeup time from Sleep mode, Deep-sleep mode, Deep-sleep mode 1, Deep-sleep mode 2 and standby mode, which refers to ***Table 2-3. Differences of power saving mode wakeup timings***.

Table 2-3. Differences of power saving mode wakeup timings characteristics

Part Numbers	Symbol	Parameter	Typ	Unit
GD32E50x	t_{Sleep}	Wakeup from Sleep mode	1.7	μs
	$t_{Deep-sleep}$	Wakeup from Deep-sleep mode (LDO On)	3.1	
		Wakeup from Deep-sleep mode (LDO in low power mode)	3.1	
		Wakeup from Deep-sleep mode1 (LDO in low power and low driver mode)	4.3	
		Wakeup from Deep-sleep mode2 (LDO in low power and low driver mode)	11.7	
	$t_{Standby}$	Wakeup from Standby mode	77.2	
GD32E51x	t_{Sleep}	Wakeup from Sleep mode	2.16	
	$t_{Deep-sleep}$	Wakeup from Deep-sleep mode (LDO On)	4.74	
		Wakeup from Deep-sleep mode (LDO in low power mode)	4.74	
		Wakeup from Deep-sleep mode1 (LDO in low power and low driver mode)	7.16	
		Wakeup from Deep-sleep mode2 (LDO in low power and low driver mode)	7.84	
	$t_{Standby}$	Wakeup from Standby mode	105.2	

Note:

(1) Based on characterization, not tested in production.

(2) The wakeup time is measured from the wakeup event to the point at which the application code reads the first instruction under the below conditions: V_{DD} = V_{DDA} = 3.3 V, IRC8M = System clock = 8 MHz.

2.4. Power consumption

The power consumption differences are reflected in supply current in deep-sleep mode and standby mode, which refers to ***Table 2-4. Differences of power consumption characteristics in deep-sleep mode***, ***Table 2-5. Differences of power consumption characteristics in deep-sleep mode 1***, ***Table 2-6. Differences of power consumption characteristics in deep-sleep mode 2*** and ***Table 2-7. Differences of Power consumption***

characteristics in standby mode.

Table 2-4. Differences of power consumption characteristics in deep-sleep mode

Part Numbers	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
GD32E50x	$I_{DD}+I_{DDA}$	Supply current (Deep-Sleep mode)	V_{DD} = V_{DDA} = 3.3 V, LDO in normal power and normal driver mode, IRC40K off, RTC off, all GPIOs are configured as analog mode	—	461.33	—	μA
			V_{DD} = V_{DDA} = 3.3 V, LDO in low power and normal driver mode, IRC40K off, RTC off, all GPIOs are configured as analog mode	—	413.00	—	μA
			V_{DD} = V_{DDA} = 3.3 V, LDO in normal power and low driver mode, IRC40K off, RTC off, all GPIOs are configured as analog mode	—	258.00	—	μA
			V_{DD} = V_{DDA} = 3.3 V, LDO in low power and low driver mode, IRC40K off, RTC off, all GPIOs are configured as analog mode	—	210.67	—	μA
GD32E51x			V_{DD} = V_{DDA} = 3.3 V, LDO in normal power and normal driver mode, IRC40K off, RTC off, all GPIOs are configured as analog mode	—	146.47	—	μA
			V_{DD} = V_{DDA} = 3.3 V, LDO in low power and normal driver mode, IRC40K off, RTC off, all GPIOs are configured as analog mode	—	96.70	—	μA
			V_{DD} = V_{DDA} = 3.3 V, LDO in normal power and low driver mode, IRC40K off, RTC off, all GPIOs are configured as analog mode	—	106.67	—	μA
			V_{DD} = V_{DDA} = 3.3 V, LDO in low power and low driver mode, IRC40K off, RTC off, all GPIOs are configured as analog mode	—	59.20	—	μA

Table 2-5. Differences of power consumption characteristics in deep-sleep mode 1

Part Numbers	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
GD32E50x	$I_{DD}+I_{DDA}$	Supply current	V_{DD} = V_{DDA} = 3.3 V, LDO in low	—	163.3	—	μA

Part Numbers	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		(Deep-Sleep 1 mode)	power and low driver mode, IRC40K off, RTC off, all GPIOs are configured as analog mode		3		
GD32E51x				—	48.30	—	μA

Table 2-6. Differences of power consumption characteristics in deep-sleep mode 2

Part Numbers	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
GD32E50x	I_{DD}+I_{DDA}	Supply current (Deep-Sleep 2 mode)	V_{DD} = V_{DDA} = 3.3 V, LDO in low power and low driver mode, IRC40K off, RTC off, all GPIOs are configured as analog mode	—	68.00	—	μA
GD32E51x				—	30.04	—	μA

Table 2-7. Differences of Power consumption characteristics in standby mode

Part Numbers	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
GD32E50x	I_{DD}+I_{DDA}	Supply current (Standby mode)	V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC40K on, RTC on	—	3.79	—	μA
			V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC40K on, RTC off	—	3.58	—	
			V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC40K off, RTC off	—	3.08	—	
GD32E51x			V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC40K on, RTC on	—	3.07	—	μA
			V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC40K on, RTC off	—	2.82	—	
			V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC40K off, RTC off	—	2.06	—	

Note: Based on characterization, not tested in production.

2.5. Electro magnetic compatibility (EMC)

The EMC differences are reflected in EMS and EMI, which refers to ***Table 2-8. Differences of EMS characteristic*** and ***Table 2-9. Differences of EMI characteristic***.

Table 2-8. Differences of EMS characteristics

Part Numbers	Symbol	Parameter	Conditions	Level/Class
GD32E50x	V_{ESD}	Voltage applied to all device pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144, f_{HCLK} = 180 MHz, conforms to IEC 61000-4-2	3A
	V_{FTB}	Fast transient voltage burst applied to induce a functional disturbance through 100 pF on VDD and VSS pins	V_{DD} = 3.3 V, LQFP144, f_{HCLK} = 180 MHz, conforms to IEC 61000-4-4	4A
GD32E51x	V_{ESD}	Voltage applied to all device pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144, f_{HCLK} = 180 MHz, conforms to IEC 61000-4-2	4A
	V_{FTB}	Fast transient voltage burst applied to induce a functional disturbance through 100 pF on VDD and VSS pins	V_{DD} = 3.3 V, LQFP144, f_{HCLK} = 180 MHz, conforms to IEC 61000-4-4	4A

Note: Based on characterization, not tested in production.

Table 2-9. Differences of EMI characteristics

Part Numbers	Symbol	Parameter	Conditions	Tested frequency band	Max vs. [f_{HXTAL}/f_{HCLK}] 8/180 MHz	Unit
GD32E50x	S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = +23 °C, LQFP144, f_{HCLK} = 180 MHz, conforms to SAE J1752-3:2017	0.15 MHz to 30 MHz	-7.58	dBμV
				30 MHz to 130 MHz	3.35	
				130 MHz to 1 GHz	4.25	
GD32E51x				0.15 MHz to 30 MHz	-0.03	
				30 MHz to 130 MHz	5.04	
				130 MHz to 1 GHz	13.07	

Note: Based on characterization, not tested in production.

2.6. Electrostatic discharges (ESD)

The ESD difference refers to ***Table 2-10. Differences of ESD level***.

Table 2-10. Differences of ESD level(1)

Part Numbers	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
GD32E50x	$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A=25 °C; ESDA/JEDEC JS-001-2017	—	6000	—	V
	$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A=25 °C; ESDA/JEDEC JS-002-2018	—	1000	—	
GD32E51x	$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A=25 °C; ESDA/JEDEC JS-001-2017	—	5000(2)	—	
	$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A=25 °C; ESDA/JEDEC JS-002-2018	—	500	—	

Note:

(1) Based on characterization, not tested in production.

(2) When the chip is GD32E513xx, the value is 4000.

2.7. External clock

The external clock difference is reflected in LXTAL startup time, which refers to ***Table 2-11. Differences of LXTAL startup time***.

Table 2-11. Differences of LXTAL startup time

Part Numbers	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
GD32E50x	$t_{SULXTAL}$(1)(2)	Crystal or ceramic startup time	—	—	2	—	s
GD32E51x				—	0.6	—	

Note:

(1) Based on characterization, not tested in production.

(2) $t_{SULXTAL}$ is the startup time measured from the moment it is enabled (by software) to the 32.768 kHz oscillator stabilization flags is SET. This value varies significantly with the crystal manufacturer.

2.8. Internal clock

The internal clock differences are reflected in IRC40K and IRC48M startup time, which refers to ***Table 2-12. Differences of IRC40K startup time*** and ***Table 2-13. Differences of IRC48M startup time***.

Table 2-12. Differences of IRC40K startup time

Part Numbers	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
GD32E50x	$t_{SUIRC40K}$	IRC40K oscillator startup time	V_{DD} = 3.3 V	—	80	—	μs

GD32E51x				—	1.3	—	

Note: Based on characterization, not tested in production.

Table 2-13. Differences of IRC48M startup time

Part Numbers	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
GD32E50x	$t_{SUIRC48M}$	IRC48M oscillator startup time	V_{DD} = V_{DDA} = 3.3 V, f_{HCLK} = f_{HXTAL_PLL} = 180 MHz	—	3.68	—	µs
GD32E51x				—	1.3	—	

Note: Based on characterization, not tested in production.

2.9. Flash memory

The flash memory characteristics differences are reflected in word programming, page erasing and mass erasing time, which refers to ***Table 2-14. Differences of flash operating time***.

Table 2-14. Differences of flash operating time

Part Numbers	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
GD32E50x	PE_{CYC}	Number of guaranteed program / erase cycles before failure (Endurance)	T_A = -40 °C ~ +85 °C	10	—	—	kcycles
	t_{PROG}	Word programming time		—	37.5	—	µs
	t_{ERASE}	Page erase time		—	11	—	ms
	t_{MERASE}	Mass erase time		—	12	—	ms
GD32E51x	PE_{CYC}	Number of guaranteed program / erase cycles before failure (Endurance)		100	—	—	kcycles
	t_{PROG}	Word programming time		—	20	—	µs
	t_{ERASE}	Page erase time		1	—	20	ms
	t_{MERASE}	Mass erase time		—	20	—	ms

Note: Guaranteed by design, not tested in production.

2.10. Temperature sensor characteristics

The temperature sensor difference is reflected in voltage value at 25℃, which refers to ***Table***

2-15. Differences of temperature sensor characteristics.

Table 2-15. Differences of temperature sensor characteristics

Part Numbers	Symbol	Parameter	Min	Typ	Max	Unit
GD32E50x	V_{25}	Voltage at 25 ℃	—	1.45	—	V
GD32E51x			—	1.43	—	V

Note: Based on characterization, not tested in production.

2.11. Analog-to-digital converter (ADC)

The ADC characteristics differences are reflected in operating voltage and positive reference voltage, which refers to *Table 2-16. Electric characteristic differences of ADC*.

Table 2-16. Electric characteristic differences of ADC

Part Numbers	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
GD32E50x	V_{DDA}(1)	Operating voltage	—	1.71	3.3	3.63	V
	V_{REFP}(2)	Positive reference voltage	—	1.71	—	V_{DDA}	V
GD32E51x	V_{DDA}(1)	Operating voltage	—	1.62	3.3	3.63	V
	V_{REFP}(2)	Positive reference voltage	—	1.62	—	V_{DDA}	V

Note:

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

3. Peripheral function differences

3.1. Flash memory controller (FMC)

The FMC differences are reflected in the programming width and Flash ECC function, which refers to ***Table 3-1. Differences of*** .

Table 3-1. Differences of FMC function

Part Numbers	Programming width	Flash ECC check
GD32E50x	32 bit	Not supported
GD32E51x	64 bit	Supported

3.2. Controller area network (CAN)

The CAN differences are reflected in the receiving FIFO overrun detection function, which refers to ***Table 3-2. Differences of CAN function***. The receiving FIFO overrun detection flag can be obtained through the eighth bit in the CAN_RFIFO0 register (RFOVRN0) and the eighth bit in the CAN_RFIFO1 register (RFOVRN1), refer to ***Table 3-3. Bit field description of RFOVRN0/ RFOVRN1***.

Table 3-2. Differences of CAN function

Part Numbers	Receiving FIFO overrun detection
GD32E50x	Not supported
GD32E51x	Supported

Table 3-3. Bit field description of RFOVRN0/ RFOVRN1

Fields	Descriptions
RFOVRN0	Rx FIFO0 overrun This bit is set by hardware when Rx FIFO overwrite enabled and the Rx FIFO0 is overrun. 0: The Rx FIFO0 is not overrun 1: The Rx FIFO0 is overrun **Note:** when this bit is set, don't read data from FIFO.
RFOVRN1	Rx FIFO1 overrun This bit is set by hardware when Rx FIFO overwrite enabled and the Rx FIFO1 is overrun. 0: The Rx FIFO1 is not overrun 1: The Rx FIFO1 is overrun **Note:** when this bit is set, don't read data from FIFO.

4. Other differences

4.1. Number of peripherals

Number of peripherals difference refers to ***Table 4-1. Differences of number of peripherals***.

Table 4-1. Differences of number of peripherals

Part Numbers	DAC	TIMER
GD32E50x	DAC	TIMER0/1/2/3/4/5/6/7/8/9/10/11/12/13
GD32E51x	DAC0/1	TIMER0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15/16

4.2. Flash memory

Flash memory difference refers to ***Table 4-2. Differences of flash memory bus***.

Table 4-2. Differences of flash memory bus

Part Numbers	Flash memory interface bus width
GD32E50x	128 bits
GD32E51x	64 bits

4.3. Processor performance

Processor performance difference refers to ***Table 4-3. Differences of processor performance@180MHz*** and ***Table 4-4. Differences of processor performance@120MHz***.

Table 4-3. Differences of processor performance@180MHz

Part Numbers	Clock	Boot configuration	Cache configuration	CoreMark/MHz
GD32E50x	AHB=SYSCLK=180MHz	FLASH，latency=4	DCEN=1，ICEN=1，PFEN=1	3.259107
		FLASH，latency=5	DCEN=1，ICEN=1，PFEN=1	3.243173
		FLASH，latency=5	DCEN=0，ICEN=0，PFEN=0	1.760246
GD32E51x		FLASH，latency=4	DCEN=1，ICEN=1，PFEN=1	3.169622
		FLASH，latency=5	DCEN=1，ICEN=1，PFEN=1	3.123511
		FLASH，latency=5	DCEN=0，ICEN=0，PFEN=0	1.303585

Table 4-4. Differences of processor performance@120MHz

Part Numbers	Clock	Boot configuration	Cache configuration	CoreMark/MHz
GD32E50x	AHB=SYSCLK=120MHz	FLASH，latency=3	DCEN=1，ICEN=1，PFEN=1	3.269897
		FLASH，latency=3	DCEN=0，ICEN=0，PFEN=0	2.232791
GD32E51x		FLASH，latency=3	DCEN=1，ICEN=1，PFEN=1	3.215330
		FLASH，latency=3	DCEN=0，ICEN=0，PFEN=0	1.823386

Note: The above test conditions are ARMCLANG 6.15 compiler, the Optimization level is -Ofast, Link-Time optimization is not checked.

5. Revision history

Table 5-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Jun.25, 2024
1.1	Add EMC differences, refer to ***Electro magnetic compatibility (EMC)***	Mar.5, 2025
1.2	1. Add CAN differences, refer to ***Controller area network (CAN)*** 2. Add flash memory and processor performance differences, refer to ***Flash memory*** and ***Processor performance*** in the ***Other differences*** section	Dec.4, 2025

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