GigaDevice Semiconductor Inc.

GD32M531x Hardware Development Guide

Application Note
AN251

Revision 1.0

(Mar, 2025)

Table of Contents

List of Figures

List of Tables

1. Introduction

The article is specially provided for developers of 32-bit general-purpose MCU GD32M531x series based on Arm® Cortex®-M33 architecture. It provides an overall introduction to the hardware development of GD32M531x series products, such as power supply, reset, clock, boot mode settings and download debugging. The purpose of this application notes is to allow developers to quickly get started and use GD32M531x series products, and quickly develop and use product hardware, save the time of studying manuals, and speed up product development progress.

This application note is divided into seven parts to describe:

1. Power supply, mainly introduces the design of GD32M531x series power management, power supply and reset functions.
2. Clock, mainly introduces the functional design of GD32M531x series high and low speed clocks.
3. Boot configuration, mainly introduces the BOOT configuration and design of GD32M531x series.
4. Typical peripheral modules, mainly introduces the hardware design of the main functional modules of the GD32M531x series.
5. Download and debug circuit, mainly introduces the recommended typical download and debug circuit of GD32M531x series.
6. Reference circuit and PCB Layout design, mainly introduces GD32M531x series hardware circuit design and PCB Layout design notes.
7. Package description, mainly introduces the package forms and names included in the GD32M531x series.

This document also satisfies the minimum system hardware resources used in application development based on GD32M531x series products.

Table 1-1. Applicable Products

Type	Part Numbers
MCU	GD32M531x series

2. Hardware design

2.1. Power supply

The V_{DD} / V_{DDA} operating voltage range of GD32M531x series products is 2.7V ~ 5.5V. For GD32M531x series, there are two power domains, including V_{DD} / V_{DDA} domain and 1.2V domain, as is shown in *错误!未找到引用源。* .The V_{DD}/V_{DDA} domain is powered directly by the power supply, and an LDO is embedded in the V_{DD}/V_{DDA} domain to power the 1.2 V domain.

Figure 2-1. GD32M531x Power supply overview

LVD: Low Voltage Detector   LDO: Voltage Regulator
POR: Power On Reset   PDR: Power Down Reset
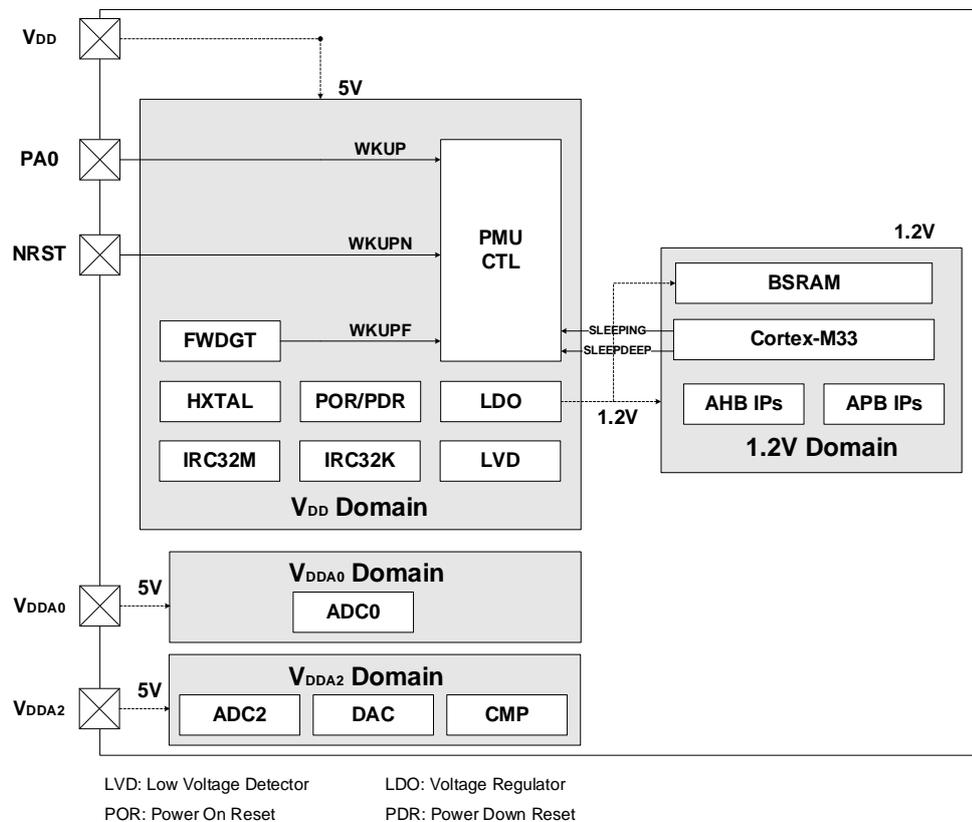
2.1.1. V_{DD} / V_{DDA} power domain

V_{DD} / V_{DDA} domain includes two parts: V_{DD} domain and V_{DDA} domain. V_{DD} domain includes HXTAL (High Speed Crystal oscillator), LDO (Voltage Regulator), POR / PDR (Power On / Down Reset), FWDGT (Free Watchdog Timer), and all PADs except PD4 / PD5, PC0-PC12, as well as the IRC32M (internal 32M RC oscillator), IRC32K (internal 32KHz RC oscillator), PLLs (phase-locked loops), and LVD (low voltage detector), etc. The V_{DDA} domain includes two parts: V_{DDA0} and V_{DDA2}, where V_{DDA0} includes ADC0, and V_{DDA2} includes ADC2, DAC (analog-to-digital / digital-to-analog converter), CMP (comparator), and so on.

VDD domain

The LDO, which is implemented to supply power for the 1.2V domain, is always enabled after the reset. It can be configured to operate in three different status, including the Sleep mode (full power on), in the Deep-sleep mode (on or low power), and in the Standby mode (power off).

VDDA domain

Generally, digital circuits are powered by V_{DD}, while most of analog circuits are powered by V_{DDA}. To improve the ADC and DAC conversion accuracy, the independent power supply V_{DDA} is implemented to achieve better performance of analog circuits. V_{DDA} can be externally connected to V_{DD} through the external filtering circuit that avoids noise on V_{DDA}, and V_{SSA} should be connected to V_{SS} through the specific circuit independently.

2.1.2. Power saving modes

After a system reset or a power reset, the GD32M531 MCU operates at full function state and all power domains are active. Users can achieve lower power consumption through slowing down the system clocks (HCLK, PCLK1 and PCLK2), closing the clocks of the unused peripherals. Besides, three power saving modes are provided to achieve even lower power consumption. They are Sleep mode, Deep-sleep mode and Standby mode. The three power-saving modes are summarized in *Table 2.1. Power saving mode summary.*

Table 2-1. Power saving mode summary

Mode	Sleep	Deep-sleep	Standby
Description	Only CPU clock is off	1. All clocks in the 1.2V domain are off 2. Disable IRC32M, HXTAL and PLL	1. The 1.2V domain is powered off 2. Disable IRC32M, HXTAL and PLL
LDO Status	On (normal power mode)	On (normal or low power mode)	Off
Configuration	SLEEPDEEP = 0	SLEEPDEEP = 1 STBMOD = 0	SLEEPDEEP = 1 STBMOD = 1, WURST=1
Entry	WFI or WFE	WFI or WFE	WFI or WFE
Wakeup	Any interrupt for WFI. Any event (or interrupt when SEVONPEND is 1) for WFE	Any interrupt from EXTI lines for WFI Any event(or interrupt when SEVONPEND is 1) from EXTI for WFE	1. NRST pin 2. WKUP pin 3. FWDGT reset
Wakeup Latency	None	IRC32M wakeup time, LDO wakeup time added if LDO is in low power mode	Power on sequence

Note: In Standby mode, all I/Os are in high-impedance state except NRST pin, and WKUP pin if enabled.

2.1.3. Power supply design

The system needs a stable power supply. There are some important things to pay attention to when developing and using:

■ The VDD pin must be connected with an external capacitor (N*100nF ceramic capacitor + not less than 4.7uF tantalum capacitor, at least one VDD needs to be connected to GND with a capacitor of not less than 4.7uF, and other VDD pins are connected to 100nF).

■ The VDDA/VREFP pin must be connected with an external capacitor (10nF+1uF ceramic capacitor is recommended).

■ VCAP pin must be externally connected to a ground capacitor (470 nF + 1 nF ceramic capacitor recommended).

Figure 2-2. GD32M531x Recommended Power Supply Design
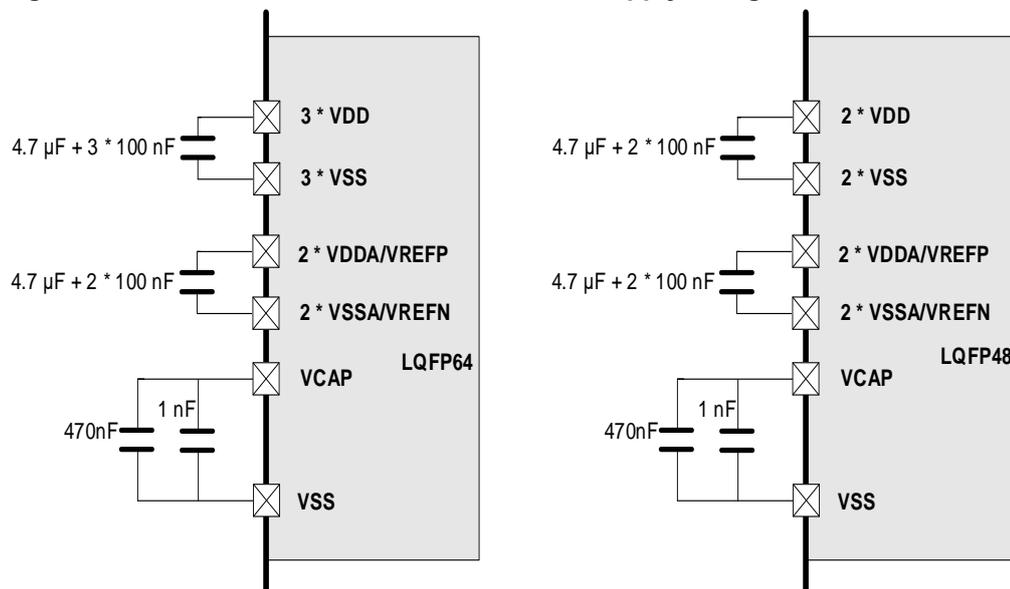
Note:

1. All decoupling capacitors must be placed close to the corresponding V_{DD}, V_{DDA}/V_{REFP}, VCAP pins of the chip;

2. When the MCU power supply voltage is unstable or there is a risk of voltage drop, it is recommended to adjust the 4.7uF capacitor not less than 10uF;

3. The connection length between the VCAP pin and the capacitor should be less than or equal to 8mm (if possible, less than or equal to 4mm), otherwise the increase in the parasitic resistance value will reduce the effectiveness of the capacitor and may have an impact on the noise level of the VDD.If the cable length between the VCAP pin and the capacitor is greater than 8mm, the parasitic resistance should be less than 1 ohm, as shown in *Figure 2-3.The calculation formula of parasitic resistance* is given.

Figure 2-3.Parasitic resistance calculation formula
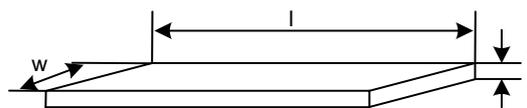
$$R = \frac{l}{\sigma wt}(\Omega)$$

$$L = 0.2l[\ln\left\{\frac{2l}{w+t}\right\} + 0.5](uH)$$

$$\omega L = 2\pi fL(\Omega)$$

$$f = 20(MHz)$$

$$R_P = R + 2\pi fL(\Omega) < 1(\Omega)$$

σ is the conductivity of copper

2.2. Power supply detection and reset

2.2.1. LVD

Three Low Voltage Detectors (LVD) to detect low voltage events.

LVD0

The LVD0 is used to detect whether the V_{DD} supply voltage is lower than a programmed threshold selected by the LVD0T[7:6] bits in the option bytes. If LVD0EN in the option byte is set to 0, a system reset will be generated when LVD0 detects that the voltage is lower than the set threshold voltage.

Figure 2-4. Low Voltage Detectors 0 block diagram
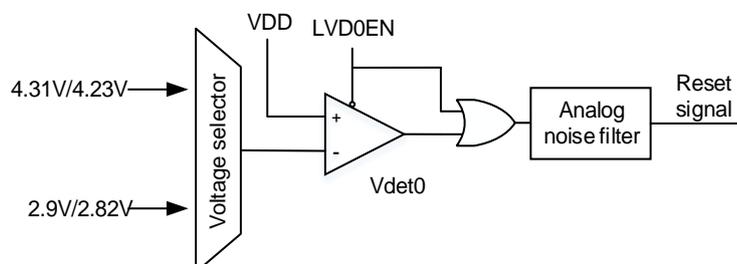
LVD1

The Low Voltage Detectors 1 (LVD1) is used to detect whether the V_{DD} / V_{DDA} supply voltage

is lower or higher than a programmed threshold selected by the LVD1T[3:0] bits in the Low Voltage Detector 1 control register(PMU_LVD1CTL). When LVD1 is enabled, if V_{DD} / V_{DDA} > Vdet1 or V_{DD} / V_{DDA} <= Vdet1 is detected, LVD1 can generate a system reset or interrupt.

Figure 2-5. Low Voltage Detectors 1 block diagram
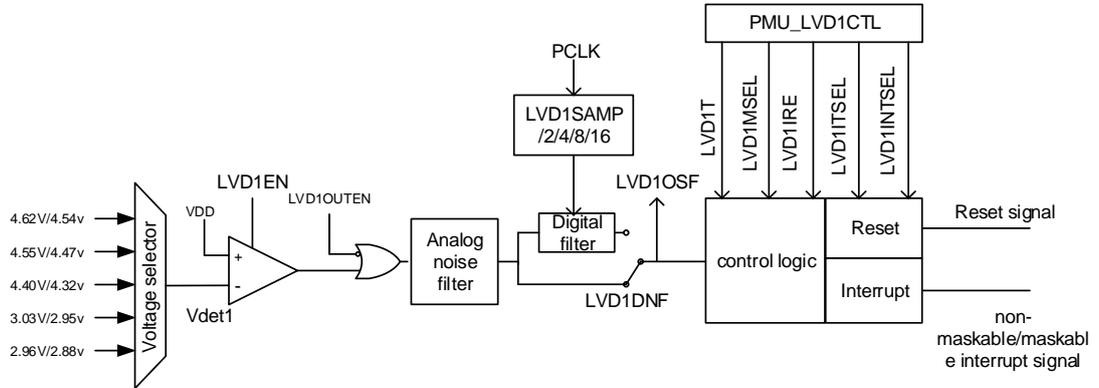
Through the following register setting sequence, LVD1 can generate an interrupt.

1. Unlock the PMU_LVD1CTL by setting the PRCFG2 bits in the SYSCFG_PRCFG.
2. Select the detection voltage threshold for LVD1 by setting the LVD1T[3:0] bits.
3. Select the interrupt mode of LVD1 by setting the LVD1MSEL bit.
4. Set the condition for generating LVD1 interrupts by configuring the LVD1INTSEL[1:0] bits.
5. Set the type of interrupt by configuring the LVD1ITSEL bit.
6. Enable LVD1 by setting the LVD1EN bit.
7. Enable LVD1 comparison result output by setting the LVD1OUTEN bit.
8. Set the LVD1DETF bit to 0.
9. Enable LVD1 interrupt by setting the LVD1IRE bit.

Note: Step 1.2.5 is not required in the following two situations:

a. Monitoring is restarted without changing the monitoring settings after stopping monitoring.

b. After monitoring is stopped, changing LVD1ITSEL and LVD1INTSEL monitoring will restart.

Through the following step register setting sequence, LVD1 can generate a system reset.

1. Select the detection voltage threshold for LVD1 by setting the LVD1T[3:0] bits.
2. Select the Reset mode of LVD1 by setting the LVD1MSEL bit.
3. Set the type of reset negation by setting the LVD1RSTSEL bit.
4. Enable LVD1 Reset mode by setting the LVD1IRE bit.
5. Enable LVD1 by setting the LVD1EN bit.
6. Enable LVD1 comparison result output by setting the LVD1OUTEN bit.

LVD2

The Low Voltage Detectors 2 (LVD2) is used to detect whether the V_{DD} / V_{DDA} supply voltage is lower or higher than a programmed threshold selected by the LVD2T[3:0] bits in the Low

Voltage Detector 2 control register(PMU_LVD2CTL). When LVD2 is enabled, if V_{DD} / V_{DDA} > Vdet2 or V_{DD} / V_{DDA} <= Vdet2 is detected, LVD2 can generate a system reset or interrupt.

Figure 2-6. Low Voltage Detectors 2 block diagram

Through the following register setting sequence, LVD2 can generate an interrupt.

1. Unlock the PMU_LVD2CTL by setting the PRCFG2 bits in the SYSCFG_PRCFG.
2. Select the detection voltage threshold for LVD2 by setting the LVD2T[1:0] bits.
3. Select the interrupt mode of LVD2 by setting the LVD2MSEL bit.
4. Set the condition for generating LVD2 interrupts by configuring the LVD2INTSEL[1:0] bits.
5. Set the type of interrupt by configuring the LVD2ITSEL bit.
6. Enable LVD2 by setting the LVD2EN bit.
7. Enable LVD2 comparison result output by setting the LVD2OUTEN bit.
8. Set the LVD2DETF bit to 0.
9. Enable LVD2 interrupt by setting the LVD2IRE bit.

Note: Step 1.2.5 is not required in the following two situations:

a. Monitoring is restarted without changing the monitoring settings after stopping monitoring.

b. After monitoring is stopped, changing LVD2ITSEL and LVD2INTSEL monitoring will restart.

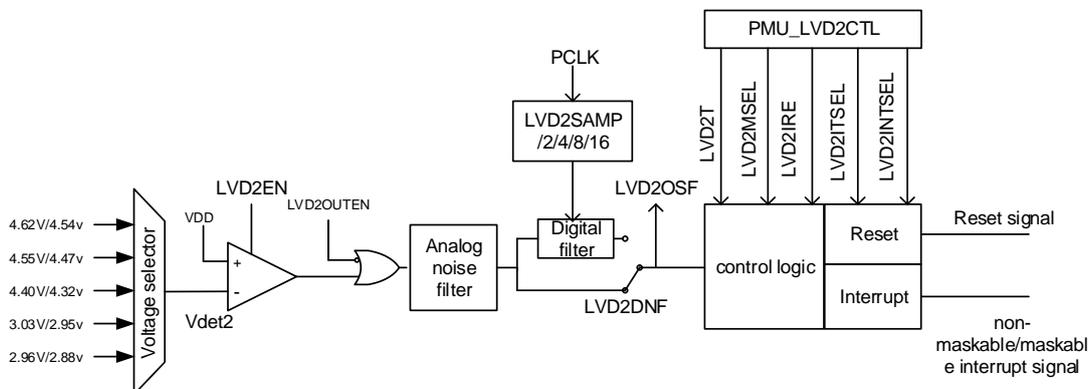Through the following step register setting sequence, LVD2 can generate a system reset.

1. Select the detection voltage threshold for LVD2 by setting the LVD2T[1:0] bits.
2. Select the Reset mode of LVD2 by setting the LVD2MSEL bit.
3. Set the type of reset negation by setting the LVD2RSTSEL bit.
4. Enable LVD2 Reset mode by setting the LVD2IRE bit.
5. Enable LVD2 by setting the LVD2EN bit.

Enable LVD2 comparison result output by setting the LVD2OUTENbit.

2.2.2.   POR / PDR

The POR/PDR (power-on/Power-off reset) circuit detects VDD/VDDA and generates a power reset signal to reset the entire chip when the voltage falls below a specific threshold.

Figure 2-6. Waveform of power-on/power-off reset shows the relationship between the supply voltage and the power reset signal.V_{POR} indicates the threshold voltage for power-on reset. V_{PDR} indicates the threshold voltage for power-off reset. Hysteresis voltage Vhyst Value Refer to the data manual.

Figure 2-7. Waveform of power-on/power-off reset
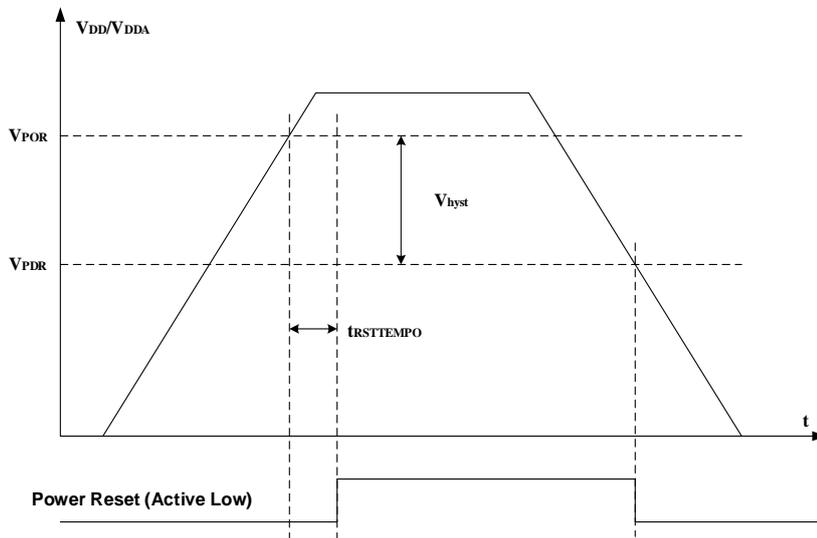
2.2.3. NRST Pin

GD32M531 reset control includes the control of 2 kinds of reset: power reset, system reset. The power on reset, known as a cold reset, resets the full system during a power up. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller. The resets can be triggered by an external signal, internal events and the reset generators. More information about these resets will be described in the following sections.

Power Reset

The power reset is generated by either an external reset as power on and power down reset (POR/PDR reset), or by the internal reset generator when exiting standby mode. The power reset sets all registers to their reset values. The power reset which active signal is low will be de-asserted when the internal LDO voltage regulator is ready to provide 1.2V power for GD32M531 series. The reset service routine vector is fixed at address 0x0000_0004 in the memory map.

System Reset

A system reset is generated by the following events:

1. A power reset (POWER_RSTn)
2. An external pin reset (NRST)
3. A window watchdog timer reset (WWDGT_RSTn)
4. A free watchdog timer reset (FWDGT_RSTn)
5. The SYSRESETREQ bit in Cortex®-M33 application interrupt and reset control register

is set (SW_RSTn)

6. Option byte loader reset (OBL_RSTn)

7. Reset generated when entering Standby mode when resetting nRST_STDBY bit in user option bytes (OB_STDBY_RSTn)

8. Reset generated when entering Deep-sleep mode when resetting nRST_DPSLP bit in user option bytes (OB_DPSLP_RSTn)

9. Low voltage 0 detect reset (LVD0_RSTn)

10. Low voltage 1 detect reset (LVD1_RSTn)

11. Low voltage 2 detect reset (LVD2_RSTn)

12. Loss-of-HXTAL reset (LOH_RSTn)

13. Loss-of-PLL reset (LOP_RSTn)

14. CPU lockup reset (LOCKUP_RSTn)

LVD_RSTn / LOH_RSTn / LOP_RSTn / LOCKUP_RSTn should be enable by software.

A system reset resets the processor core and peripheral IP components except for the SW-DP controller.

A system reset pulse generator guarantees low level pulse duration of 20 μs for each reset source (external or internal reset).

Figure 2-8. The system reset circuit
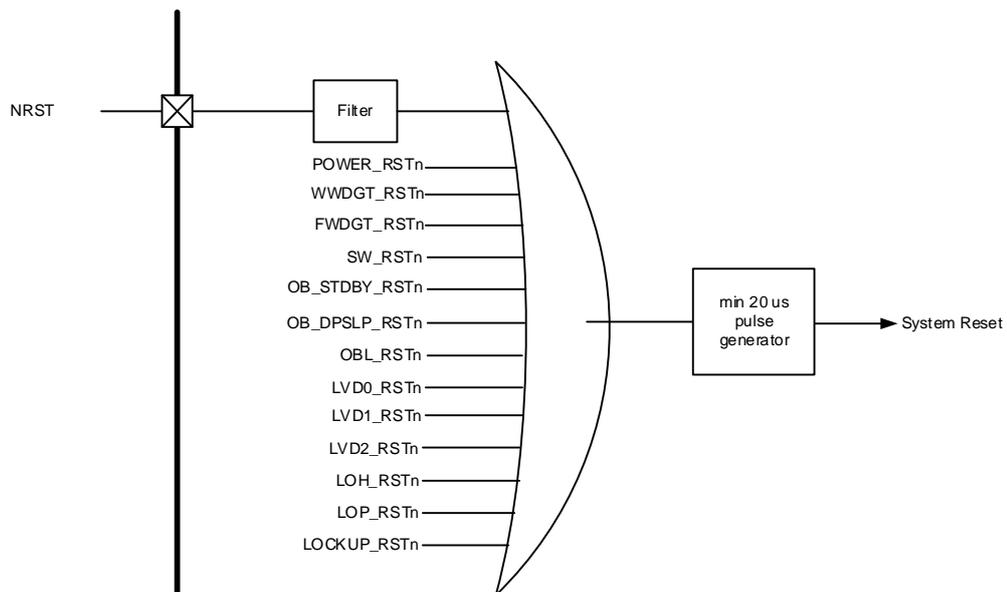
Note: It is conditional for LVD_RSTn / LOH_RSTn / LOP_RSTn / LOCKUP_RSTn to generate a reset. LVD0RSTEN / LVD1RSTEN / LVD2RSTEN in PMU section and LOHRSTEN / LOPRSTEN / LOCKUPRSTEN bit in Reset source/clock register (RCU_RSTSCK) must be set.

Figure 2-9. Recommend External Reset Circuit

GD32M531x
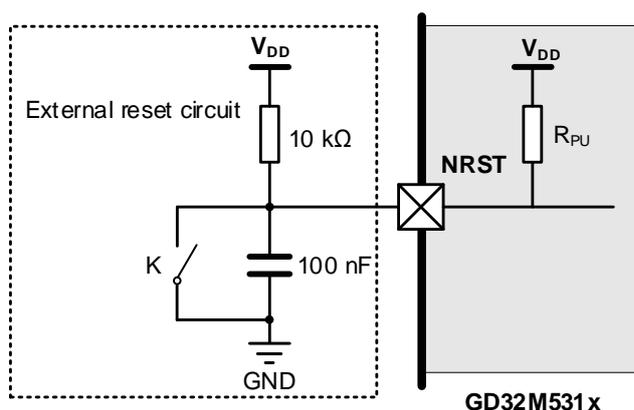
Note:

1. The pull-up resistor is recommended to be 10kΩ, so that voltage interference will not cause the chip to work abnormally;
2. If the influence of static electricity is considered, an ESD protection diode can be placed at the NRST pin;
3. Although there is a hardware POR circuit inside the MCU, it is still recommended to add an external NRST reset resistor-capacitor circuit;
4. If the MCU starts abnormally (due to voltage fluctuations, etc.), the capacitance value of NRST to ground can be appropriately increased, and the MCU reset completion time can be extended to avoid the abnormal power-on sequence area.

2.3. Clock

The GD32M531x series has a complete clock system. You can select a proper clock source according to different applications.Main features of the clock:

- 1 to 24 MHz High speed crystal oscillator (HXTAL)
- Internal 32 MHz RC oscillator (IRC32M)
- Internal 32 kHz RC oscillator (IRC32K)
- PLL clock source can be HXTAL or IRC32M
- HXTAL clock monitor

Figure 2-10. Clock tree
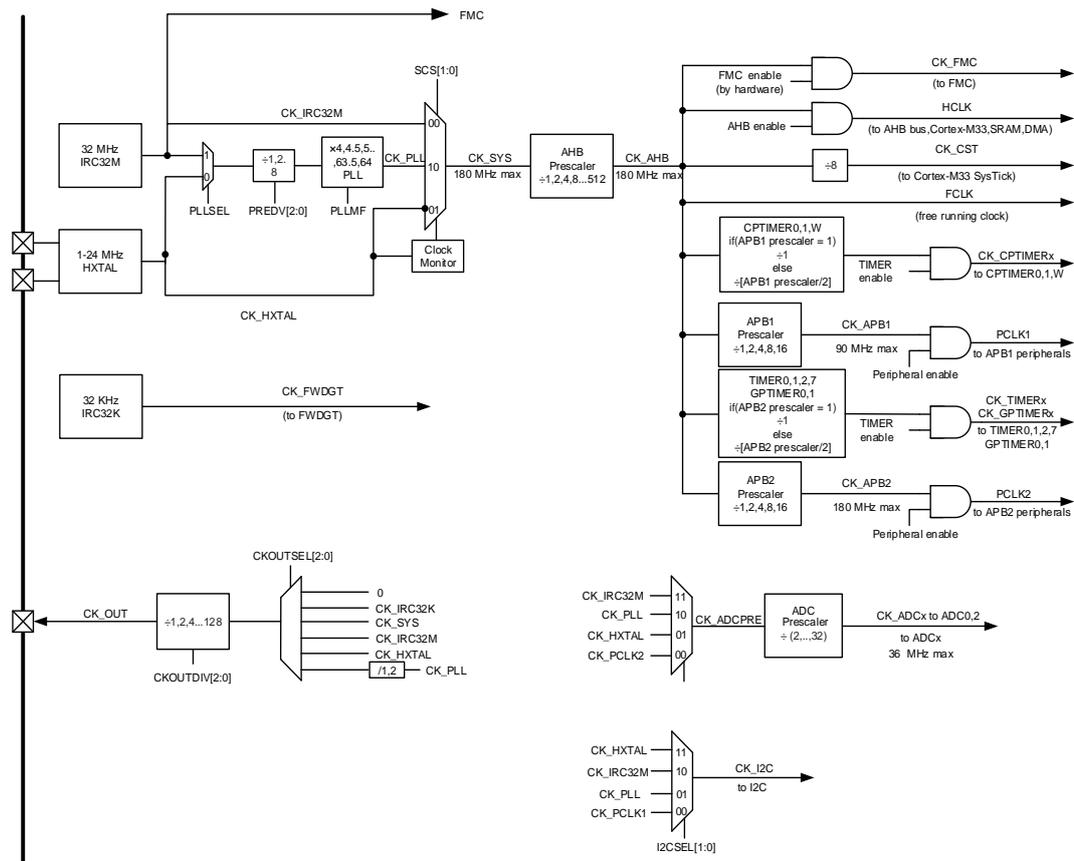
Note: The GD32M531x series MCU has a maximum master frequency of 180 MHz.

2.3.1. High Speed Crystal Oscillator (HXTAL)

1-24 MHz external high speed crystal oscillator (passive crystal) to provide a precise master clock for the system.The crystal of this particular frequency must be placed close to the HXTAL pin, and the external resistors and matching capacitors connected to the crystal must be adjusted according to the selected oscillator parameters.Control register RCU_CTL's HXTALBPS and HXTALEN positions' 1 'to enable external bypass mode.When the bypass input is used, the signal is connected to OSCIN and OSCOUT remains in the suspended state. In this case, the CK_HXTAL is the external clock that drives the OSCIN pin.Select the HXTAL frequency range by using the HXTALSCAL bit in the control register (RCU_CTL).If the HXTAL frequency is higher than 10 MHz, the HXTALSCAL must be placed at position 1.

Figure 2-11. HXTAL clock source

Figure 2-12. HXTAL clock source in bypass mode
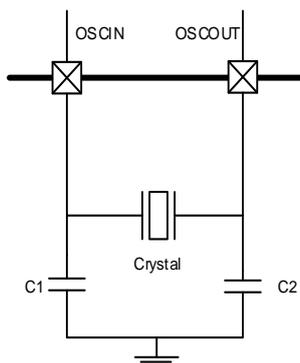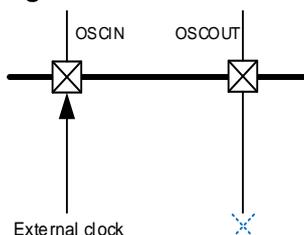

Note:

1. When using the bypass input, the signal is input from OSC_IN, and OSC_OUT remains floating.

2. For the size of the external matching capacitor, please refer to the formula: $C_1 = C_2 = 2*(C_{LOAD} - C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, with a typical value of 10pF. When it is recommended to use an external high-speed crystal, try to choose a crystal load capacitance of about 20pF, so that the external matching capacitors C_1 and C_2 can be 20pF, and the PCB layout should be as close to the crystal pin as possible.

3. C_S is the parasitic capacitance on the PCB board traces and IC pins. The closer the crystal is to the MCU, the smaller the C_S, and vice versa. Therefore, in practical applications, when the crystal is far away from the MCU, causing the crystal to work abnormally, the external matching capacitor can be appropriately reduced.

4. When using an external high-speed crystal, it is recommended to connect a 1MΩ resistor in parallel at both ends of the crystal to make the crystal easier to vibrate.

5. Accuracy: external active crystal oscillator > external passive crystal > internal IRC32M.

6. When the active crystal oscillator is used normally, Bypass will be turned on. At this time, the high level is required to be no less than 0.7 V_{DD}, and the low level is no more than 0.3 V_{DD}.

7. The traces connecting the resonator to the MCU clock pins may cause inconsistent lengths of the traces connected to the OSC_OUT and OSC_IN pins due to the space constraints of the PCB layout. This will make the stray capacitances introduced by the two PCB traces inconsistent, so that the load capacitances on both sides of the resonator cannot be equal in value, and there needs to be a difference to match the actual PCB board. In this case, it is recommended to contact the resonator manufacturer to calculate the actual value.

2.3.2. Internal High Speed Oscillator clock (IRC32M)

The Internal 32 MHz RC oscillator, IRC32M, has a fixed frequency of 32 MHz and is the default clock source selection for the CPU when the device is powered up. The IRC32M oscillator provides a lower cost type clock source as no external components are required. The IRC32M RC oscillator can be switched on or off using the IRC32MEN bit in the control register, RCU_CTL. The IRC32MSTB flag in the control register, RCU_CTL is used to indicate if the internal RC oscillator is stable. The start-up time of the IRC32M oscillator is shorter than the HXTAL crystal oscillator. An interrupt can be generated if the related interrupt enable bit, IRC32MSTBIE, in the interrupt register, RCU_INT, is set when the IRC32M becomes stable. The IRC32M clock can also be used as the PLL input clock.

The frequency accuracy of the IRC32M can be calibrated by the manufacturer, but its operating frequency is still less accurate than HXTAL. The application requirements, environment and cost will determine which oscillator type is selected.

If the HXTAL or PLL is the system clock source, to minimize the time required for the system to recover from the Deep-sleep Mode, the hardware forces the IRC32M clock to be the system clock when the system initially wakes-up.

2.3.3. Clock Output Capability (CKOUT)

The Clock output function outputs clocks from 32kHz to 180MHz.By setting the CK_OUT clock source select bit in the clock configuration register RCU_CFG0, the CKOUTSEL is able to select different clock signals.The corresponding GPIO pin should be configured to multiplexed function I/O (AFIO) mode to output the selected clock signal.

Table 2-2. Clock source select

Clock Source Selection bits	Clock Source
000	No Clock
001	Reserved
010	CK_IRC32K
011	Reserved
100	CK_SYS
101	CK_IRC32M
110	CK_HXTAL
111	CK_PLL or CK_PLL/8

The CK_OUT frequency can be reduced by a configurable binary divider, controlled by the CKOUTDIV[2:0] bits, in the configuration register 0(RCU_CFG0).

2.3.4. HXTAL Clock Monitor (CKM)

The HXTAL clock monitor function is enabled by the HXTAL clock monitor enable bit, CKMEN, in the control register, RCU_CTL. This function should be enabled after the HXTAL start-up

delay and disabled when the HXTAL is stopped. Once the HXTAL failure is detected, Loss-of-HXTAL reset will generate decided by LOHRSTEN in the reset source /clock register, RCU_RSTSCK. Or an NMI Interrupt may generate decided by the CKMNMIIE bit in SYSCFG_CFG3 register.

If LOHRSTEN is 0, the HXTAL clock stuck flag, CKMIF, in the interrupt register, RCU_INT, will be set and the HXTAL failure event will be generated. The HXTAL will be automatically disabled. This failure interrupt is connected to the Non-Maskable interrupt, NMI, of the Cortex®-M33. If the HXTAL is selected as the clock source of CK_SYS or PLL, the HXTAL failure will force the CK_SYS source to IRC32M and the PLL will be disabled automatically.

If LOHRSTEN is 1, Loss-of-HXTAL reset will generate.

2.4. Startup Configuration

The GD32M531 devices provide two kinds of boot sources which can be selected by the BOOT-PN6. The details are shown in the following table. The value on the two pins is latched on the 4th rising edge of CK_SYS after a reset. It is up to the user to set the BOOT-PN6 pin after a power-on reset or a system reset to select the required boot source. Once the pin has been sampled, it is free and can be used for other purposes.

After the power-on sequence or system reset, the Arm® Cortex®-M33 processor gets the top of the stack value from the address 0x0000 0000 and the base address of the startup code from 0x0000 0004.It then starts executing the code from the base address of the startup code.

Depending on the selected boot source, either the main Flash (storage starting at 0x0800 0000) or system memory (storage starting at 0x1FFF E000) is mapped to boot memory space starting at address 0x0000 0000.

The embedded Bootloader is stored in the system storage space and is used to reprogram the FLASH memory.Bootloader can use UART2(PF9/PF10, AF6), UART4(PF11/PF12, AF7), UART3(PF13/PF14, AF7) Slave mode and external interaction.

Table 2-3. Boot modes

BOOT mode	BOOT-PN6
System Memory	0
Main Flash Memory	1

Figure 2-13. Recommend BOOT Circuit Design
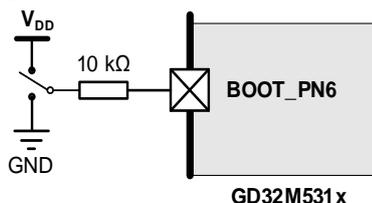
Note:

1.   After the MCU is running, if the BOOT state is changed, it will take effect after the system

is reset. MCU.

2.5.   Typical Peripheral Modules

2.5.1.   GPIO Circuit

The GD32F5xx supports up to 53 general purpose I/O pins (GPIOs), which are PA0 ~ PA1, PA9, PB0 ~ PB2, PB14 ~ PB15, PC0 ~ PC12, PD4 ~ PD14, PE8 ~ PE14, PF8 ~ PF14, PG11, PA0 ~ PB2, PD4 ~ PC12, PD4 ~ PD14.PG13, PG15, PN2, PN5, PN6, PN7.

Each on-chip device uses it to implement logical input/output functions.Each GPIO port has associated control and configuration registers to meet the needs of the specific application.External interrupts on GPIO pins have associated control and configuration registers in the Interrupt/Event Controller (EXTI).*Figure 2-14 shows the basic structure of the GPIO port. Basic structure of standard IO*.

Figure 2-14. Basic structure of standard IO
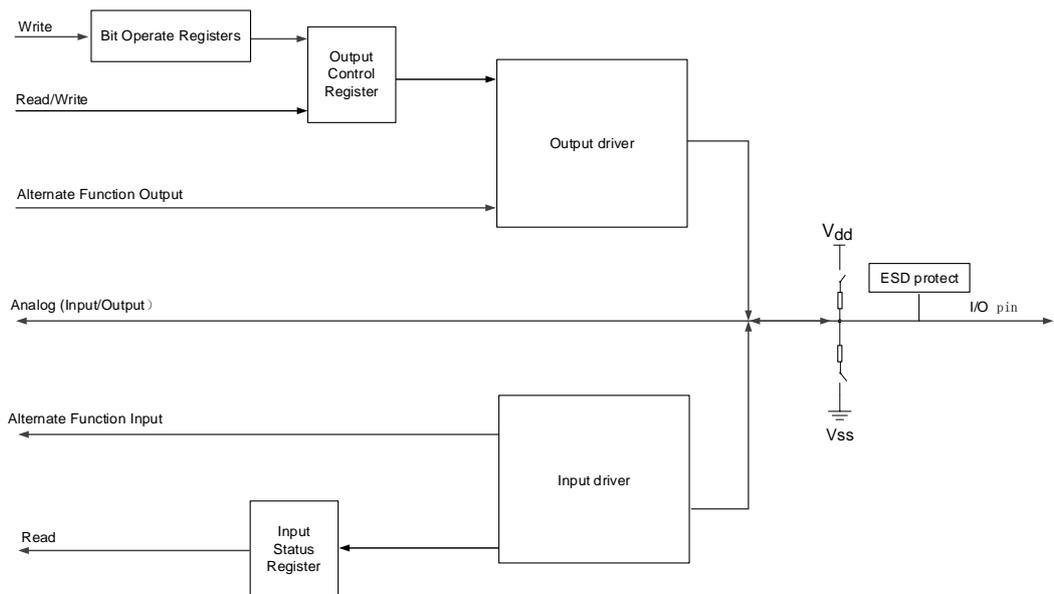
Note:

1.   The IO port is divided into 5V tolerant a The IO port is divided into 5V tolerance and non-5V tolerance. Except PF8, PF9 and PF10, the three pins are 5V tolerance, and the rest are non-5V tolerance. When the pin voltage is greater than VDD+0.3V, please use the 5V tolerance pin.

2.   When the 5V-tolerant IO port is directly connected to 5V, it is recommended that the IO port be configured in open-drain mode and externally pull up to work.

3.   After the IO port is powered on and reset, the default mode is floating input, and the level characteristics are uncertain. In order to obtain more consistent power consumption, it is recommended that all IO ports be configured as analog inputs and then modified to the corresponding mode according to application requirements (chip Ports that are not exported internally also need to be configured).
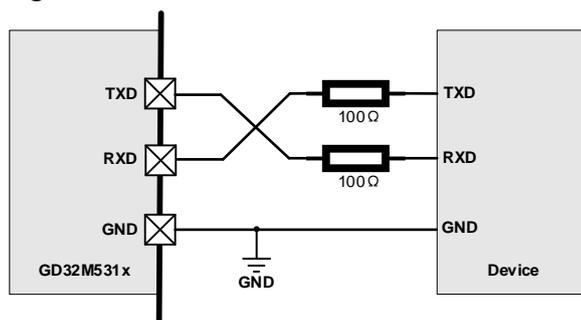
4. To improve EMC performance, it is recommended to pull up or pull down the unused IO pins by hardware.

2.5.2. UART Circuit

The GD32M531x series provides 4 UART channels (UART0, UART1, UART2, UART3).When using UART, pay attention to the cross-connecting pins, as shown in *Figure 2-15. The UART reference circuit* is for reference.

Figure 2-15. UART reference circuit

2.5.3. CAN Circuit

The GD32M531x series chip provides one CAN communication peripheral. *Figure 2-16 CAN reference circuit* for reference.

Figure 2-16. CAN reference circuit
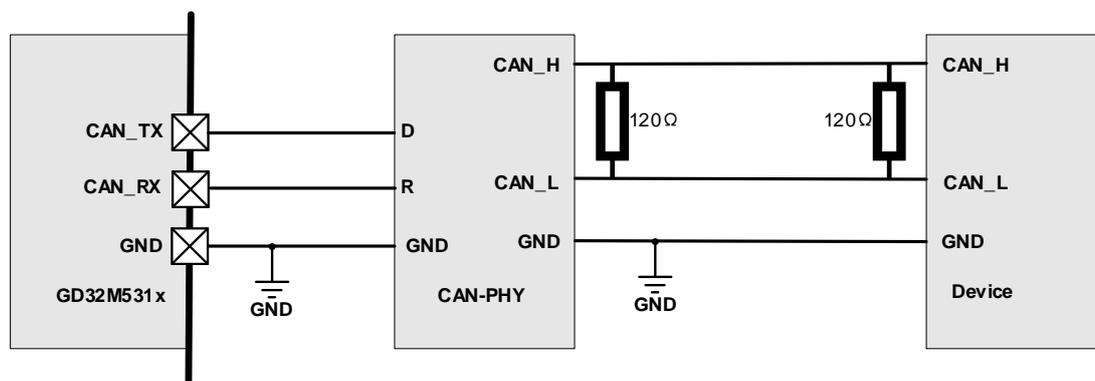
The two 120Ω impedance matching resistors in the figure above can determine the resistance value of the impedance matching resistor and whether it is needed according to the actual situation.

In CAN communication, impedance matching has three functions:
1. Improve anti-interference ability;
2. Prevent signal reflection and improve signal quality;
3. Ensure that the bus rising/falling edge is reached quickly.

2.5.4. I2C Circuit

The GD32M531x series chip provides one I2C peripherals, supporting standard speed (up to 100 KHz), fast (up to 400 KHz) and fast + mode (up to 1 MHZ, which must be enabled in SYSCFG_CFG1 with I2CFMPEN).Both SDA and SCL are bidirectional lines, and all I2C channels can operate in either host or slave mode.It also supports multi-host mode.I2C interface module also supports DMA mode, which can effectively reduce the burden of CPU.

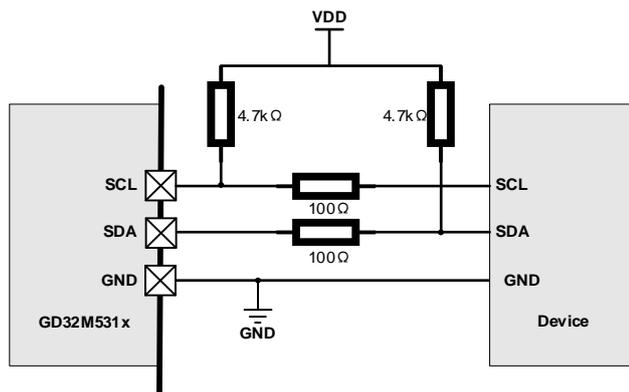**Figure 2-17. I2C reference circuit**

If you need to connect to the output pole of the I2C bus device, take into account the line and, the idle level needs to be set high.

For OC/OD circuits, the circuit reaction speed and power consumption are determined by the pull-up resistance.The pull-up resistance is small, the reaction speed is fast, the signal edge is steep, that is, the signal quality is good, but the power consumption is high.On the contrary, if the pull-up resistance is large, the circuit reaction speed is slow, the signal edge is relatively flat, that is, the signal quality is poor, but the power consumption is low.

Table 2-4. Reference relation between transmission mode and pull-up resistance

Transmission Mode	Pull-up（kΩ）
Standard mode	4.7
Fast mode	2.2
Fast mode plus	1.5

Considering actual wiring of I2C and complex conditions of the circuit board, the resistances of the pull-up resistor listed in *错误!未找到引用源。* are for reference only. In actual use, a string set can be installed between SDA and SCL to adjust the signal quality.

2.5.5. SPI Circuit

The GD32M531x series chip provides a 1-way SPI, where the SPI can be configured with registers to expand to a four-wire mode.With the exception of the 4-wire mode SPI, SPI channels can operate in either host or slave mode.When SPI works in four-wire mode, it can only be used as the host, not as the slave.It can be used as a slave machine when not working in 4-wire mode.

Figure 2-18. SPI four-wire mode reference circuit
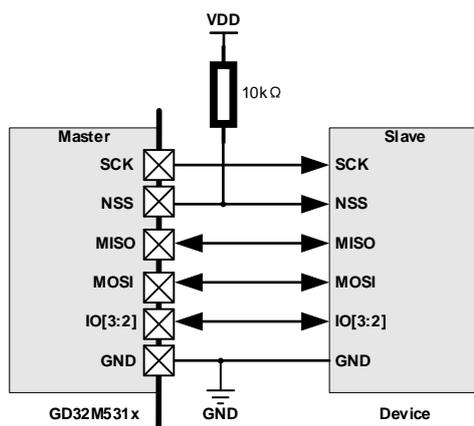
The above figure can only be referred to when the SPI works in 4-wire mode, and the GD32M531x series chip can only serve as the host.For the general SPI, after proper configuration of the register, there are the following four typical working mode connection methods for reference.In the following four operating modes, the GD32M531x series chip can be used as a host or slave.

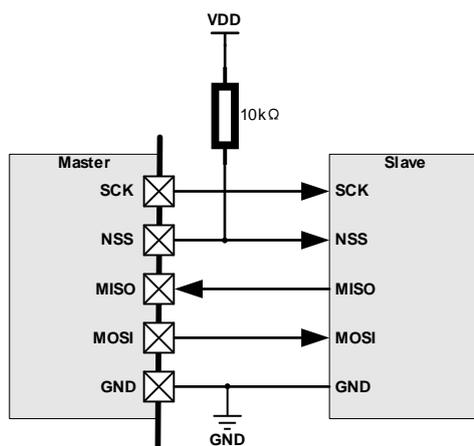**Figure 2-19. SPI typical full duplex mode connection**

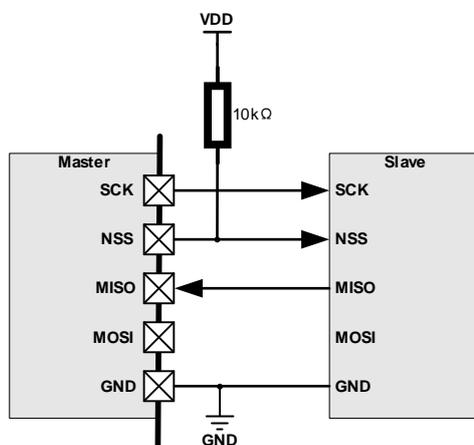**Figure 2-20. Typical simplex connection of SPI (host: receive, slave: transmit)**

Figure 2-21. Typical simplex connection of SPI (host: receive, slave: transmit)
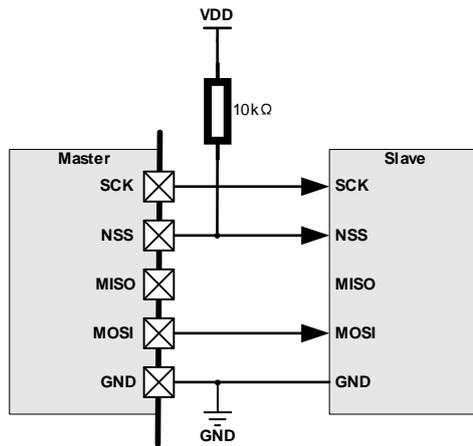
Figure 2-22. Typical bidirectional cable connection of SPI
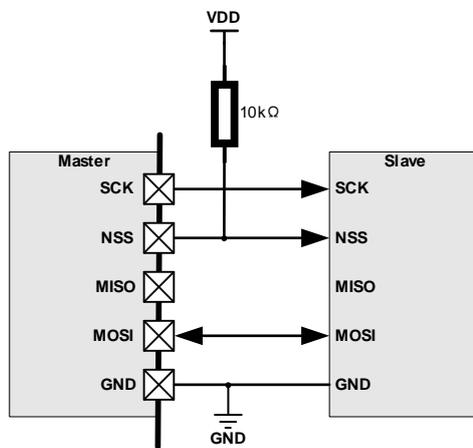
2.5.6. ADC Circuit

The GD32M531x series MCU integrates two 12-bit successive approximation analog-to-digital converter modules (ADC0/1) on chip and operates independently.The ADC0 can sample analog signals from seven external channels.ADC1 can sample analog signals from 10 external channels and 2 internal channels (V_{REFINT}, V_{SENSE}).In each ADC module, these selected sampling channels support a variety of scanning modes: Group_pri1 group single scan mode, Group_pri1 group continuous scan mode, or multi-group scan mode.After each channel is sampled and converted, the conversion results can be stored in the corresponding data register according to the least significant bit (LSB) alignment or the most significant bit (MSB) alignment.

If the ADC collects the external input voltage during use, if the sampled data fluctuates significantly, which may be due to interference caused by power supply fluctuations, it can be calibrated by sampling the internal V_{REFINT} to invert the external sampled voltage.

When designing the ADC circuit, it is recommended to place a small capacitor at the ADC input pin, and it is recommended to place a small capacitor of 500 pF.

Table 2-5. ADC internal signals

| Internal signal name	Signal type	Description
V_{REFINT}	Input	Internal voltage reference output voltage (only for ADC2)
V_{SENSE}	Input	Internal temperature sensor output voltage (only for ADC2)

Table 2-6. ADC pins definition

Signal name	Signal type	Description
V_{DDA}/V_{REFP}	Input, analog power supply	Analog power supply, positive reference voltage, 2.7V ≤V_{DDA}/V_{REFP} ≤ 5.5V.
V_{SSA}/V_{REFN}	Input, analog power ground	Analog, negative reference voltage, equal to VSS
ADCx_INy	Input, analog signal	7 external analog inputs for ADC0 10 external analog inputs for ADC2

Figure 2-23. ADC Acquisition Circuit Design
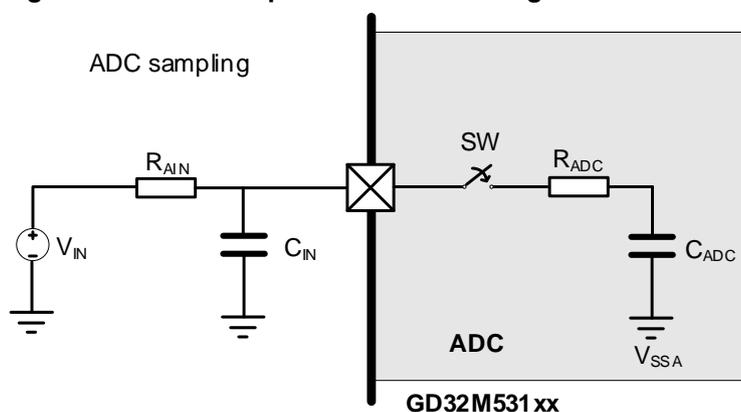
In order to obtain better conversion results, it is recommended to reduce the frequency of fADC as much as possible, select a larger sampling period as much as possible, and minimize the input impedance when designing the external circuit. If necessary, the input impedance is reduced by using the op amp follower.When f_{ADC} = 36 MHz, the relation between input impedance and sampling period is as follows.

Table 2-7. f_{ADC} = 36MHz sampling period and external input impedance

T_s (cycles)	t_s (us)	$R_{AIN\ max}$ (kΩ)
2.5	0.069	0.39
7.5	0.208	2.18
13.5	0.375	4.33
28.5	0.791	9.69
41.5	1.15	14.35
55.5	1.54	19.36
71.5	1.98	25.08
255.5	7.09	90.92

2.5.7. Internal temperature sensor

A temperature sensor is integrated into the GD32M531x series MCU.The output voltage of the temperature sensor varies linearly with the temperature.To ensure accurate temperature measurement, the ADC needs to be provided with an accurate, low-temperature reference voltage V_{DDA}/V_{REFP}.

The output voltage of the temperature sensor changes linearly with temperature, and due to the diversity of the chip production process, the deviation of the temperature change curve will vary from chip to chip (up to 45°C).Internal temperature sensors are more suitable for detecting changes in temperature than for measuring absolute temperature. If an accurate temperature measurement is required, an external temperature sensor should be used to calibrate this offset.

To use the temperature sensor:
1. Configure the GPxTEMP bit in ADC_CHSEL0/1 register and the sampling time (t_{s_temp} μs or longer) for the channel by SPTTEMP[7:0] bits in ADC_SAMPR1 register.
2. Start the ADC conversion by the triggers.
3. Read the temperature data ($V_{temperature}$) in ADC_TEMPDATA register, and get the temperature with the following equation.

$$\text{Temperature (°C)} = \frac{(V_{temperature}-V_{-40})*(-40-105)}{V_{-40}-V_{105}}-40$$

V_{-40}: internal temperature sensor output voltage at -40°C, the typical value and factory calibration value address please refer to the datasheet (TS_CAL1).

V_{105}: internal temperature sensor output voltage at 105°C, the typical value and factory calibration value address please refer to the datasheet (TS_CAL2).

2.5.8. DAC Circuit

The digital/analog converter of GD32M531x series MCU can convert 12-bit digital data to voltage output on external pins.Data can be in 8-bit or 12-bit mode, left-justified or right-justified.When external triggering is enabled, DMA can be used to update input digital data.At the output voltage, you can make use of enabling the DAC output buffer to obtain higher drive capability.The two channels of each DAC can work independently or concurrently.

Table 2-8. DAC I/O description

signal name	Description	Signal type
V_{DDA}/V_{REFP}	Analog power supply	Input, analog supply
V_{SSA}/V_{REFN}	Ground for analog power supply	Input, analog supply ground
DACy_OUTx	DACx analog output	Analog output signal

Before enabling the DAC module, the GPIO port should be configured in analog mode.

2.5.9. CMP Circuit

The GD32M531x series MCU integrates four rail-to-rail comparators (CMP).Multiple input and output sources can be configured for each comparator. The CMP0 is used as an example, as shown in *Figure 2-24.The comparator block diagram* shows its internal structure:

Figure 2-24. The comparator block diagram
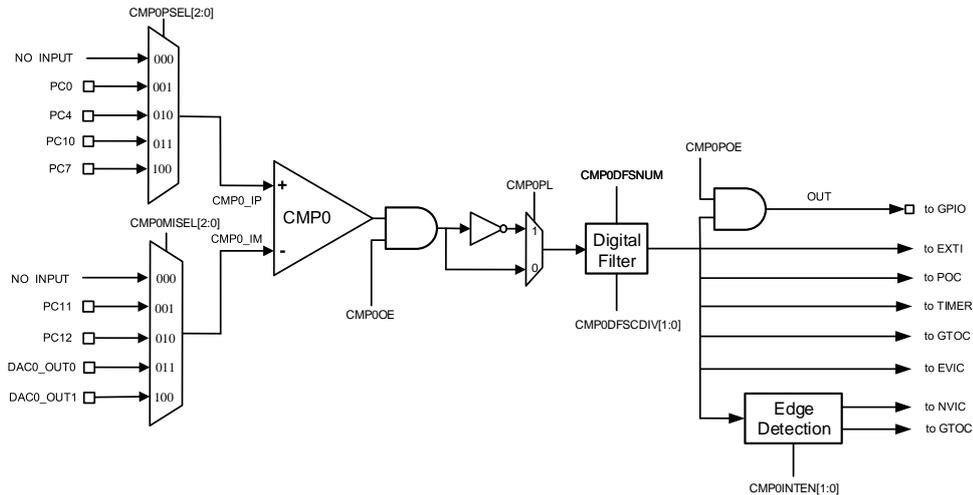
Before being selected as a comparator input, the corresponding pins must be configured in analog mode.The output of the comparator can also achieve both internal and external outputs. *Table 2-9. CMP Input and Output Summary* describes the input and output of the CMP in detail.

Table 2-9. CMP input and output summary

	CMP0	CMP1	CMP2	CMP3
CMP In-phase inputs are connected to I/O	PC0 PC4 PC10 PC7	PC1 PC5 PC11 PC0	PC2 PC6 PC12 PC3 PC10	PC3 PD2 PD4 PD5 PC9
CMP Inverting input is connected to I/O	PC11 PC12			
CMP The inverting input is connected to the internal signal	DAC0_OUT0 DAC0_OUT1			
CMP Output connection to I/O	PA0	PA1	PB2	PB1
CMP Output connection to EXTI	●			
CMP Output connection to NVIC	●			
CMP Output connection	●			

	CMP0	CMP1	CMP2	CMP3
to POC				
CMP Output connection to GTOC		•		
CMP Output connection to EVIC		•		
CMP Output connection to the internal signal	TIMER0、TIMER1、TIMER2、TIMER7			
CMP output (Motor control protection)	TIMER0 BREAK TIMER7 BREAK			

In order to avoid the false output caused by noise signal, the programmable hysteresis function is designed, and the hysteresis voltage is controlled by configuring the control status register.This function can be turned off when it is not needed.*__Comparator lag is shown in Figure 2.25__*

Figure 2-25. comparator hysteresis
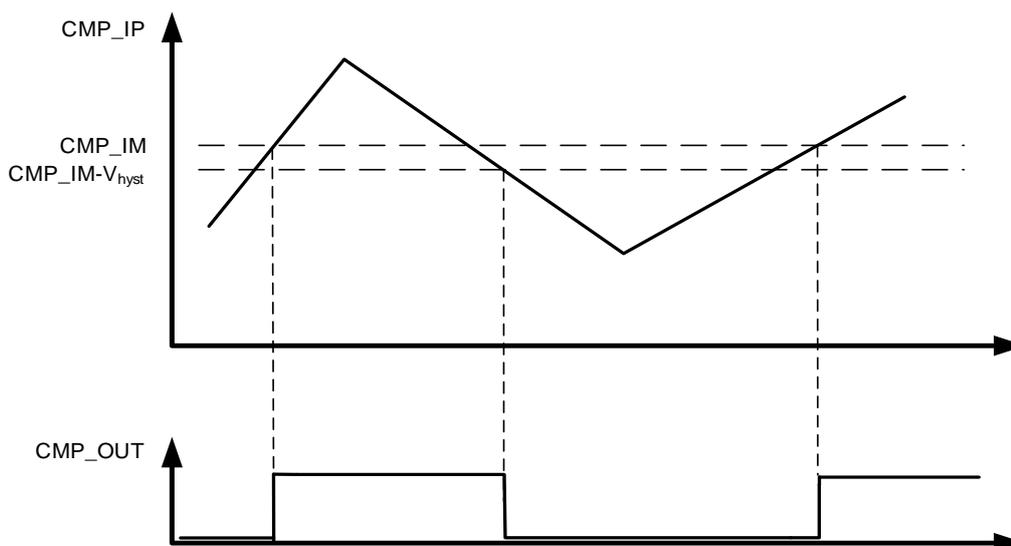
2.5.10. Standby mode wake-up circuit

The standby mode is also based on the Cortex®-M33 SLEEPDEEP mode.In standby mode, the entire 1.2V domain is shut down, and the LDO, including IRC32M, HXTAL, and PLL, are also shut down.Before entering the standby mode, set the SLEEPDEEP position 1 of the Cortex®-M33 system control register, set the STBMOD position 1 of the PMU_CTL register, clear the WUF bit of the PMU_CS register, and then execute the WFI or WFE command to enter the standby mode.The STBF bit status of the PMU_CS register indicates whether the MCU has entered standby mode.The standby mode has three wake sources, including an external reset from the NRST pin, a FWDGT reset, and a rising edge from the WKUP pin.The

standby mode provides the lowest power consumption but the longest wake-up time.In addition, once in standby mode, the contents of the SRAM and 1.2V power domain registers are lost. When you exit standby mode, a power-on reset occurs, after which the Cortex®-M33 executes the command code from the address 0x0000 0000.

Figure 2-26. Recommend Standby external wake-up pin circuit design
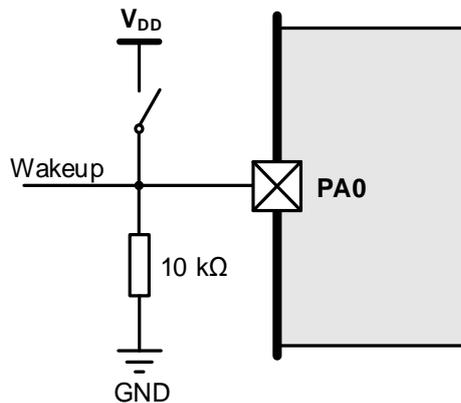
Note: In this mode, attention should be paid to the circuit design. If there is a series resistance between the WKUP pin and V_{DD}, additional power consumption may be added.

2.6.   Download the debug circuit

GD32M531x series cores support JTAG debug interface and SWD debug interface. The JTAG interface standard is a 20-pin interface, including 5 signal interfaces, and the SWD interface standard is a 5-pin interface, including 2 signal interfaces. The ONE-LINE interface is a standard 4-pin interface with one signal interface.

The GD32M531Cx (LQFP48) supports two debugging interfaces, SWD and ONE-LINE.

The GD32M531Rx (LQFP64) supports three debugging interfaces, JTAG debugging interface, SWD debugging interface and ONE-LINE, details are as follows:

Table 2-10. JTAG download debug interface assignment

Alternate function	GPIO port
JTMS	PG14
JTCK	PG12
JTDI	PG13
JTDO	PG11
NJTRST	PG15

Note: After reset, the debug related ports are in input PU/PD mode, where:
PG13：JTDI is in pull-up mode.
PG12：JTCK/SWCLK in pull-down mode.
PG14：JTMS/SWDIO in pull-up mode.

PG15：NJTRST is in pull-up mode.

PG11：JTDO is floating mode.
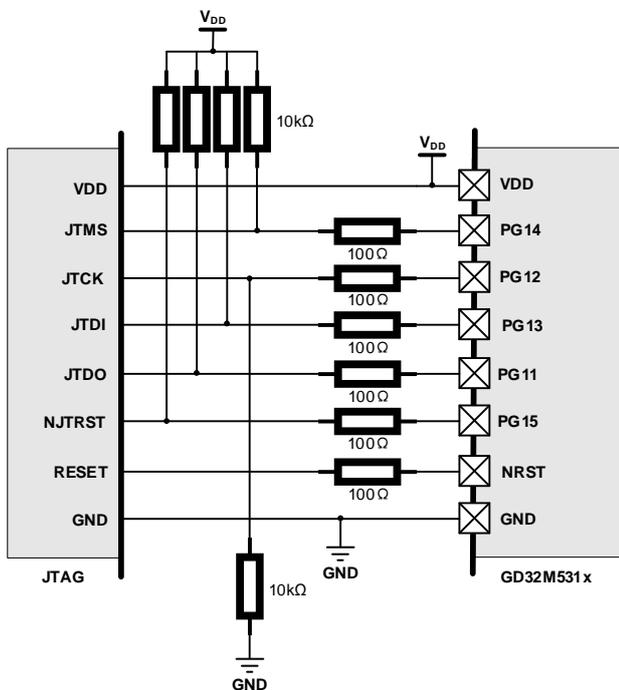
Figure 2-27. Recommend JTAG Wiring Reference Design

Table 2-11. SWD Download Debug Interface Assignment

Alternate function	GD32M531Cx GPIO port	GD32M531Rx GPIO port
SWDIO	PG13	PG14
SWCLK	PN2	PG12

Note: After reset, the debug related ports are in input PU/PD mode, where:

PN2/PG12：JTCK/SWCLK in pull-down mode.

PG13/PG14：JTMS/SWDIO in pull-up mode.

Figure 2-28. Recommend SWD Wiring Reference Design
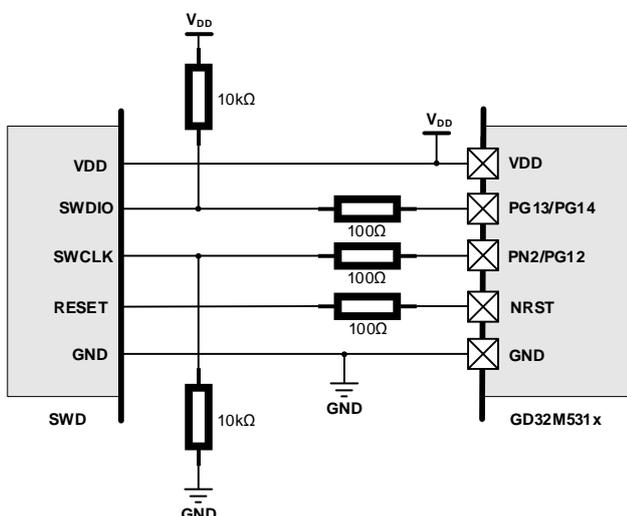
There are several ways to improve the reliability of SWD download and debugging communication and enhance the anti-interference ability of download and debugging.

1. Shorten the length of the two SWD signal lines, preferably within 15cm.
2. Weave the two SWD wires and the GND wire into a twist and twist them together.
3. Connect separately tens of pF small capacitors in parallel between the two signal lines of the SWD and the ground.
4. Any IO of the two signal lines of SWD is connected in series with a 100Ω ~ 1kΩ resistor.

Table 2-12. ONE-LINE Download Debug Interface Assignment

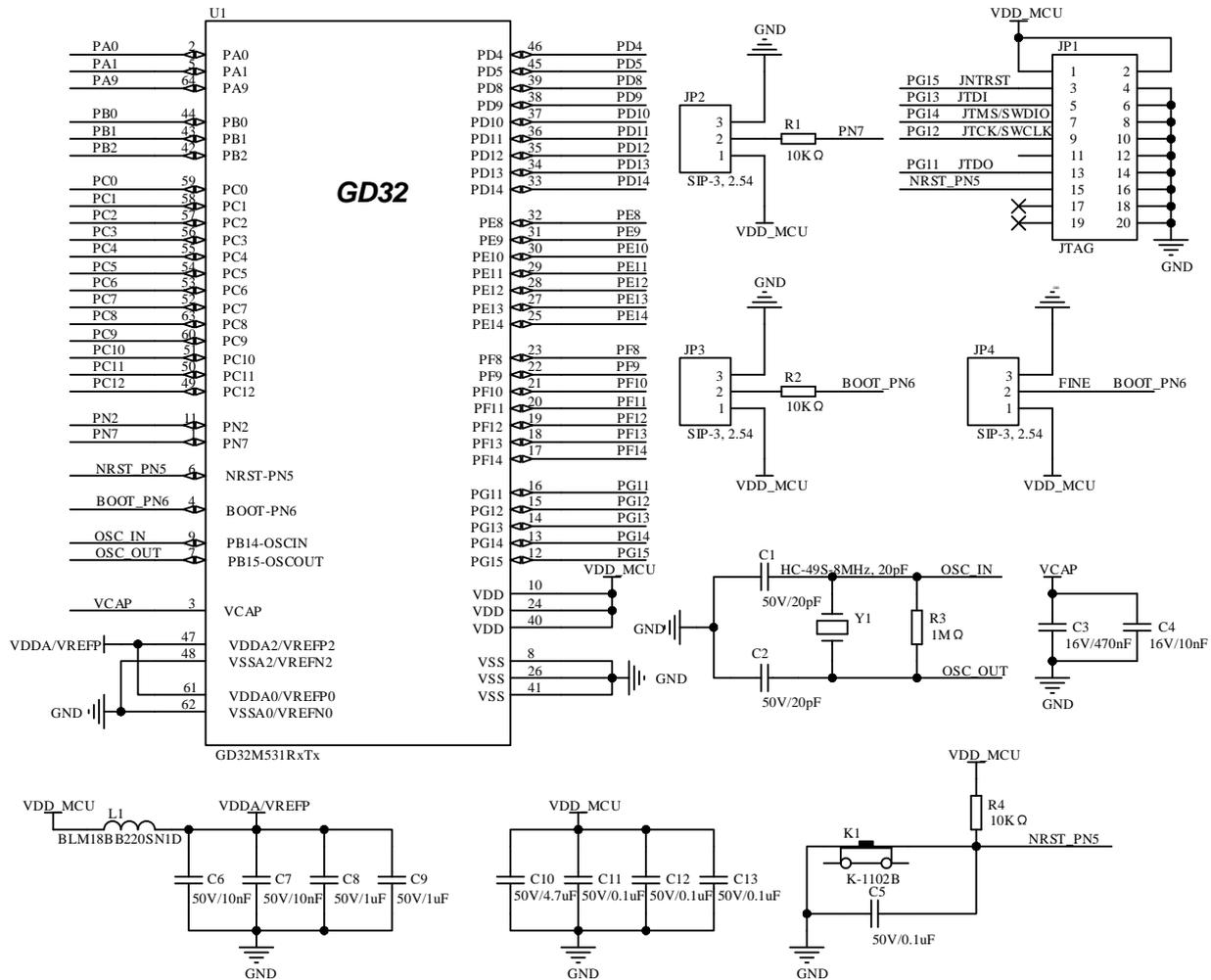| Alternate function	GPIO port
ONE-LINE	BOOT-PN6

Note: After the reset, the debugging port is in PU/PD mode. BOOT-PN6: ONE-LINE is in pull-up mode.

Figure 2-29. Recommend ONE-LINE Wiring Reference Design
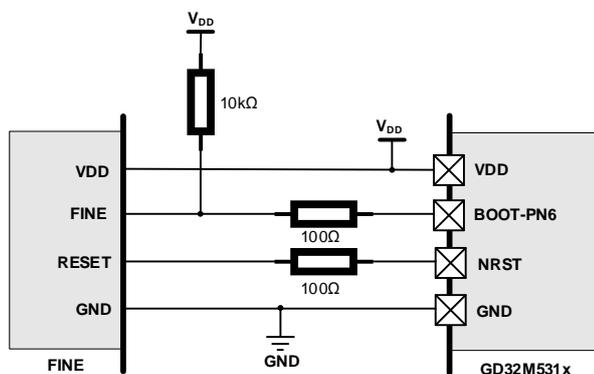
2.7. Reference Schematic Design

**Figure 2-30. GD32M531x Recommend Reference Schematic Design**

3. PCB Layout Design

In order to enhance the functional stability and EMC performance of the MCU, it is not only necessary to consider the performance of the supporting peripheral components, but also the PCB Layout. In addition, when conditions permit, try to choose a PCB design solution with an independent GND layer and an independent power supply layer, which can provide better EMC performance. If conditions do not allow, independent GND layer and power supply layer cannot be provided, then it is also necessary to ensure a good power supply and grounding design, such as making the GND plane under the MCU as complete as possible. For packages with EPAD, it is recommended that EPAD be grounded on the PCB Layout.

In applications with high power or strong interference, it is necessary to consider keeping the MCU away from these strong interference sources.

Figure 3-1. GD32M531x Recommended Layout Reference design
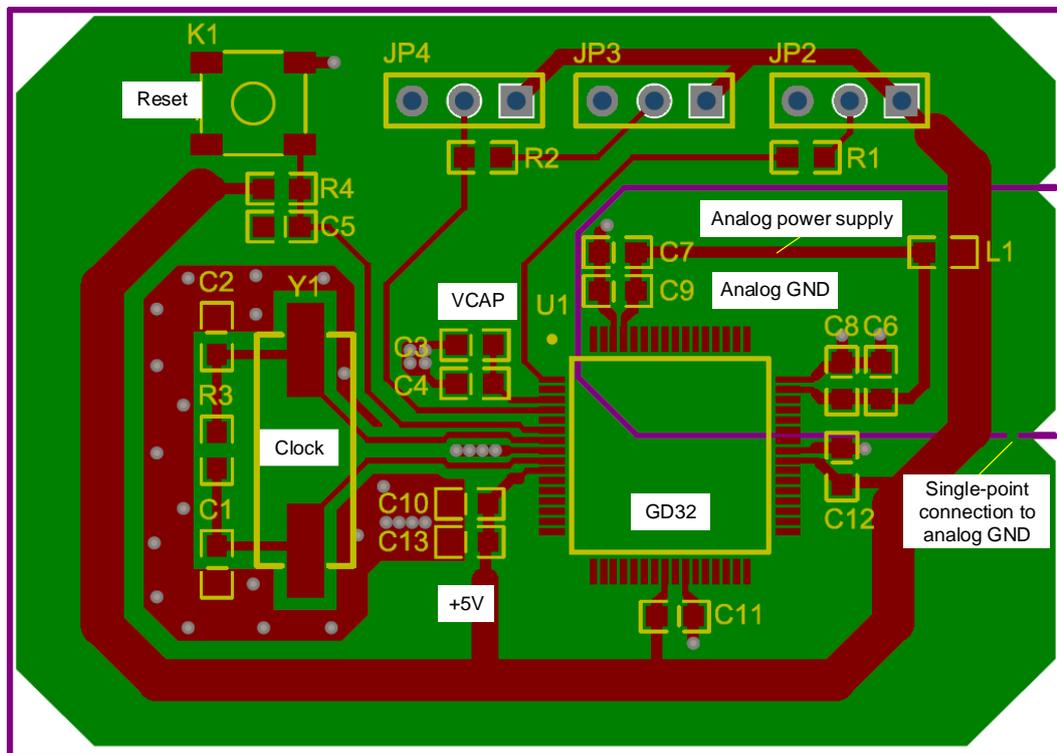
3.1. Power Supply Decoupling Capacitors

The GD32M531x series power supply has two power supply pins: VDD and VDDA/VREFP. The 100nF decoupling capacitor can be made of ceramic, and it is necessary to ensure that the position is as close to the power supply pin as possible. The power trace should try to make it pass through the capacitor first and then reach the MCU power pin, It is recommended to punch holes near the capacitor pad to connect with GND.

Figure 3-2. Recommend Power Pin Decoupling Layout Design
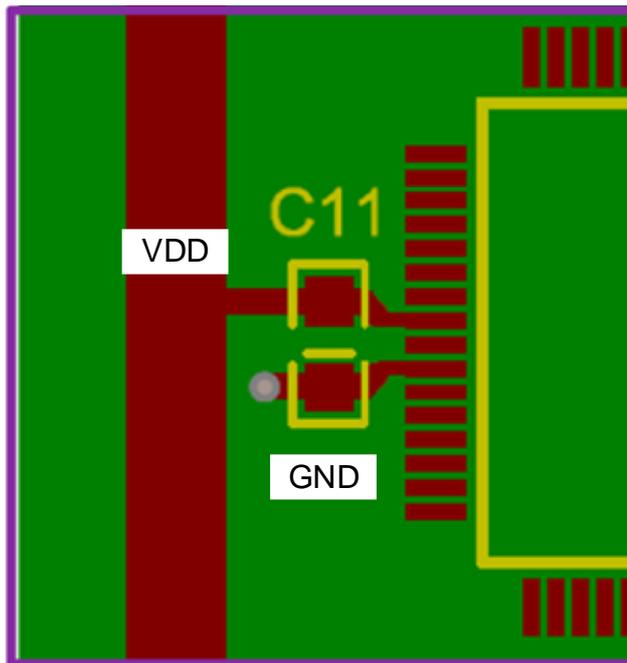
The VCAP pin of the GD32M531x series must be externally connected to the ground capacitor, 470 nF + 1 nF ceramic MLCC capacitor is recommended, and the wiring length between the VCAP pin and the capacitor, a and b should be less than or equal to 8mm, and less than or equal to 4mm if conditions permit.If the wiring length between the VCAP pin and the capacitor is greater than 8mm, the wiring should be designed so that the parasitic resistance is less than 1Ω.

Figure 3-3. The VCAP pin decoupled Layout design is recommended
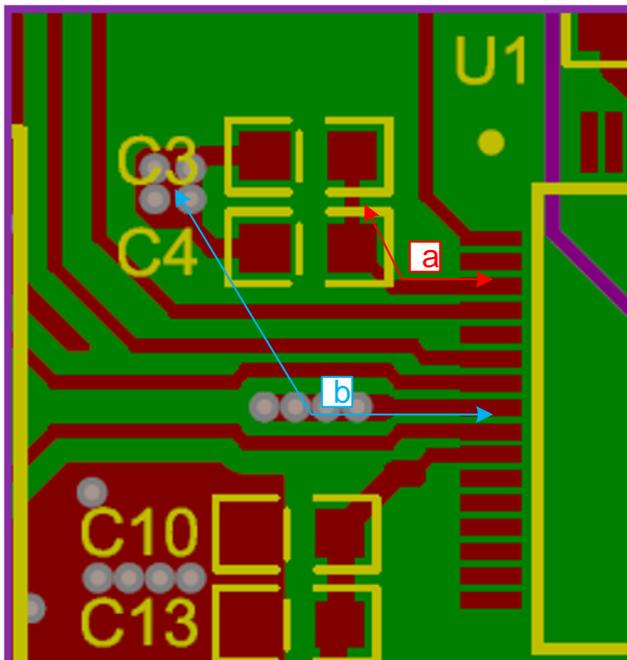
3.2. Clock Circuit

GD32M531x series clocks have HXTAL and LXTAL, and the clock circuit (including crystal or crystal oscillator and capacitor, etc.) is required to be placed close to the MCU clock pin, and the clock trace should be wrapped by GND as much as possible.

Figure 3-4. Recommended clock pin Layout (passive crystal)
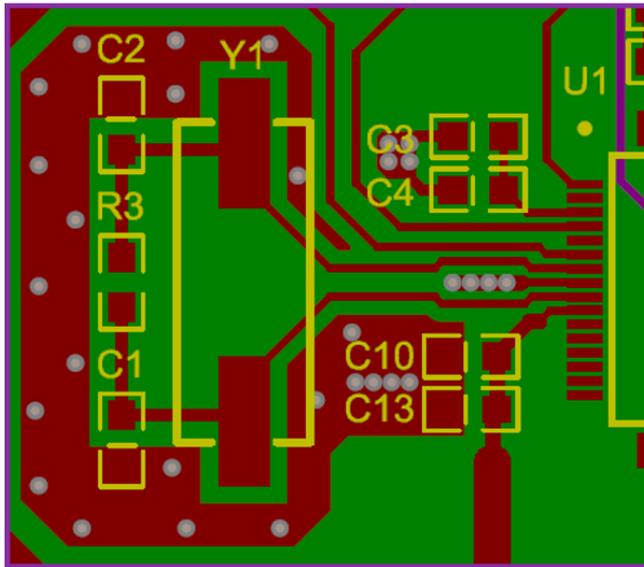
Note:

1. The crystal should be as close to the MCU clock pin as possible, and the matching capacitor should be as close as possible to the crystal.
2. The whole circuit should be on the same layer as the MCU, and the wiring should not go through the layer as much as possible.
3. The PCB area of the clock circuit should be kept as empty as possible, and no traces unrelated to the clock should be taken.
4. High-power, high-interference risk devices and high-speed wiring should be kept away from the clock crystal circuit as far as possible.
5. The clock line is grounded to achieve a shielding effect.

3.3. Reset Circuit

NRST trace PCB Layout reference is as follows:

Figure 3-5. NRST Layout design is recommended
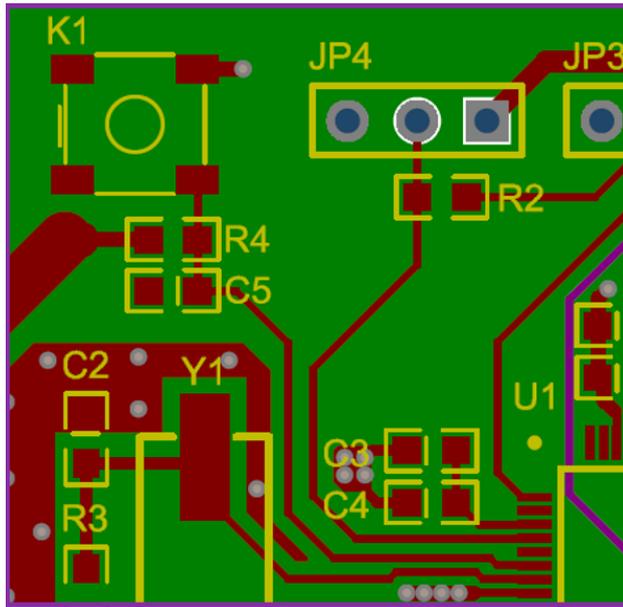
Note: The resistance and capacitance of the reset circuit should be as close as possible to the NRST pin of the MCU, and the NRST trace should be kept away from devices with strong interference risk and high-speed traces as far as possible. If conditions permit, it had better to wrap the NRST traces for better shielding effect.

4.   Package Description

GD32M531x series has a total of two package types, namely LQFP48 and LQFP64.

Table 4-1. Package Description

Ordering code	Package
GD32M531CBT7	LQFP48(7x7, 0.5pitch)
GD32M531CCT7	LQFP48(7x7, 0.5pitch)
GD32M531CZT7	LQFP48(7x7, 0.5pitch)
GD32M531RCT7	LQFP64(10x10, 0.5pitch)
GD32M531RBT7	LQFP64(10x10, 0.5pitch)

(Original dimensions are in millimeters)

5. Revision history

Table 5-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Mar.7, 2025

Important Notice

This document is the property of GigaDevice Semiconductor Inc. and its subsidiaries (the "Company"). This document, including any product of the Company described in this document (the "Product"), is owned by the Company according to the laws of the People's Republic of China and other applicable laws. The Company reserves all rights under such laws and no Intellectual Property Rights are transferred (either wholly or partially) or licensed by the Company (either expressly or impliedly) herein. The names and brands of third party referred thereto (if any) are the property of their respective owner and referred to for identification purposes only.

To the maximum extent permitted by applicable law, the Company makes no representations or warranties of any kind, express or implied, with regard to the merchantability and the fitness for a particular purpose of the Product, nor does the Company assume any liability arising out of the application or use of any Product. Any information provided in this document is provided only for reference purposes. It is the sole responsibility of the user of this document to determine whether the Product is suitable and fit for its applications and products planned, and properly design, program, and test the functionality and safety of its applications and products planned using the Product. The Product is designed, developed, and/or manufactured for ordinary business, industrial, personal, and/or household applications only, and the Product is not designed or intended for use in (i) safety critical applications such as weapons systems, nuclear facilities, atomic energy controller, combustion controller, aeronautic or aerospace applications, traffic signal instruments, pollution control or hazardous substance management; (ii) life-support systems, other medical equipment or systems (including life support equipment and surgical implants); (iii) automotive applications or environments, including but not limited to applications for active and passive safety of automobiles (regardless of front market or aftermarket), for example, EPS, braking, ADAS (camera/fusion), EMS, TCU, BMS, BSG, TPMS, Airbag, Suspension, DMS, ICMS, Domain, ESC, DCDC, e-clutch, advanced-lighting, etc.. Automobile herein means a vehicle propelled by a self-contained motor, engine or the like, such as, without limitation, cars, trucks, motorcycles, electric cars, and other transportation devices; and/or (iv) other uses where the failure of the device or the Product can reasonably be expected to result in personal injury, death, or severe property or environmental damage (collectively "Unintended Uses"). Customers shall take any and all actions to ensure the Product meets the applicable laws and regulations. The Company is not liable for, in whole or in part, and customers shall hereby release the Company as well as its suppliers and/or distributors from, any claim, damage, or other liability arising from or related to all Unintended Uses of the Product. Customers shall indemnify and hold the Company, and its officers, employees, subsidiaries, affiliates as well as its suppliers and/or distributors harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of the Product.

Information in this document is provided solely in connection with the Product. The Company reserves the right to make changes, corrections, modifications or improvements to this document and the Product described herein at any time without notice. The Company shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. Information in this document supersedes and replaces information previously supplied in any prior versions of this document.