

GigaDevice Semiconductor Inc.

GD32H75E Hardware Development Guide

Application Note

AN312

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1. Introduction

The article is specifically provided for developers of 32-bit general-purpose MCU GD32H75E series based on Arm® Cortex®-M7 architecture. It provides an overall introduction to hardware development for the GD32H75E series products, including power supply, reset, clock, boot mode settings, and download debugging. The purpose of this application note is to help developers quickly get started with the GD32H75E series products, facilitate hardware development, save time spent studying manuals, and accelerate product development progress.

This application development guide is divided into seven sections:

1. Power: Main introduction to the power domains and power supply design of the GD32H75E series.
2. Reset and Power Management: Main introduction to the reset functions and power management of the GD32H75E series.
3. Clock: Main introduction to the functional design of high-speed and low-speed clocks in the GD32H75E series.
4. Boot Configuration: Main introduction to the BOOT configuration and design of the GD32H75E series.
5. Typical peripheral modules, mainly introducing the hardware design of the main functional modules in the GD32H75E series.
6. Thermal management and low-power modes, mainly introducing the thermal management and low-power modes of the GD32H75E series.
7. Download and debug circuit, mainly introducing the recommended typical download and debug circuit for the GD32H75E series.
8. Reference circuit and PCB Layout design, mainly introducing hardware circuit design and PCB Layout design considerations for the GD32H75E series.
9. Stencils and soldering, mainly introducing stencil selection and usage methods, as well as reflow soldering temperature profiles.
10. Package description, mainly introducing the package types and naming conventions included in the GD32H75E series.

This document also satisfies the minimum system hardware resources used in application development based on the GD32H75E series products.

Table 1-1. Applicable Products

Type	Part Numbers
MCU	GD32H75Exx series

Note: This application note is for reference only. In case of any conflict with the user manual or datasheet, the user manual or datasheet shall prevail.

2. Hardware design

2.1. Power supply

The GD32H75E series devices have multiple power domains, including the V_{DD} / V_{DDA} domain, 0.9V domain, backup domain, V_{DD33} / V_{DD3AX} domain, V_{DDIO} domain, and 1.1V domain. The $V_{DD} / V_{DDA} / V_{DD33} / V_{DD3AX} / V_{DDIO}$ domains are powered directly by the power supply. The GD32H75E series integrates LDO and a low-power buck regulator (SMPS buck regulator) to supply power to the 0.9V and 1.1V domains. The backup domain includes a power switch, which can switch the backup domain's power to the VBAT pin when the V_{DD} power supply is off. In this case, the backup domain is powered by the VBAT pin (battery). The USB module has dedicated external power supply pins and voltage regulators, supporting either 5V or 3.3V power input.

2.1.1. Backup domain

The backup domain operates within a voltage range of 1.8V to 3.6V. It is powered by an internal power switch that selects either V_{DD} or V_{BAT} (battery), and the V_{BAK} supplies power to the backup domain. The backup domain includes the RTC (Real-Time Clock), LXTAL (Low-Speed External Crystal Oscillator), BPOR (Backup Domain Power-On Reset), BREG, and three BKP PADs: PC13 to PC15. To ensure the retention of register contents in the backup domain and proper operation of the RTC, the VBAT pin can be connected to a battery or other backup power source when V_{DD} is off. The power switch is controlled by the V_{DD} / V_{DDA} domain power-down reset circuit. For applications without an external battery, it is recommended to connect the VBAT pin to the VDD pin through a 100nF capacitor to ground.

The reset sources for the backup domain include power-on reset (BPOR) and backup domain software reset. Before V_{BAK} is fully powered up, the BPOR signal forces the device to remain in the reset state. The application software can trigger a backup domain software reset by setting the BKPRST bit in the RCU_BDCTL register.

The clock source of RTC can be a low-speed internal 32kHz RC oscillator (IRC32K) or a low-speed external crystal oscillator (LXTAL), or a high-speed external crystal oscillator (HXTAL) clock divider controlled by the RTCDIV[5:0] (located in the RCU_CFG0 register) bit domain. When V_{DD} is turned off, RTC can only select LXTAL as the clock source. Before entering power-saving mode through WFI / WFE commands, Cortex®-M7 can achieve RTC timer wake-up events by setting the expected wake-up time in the RTC register and enabling wake-up function or based on EXTI. After entering the power saving mode for a certain period of time, when the elapsed time matches the preset wake-up time, the RTC will wake up the device.

When the backup domain is powered by V_{DD} (V_{BAK} connected to V_{DD}), the following functions are available:

- PC13 can be used as a general-purpose I/O pin or an RTC function pin;
- PC14 and PC15 can be used as general-purpose I/O pins or LXTAL oscillator pins.

When the backup domain is powered by V_{BAT} (V_{BAK} connected to V_{BAT}), the following functions are available:

- PC13 can only be used as an RTC function pin;
- PC14 and PC15 can only be used as LXTAL oscillator pins.

Note:

1. Since the PC13 to PC15 pins are powered through the supply switch, which can only provide small currents, the operating speed of PC13 to PC15 GPIOs in output mode must not exceed 2 MHz (maximum load of 30 pF);
2. The LDO of the backup domain can generate the V_{CORE_BKP} voltage. When the V_{DD} / V_{DDA} is powered on, the BKP RAM in the 0.9V power domain is powered by V_{CORE} ; when V_{DD} / V_{DDA} is powered off, the BKP RAM in the 0.9V power domain is powered by V_{CORE_BKP} .

V_{DD} can charge an external battery through an internal resistor. The internal resistor value can be selected as 5k Ω or 1.5k Ω for charging the external V_{BAT} battery by configuring the VCRSEL bit in the PMU_CTL2 register. Setting the VCEN bit in the PMU_CTL2 register to 1 enables V_{BAT} battery charging. In BKP only mode, V_{BAT} battery charging is not available.

Note: In BKP only mode, when V_{DD} is powered off, the backup domain is powered by the V_{BAT} pin.

2.1.2. V_{DD} / V_{DDA} domain

The V_{DD} / V_{DDA} power domain includes both the V_{DD} domain and the V_{DDA} domain. If V_{DDA} is not equal to V_{DD} , the voltage difference between them must not exceed 300 mV (V_{DDA} and V_{DD} are connected internally through back-to-back diodes). To minimize noise, V_{DDA} can be connected to V_{DD} through an external filtering circuit, and the corresponding V_{SSA} should be connected to V_{SS} via a specific circuit (single-point grounding, through 0 Ω resistors or magnetic beads, etc.).

In order to improve the conversion accuracy of the ADC, the independent power supply for V_{DDA} can make the analog circuit achieve better characteristics. GD32H75E is internally integrated with VREFP pin specially designed for independent power supply of ADC (External power supply: Using 12bit ADC, $1.8\text{ V} \leq V_{REFP} \leq V_{DDA}$. Using 14bit ADC, when $V_{DDA} \geq 2.4\text{ V}$, $2.4\text{ V} \leq V_{REFP} \leq V_{DDA}$; when $V_{DDA} < 2.4\text{ V}$, $1.8\text{ V} \leq V_{REFP} \leq V_{DDA}$).

- In the BGA240 package, VREFP and VREFN pins are provided. VREFP can use an external reference voltage or be directly connected to V_{DDA} , while VREFN must be connected to V_{SSA} .
- The VREFP pin is connected to the V_{DDA} pin through an internal diode. When $V_{REFP} \geq V_{DDA} + 0.3\text{V}$, there will be leakage to the V_{DDA} pin.
- The GD32H75E series is equipped with V_{REFBUF} . When the VREFP pin is not connected to an external reference power source, V_{REFBUF} can generate four levels of reference

voltages ranging from 1.5V to 2.5V. For details, please refer to the user guide and datasheet.

2.1.3. 0.9V domain

Using the SMPS buck converter and LDO, the supply power for the 0.9V power domain can be configured. Four effective 0.9V power domain supply modes are available depending on the configuration. The modes correspondence table is shown in [Table 2-1. Power Supply Modes Correspondence Table](#).

Table 2-1. Power Supply Modes Correspondence Table

Mode	Power supply mode
0	Unconfigured supply mode (default supply mode)
1	LDO supply mode
2	SMPS supply mode
6	Bypass mode

■ Unconfigured supply mode (default supply mode)

Unconfigured power supply mode, which is the initial transition mode. After the chip reset, if the software does not configure any power modes, the chip remains in this mode. At this time, all registers are in their reset state, and both SMPS and LDO are enabled. During this stage, the following situations may occur based on hardware configurations:

1. When the hardware is configured to the LDO supply mode, the LDO outputs 0.9V to supply the $V_{0.9V}$ domain. This state is identical to the LDO supply mode;
2. When the hardware is configured to SMPS supply mode, the SMPS outputs 1V to V_{CORE} . However, the LDO is also enabled, resulting in V_{DDLDO} being shorted to V_{CORE} , which causes fluctuations in the V_{CORE} voltage. Therefore, the software should configure the system to SMPS supply mode after reset to ensure system reliability;
3. When the hardware is set to bypass mode, the LDO is enabled but forced into bypass by hardware, with power supplied by external input, which may pose unknown risks. In summary, in this situation, the software should immediately configure the system to bypass mode after reset to ensure safety.

In summary, this mode is the initial transition state during chip startup. Long-term use may pose unpredictable risks, and the software and hardware should be configured to other modes during normal chip operation.

The default state of registers is shown in [Table 2-2. Default power supply mode register initial state](#):

Table 2-2. Default power supply mode register initial state

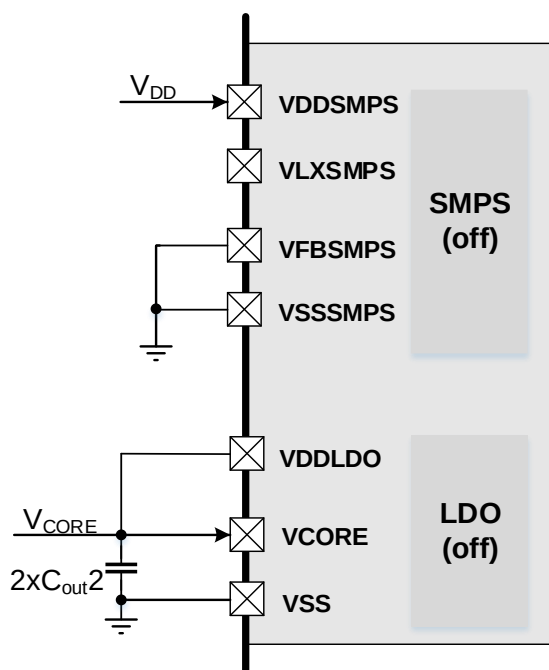
Symbol	Description
DVSEN	1: SMPS enable
LDOEN	1: LDO enable
LDOVS[2:0]	010: LDO output 0.9V

Symbol	Description
BYPASS	0: BYPASS disabled

■ Bypass mode

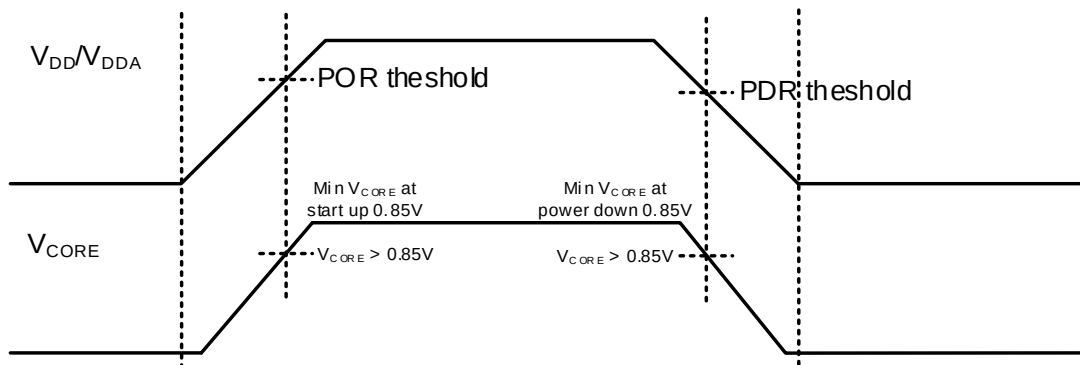
In this mode, SMPS is disabled, LDO is disabled, and the external circuit supplies the $V_{0.9V}$ domain through the V_{CORE} pin. For specific circuits, refer to [Figure 2-1. Bypass Mode](#) (when the SMPS module is disabled, the VDDSMPS pin must be connected to V_{DD} or V_{SS}).

Figure 2-1. Bypass Mode



The power-up sequence diagram for Bypass Mode is shown in [Figure 2-2. Bypass Mode Power-Up and Power-Down Timing Diagram](#). Before the V_{DD}/V_{D_{DA}} voltage of the MCU rises to the POR threshold, ensure that the V_{CORE} voltage is greater than 0.85V. Before the MCU's V_{DD} / V_{D_{DA}} voltage falls to the PDR threshold, ensure that the V_{CORE} voltage is greater than 0.85V. Additionally, under any operating conditions, it is necessary to ensure that the V_{DD} / V_{D_{DA}} voltage is greater than the V_{CORE} voltage.

Figure 2-2. Bypass Mode Power-Up and Power-Down Timing Diagram



The configuration method for entering this power supply mode is as follows: the DVSEN bit is 0b0, the values of the DVSCFG and DVSV[1:0] have no effect, the SMPS step-down regulator is turned off; the LDOEN bit is 0b0, so the LDO is turned off; the BYPASS bit is 0b1, meaning the 0.9V power domain is powered through the V_{CORE} pin. The register configuration for the SMPS and LDO output voltage is shown in [Table 2-3. Bypass mode Register Configuration Table](#):

Table 2-3. Bypass mode Register Configuration Table

Symbol	Description
DVSEN	0: SMPS disable
LDOEN	0: LDO disable
BYPASS	1: BYPASS enable

Note:

1. In bypass mode, when the external device outputs voltage to V_{CORE}, ensure that its typical value is 0.9V, with a voltage range within 0.873V to 0.955V. Even in harsh application scenarios, ensure that the power fluctuation range is within 50mV;
2. Operating in bypass mode will cause relatively large current to flow into the V_{0.9V} power domain from the external device through the V_{CORE} pin (simulation and test results show this current can reach up to 400mA). Therefore, there are higher requirements for the external power supply devices. We recommend that the load capacity of the external device be greater than 600mA and the output voltage fluctuation range under different loads meets the aforementioned 50mV requirement. Considering power stability requirements, it is recommended to use an external LDO for power supply in bypass mode;
3. Considering the ESR effect and IR drop of large current on PCB traces, when routing the PCB, it is necessary to consider widening the trace width from the external power supply to the V_{CORE} pin to reduce ESR and ensure that the voltage at the chip's V_{CORE} pin meets the amplitude and fluctuation requirements;
4. It is recommended that multiple V_{CORE} pins on the package be connected together externally through routing. Concerning decoupling and filter capacitors at the V_{CORE} pin, when operating in bypass mode, it is recommended to place a 100nF capacitor near each V_{CORE} pin. If there is a third V_{CORE} pin on the package, it only needs to be connected to the other two V_{CORE} pins without adding additional capacitors;
5. When using bypass mode to enter standby mode, first enter standby mode and then turn off the external V_{CORE} power; the external V_{CORE} power must be turned off. When exiting standby mode, first turn on the external V_{CORE} power and then exit standby mode.

Note: Except for the valid combinations mentioned above, all other configuration combinations of DVSEN, DVSCFG, DVSV[1:0], LDOEN, BYPASS bits or bit values are invalid. The power state of the 0.9V power domain remains unchanged after reset (no configured power mode).

Note: When the SMPS voltage regulator supplies power to the 0.9V power domain and the DVSV[1:0] is configured with an incorrect value, it will cause the SMPS voltage regulator to

output high voltage to the 0.9V power domain. At this time, the 0.9V power domain will activate hardware overvoltage protection, and the hardware will be set to DVSV[1:0] 0b00.

Note: The maximum operating frequency is related to the power supply voltage, please refer to the data manual for details

2.1.4. V_{DD33} / V_{DD3Ax} domain

The V_{DD33} / V_{DD3Ax} power domain consists of the V_{DD33} domain and V_{DD3Ax} domain, which respectively supply power to the internal LDO and PHY of the ESC device. To reduce noise, V_{DD3Ax} can be connected to V_{DD33} through an external filtering circuit.

2.1.5. V_{DDIO} domain

The V_{DDIO} power domain is the power pin that supplies power to the GPIO of the ESC device. To reduce noise, it can be connected to V_{DD33} through an external filtering circuit.

2.1.6. 1.1V domain

The 1.1 V power domain includes V_{DDCR} and V_{DD1Ax} . Using the internal regulator, the supply power of the 1.1 V power domain can be configured, and V_{DD1Ax} can be connected to V_{DDCR} through an external filter circuit. Two valid 1.1 V power domain supply modes are available for different configurations, as shown in [Table 2-4. Power Supply Modes Mapping Table](#).

Table 2-4. Power Supply Modes Mapping Table

REG_EN	Power supply mode
H	LDO supply mode
L	Bypass mode

The power supply mode is configured by hardware. When the REG_EN pin is set high, 1.1 V is supplied to the $V_{1.1V}$ domain through the internal LDO. When the REG_EN pin is set low, an external 1.1 V supply must be provided for the $V_{1.1V}$ domain.

2.1.7. Oscillator Power supply

To enhance the stability of the clock circuit, the GD32H75E series ESC oscillators integrate a regulator internally, providing 1.1 V to the oscillator circuit. Users can set the REG_EN pin high to enable the OSC_LDO regulator and connect the VDD33 pin to a 3.3 V power supply to power the oscillator module. When REG_EN is set low, the regulator is disabled, and the OSCVDD11 pin must be connected to an external 1.1 V power supply to power the oscillator module, as shown in [Table 2-5. Oscillator Power Supply Modes Mapping Table](#).

Table 2-5. Oscillator Power Supply Modes Mapping Table

REG_EN	Power supply mode
H	OSC_LDO supply mode
L	Bypass mode

Note: The OSCVSS pin must be grounded under all circumstances.

2.1.8. USB Power supply

The GD32H75E series USB integrates a voltage regulator internally, which users can choose to enable. Connect the VDD50USB pin to a 5 V power supply to provide power for the USB module, as shown in [Figure 2-3. Connection diagram of USB voltage regulator during power supply](#); Alternatively, bypass the voltage regulator and connect the VDD33USB pin to a 3.3 V power supply to provide power to the USB module, as shown in [Figure 2-4. Connection diagram for USB voltage regulator bypass](#).

Figure 2-3. Connection diagram of USB voltage regulator during power supply

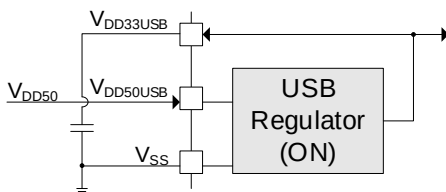
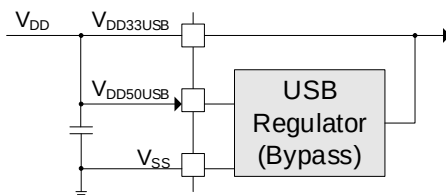


Figure 2-4. Connection diagram for USB voltage regulator bypass



Note:

1. When $V_{DD} \geq 3V$, the USB power supply can operate in either USB regulator supply mode or bypass mode; when $V_{DD} < 3V$, the USB power supply can only operate in USB regulator supply mode;
2. When using the USB module or the ISP download function, $V_{DD33USB}$ must be powered, which can be supplied through one of the two methods mentioned above.

2.1.9. Power supply design

The system requires a stable power supply, and some important considerations must be noted during development:

- The VDD pin must be connected with an external capacitor (N*100nF ceramic capacitor + not less than 4.7uF tantalum capacitor, at least one VDD needs to be connected to GND with a capacitor of not less than 4.7uF, and other VDD pins are connected to 100nF);
- The VDDA pin must be externally connected to capacitors (recommended 10nF + 1uF ceramic capacitors);
- The VREFP pin can be internally generated or directly connected to VDDA, and a 10nF + 1uF ceramic capacitor should be connected between the VREFP pin and ground;
- The VDD33 pin must be externally connected to capacitors (100nF ceramic capacitor + 4.7uF tantalum capacitor);

- The VDDIO pin must be externally connected to capacitors (N * 100nF ceramic capacitors);
- The VDDCR pin must be externally connected to capacitors (N * 100nF ceramic capacitors + 1uF ceramic capacitor + 470pF ceramic capacitor);
- The VDD3Ax pin must be externally connected to capacitors (recommended 100nF + 4.7uF ceramic capacitors);
- The VDD1Ax pin must be externally connected to capacitors (N * 100nF ceramic capacitors).

Figure 2-5. Recommended power supply design for GD32H75E series (enable ESC internal regulator)

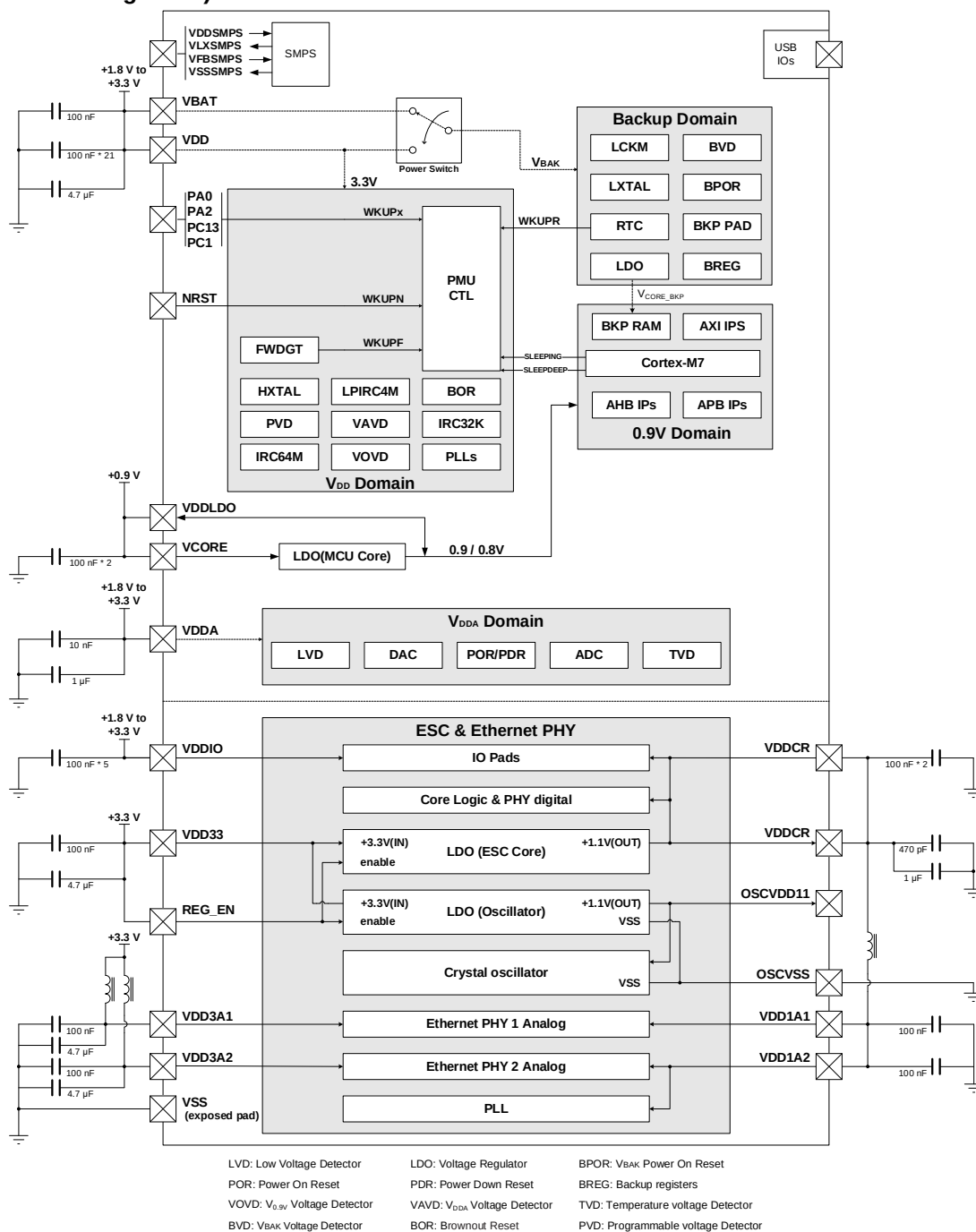
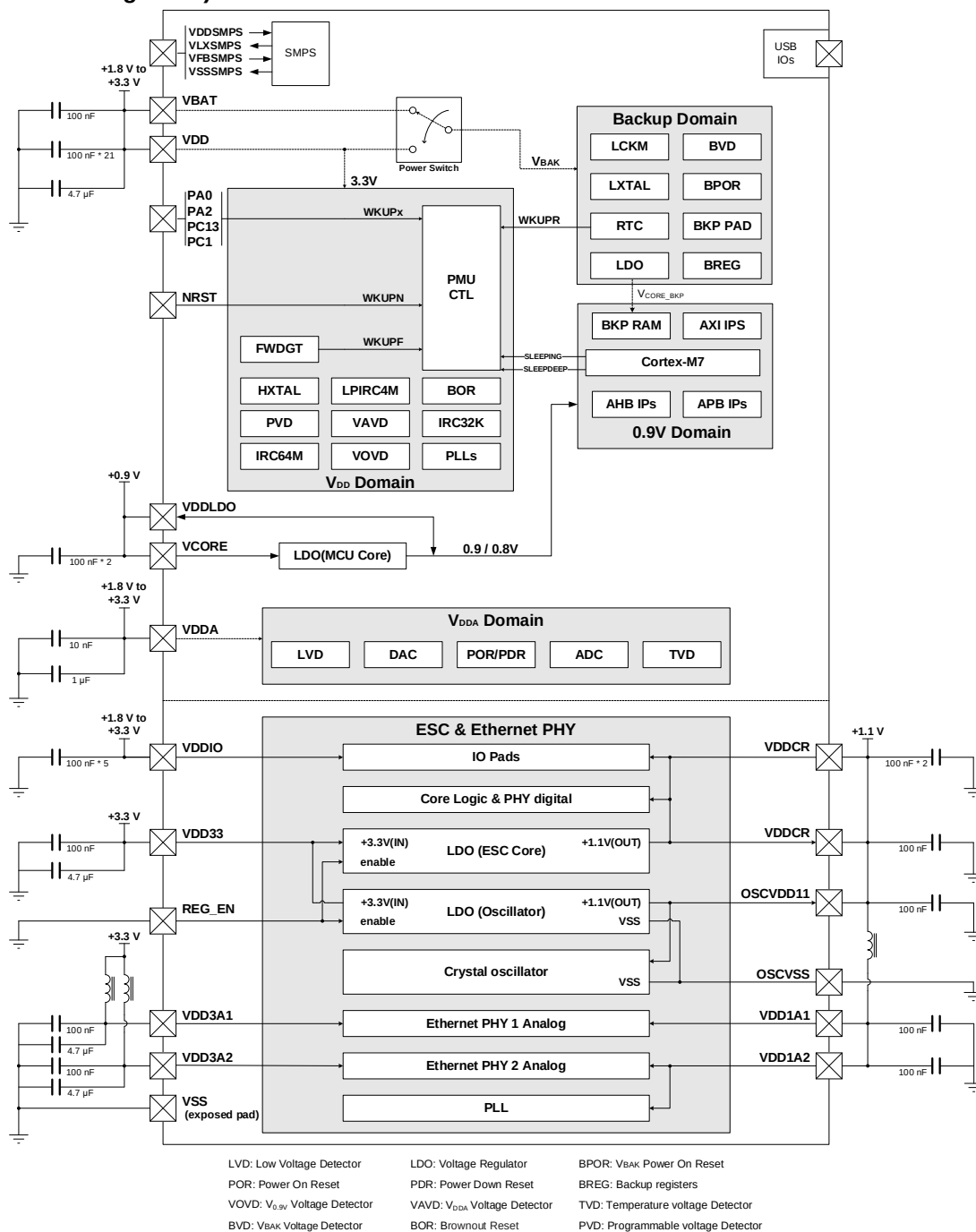


Figure 2-6. Recommended power supply design for GD32H75E series (disable ESC internal regulator)



Note:

1. All decoupling capacitors must be placed close to the corresponding VDD, VDDA, VBAT, VREFP, VCORE, VDDIO, VDD33, VDD3Ax, VDDCR, OSCVDD11, and VDD1Ax pins of the chip;
2. Regardless of whether the LDO is enabled, all VDDCR pins of the chip should be connected together, all VCORE pins should be connected together, and all VDDLDO pins should be connected together; refer to Section [0.9V domain](#) for details;
3. When LDO (MCU CORE) is enabled, it is recommended to connect two 2.2μF ceramic capacitors between VCORE and GND; when LDO (MCU CORE) is bypassed, it is

recommended to connect two 100nF ceramic capacitors between V_{CORE} and GND;

- When the MCU power supply voltage is unstable or at risk of voltage drops, it is recommended to replace the 4.7uF capacitors on V_{DD}, V_{DD33}, and V_{DD3Ax} with capacitors no less than 10uF.

The recommended design of the SMPS circuit is shown in [Figure 2-7. GD32H75E Recommended SMPS circuit Design](#), and the typical value of the device are shown in [Table 2-6. Characteristics of SMPS step-down converter external components](#).

Figure 2-7. GD32H75E Recommended SMPS circuit Design

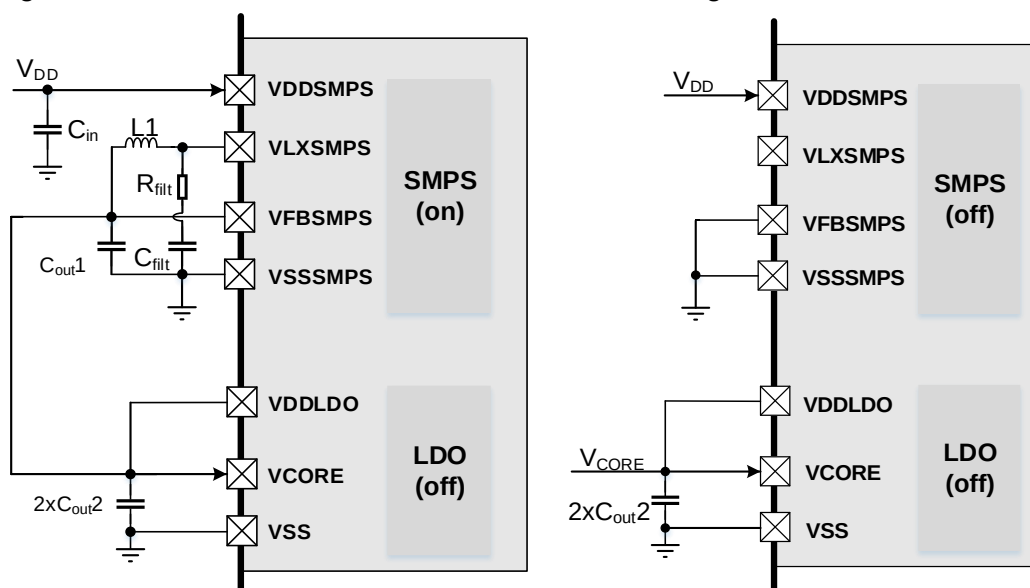


Table 2-6. Characteristics of SMPS step-down converter external components

Fields	Descriptions	Recommended value	Footprint
C _{in}	VDDSMPS external capacitor	10uF	0805
C _{filt}	VLXSMPS external capacitor	220pF	0603
R _{filt}	VLXSMPS external resistor	50Ω	0603
C _{OUT1}	VFBSMPS external capacitor	10uF	0805
C _{OUT2}	V _{CORE} external capacitor	100nF/2.2uF	0603/0805
L1	VLXSMPS external inductor	2.2uH	0806

2.2. Reset and Power Management

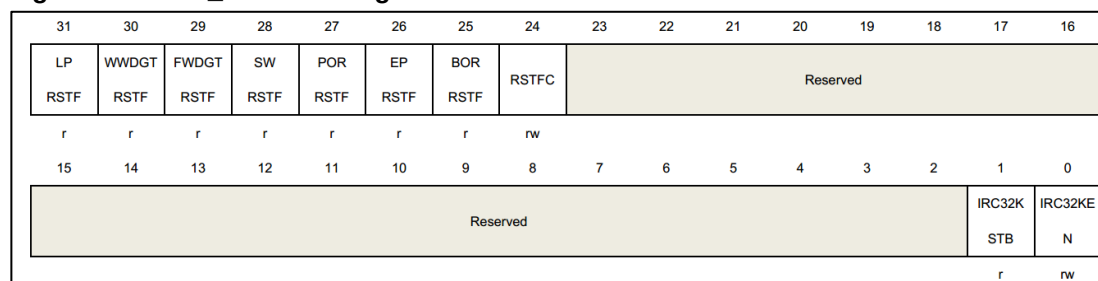
In this section, the default is that the V_{DD} and V_{DDA} pins remain connected and are powered by the same power source.

The GD32H75E series reset control includes five types of resets: Power Reset, System Reset, Backup Domain Reset, ESC System Reset, and ESC Module Reset. The Power Reset is a cold reset that resets all systems except the Backup Domain during power-up.

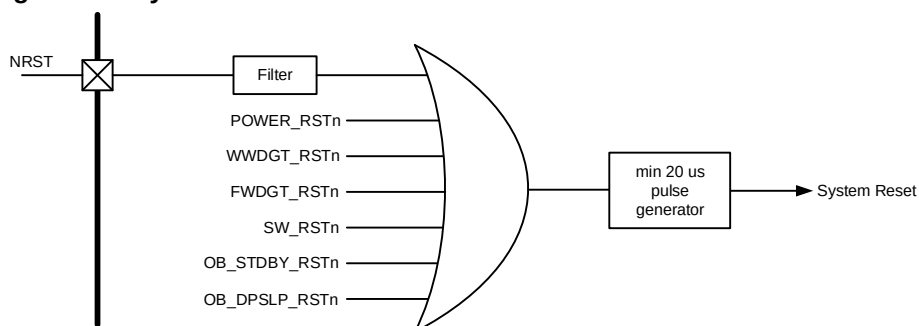
Table 2-7. Reset Contents for Different Reset Types

Reset types	Reset content
Power reset	All systems except the backup domain
System reset	All parts except the SW-DP controller, backup domain, and EtherCAT devices, including the processor core and peripheral IP.
Backup domain reset	Backup area
ESC system reset	Reset all circuits in the EtherCAT device
ESC module reset	Reset one or more modules in the EtherCAT device

The MCU reset source can be searched by the register RCU_RSTSCK (0x40021024). This register can only clear the flag bit after power-on reset. Therefore, during use, after the reset source is obtained, the reset flag can be cleared through the RSTFC control bit, so that a watchdog reset or other reset events can be more accurately reflected in the RCU_RSTSCK register:

Figure 2-8. RCU_RSTSCK Register


The MCU integrates internal Power-On/Power-Down Reset circuits. When a reset occurs, the system reset pulse generator ensures that each reset source (external or internal) generates a low-level pulse delay of at least 20μs. To prevent accidental reset triggers, it is recommended to place a capacitor (typical value: 100nF) on the NRST pin.

Figure 2-9. System Reset Circuit


When one of the following events occurs, a backup domain reset is generated:

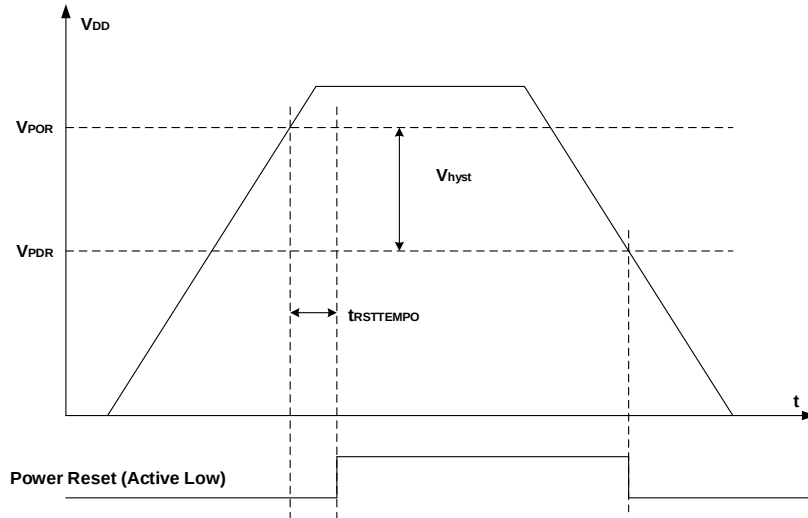
1. Set the BKPRST bit in the backup domain control register to '1';
2. Backup domain power-on reset (VDD power restored).

2.2.1. Power-On Reset (POR) / Power-Down Reset (PDR)

The POR / PDR circuit monitors V_{DD} and generates a power reset signal to reset the entire chip except for the backup domain when the voltage falls below a specific threshold. [Figure](#)

[2-10. Waveform of the POR / PDR](#) shows the relationship between the power reset and V_{DD} when BOR is disabled. When BOR is enabled, the effect of BOR on the power reset level needs to be considered. Information related to BOR will be introduced in the next subsection. V_{POR} indicates the threshold voltage for power-on reset, while V_{PDR} indicates the threshold voltage for power-down reset. The hysteresis voltage V_{hyst} is approximately 50mV.

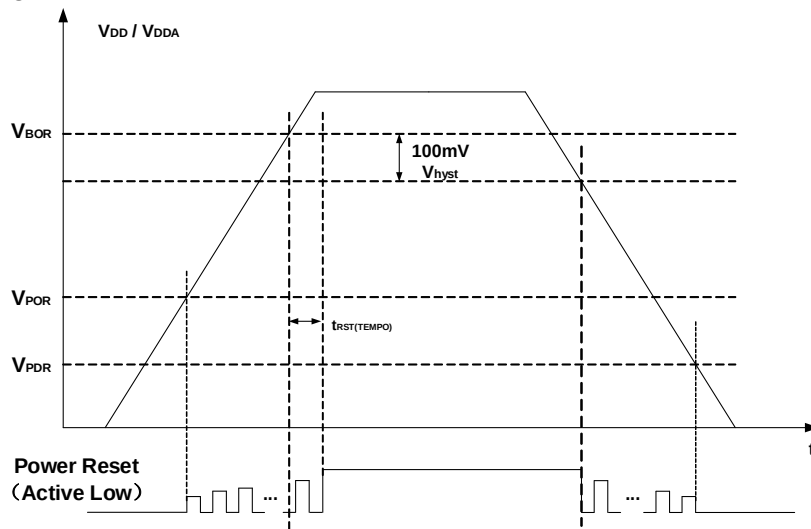
Figure 2-10. Waveform of the POR / PDR



2.2.2. Brown-Out Reset (BOR)

The BOR circuit monitors V_{DD} and generates a power reset signal to reset the entire chip, except for the backup domain, when BOR_TH is not 0b11 and the voltage falls below the threshold defined by the BOR_TH option byte. Regardless of whether BOR is enabled, the POR / PDR circuit is always in detection mode. Therefore, the power reset level will be pulled high when V_{DD} rises to V_{POR} , regardless of whether BOR is enabled. When BOR is enabled, it will quickly pull the elevated power reset level low. The POR / PDR circuit, upon detecting $V_{DD} > V_{POR}$, will pull the power reset level high again, and BOR will pull it low. This cycle continues, forming a square wave on the NRST pin. Only after the V_{DD} / V_{DDA} voltage exceeds V_{BOR} will BOR no longer pull the power reset level low, and the power reset will remain high. A square wave will only appear when V_{DD} / V_{DDA} voltage is greater than V_{POR} and less than V_{BOR} . [Figure 2-11. Waveform of the BOR](#) shows the relationship between the supply voltage and the BOR reset signal. V_{BOR} indicates the threshold voltage for BOR reset, which is defined in the option byte BOR_TH. The hysteresis voltage V_{hyst} is 100mV.

Figure 2-11. Waveform of the BOR

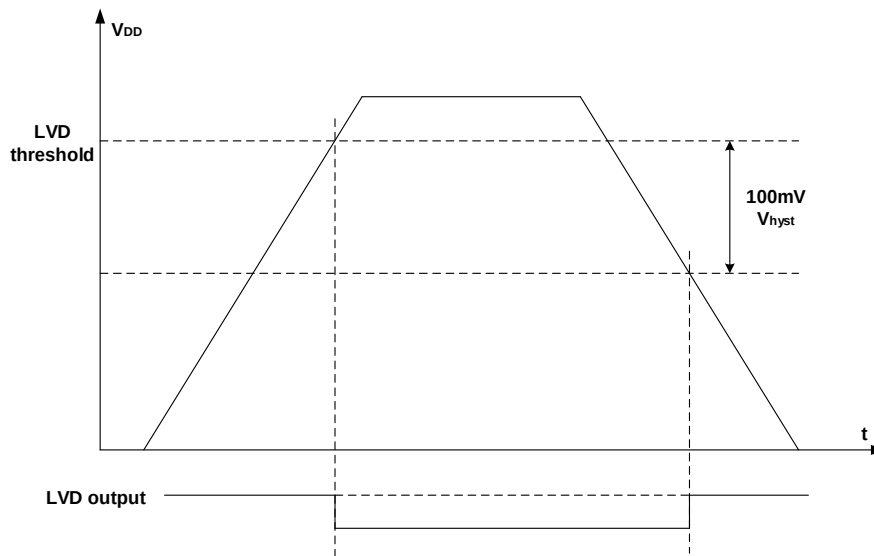


2.2.3. Low Voltage Detector (LVD)

The function of LVD is to detect whether the V_{DD} supply voltage is lower than the low voltage detection threshold, which is configured by the $LVDT[2:0]$ bit in the power control register 0 (PMU_CTL0). LVD is enabled by $LVDEN$ setting. The $LVDF$ bit in the power supply status register (PMU_CS) indicates whether a low voltage event occurs. This event is connected to the 16th line of $EXTI$. The user can generate a corresponding interrupt by configuring the 16th line of $EXTI$. [Figure 2-12. Waveform of the LVD](#) shows the relationship between V_{DD} supply voltage and LVD output signal. (LVD interrupt signal depends on the rising or falling edge configuration of $EXTI$ line 16). The hysteresis voltage V_{hyst} is 100 mV.

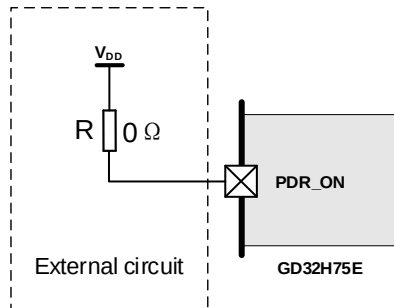
LVD Application Scenario: When the MCU power supply is subject to external interference, such as a voltage drop, we can set a low voltage detection threshold with LVD (this threshold is greater than the PDR value). Once the voltage drops to this threshold, the LVD interrupt is triggered. In the interrupt function, operations such as a software reset can be set to prevent other anomalies from occurring in the MCU.

Figure 2-12. Waveform of the LVD



The internal power monitor of the GD32H75E series can be enabled or disabled through the PDR_ON pin. To ensure the chip operates normally and to improve anti-interference capability, as well as to generate effective reset signals during power-up / power-down stages, the recommended circuit for PDR_ON is shown in [Figure 2-13. Recommended PDR_ON Pin Circuit Design](#).

Figure 2-13. Recommended PDR_ON Pin Circuit Design



Note: The PDR_ON pin must be kept at high level. The user can flexibly adjust the value of the pull-up resistor R according to the specific scenario for a better performance.

When PDR_ON is connected to GND, the following functions will be disabled:

1. Internal Power On Reset(POR) / Pwer Down Reset(PDR) disabled;
2. Internal Brown Out Reset(BOR) disabled;
3. Internal Low Voltage Detection(LVD) disabled;
4. V_{BAT} function disabled, V_{BAT} pin should be connected to V_{DD}.

2.2.4. ESC system reset

ESC system reset includes Power-On Reset (POR), external pin reset (RSTN), and EtherCAT system reset, which can reset all circuits in the EtherCAT device. ESC module reset includes digital reset, PHY reset, and EtherCAT core reset, which can reset the corresponding

modules.

POR (Power-On Reset) occurs when the device is powered on or after power is lost and reapplied. RSTN pin reset is triggered by driving the RSTN input pin to a low level to initiate external pin reset. EtherCAT system reset is initiated by three consecutive special frame/command sequences.

2.2.5. ESC module reset

ESC multi-module reset: Perform a digital reset by setting the DRST bit in the configuration register (RCU_RSTCFG). The digital reset resets all EtherCAT device submodules except PHY.

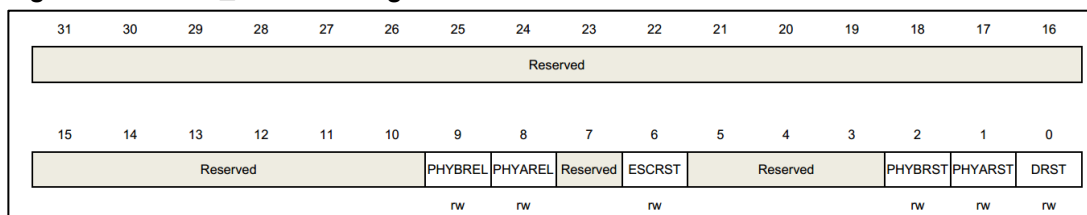
ESC single-module reset: The single-module reset only resets the specified module. The single-module reset does not lock configuration pins, including PHY reset for Port A, PHY reset for Port B, and EtherCAT controller reset. The single-module reset is described as follows:

Port A PHY reset can be performed by setting the PHYARST bit in the reset configuration register (RCU_RSTCFG) or the MR_MAIN_REST bit in the PHY control register (PHY_MII_CTL). After the PHY reset for Port A, the PHYARST bit and the software reset bit will be automatically cleared. This reset does not affect other modules of the device. The completion of Port A PHY reset can be checked by verifying whether the PHYARST bit in the reset configuration register (RCU_RSTCFG) or the MR_MAIN_REST bit in the PHY control register (PHY_MII_CTL) is cleared.

Port B PHY reset can be performed by setting the PHYBRST bit in the reset configuration register (RCU_RSTCFG) or the MR_MAIN_REST bit in the PHY control register (PHY_MII_CTL). After the PHY reset for Port B, the PHYBRST bit and the software reset bit will be automatically cleared. This reset does not affect other modules of the device. The completion of Port B PHY reset can be checked by verifying whether the PHYBRST bit in the reset configuration register (RCU_RSTCFG) or the MR_MAIN_REST bit in the PHY control register (PHY_MII_CTL) is cleared.

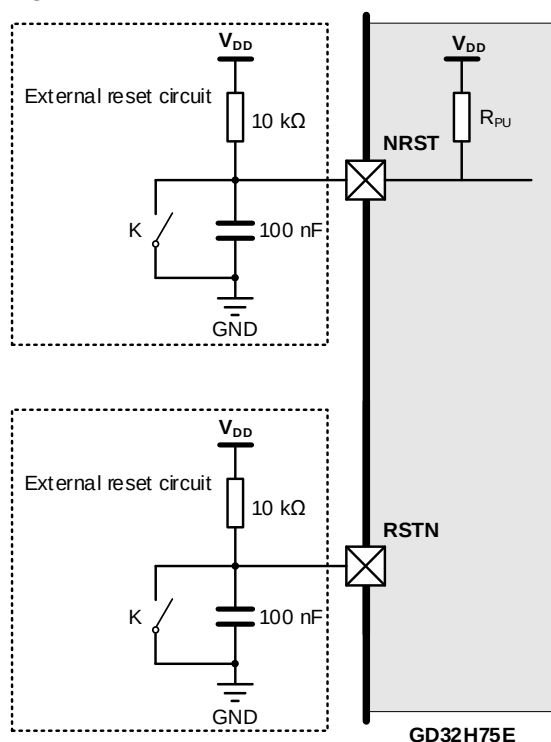
EtherCAT controller individual reset can be performed by clearing the ESCRST bit in the configuration register (RCU_RSTCFG), which resets the EtherCAT core and its registers.

Figure 2-14. RCU_RSTCFG Register



2.2.6. External reset circuit

Figure 2-15. Recommended External Reset Circuit

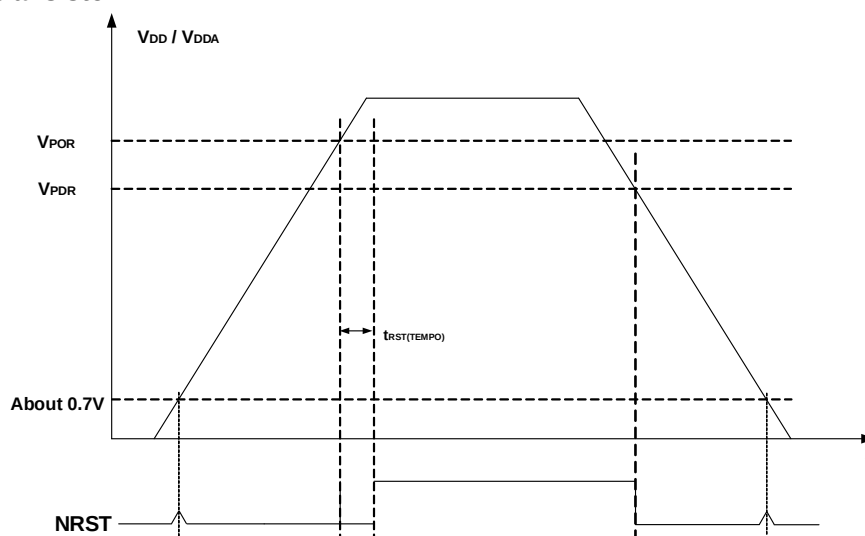


Note:

1. Internal pull-up resistor $R_{PU} = 40k\Omega$. It is recommended to connect an external pull-up resistor of $10k\Omega$ to prevent voltage interference from causing abnormal chip operation;
2. To account for effects such as static electricity, an ESD protection diode can be placed at the NRST pin (for more hardware protection designs, refer to the official website's [AN163 GD32 MCU EMC Hardware Protection Design Reference](#));
3. Although the MCU has an internal hardware POR circuit, it is still recommended to add an external RC reset circuit for NRST and RSTN;
4. If the MCU starts abnormally (due to voltage fluctuations, etc.), the capacitance value of NRST to ground can be appropriately increased, and the MCU reset completion time can be extended to avoid the abnormal power-on sequence area.

Due to the threshold voltage characteristics of the MOS transistor, during the power-up and power-down process of the chip, when $V_{DD} / V_{DDA} < 0.7$ V, the internal pull-down MOS transistor of the chip will not pull down the NRST pin. Therefore, during the power-up and power-down process, when $V_{DD} / V_{DDA} \approx 0.7$ V, a small pulse occurs, which does not affect the normal operation of the chip, as shown by the red pulse in [Figure 2-16. The illustration of the pulse of the NRST pin power-up/down MOS transistor](#).

Figure 2-16. The illustration of the pulse of the NRST pin power-up/down MOS transistor



Due to the difference in charging and discharging speeds, the pulse duration of the falling edge is slightly longer than that of the rising edge, both of which are at the millisecond level.

2.3. Clock

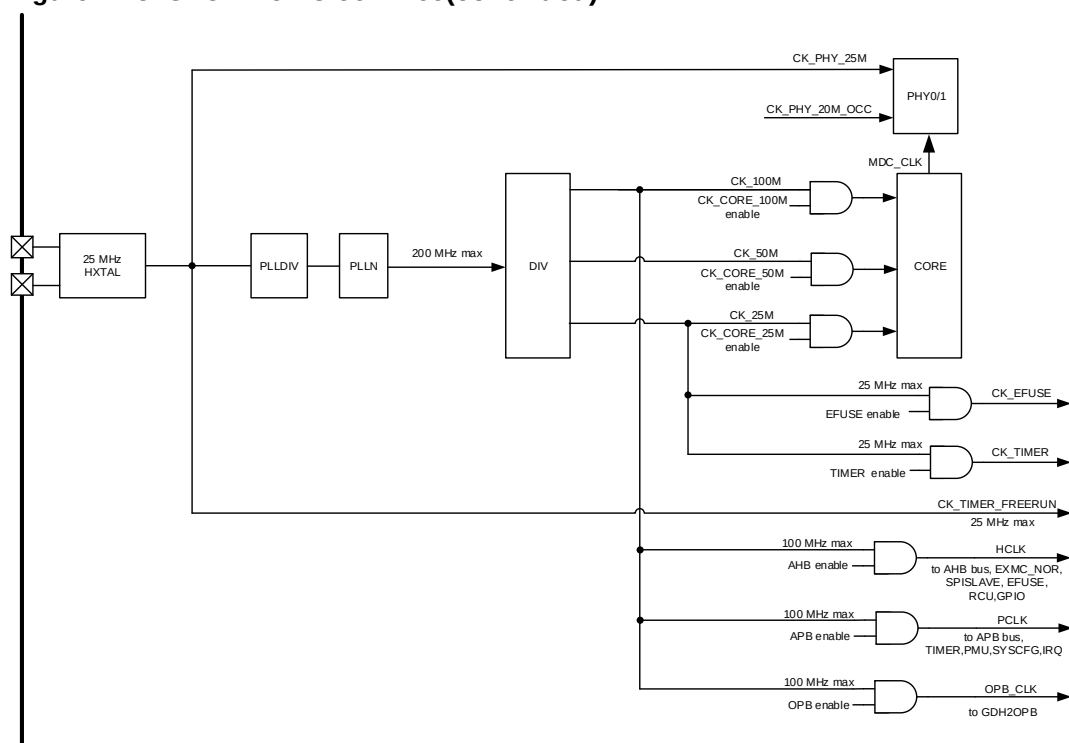
The GD32H75E series features a comprehensive internal clock system. The system clock is usually provided by the OSCIN and OSCOUT of a 4 to 50 MHz passive crystal oscillator, or driven by the OSCIN pin of a single-ended 4 to 50 MHz clock source driver.

The ESC clock control unit mainly consists of an external high-speed crystal oscillator (HXTAL) and a phase-locked loop (PLL). The ESC clock is typically provided by the OSCI and OSCO of a 25 MHz passive crystal oscillator, or driven by the OSCI pin of a single-ended 25 MHz clock source driver.

Users can select an appropriate clock source based on different application scenarios. Main clock features:

- 4 - 50 MHz External High-Speed Crystal Oscillator (HXTAL)
- 25 MHz External High-Speed Crystal Oscillator (HXTAL)
- Internal 64 MHz RC Oscillator (IRC64M)
- Internal 48 MHz RC Oscillator (IRC48M)
- 32.768 kHz External Low-Speed Crystal Oscillator (LXTAL)
- Internal 32 kHz RC Oscillator (IRC32K)
- Low-Power Internal 4 MHz RC Oscillator (LPIRC4M)
- PLL clock source options include HXTAL, LPIRC4M, or IRC64M.
- PLLs support integer and fractional multiplication factors.
- The fractional multiplication factor of PLLs can be modified during runtime.
- The peripheral clock supports dynamic switching.
- HXTAL clock monitor
- LXTAL clock monitor

Figure 2-18. GD32H75E Clock Tree(continued)

**Note:**

1. REFSEL is the LPDTS reference clock selection bit, which can be selected as CK_PCLK4 or CK_LXTAL;
2. CK_PER is the peripheral clock, which can be CK_LPIRC64MDIV, CK_LPIRC4M, or CK_HXTAL;
3. CK_TPIU is the Trace Port Interface Unit (TPIU) clock, which can be CK_IRC64MDIV, CK_LPIRC4M, CK_HXTAL, or CK_PLL0R;
4. CK_RSPDIF_SYMB is the RSPDIF symbol clock;
5. ADCSCK is the ADC synchronous clock selection bit;
6. USBHSx 60M is the internal PHY 60M input clock source of USBHSx.

2.3.1. External High-Speed Crystal Oscillator Clock (HXTAL)

The External High-Speed Crystal Oscillator can provide a more accurate clock source for the system clock. A crystal with a specific frequency must be connected close to the two HXTAL pins. The external resistors and capacitors connected to the crystal must be adjusted according to the selected oscillator.

Figure 2-19. HXTAL External Crystal Circuit

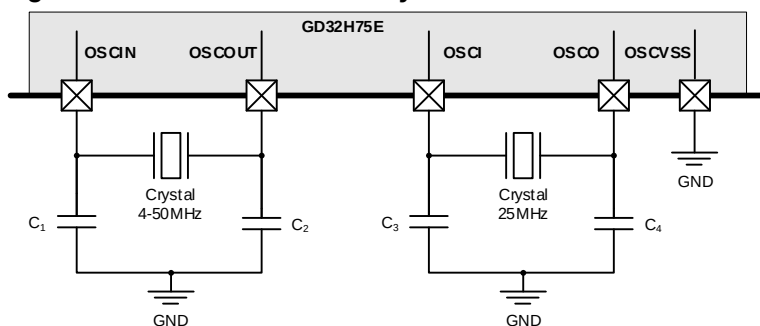
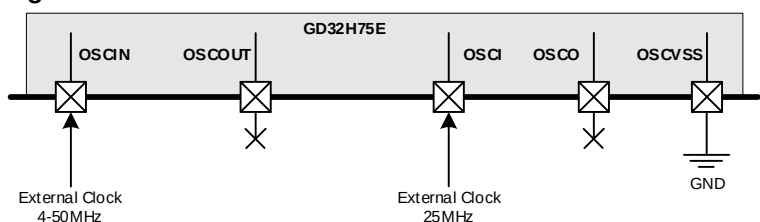


Figure 2-20. HXTAL External Clock Circuit

**Note:**

1. When using bypass input, the signal is input from OSCIN and OSCI, while OSCOUT and OSCO remain floating;
2. For the value of external matching capacitors, refer to the formula: $C_1 = C_2 = 2 * (C_{LOAD} - C_S)$, where C_S represents the parasitic capacitance of the PCB and MCU pins, typically 10pF. When selecting external high-speed crystals, it is recommended to use crystals with a load capacitance around 20pF. In this case, the values of the external matching capacitors C_1 and C_2 can be 20pF. Additionally, during PCB layout, place these capacitors as close as possible to the crystal pins. For more details on oscillator circuit design based on resonators, refer to [AN052 GD32 MCU Resonator-Based Clock Circuit](#);
3. C_S represents the parasitic capacitance on the PCB traces and MCU pins. The closer the crystal is to the MCU, the smaller the C_S , and vice versa. Therefore, in practical applications, if the crystal is far away from the MCU and causes abnormal operation, the external matching capacitors can be appropriately reduced;
4. When using an external high-speed crystal, it is recommended to connect a 1MΩ resistor in parallel across the crystal terminals to facilitate oscillation;
5. Accuracy: external active crystal oscillator > external passive crystal > internal crystal oscillator;
6. When using an active crystal oscillator normally, Bypass is enabled. At this time, the high level should not be lower than 0.7V_{DD}, and the low level should not exceed 0.3V_{DD};
7. The traces connecting the resonator to the MCU clock pins may have unequal lengths due to PCB layout constraints when connected to the OSCOUT and OSCIN pins. This results in inconsistent parasitic capacitance introduced by the two PCB traces, requiring the load capacitors on both sides of the resonator to differ in value to match the actual PCB. For such cases, it is recommended to contact the resonator manufacturer to calculate the actual values;

8. Clock circuit hardware protection design reference: [AN163 GD32 MCU EMC Hardware Protection Design Reference](#).

2.3.2. External Low-Speed Crystal Oscillator Clock (LXTAL)

LXTAL is an external low-speed crystal or ceramic resonator with a frequency of 32.768kHz. It provides a low-power and high-precision clock source for real-time clock circuits. The LXTAL oscillator can be turned on and off by setting the LXTALEN bit in the backup domain control register (RCU_BDCTL). The LXTALSTB bit in the backup domain control register RCU_BDCTL is used to indicate whether the LXTAL clock is stable. If the corresponding interrupt enable bit LXTALSTBIE in the interrupt register RCU_INT is set to '1', an interrupt will be generated after LXTAL stabilizes.

The external clock bypass mode can be selected by setting the LXTALBPS and LXTALEN to 1 'of the backup domain control register RCU_BDCTL. CK_LXTAL is consistent with the external clock signal connected to the OSC32IN pin.

Figure 2-21. LXTAL External Crystal Circuit

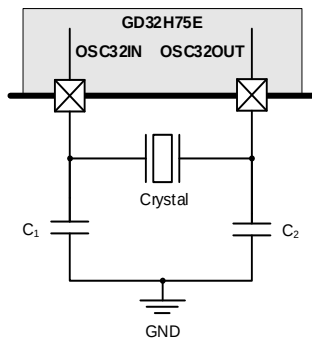
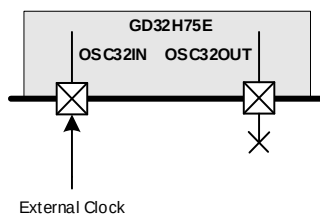


Figure 2-22. LXTAL External Clock Circuit



Note:

1. When using the bypass input, the signal is input from OSC32IN, and OSC32OUT remains floating;
2. For the size of the external matching capacitor, please refer to the formula: $C_1 = C_2 = 2 \cdot (C_{LOAD} - C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, the empirical value is between 2pF ~ 7pF, and 5pF is recommended as a reference value calculation. When it is recommended to use an external crystal, try to choose a crystal load capacitance of about 10pF, so that the externally connected matching capacitors C_1 and C_2 can be 10pF, and the PCB layout should be as close to the crystal pin as possible;

3. When the RTC selects IRC32K as the clock source and uses VBAT external independent power supply, if the MCU loses power at this time, the RTC will stop counting. After re powering on, the RTC will continue to accumulate timing based on the previous count value. If the application needs to use VBAT to power the RTC, and the RTC can still clock normally, the RTC must choose LXTAL as the clock source;
4. MCU can set the driving capacity of LXTAL. If during actual debugging, it is found that external low-speed crystals are difficult to vibrate, try adjusting the driving capacity of LXTAL to high;
5. The traces connecting the resonator to the MCU clock pins may cause inconsistent lengths of the traces connected to the OSCOUT and OSCIN pins due to the space constraints of the PCB layout. This will make the stray capacitances introduced by the two PCB traces inconsistent, so that the load capacitances on both sides of the resonator cannot be equal in value, and there needs to be a difference to match the actual PCB board. In this case, it is recommended to contact the resonator manufacturer to calculate the actual value.

2.3.3. Clock Output Capability (CKOUT)

The GD32H75E series can output internal related clock signals, and different clock signals can be selected by setting the CK_OUT0 clock source selection bit field CKOUT0SEL in the clock configuration register 0 (RCU_CFG2). The corresponding GPIO pin should be configured as a backup function I/O (AFIO) mode to output the selected clock signal. The selection of CK_OUT1 clock output source is achieved by setting the CKOUT1SEL bit field in the clock configuration register RCU_CFG2.

Table 2-8. Clock source selection for clock output 0

CKOUT0SEL[2:0]	Clock source
000	CK_IRC64MDIV
001	CK_LXTAL
010	CK_HXTAL
011	CK_PLL0P
100	CK_IRC48M
101	CK_PER
110	USBHS0 60M
111	USBHS1 60M

Table 2-9. Clock source selection for clock output 1

CKOUT1SEL[2:0]	Clock source
000	CK_SYS
001	CK_PLL1R
010	CK_HXTAL
011	CK_PLL0P
100	CK_LPIRC4M
101	CK_IRC32K

CKOUT1SEL[2:0]	Clock source
110	CK_PLL2R

By configuring the CKOUT0DIV bit field in the RCU_CFG2 register, the frequency of the CK_OUT0 output clock can be divided proportionally, thereby reducing the output frequency of CK_OUT0.

By configuring the CKOUT1DIV bit field in the RCU_CFG0 register, the frequency of the CK_OUT1 output clock can be divided proportionally, thereby reducing the output frequency of CK_OUT1.

2.3.4. HXTAL Clock Monitor (CKM)

Set the HXTAL clock monitoring enable bit CKMEN in the control register RCU_CTL, which enables the clock monitoring function. This function must be enabled after the delay of HXTAL start is completed, and disabled after HXTAL stop. Once an HXTAL fault is detected, HXTAL will automatically be disabled, and the HXTAL clock blocking interrupt flag bit CKMIF in the interrupt register RCU_INT will be set to '1', generating an HXTAL fault event. The interrupt caused by this fault is connected to the non maskable interrupt NMI of Cortex®-M7. If HXTAL is selected as the clock source for the system or PLL0, a HXTAL fault will prompt the selection of IRC64M as the system clock source and PLL0 will be automatically disabled. If HXTAL is selected as the clock source for PLLs, a HXTAL fault will cause the PLL to be automatically disabled.

2.3.5. LXTAL Clock Monitor (LCKM)

Set the LXTAL clock monitoring enable bit LCKMEN in the clock control register RCU_BDCTL, which enables the clock monitoring function. This function must be enabled after the LXTAL start delay is completed. The clock monitor on LXTAL operates in all modes except V_{BAT}. If a fault is detected on an external 32 kHz oscillator, an interrupt can be sent to the CPU. Then the software must disable the LCKMEN bit, stop the defective 32 kHz oscillator, and change the RTC clock source, or take any necessary measures to protect the application.

When LCKMEN is enabled, a 4-bit plus a counter will operate in the IRC32K domain. If the LXTAL clock gets stuck at 0 / 1 error or slows down by about 20KHz, the counter will overflow. LXTAL clock fault will be detected. Once an LXTAL fault is detected, the LXTAL clock blocking interrupt flag bit LCKMIF in the interrupt register RCU_INT will be set to '1', generating an LXTAL fault event. This interrupt is connected to the EXTI 18 interrupt line and can be used to wake up from sleep or deep sleep mode. LXTAL fault events can also wake up the system from standby mode.

2.3.6. ESC Clock Output Test Mode

To perform system debugging and observe the clock status, the IRQCKOUT bit in the INTC_CTL register can be set to 1 to output the oscillator clock on the IRQ pin. At this time,

the IRQ pin must be configured as push-pull output mode (IRQMODE = 1) for optimal performance.

2.4. Startup Configuration

The GD32H75E series MCU provides different boot sources, which can be selected through the boot pin and boot address 0/1 [15:0] in the Arm® Cortex®-M7 core register (FMCBTADDRMDF) boot address. Details can be found in [Table 2-10. BOOT Mode Selection](#) and [Table 2-11. Details of BOOT mode](#). The level state of the BOOT pin will be latched on the rising edge of the fourth CKSYS (system clock) after reset. Users can choose the desired boot source by setting the pin level of the BOOT after power on reset and system reset.

The BOOT_ADDR0[15:0] and BOOT_ADDR1[15:0] addresses allow the boot memory address to be configured to any address between 0x0000 0000 and 0x9000 0000. The boot mode can be obtained from the BOOT_MODE [2:0] bit field of the SYSCFG_USERCFG0 register.

Table 2-10. BOOT Mode Selection

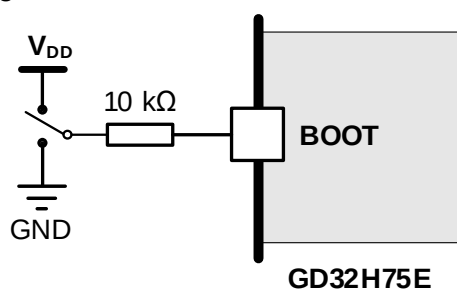
Boot source address	Boot mode selection pin
	BOOT
Boot address high bits: defined by BOOT_ADDR0[15:0] Boot address low bits: 0x0000	0
Boot address high bits: defined by BOOT_ADDR1[15:0] Boot address low bits: 0x0000	1

Table 2-11. Details of BOOT mode

SCR	SPC[7:0]	BOOT_ADDRESS (configured in BOOT_ADDRx(x = 0,1))	BOOT_MODE	Boot from
1	x	XXXX	SECURITY BOOT	ROM
0	Protection level high	0x9000_0000	USER BOOT	OSPI0
		0x7000_0000	USER BOOT	OSPI1
		0x0800_0000~max user flash	USER BOOT	BOOT_ADDRESS
		other	USER BOOT	0x0800_0000
	No protection / Protection level low	0x9000_0000	USER BOOT	OSPI0
		0x7000_0000	USER BOOT	OSPI1
		0x2408_0000~ max RAM shared(ITCM/DTCM/AXI)	SRAM BOOT(RAM shared)	BOOT_ADDRESS
		0x2400_0000~ max AXI SRAM	SRAM BOOT(AXI SRAM)	BOOT_ADDRESS
		0x2000_0000	SRAM BOOT(DTCM)	0x2000_0000
		0x0800_0000~max user flash	USER BOOT	BOOT_ADDRESS

SCR	SPC[7:0]	BOOT_ADDRESS (configured in BOOT_ADDRx(x = 0,1))	BOOT_MODE	Boot from
		0x0000_0000	SRAM BOOT(ITCM)	0x0000_0000
		0x1FF0_0000	SYSTEM BOOT	BootLoader
		Other	USER BOOT	0x0800_0000 (BOOT Pin = 0)
			SYSTEM BOOT	BootLoader (BOOT Pin = 1)

Figure 2-23. Recommended BOOT Circuit Design



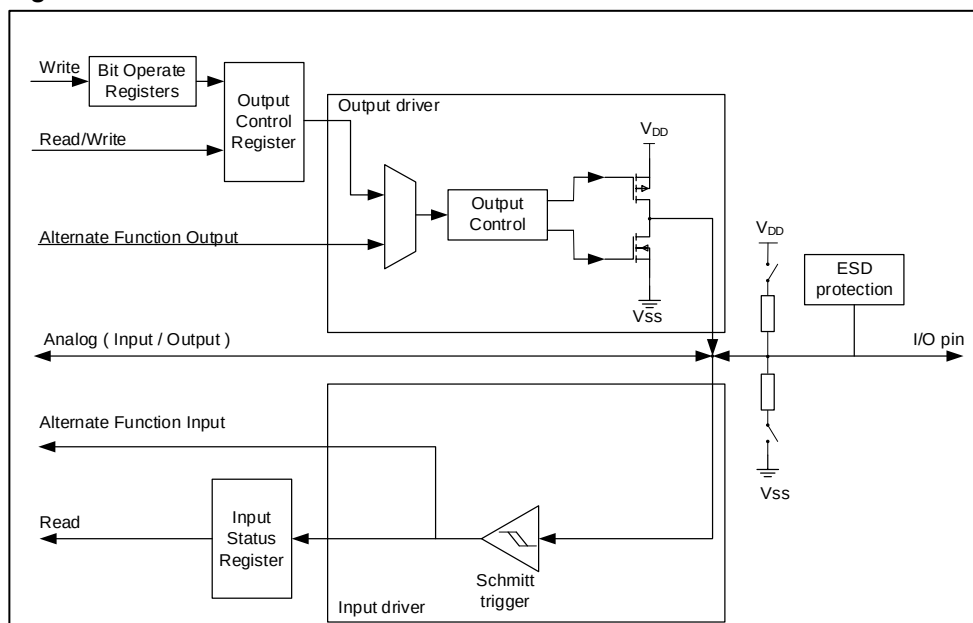
Note: After the MCU starts running, any changes to the BOOT state will only take effect after a system reset.

2.5. Typical Peripheral Modules

2.5.1. GPIO Circuit

The GD32H75E supports up to 116 general-purpose I/O pins (GPIO), which are categorized as PA0 ~ PA15, PB0 ~ PB15, PC0 ~ PC15, PD0 ~ PD15, PE0 ~ PE15, PF5 ~ PF15, PG6 ~ PG9, PG13 ~ PG15, PH0 ~ PH13, PA0_C, PA1_C, PC2_C, PC3_C. Each on-chip device uses it to implement logical input / output functions. Each GPIO port has relevant control and configuration registers to meet the specific application requirements. The external interrupt of the GPIO pin of the on-chip device is controlled and configured by the register of the EXTI module. The basic structure of the GPIO port is shown in [Figure 2-24. Basic structure of standard IO.](#)

Figure 2-24. Basic structure of standard IO

**Note:**

1. IO ports are divided into 5V-tolerant and non-5V-tolerant. Pay attention to the voltage tolerance of IO ports during use; refer to the datasheet for details;
2. 5V-tolerant IO ports can be connected to a 5V voltage when configured in open-drain output mode or input mode. When configured in push-pull output mode, connecting to a 5V voltage is prohibited;
3. During or after reset, IO ports with alternate functions not activated default to floating input mode with undefined electrical characteristics. To achieve consistent power consumption, it is recommended to configure all IO ports as analog input mode initially, and then modify them to the required mode based on application needs (this includes ports not bonded out);
4. To improve EMC performance, unused IO pins are recommended to be hardware-pulled up or pulled down;
5. The drive capability of PC13, PC14, and PC15 IO ports is weaker, with limited output current capacity (around 3mA). When configured in output mode, their operating speed should not exceed 2MHz (maximum load of 30pF);
6. Within the same group, only one IO port with the same PIN number can be configured as an external interrupt. For example, PA0, PB0, and PC0 support only one of these IO ports generating an external interrupt, they cannot all be configured in external interrupt mode simultaneously;
7. For non-5V-tolerant IOs, applying a voltage exceeding V_{DD} externally may cause sink current;
8. Pins connected to external devices, switches, or buttons should have ESD protection circuits added near the external connection. For more hardware protection design details, refer to the official website's [AN163 GD32 MCU EMC Hardware Protection Design Reference](#).

2.5.2. ESC-GPIO Circuit

Supports up to 35 general-purpose input/output pins (GPIO) for mode configuration. Each GPIO port determines its current function based on the chip's current operating mode, including input/output mode. Each GPIO pin can be configured as pull-up, pull-down, or floating. When the pin is in output mode, it can be configured as push-pull, open-drain, or open-source output.

- Each pin has weak pull-up/pull-down functionality.
- Push-pull/open-drain/source-drain output enable control.
- Configure the functionality of selected pins based on the chip mode.

When the chip is in different modes, each pin has different functions.

SPI mode: When PDI_TYPE equals 0x80 and the MCU_PDI_TYPE pin equals 0, AFIO is configured to SPI mode.

Table 2-12. GPIO Configuration Table

Mode name	Register/signal	Description
spi8w_gpio	pdi_type / mcu_pdi_type / spi_ext_mode / sip_mode / line_mode	pdi_type == 0x80; mcu_pdi_type == 1'b0; sip_mode == 1'b0; line_mode == 2'b11; LINKACTLED0 Pin must be externally drop-down LINKACTLED1 Pin must be externally drop-down
spi8w_mii_down	pdi_type / mcu_pdi_type / spi_ext_mode / sip_mode / line_mode / chip_mode	pdi_type == 0x80; mcu_pdi_type == 1'b0; sip_mode == 1'b0; line_mode == 2'b10; chip_mode == 2'b10 LINKACTLED0 Pin must be externally drop-down LINKACTLED1 Pin must be externally pull-up
spi8w_mii_up	pdi_type / mcu_pdi_type / spi_ext_mode / sip_mode / line_mode / chip_mode	pdi_type == 0x80; mcu_pdi_type == 1'b0; sip_mode == 1'b0; line_mode == 2'b10; chip_mode == 2'b11; LINKACTLED0 Pin must be externally pull-up LINKACTLED1 Pin must be externally pull-up

Introduce ESC pins according to different function groups:

Table 2-13. LAN Port A Pin Description

Pin number	Pin name	Pin function	Pin type	Description
J17	TXPA	TXPA	I/O	Port A twisted pair transmit/receive positive channel 1. Refer to Note 1.

Pin number	Pin name	Pin function	Pin type	Description
H17	TXNA	TXNA	I/O	Port A twisted pair transmit/receive negative channel 1. Refer to Note 1.
G17	RXPA	RXPA	I/O	Port A twisted pair transmit/receive positive channel 2. Refer to Note 1.
F17	RXNA	RXNA	I/O	Port A twisted pair transmit/receive negative channel 2. Refer to Note 1.
G13	RTXA	RTXA	I	Configure pin, external 6kΩ grounded. Refer to Note 2.

Table 2-14. LAN Port B Pin Description

Pin number	Pin name	Pin function	Pin type	Description
E17	TXPB	TXPB	I/O	Port A twisted pair transmit/receive positive channel 1. Refer to Note 1.
D17	TXNB	TXNB	I/O	Port A twisted pair transmit/receive negative channel 1. Refer to Note 1.
C17	RXPB	RXPB	I/O	Port A twisted pair transmit/receive positive channel 2. Refer to Note 1.
B17	RXNB	RXNB	I/O	Port A twisted pair transmit/receive negative channel 2. Refer to Note 1.
B13	RTXB	RTXB	I	Configure pin, external 6kΩ grounded. Refer to Note 2.

Note:

1. In copper twisted-pair mode, Channel 1 and Channel 2 are used as one transmit pair and one receive pair. Twisted-pair pin naming conventions apply to standard connections. If Auto-MDIX is enabled and a crossover connection is detected or manually selected, RX and TX pins will be internally swapped.
2. Ensure the 6KΩ is placed close to the IC.
3. Port A is connected to EtherCAT port 0 or 2, and port B is connected to EtherCAT port 1.

Table 2-15. LAN Port A and Port B Power Pin Description

Pin number	Pin name	Pin function	Pin type	Description
D12	VDD3A1	VDD3A1	P	+3.3V Port A analog power supply. Refer to Note 4.
B12	VDD3A2	VDD3A2	P	+3.3V Port B analog power supply. Refer to Note 4.
A14	VDD1A1	VDD1A1	P	+1.1V Port A analog power supply. This pin must be connected to the VDD1A2 pin for proper operation. Refer to Note 4.

Pin number	Pin name	Pin function	Pin type	Description
A13	VDD1A2	VDD1A2	P	+1.1V Port B analog power supply. This pin must be connected to the VDD1A1 pin for proper operation. Refer to Note 4.

Note:

- For detailed circuit connections, refer to [Figure 2-5. Recommended power supply design for GD32H75E series \(enable ESC internal regulator\)](#) and [Figure 2-41. GD32H75E Recommended Reference Schematic Design](#).

Table 2-16. EtherCAT MII Port and Configuration Pin Description

Pin number	Pin name	Pin function	Pin type	Description
D7	OE_EXT	ESC_CLKOUT_25M	I/O, 5VT	25MHz clock pin. This pin is a free-running 25MHz clock and can be used as the clock input for the PHY. Refer to Note 5.
E6, F5, E5, E4	IO15, IO14, IO13, IO12	MII_RXD[3:0]	I/O, 5VT	Receive data pins. These pins receive data from the external PHY.
D6	IO11	MII_RX_DV	I/O, 5VT	Receive data valid pin. This pin receives the data valid signal from the external PHY.
H2	IO9	MII_RX_ER	I/O, 5VT	Receive error pin. This pin receives the error signal from the external PHY.
K2	IO0	MII_RX_CLK	I/O, 5VT	Receive clock pin. This pin receives the clock from the external PHY.
B8, A8, A5, B5	IO8, IO7, IO6, IO5	MII_TXD[3:0]	I/O, 5VT	Transmit data pins. These pins send data to the external PHY.
B8, A8	IO8, IO7	TX_SHIFT[1:0]	I/O, 5VT	MII transmit timing shift configuration pin. Refer to Note 6. TX_SHIFT[1] is on MII_TXD[3], TX_SHIFT[0] is on MII_TXD[2].
A4	IO4	MII_TXEN	I/O, 5VT	Transmit data enable pin. This pin sends a data enable signal to the external PHY.
B14	IO3	MII_LINK	I/O, 5VT	Link status indication pin. This pin signal is provided by the PHY to indicate a 100Mbps full-duplex link is established. The signal polarity is configured by the MII_LINKPOL configuration pin.
J4	IO1	ESC_MDC	I/O, 5VT	SMI clock pin. This pin is the serial management clock for the external PHY.
K3	IO2	ESC_MDIO	I/O, 5VT	SMI data pin. This pin is the serial management interface data input/output for the external PHY. Refer to Note 7.
F2	IO10	MII_LINKPOL	I/O, 5VT	MII_LINK polarity configuration pin. Refer to Note 6.

Note:

5. When connecting to an ESC chip with an external PHY, ESC_CLKOUT_25M cannot be used in OSPI+MII mode, and the same active clock needs to be used. It is recommended to refer to the typical circuit [Figure 2-29. Connection diagram for using external PHY](#).
6. The pin configuration is latched during power-on reset or RSTN pin reset. For detailed information, refer to [2.5.4 ESC Hardware Configuration Table](#).
7. An external pull-up is required to ensure the non-driven state of the ESC_MDIO signal is logic 1.

Table 2-17. OSPI Pin Description

Pin number	Pin name	Pin function	Pin type	Description
-	-	CSN	-	OSPI chip select signal. Connect to PG12, refer to Note 8.
-	-	SCK	-	OSPI serial clock signal. Connect to PF4, refer to Note 8.
-	-	SIO0	-	OSPI serial data input and output. Connect to PF0, refer to Note 8.
-	-	SIO1	-	OSPI serial data input and output. Connect to PF1, refer to Note 8.
-	-	SIO2	-	OSPI serial data input and output. Connect to PF2, refer to Note 8.
-	-	SIO3	-	OSPI serial data input and output. Connect to PF3, refer to Note 8.
-	-	SIO4	-	OSPI serial data input and output. Connect to PG0, refer to Note 8.
-	-	SIO5	-	OSPI serial data input and output. Connect to PG1, refer to Note 8.
-	-	SIO6	-	OSPI serial data input and output. Connect to PG10, refer to Note 8.
-	-	SIO7	-	OSPI serial data input and output. Connect to PG11, refer to Note 8.

Note:

8. OSPI signals do not have external pins and are internally connected within the chip.

Table 2-18. EtherCAT Distributed Clock Pin Description

Pin number	Pin name	Pin function	Pin type	Description
B7	SYNC1_LAT CH1	SYNC1	I/O, 5VT	Synchronous (output) signals. These signal directions can be configured bitwise. Refer to Note 9.
		LATCH1		Latched (input) signals. These signal directions can be configured bitwise. Refer to Note 9.

H3	SYNC0_LATCH0	SYNC0	I/O, 5VT	Synchronous (output) signals. These signal directions can be configured bitwise. Refer to Note 9.
		LATCH0		Latched (input) signals. These signal directions can be configured bitwise. Refer to Note 9.

Note:

9. Do not drive these signals (high-impedance state) before loading the EEPROM.

Table 2-19. EtherCAT GPIO Pin Description

Pin number	Pin name	Pin function	Pin type	Description
-	IO[15:0]	PDI_GPIO[15:0]	I/O, 5VT	These pins are input/output or bidirectional data. Refer to Note 9.
B9	IO16	MCU_PDI_TYPE	I/O, 5VT	Bus interface configuration pin. Refer to Note 6.
C9	IO17	EFUSE_LDO_BYP	I/O, 5VT	EFUSE_LDO configuration pin. Refer to Note 6.
D10	IO18	PHYRST_MODE	I/O, 5VT	PHYRST_MODE configuration pin. Refer to Note 6.
N15	OUTVALID	OUTVALID	I/O, 5VT	Output valid pin. This pin indicates output is valid and can be captured in an external register. Refer to Note 9.
M14	LATCH_IN	LATCH_IN	I/O, 5VT	Latch input pin. This pin is the external data latch signal. Input data is sampled on each rising edge of LATCH_IN.
N14	WD_TRIG	WD_TRIG	I/O, 5VT	Watchdog trigger pin. This pin outputs the SyncManager watchdog trigger signal. Refer to Note 9.
M15	WD_STATE	WD_STATE	I/O, 5VT	Watchdog status pin. This pin outputs the SyncManager watchdog status. 0 indicates watchdog timeout. Refer to Note 9.
F16	SOF	SOF	I/O, 5VT	Frame start. This pin outputs the frame start signal, indicating the start of Ethernet/EtherCAT frames. Refer to Note 9.
H16	EOF	EOF	I/O, 5VT	Frame end. This pin outputs the frame end signal, indicating the end of Ethernet/EtherCAT frames. Refer to Note 9.
D7	OE_EXT	OE_EXT	I/O, 5VT	Output enable pin. This pin controls the output enable. When low, it clears the output data.

Note:

10. In OSPI mode, due to the large number of SPI Pins used, PDI_GPIO15 cannot be used in OSPI+GPIO mode.

Table 2-20. EEPROM Pin Description

Pin number	Pin name	Pin function	Pin type	Description
K4	EESCL	EEPROM_CLK	I/O, 5VT	This pin is the I2C serial data input/open-drain output. Refer to Note 11.
L4	EESDA	EEPROM_DATA	I/O, 5VT	This pin is the I2C clock open-drain output. Refer to Note 11.

Note:

11. This pin must always be pulled up via an external resistor.

Table 2-21. LED and configuration pin descriptions

Pin number	Pin name	Pin function	Pin type	Description
E11	LINKACTLED0	LINKACTLED0	I/O, 5VT	This pin is the Port 0 link/activity LED output (Off = No link; On = Link but no activity; Blinking = Link with activity). This pin is configured as an open-drain/open-source output. The selection of open-drain or open-source and polarity is determined by the configuration pin value sampled during reset.
		CHIP_MODE0		This configuration pin, together with CHIP_MODE1, configures the chip mode. Refer to Note 6.
F13	LINKACTLED1	LINKACTLED1	I/O, 5VT	This pin is the Port 1 link/activity LED output (Off = No link; On = Link present but no activity; Blinking = Link present with activity). This pin is configured as an open-drain/open-source output. The selection of open-drain or open-source and polarity is determined by the configuration pin value sampled during reset.
		CHIP_MODE1		This pin is configured with CHIP_MODE0 to set the chip mode. Refer to Note 6.
F2	IO10	LINKACTLED2	I/O, 5VT	This pin is the Port 2 link/activity LED output (Off = No link; On = Link present but no activity; Blinking = Link present with activity). This pin is configured as an open-drain/open-source output. The selection of open-drain or open-source and polarity is determined by the configuration pin value sampled during reset.
F14	EESIZE	RUNLED	I/O, 5VT	This pin is the Port 1 link/activity LED output (Off = No link; On = Link present but no activity; Blinking = Link present with activity). This pin is configured as an open-drain/open-source output. The selection of open-drain or

Pin number	Pin name	Pin function	Pin type	Description
				open-source and polarity is determined by the configuration pin value sampled during reset.
		EEPROM_SIZE		This configuration pin sets the EEPROM size value. Refer to Note 6.

Table 2-22. Other pin descriptions

Pin number	Pin name	Pin function	Pin type	Description
-	IRQ	IRQ	-	Interrupt request output pin. Refer to Note 12.
A9	RSTN	RSTN	-	System reset input pin. External low-level signal to reset the device.
A10	REG_EN	REG_EN	I/O	ESC internal LDO enable pin. Active high.
G14	TESTMODE	TESTMODE	I/O, 5VT	Test mode pin. This pin must be connected to the V _{SS} pin for proper operation.
A11	OSCI	OSCI	I/O	Oscillator input pin. External 25MHz oscillator input. This pin can also be driven by an active oscillator, in which case OSCO should remain unconnected.
B11	OSCO	OSCO	I/O	Oscillator output pin. External 25MHz oscillator input.
A12	OSCVDD11	OSCVDD11	P	Oscillator +1.1V power supply. When the internal regulator is disabled, this pin must supply power to the oscillator.
C11	OSCVSS	OSCVSS	P	Oscillator ground. This pin must be grounded under all circumstances.

Note:

12. The IRQ pin and PJ10 pin have no external pins and are internally connected within the chip.

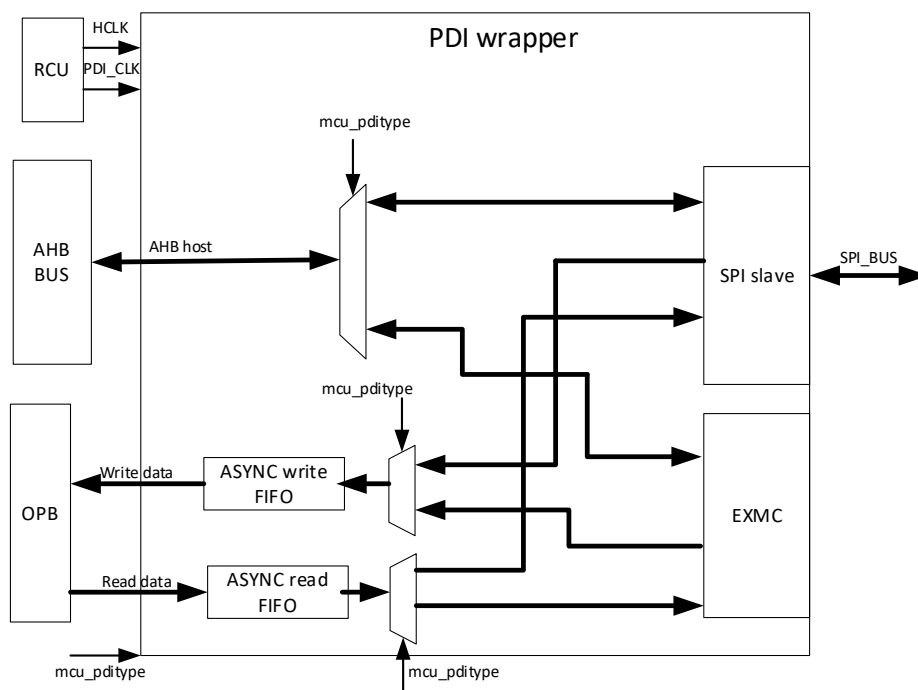
Table 2-23. Core and I/O power pin descriptions

Pin number	Pin name	Pin function	Pin type	Description
-	VDD33	VDD33	P	Internal regulator +3.3V power supply. This pin must be connected to +3.3V under all circumstances.
-	VDDIO	VDDIO	P	I/O power supply. Supports +1.8V to +3.3V.
-	VDDCR	VDDCR	P	+1.1V digital core power supply. When the internal regulator is disabled, these pins must supply power to the core.
-	VSS	VSS	P	Common ground terminal.

2.5.3. ESC Bus Interface (PDI Wrapper) Circuit

In ESC, EXMC and SPI SLAVE are encapsulated into a wrapper for system integration. The PDI Wrapper can only be used with SPI. Two asynchronous FIFOs are internally integrated, each being 16 x 32-bit. It operates only in SPI SLAVE mode, selected by the MCU_PDI_TYPE pin.

Figure 2-25. PDI Wrapper block diagram



Note:

1. The MCU_PDI_TYPE pin selects the working access interface module. When the MCU_PDI_TYPE pin is 0, the SPI slave can access internal data;
2. PDI_CLK provides the clock for SPI_SLAVE. When the MCU_PDI_TYPE pin is 0, PDI_CLK is sourced from SPI_SCK;
3. HCLK is a 100MHz system clock that provides the clock for ASYNC_FIFO and SPI_SLAVE.

2.5.4. ESC Hardware Configuration Table

ESC hardware configuration automatically configures various device functions to user-defined values. Hardware configuration is latched during power-on reset (POR), EtherCAT system reset, or RSTN pin reset.

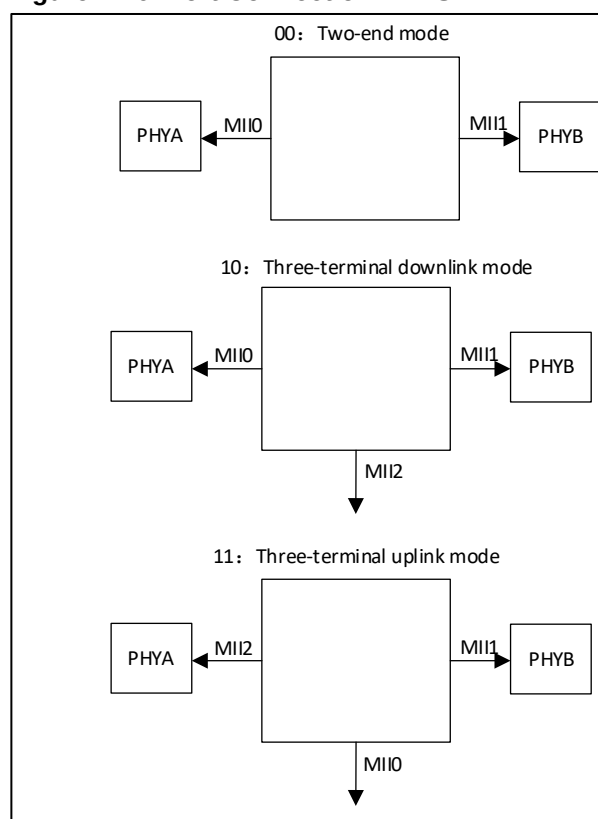
Table 2-24. ESC Hardware Configuration Table

Pin name	Pin function	Description
IO16	MCU_PDI_TYPE	Bus Interface Configuration Pin: Configures the working access interface module. 0 = SPI module. (Only supports SPI mode)
IO17	EFUSE_LDO_BYP	EFUSE_LDO Configuration Pin: Configures the EFUSE internal voltage regulator bypass. 0 = Internal LDO is active. (Default) 1 = Internal LDO is bypassed.
IO18	PHYRST_MODE	PHYRST_MODE Configuration Pin: Configures the PHY reset control register. 0 = RCU_RSTCFG[9:8] bits are invalid. (Default) 1 = RCU_RSTCFG[9:8] bits are valid, allowing PHY reset control via the register.
IO8, IO7	TX_SHIFT[1:0]	MII Transmit Timing Shift Configuration Pin: These configuration pins determine the MII transmit timing shift value for the MII port. 00 = 0 ns (Default) 01 = 10 ns 10 = 20 ns 11 = 30 ns
IO10	MII_LINKPOL	MII_LINK Polarity Configuration Pin: Configures the polarity of the MII_LINK pin. 0 = MII_LINK is active low, indicating a 100 Mbps full-duplex link is established. (Default) 1 = MII_LINK is active high, indicating a 100 Mbps full-duplex link is established.
EESIZE	EEPROM_SIZE	EEPROM Size Configuration Pin: Configures the EEPROM size range. 0 = Less than 16 Kb. 1 = More than 16 Kb.
LINKACTLED1, LINKACTLED0	CHIP_MODE[1:0]	EtherCAT Chip Mode Configuration Pin: These configuration pins determine the number of active ports and port types. 00 = Dual-port mode. EtherCAT Port 0 and Port 1 are connected to internal PHYA and PHYB. In this mode, SPI + GPIO mode output is unaffected, while MII signals are not output in SPI + MII mode. 01 = Reserved. 10 = 3-port downstream mode. EtherCAT Port 0 and Port 1 are connected to internal PHYA and PHYB. Port 2 is connected to an external MII port. 11 = 3-port upstream mode. EtherCAT Port 2 and Port 1 are connected to internal PHYA and PHYB. Port 0 is connected to an external MII port.

Pin name	Pin function	Description
TESTMODE	TESTMODE	Test Mode. 0 (Default).

Note:

1. Ensure that the configuration pins meet the timing requirements, refer to the datasheet for details. If the configuration pins are not at the correct voltage level before latching, the device may capture incorrect configuration values.
2. It is recommended to connect 10kΩ pull-up or pull-down resistors to the configuration pins externally.

Figure 2-26. Port Connection PHYS**2.5.5. Ethernet PHYS**

The GD32H75E includes two voltage-type PHYs, A and B, which are functionally identical. PHY A is connected to EtherCAT port 0 or 2, while PHY B is connected to EtherCAT port 1. These PHYs interface with their respective MAC via an internal MII interface. The PHYs comply with the IEEE 802.3 Physical Layer for Twisted Pair Ethernet and can be configured for full duplex 100 Mbps (100BASE-TX) Ethernet operation. All PHYs registers follow the IEEE 802.3 specified MII management register set and are fully configurable.

- Fully IEEE 802.3 100 Base-TX compliant and supports EEE
- Auto negotiation and parallel detection capability for automatic speed and duplex selection
- Supports MII and RMII interfaces

- Auto polarity correction in 10Base-T
- Supports Auto-MDIX function for Plug-n-Play
- Programmable loopback mode for diagnostic
- Supports programmable LED output for different applications power on LED Self-Test
- Supports WOL(Wake-On-Lan) functionality

Figure 2-27. PHY Functional Block Diagram

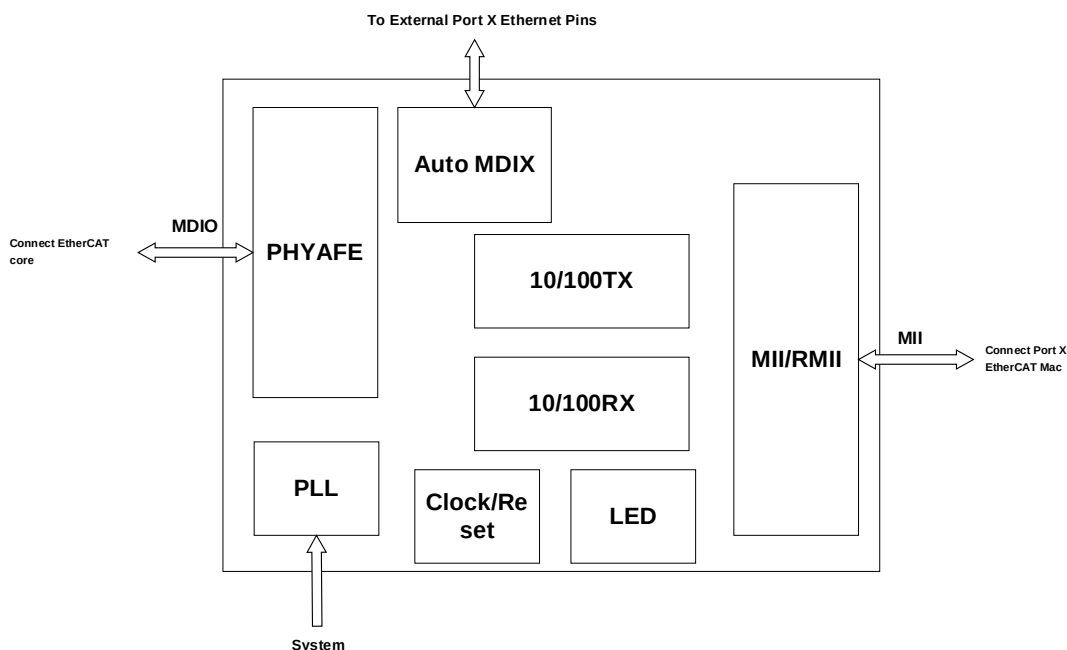
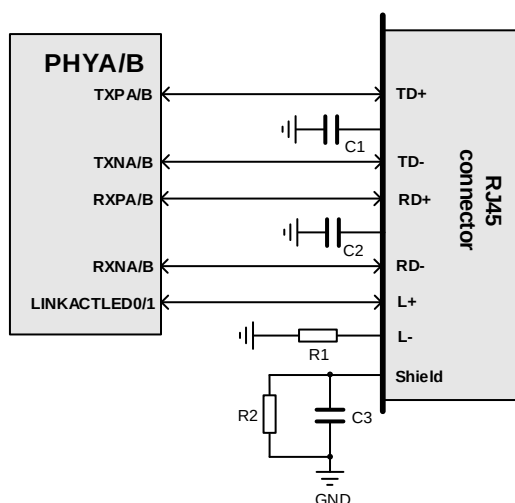


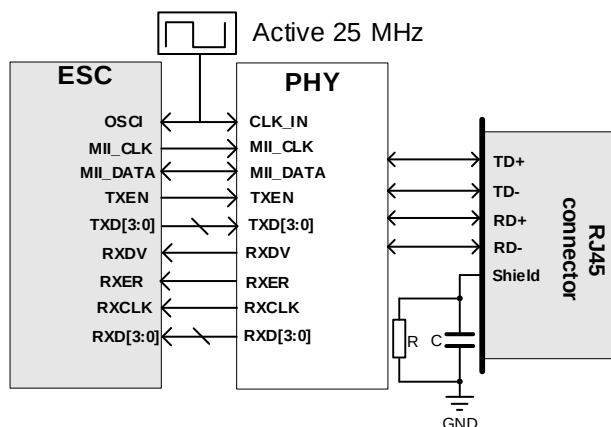
Figure 2-28. Connection Diagram of Built-in PHY with RJ45 Port (with Internal Transformer)



Recommended: R1 = 470 Ω , R2 = 1 M Ω , C1 = 0.1 μ F, C2 = 0.1 μ F, C3 = 4.7 nF.

The GD32H75E provides an MII interface for the external PHY. The connection diagram for using the external PHY is shown in [Figure 2-29. Connection diagram for using external PHY.](#)

Figure 2-29. Connection diagram for using external PHY



Note: When connecting an external PHY with the OSC chip, the same active clock must be used.

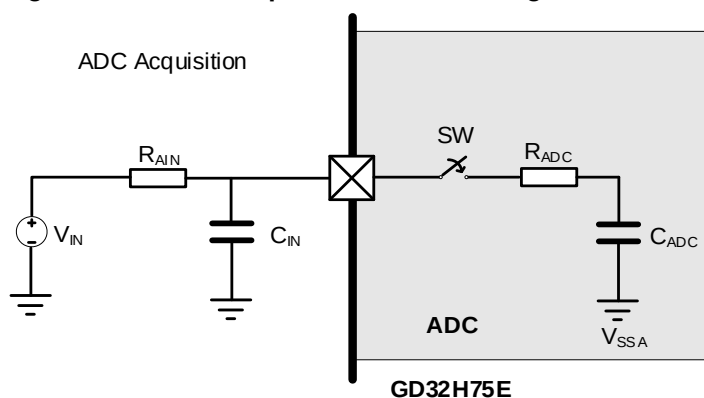
2.5.6. ADC Circuit

The GD32H75E integrates internal 12/14-bit SAR ADC modules. ADC0 has 20 external channels, 1 internal channel(DAC0_OUT0 channel), ADC1 has 18 external channels, 3 internal channels(the battery voltage, V_{REFINT} inputs channel and DAC0_OUT1 channel), ADC2 has 17 external channels, 4 internal channels(the battery voltage, V_{REFINT} inputs channel, temperature sensor and high-precision temperature sensor). After sampling and conversion, the conversion results can be stored in the corresponding data registers according to the least significant bit(LSB) alignment or the most significant(MSB) bit alignment(ADC0 / 1 are 32-bit data register, ADC2 is 16-bit data register). An on-chip hardware oversample scheme improves performances and reduces the computational burden of MCU.

If ADC is used to collect external input voltage and the sampled data fluctuates significantly, the interference might be caused by power supply fluctuations. Calibration can be performed by sampling the internal V_{REFINT} to deduce the external sampled voltage.

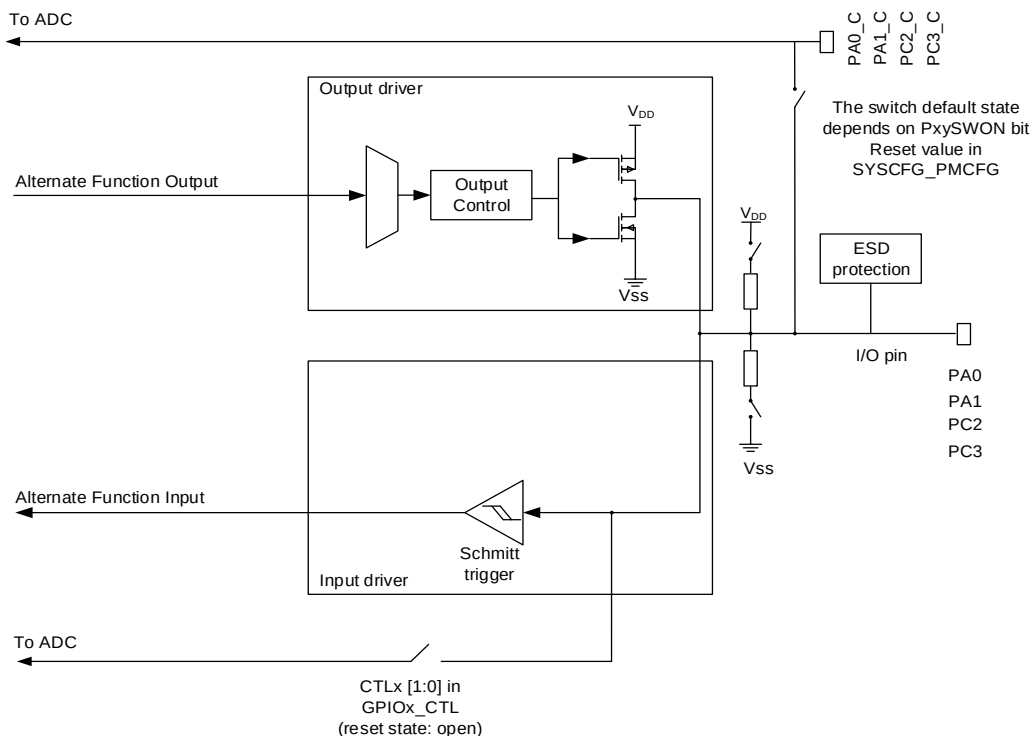
When designing the ADC circuit, it is recommended to place a small capacitor C_{IN} at the ADC input pin, as shown in [Figure 2-30. ADC Acquisition Circuit Design](#).

Figure 2-30. ADC Acquisition Circuit Design



Some pins are directly connected to the ADC analog input terminals PA0_C, PA1_C, PC2_C, and PC3_C (as shown in [Figure 2-31. ADC analog configuration](#)): Pxy_C and Pxy pins are directly connected through an analog switch.

Figure 2-31. ADC analog configuration



2.5.7. Internal Temperature Sensor Calibration

The GD32H75E series MCU is internally integrated with a temperature sensor (ADC2_CH18), a high-precision temperature sensor (ADC2_CH20) and a low power digital temperature sensor (LPDTS), with an effective temperature measurement range of -40 °C to 105 °C. The output voltage of the temperature sensor varies linearly with temperature. To ensure the accuracy of temperature measurement, it is necessary to provide an accurate and low-temperature drift reference voltage V_{REFP} for the ADC.

The output voltage of the temperature sensor varies linearly with temperature. Due to the diversity of chip production processes, the deviation of the temperature change curve may vary between chips (up to 45 °C difference). Internal temperature sensors are more suitable for detecting temperature changes than for measuring absolute temperature. If precise temperature measurement is required, an external temperature sensor should be used to calibrate this offset error.

The internal voltage reference (V_{REFINT}) provides a stable (bandgap reference) voltage output to the ADC and comparator. V_{REFINT} internal connection to ADC1_CH17 / ADC2_CH19 input channel.

Using temperature sensors:

1. Configure the conversion sequence and sampling time of the temperature sensor channel (ADC1_CH18) to ts_temp us;
2. Set the TSVEN1 bit in the ADC_CTL1 register to enable the temperature sensor;
3. Set the ADCON bit of the ADC_CTL1 register, or trigger ADC conversion externally;
4. Read and calculate the temperature sensor data $V_{\text{temperature}}$ from the ADC data register, and calculate the actual temperature using the following formula:
$$\text{Temperature}(\text{°C}) = \{(V_{25} - V_{\text{temperature}}) / \text{Avg_Slope}\} + 25$$

V_{25} : The voltage of the internal temperature sensor at 25 °C, please refer to the datasheet for typical values.

Avg_Slope: The average slope of the temperature and internal temperature sensor voltage curve, please refer to the datasheet for typical values.

Using high-precision temperature sensors:

1. Configure the conversion sequence and sampling time of the temperature sensor channel (ADC2_CH20) to ts_temp us;
2. Set the TSVEN2 bit in the ADC_CTL1 register to enable the temperature sensor;
3. Set the ADCON bit of the ADC_CTL1 register, or trigger ADC conversion externally;
4. Read and calculate the temperature sensor data $V_{\text{temperature}}$ from the ADC data register, and calculate the actual temperature using the following formula:
$$\text{Temperature}(\text{°C}) = \{(V_{\text{temperature}} - V_{25}) / \text{Avg_Slope}\} + 25$$

V_{25} : The voltage of the internal temperature sensor at 25 °C, please refer to the datasheet for typical values.

Avg_Slope: The average slope of the temperature and internal temperature sensor voltage curve, please refer to the datasheet for typical values.

Note:

1. When the high-precision temperature sensor is enabled, the ADC2 clock must not exceed 5MHz;
2. When a high-precision temperature sensor is enabled, it is necessary to wait for at least 3 ADC sampling cycles, and the first three converted data should be discarded;
3. The accuracy of high-precision temperature sensor can be improved by oversampling and software averaging (50 point averaging is generally recommended).

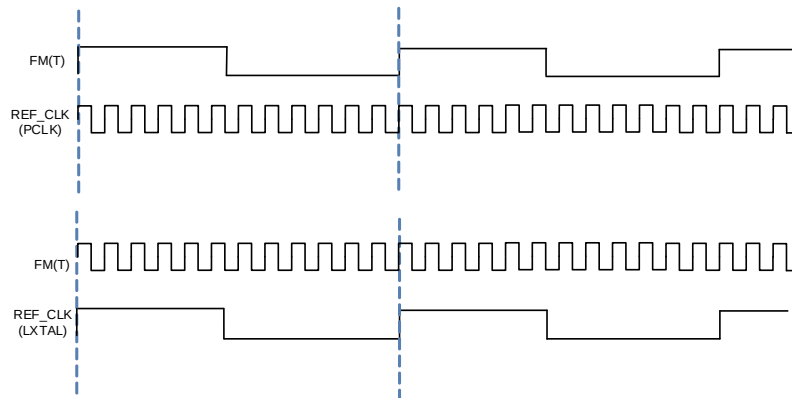
Low power digital temperature sensor(LPPTS) is used to transmit square wave, which is converted by temperature and the frequency is proportional to the absolute temperature. The frequency measurement is based on the PCLK or the LXTAL clock.

A signal is output, which FM(T) frequency (typically 641 kHz) is related to temperature, by the analog part of temperature sensor. Two counters are embedded in the temperature sensor block, which makes the counting mode relevant to the reference clock frequency. The counting result is stored in the LPPTS_DATA register.

- When the reference clock is PCLK, the measurement method is to sample one or multiple FM(T) cycles and count at the rising edge and falling edge of PCLK.
- When the reference clock is LXTAL, the measurement method is to sample one or

multiple LXTAL cycles and count at the rising edge and falling edge of FM(T).

Figure 2-32. Measurement method



The Temperature calculation formula When PCLK is used:

$$T = T_0 + ((2 \times F_{PCLK} / COVAL) \times SPT - 100 \times FREQ) / RF_CF$$

The Temperature calculation formula When LXTAL is used:

$$T = T_0 + (((F_{LXTAL} \times COVAL) / (2 \times SPT)) - (100 \times FREQ)) / RF_CF$$

T0: T0 equal to 25 °C.

COVAL: COVAL is the value of the counter output value for temperature sensor which measured and stored in the LPDTS_DATA register.

SPT: SPT is Sampling time for temperature sensor.

FREQ: FREQ is engineering value of the frequency measured at T0 for temperature sensor which measured and stored in the LPDTS_SDATA register. It is expressed in hundreds of Hertz.

RF_CF: RF_CF is the engineering value of the ramp coefficient for the temperature sensor.

2.5.8. USB Circuit

The GD32H75E series MCU has an embedded USBHS interface, providing a USB interconnection solution for portable devices. USBHS not only supports host mode and device mode, but also supports OTG mode that follows HNP (Host Negotiation Protocol) and SRP (Session Request Protocol). The USBHS includes an internal USB PHY that can be configured to either full speed or high speed, and no longer requires an external PHY chip. USBHS can support all four transmission methods defined by the USB 2.0 protocol (control transmission, batch transmission, interrupt transmission, and synchronous transmission). In addition, there is a DMA engine operation inside the USBHS that can act as an AHB bus host to accelerate data transmission between the USBHS and the system. For the operation of full speed devices, it also supports Battery Charge Detection (BCD), Additional Detection Protocol (ADP), and Link Layer Power Management (LPM).

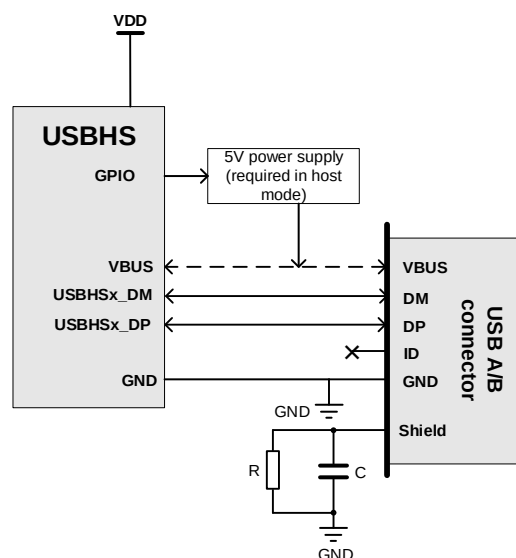
The USB protocol requires a clock accuracy of no less than 500ppm, and internal clocks may not be able to achieve such accuracy. Therefore, it is recommended to use external crystals or active crystal oscillators as the clock source for the USB module when using the USB function. When designing the circuit, in order to improve the ESD performance of USB, it is recommended to design a resistance capacitance discharge isolation circuit for the USB shell. The description of the USBHS signal line is shown in [Table 2-25. USBHS signal line description](#).

Table 2-25. USBHS signal line description

I/O port	Type	Description	Note
VBUS	Input	Bus power port	For internal PHY only
DM	Input/Output	Differential data line - port	For internal PHY only
DP	Input/Output	Differential data line + port	For internal PHY only
ID	Input	USB identification: Mini connector identification port	For internal PHY only
ULPI_D[7:0]	Input/Output	ULPI Data line	For external ULPI PHY
ULPI_NXT	Input	ULPI next line	For external ULPI PHY
ULPI_DIR	Input	ULPI Direction	For external ULPI PHY
ULPI_STP	Output	ULPI Stop	For external ULPI PHY
ULPI_CLK	Input	ULPI Clock	For external ULPI PHY

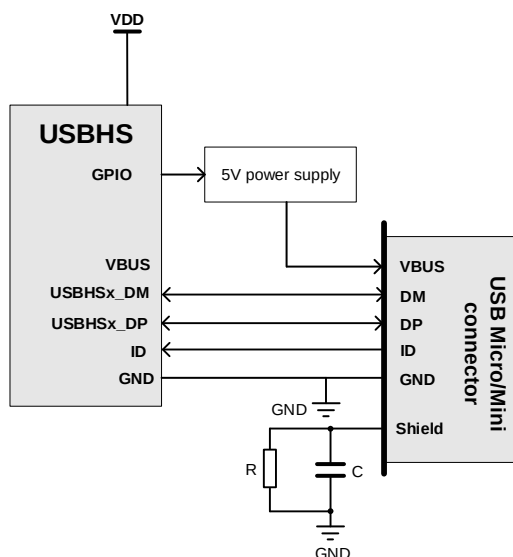
USBHS includes an internal embedded PHY that supports high, full, and low speeds in host mode, high and full speeds in device mode, and OTG protocols with HNP and SRP. The pull-up or pull-down resistors are already integrated into the internal full speed PHY, and the USBHS can automatically control based on the current mode (host, device, or OTG mode) and connection status. Connection diagram using internal PHY is shown in [Figure 2-33. Connection diagram in host or device mode](#). The connection diagram of OTG mode is shown in [Figure 2-34. Connection diagram of using internal embedded PHY in OTG mode](#).

Figure 2-33. Connection diagram in host or device mode



Recommended: $R=1\text{ M}\Omega$, $C=4700\text{ pF}$.

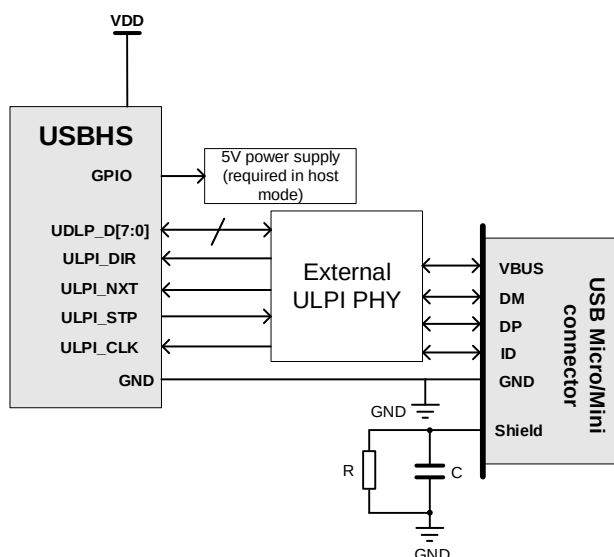
Figure 2-34. Connection diagram of using internal embedded PHY in OTG mode



Recommended: $R=1\text{ M}\Omega$, $C=4700\text{ pF}$.

USBHS provides an ULPI interface for external PHYs. If a USBHS module is required to complete high-speed USB applications, then an external high-speed ULPI PHY is required. Combined with external ULPI PHY, USBHS supports high-speed hosts and devices, as well as all modes described in the previous article for internal embedded full speed PHY. The connection diagram of using external ULPI PHY is shown in [Figure 2-35. Connection diagram of using external ULPI PHY](#).

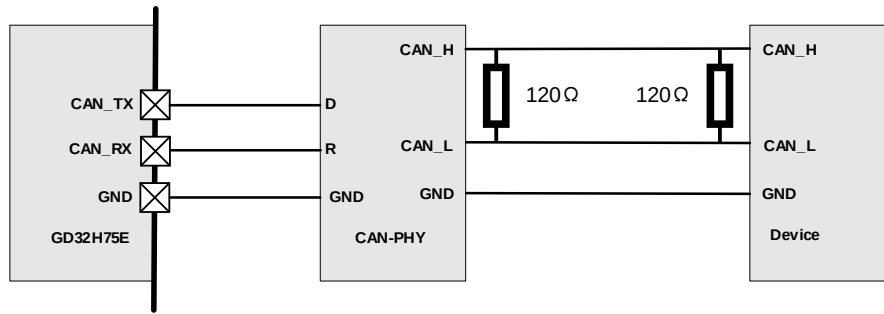
Figure 2-35. Connection diagram of using external ULPI PHY



2.5.9. CAN Circuit.

Refer to the [Figure 2-36. CAN Reference Circuit](#).

Figure 2-36. CAN Reference Circuit



The two 120 Ω termination resistors in the figure can be adjusted or omitted based on actual requirements.

In CAN communication, impedance matching serves three purposes:

1. Enhance anti-interference capability;
2. Prevent signal reflection and improve signal quality;
3. Ensure rapid rise/fall edges on the bus.

2.6. Thermal management and low-power mode

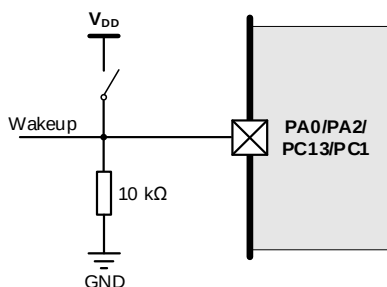
In the GD32H75E series, power consumption is high when multiple peripherals are used. Users should ensure $T_J < 125^{\circ}\text{C}$ under all operating conditions. For external circuits, refer to the [AN060 GD32MCU Thermal Characteristics Management Manual](#) and the [AN166 GD32H7xx Series Thermal Design Guidelines](#), and select an appropriate cooling method. For internal control, there are three methods to reduce chip power consumption: slowing down the system clock (HCLK, PCLK1, and PCLK2), disabling the clock of unused peripherals, or configuring the LDO output voltage using the LDOVS[2:0] bits in the PMU_CTL3 register. Note that LDOVS[2:0] can only be configured when the PLL is disabled.

Additionally, the GD32H75E series supports three MCU low-power modes and multiple ESC low-power modes to achieve further power reduction.

2.6.1. MCU low-power modes

MCU low-power modes include Sleep mode, Deep Sleep mode, and Standby mode. Among them, Standby mode has the lowest power consumption, but its wake-up time is the longest. Wake-up from Standby mode can be achieved via a rising edge on WKUP pins, with a total of 4 WKUP pins. In this case, there is no need to configure the corresponding GPIO; only the WUPENx bits in the PMU_CS register need to be configured. The recommended external wake-up pin circuit design for Standby mode is shown in [Figure 2-37. Recommended Standby External Wake-Up Pin Circuit Design](#).

Figure 2-37. Recommended Standby External Wake-Up Pin Circuit Design



Note: In this mode, attention should be paid to the circuit design. If there is a series resistance between the WKUP pin and V_{DD} , additional power consumption may be added.

2.6.2. ESC low-power modes

ESC low-power modes include four device-level energy-saving modes and three module-level energy-saving modes. The device-level energy-saving modes are MOD0, MOD1, MOD2, and MOD3, while the module-level energy-saving modes include EtherCAT clock management, PHY power management, and LED pin power management. These modes reduce power consumption and allow applications to achieve an optimal balance between conflicting demands of runtime, speed, and power consumption. The PMU also supports wake-up event detection and Power Management Event (PME) notification.

The PME module is responsible for handling the latch function of the EDWOLASTAT and EDWOLBSTAT bits in the PMU_CTL register. Refer to [Figure 2-38. PME interrupt pending](#) to understand the logic of PME interrupt control. If EDWOLAEN or EDWOLBEN is set, when energy detect / WoL event happened on port A or B PHY the PME_INT bit in interrupt status register will be set. When PMWUPCFG is set, PME events can automatically wake up the system in some device-level power saving modes.

Figure 2-38. PME interrupt pending

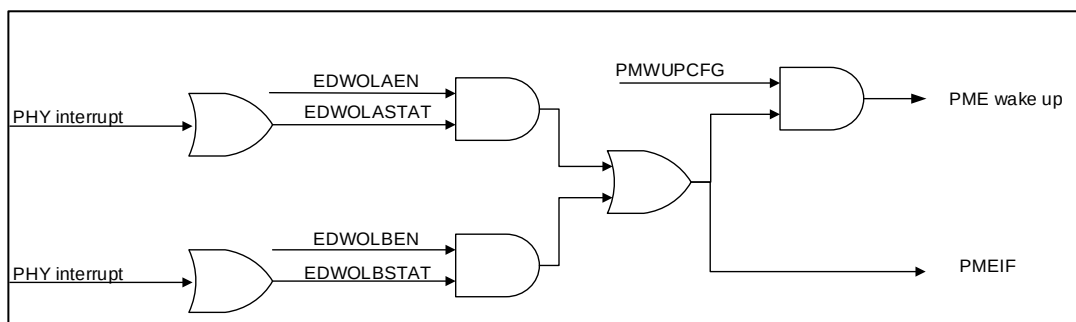


Table 2-26. Power saving mode summary

Mode	PLL	System clocks	Network clocks	XTAL
MOD0	ON	ON	usable	ON
MOD1	ON	OFF	usable	ON
MOD2	OFF	OFF	usable	ON
MOD3	OFF	OFF	OFF	OFF

2.7. Download and debug circuit

The GD32H75E series supports both JTAG debugging interface and SWD debugging interface. By default it supports SWD interface and can be modified to JTAG mode through effuse. It also supports secure JTAG, but cannot be rolled back to SWD mode, refer to [AN111 GD32H7xx Software Development Guide](#) for details. The JTAG interface standard is a 20 pin interface, with 5 signal interfaces, and the SWD interface standard is a 5 pin interface, with 2 signal interfaces.

Note: After reset, the debug related ports are in input pull-up / pull-down mode, where:

PA15: JTDI in pull-up mode.

PA14: JTCK / SWCLK in pull-down mode

PA13: JTMS / SWDIO in pull-up mode

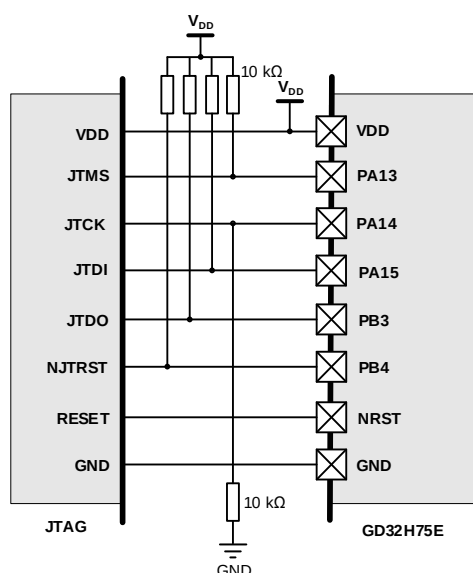
PB4: NJTRST in pull-up mode

PB3: JTDO in floating mode.

Table 2-27. JTAG download debug interface assignment

Alternate function	GPIO port
JTMS	PA13
JTCK	PA14
JTDI	PA15
JTDO	PB3
NJTRST	PB4

Figure 2-39. Recommended JTAG connection reference design



Note: After reset, the debug-related ports are in input pull-up/pull-down mode, where:

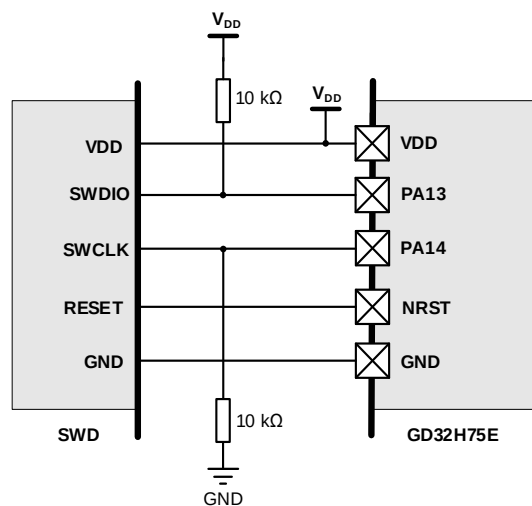
PA13: SWDIO is in pull-up mode;

PA14: SWCLK is in pull-down mode.

Table 2-28. SWD download debug interface assignment

Alternate function	GPIO port
SWDIO	PA13
SWCLK	PA14

Figure 2-40. Recommended SWD connection reference design



There are several ways to improve the reliability of SWD download and debugging communication and enhance the anti-interference ability of download and debugging.

1. Shorten the length of the two SWD signal lines, preferably within 15 cm;
2. Weave the two SWD wires and the GND wire into a twist and twist them together;
3. Connect separately tens of pF small capacitors in parallel between the two signal lines of the SWD and the ground;
4. Any IO of the two signal lines of SWD is connected in series with a $100\ \Omega \sim 1\ \text{k}\Omega$ resistor.

Figure 2-41. GD32H75E Recommended Reference Schematic Design

Figure 2-41. GD32H75E Recommended Reference Schematic Design



3. PCB Layout Design

To enhance the functional stability and EMC performance of the MCU, it is essential to consider not only the performance of peripheral components but also the PCB Layout design. Additionally, if conditions permit, adopting a PCB design solution with an independent GND layer and power layer is recommended, as it can provide better EMC performance. If independent GND and power layers are not feasible, it is still necessary to ensure good power supply and grounding design. For example, maintain the integrity of the GND plane beneath the MCU, ensure proper grounding for EPAD packages, and connect the EPAD to the ground in the PCB Layout.

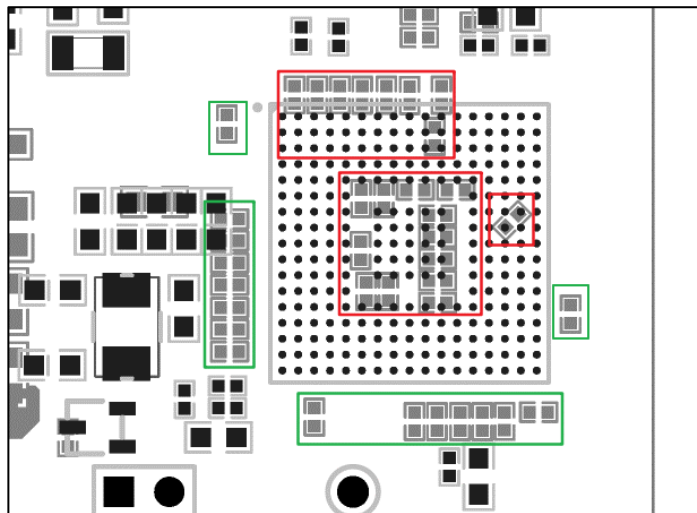
In applications with high power or strong interference sources, consider placing the MCU away from these interference sources.

3.1. Power Supply Decoupling Capacitors

The GD32H75E series power supply pins include V_{DD} , V_{DDA} , V_{REFP} , etc. Use 100nF ceramic MLCCs as decoupling capacitors, and ensure they are placed as close to the power pins as possible. The power trace should pass through the capacitors before reaching the MCU power pins. It is recommended to place vias near the capacitor pads during Layout.

[Figure 3-1. Recommended power pin decoupling layout design](#) as a reference design, where the decoupling capacitors marked in the red box are placed below the MCU, and those marked in the green box are placed near the MCU.

Figure 3-1. Recommended power pin decoupling layout design



The layout of decoupling capacitors must follow these requirements:

1. Place the capacitors near the power pins based on the decoupling radius, ideally with the capacitor pads less than 5mm from the power pins;
2. The connections of decoupling capacitors to the power plane and ground plane should be as short as possible, avoiding long traces from the pads before connecting to vias;

- Each power pin should have a decoupling capacitor. When space is limited, two power pins can share one decoupling capacitor.

3.2. 0.9V Power Domain Circuit

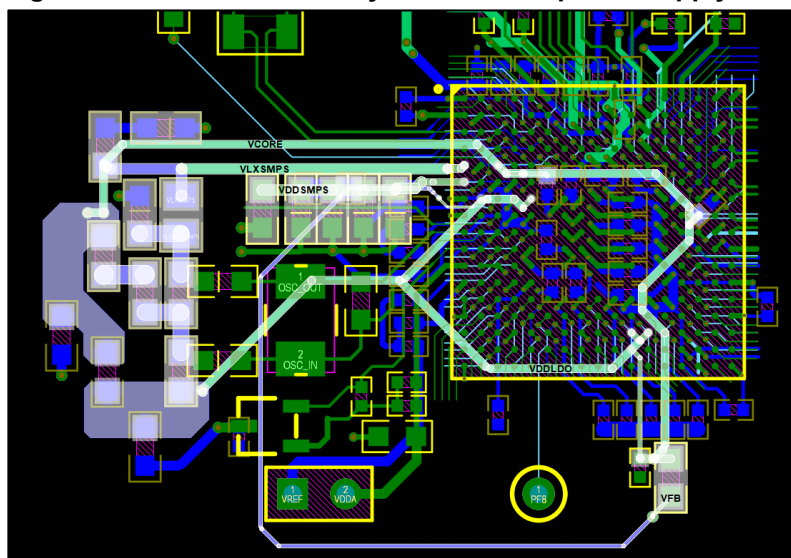
The current 0.9V power domain is recommended to use SMPS supply mode or bypass mode. To enhance the MCU's functional stability and EMC performance, the power circuit needs to consider not only the performance of peripheral components but also the PCB layout.

The PCB layout for SMPS supply mode must follow these requirements:

- The V_{LXSMPS} of the SMPS is a 2MHz voltage switching signal, with an amplitude that may exceed V_{DD} or drop below V_{SS} . Based on system-level EMC protection design, it must be shielded as much as possible from other signals.
- All traces and peripheral components of this module should be placed on the same layer as much as possible, with adjacent layers being solid ground planes whenever possible. Clock lines, V_{FBSMPS} , and other analog lines should maintain a distance and separate layer from this module, with proper ground shielding.
- To increase overcurrent capability, the line widths of V_{DDSMPS} and V_{LXSMPS} should be as wide as possible, at least 20 to 30 mil or more.
- The placement and routing of peripheral components should follow the shortest di/dt loop principle for the output current.
- To ensure output stability, the V_{FBSMPS} feedback line of the SMPS should return from the load end.
- Whether the LDO is enabled or not, all V_{DDLDO} pins and V_{CORE} pins of the chip must be connected together respectively.

The recommended layout for the SMPS power supply mode in BGA240 package is shown in [Figure 3-2. Recommended layout for SMPS power supply mode in BGA240 package](#).

Figure 3-2. Recommended layout for SMPS power supply mode in BGA240 package

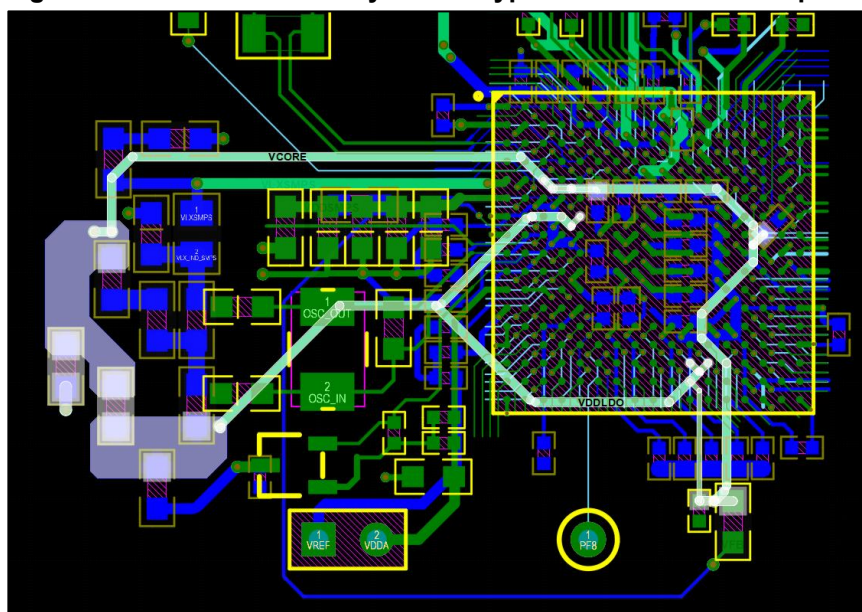


The PCB layout for bypass mode must follow the requirements below:

1. When using an external power supply to power V_{CORE} , be mindful of line losses caused by line resistance under high current output conditions to prevent the terminal voltage from falling below the specified requirement.
2. Thermal management measures must be taken to prevent the external power supply's heat generation from affecting the MCU's thermal dissipation and its own performance.
3. Ensure that all V_{DDLDO} pins and V_{CORE} pins of the chip are connected together respectively and linked to the external power supply output.

The recommended layout for bypass mode in BGA240 package is shown in [Figure 3-3. Recommended layout for Bypass mode in BGA240 package.](#)

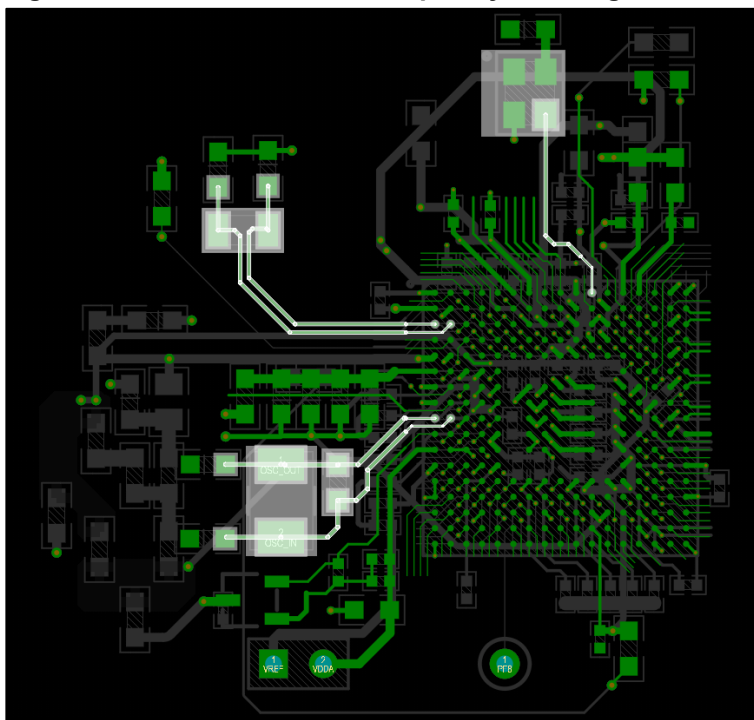
Figure 3-3. Recommended layout for Bypass mode in BGA240 package



3.3. Clock Circuit

The GD32H75E series clocks include HXTAL and LXTAL. The clock circuit (including crystal or oscillator and capacitors, etc.) must be placed close to the MCU clock pins, and the clock traces should be surrounded by GND as much as possible.

Figure 3-4. Recommended clock pin layout design

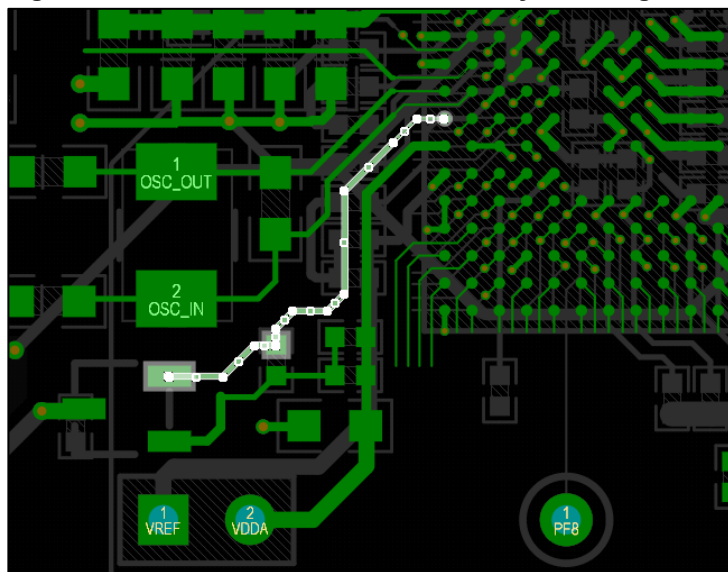
**Note:**

1. Place the crystal as close to the MCU clock pins as possible, and the matching capacitors as close to the crystal as possible;
2. Keep the entire circuit on the same layer as the MCU, and avoid via transitions for traces as much as possible;
3. The clock circuit PCB area should be kept as a no-copper zone, avoiding any traces unrelated to the clock;
4. High-power, high-interference risk devices, and high-speed traces should be kept away from the clock crystal circuit as much as possible;
5. Clock lines should be ground-shielded to achieve a shielding effect.

3.4. Reset Circuit

NRST trace PCB Layout reference is as follows:

Figure 3-5. Recommended NRST trace layout design

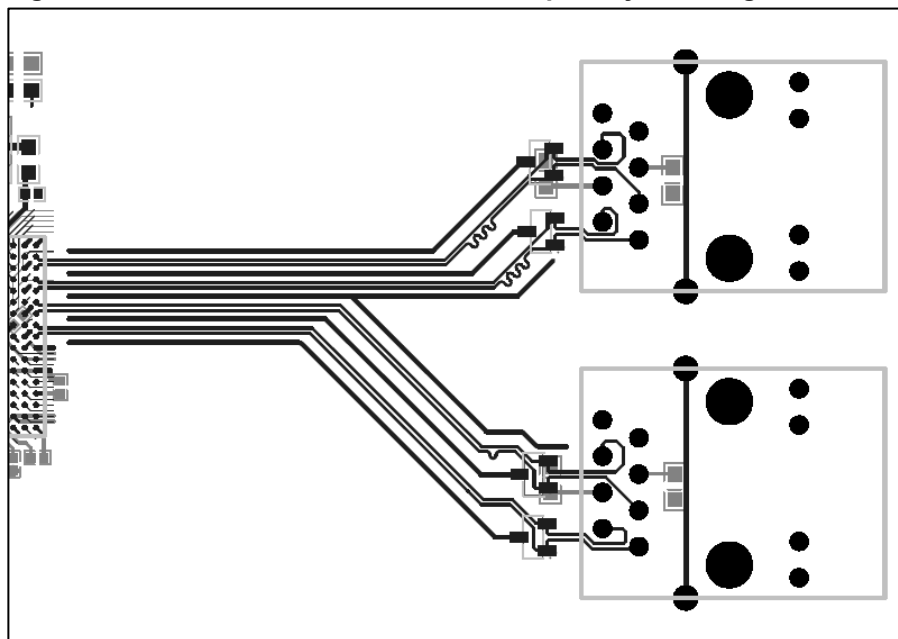


Note: Place reset circuit resistors and capacitors as close as possible to the MCU NRST pin, and keep NRST traces away from high-interference risk devices and high-speed traces. If conditions permit, it is recommended to ground-shield the NRST traces for better shielding effect.

3.5. Ethernet Interface Circuit

GD32H75E series MDI differential pair layout between PHY and network transformer reference is as follows:

Figure 3-6. Recommended MDI differential pair layout design



Note:

1. The characteristic impedance of the MDI differential pair must be strictly controlled to

- 100Ω ± 10%;
2. Avoid signal traces crossing power split areas and maintain a complete signal reference plane;
 3. MDI differential pairs should be routed on the top layer as much as possible and ground-shielded. Length matching within pairs should be controlled within 50 mils, and inter-pair length matching (e.g., between TX pair and RX pair) should be limited to 600 mils. (For microstrip serpentine traces, the suggested spacing is 7H; for stripline serpentine traces, the suggested spacing is 5H, where H is the distance from the signal trace to the reference plane. If vias are present, typically each via adds 50-100 mils trace length depending on the via length. Traces should be as short and straight as possible, with a total length recommended to be less than 2000 mils);
 4. If the signal integrity is poor, consider adding termination resistors on the PHY side.

3.6. USB Circuit

For the GD32H75E series MCU USB FS module, there are two differential signal lines DM and DP. For the USB HS module, after the external high-speed PHY is connected, the PHY chip will also lead out two differential signal lines DM and DP. It is recommended that the PCB wiring requires a characteristic impedance of 90Ω. The differential wiring should be strictly in accordance with the equal length isometric gauge, and the wiring should be as short as possible. If the two differential lines are not equal in length, a serpentine wire can be used at the terminal to compensate for the short line. It is recommended to connect DM and DP directly without matching resistors in series.

DM and DP differential wiring reference is as follows:

1. Reasonably arrange the layout to shorten the differential routing distance.
2. Give priority to drawing differential lines, try not to exceed two pairs of vias on a pair of differential lines, and place them symmetrically.
3. Symmetrical parallel wiring ensures close coupling between two wires, avoiding 90°, arc or 45° wiring methods.
4. Devices such as resistors, capacitors, EMC, or test points connected to the differential wiring should also adhere to the principle of symmetry.

For the USB HS module, the data and signal control lines between the MCU and the external HS PHY should also be kept as short as possible. It is necessary to use serpentine wires for equal length processing, and the following precautions should be taken:

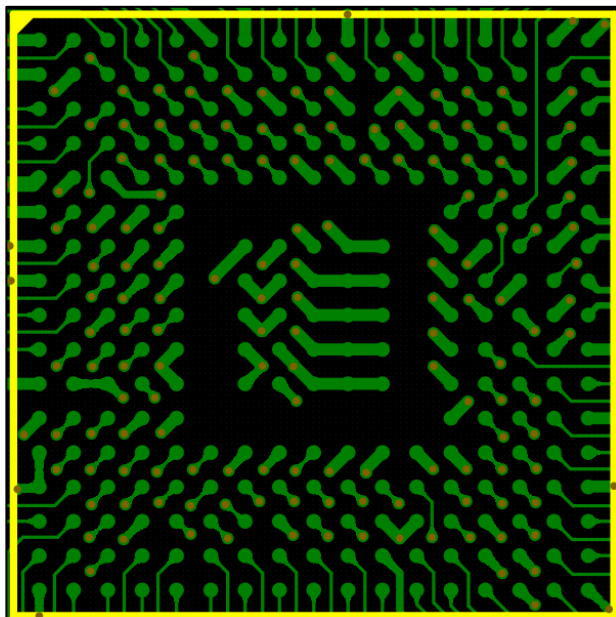
1. The layout should be arranged reasonably, and the USB HS-PHY chip should be as compact as possible between the MCU.
2. When wiring, take the longest signal wire as the target length and compensate for other signal wires through a serpentine routing.

3.7. Fan-out of BGA package

The GD32H75E series MCU is packaged in BGA240 (0.8mm Pitch). We recommend the following routing rules and fan-out methods.

It is recommended to use 4 mil line width and spacing with 8 / 12 mil vias for fan-out. After fan-out, refer to [Figure 3-7. Fan-out method for BGA240 package](#).

Figure 3-7. Fan-out method for BGA240 package



4. Steel mesh and soldering

4.1. Steel mesh

When SMT is applied, the thickness and opening size of the leak of the steel mesh depend on the type of solder paste and the distribution, density, and spacing of pad openings. Overlarge opening of the leak of the steel mesh often leads to distribution of too much solder paste, which is prone to "bridging" during soldering. Too small opening of the leak will lead to application of little solder paste and thus cause insufficient strength of the solder joint or "cold solder".

4.1.1. Recommended thickness of steel mesh

The thickness and opening size of the steel mesh generally follow these rules: The width-to-thickness ratio shall be higher than 1.5 (that is, the opening width of the steel mesh shall be 1.5 times the thickness of the steel mesh or above), and the area ratio shall be higher than 0.66 (that is, the opening area of the steel mesh shall be 0.66 times the lateral area of the opening column or above), which can ensure to the greatest extent that there is proper amount of solder paste on the pad when brushing.

The recommended thickness of the steel mesh of GD32H75E products are listed in [Table 4-1. Recommended thickness of steel mesh of GD32H75E chip](#).

Table 4-1. Recommended thickness of steel mesh of GD32H75E chip

Chip package	Thickness (mm)
BGA240 (14x14, 0.8 pitch)	0.15

In practice, the above table can only be for reference for the thickness of the steel mesh of GD32 H75E products. The thickness of the steel mesh of PCB shall be evaluated in combination with the density of PCB devices, pitch value of other chip pins, pad dimensions, and process requirements.

4.1.2. Cleaning and use of steel mesh

Cleaning

- The steel mesh shall be cleaned before use to remove contaminants contacted during transportation or long-term storage.
- The steel mesh shall be cleaned in time after use and packed in a special storage position.
- The steel mesh to be cleaned shall not be placed randomly to prevent it from being damaged or bringing other contaminants.
- The steel mesh shall be placed vertically in a special storage position and isolated from each other.

Use

- Solder paste for soldering shall be applied after being heated and stirred evenly to prevent the steel mesh from being blocked.
- The steel mesh shall be gently moved to prevent bumping against hard objects or sharp devices.
- When brushing, the steel mesh shall be kept close to PCB, and attention shall be paid to the adjustment of the pressure on the scraper until there is no residual solder paste on the intact steel mesh.
- The steel mesh shall be lifted for demolding at a proper speed about 3 s after brushing.
- When reaching the service life limit, generally 100,000 times, the steel mesh shall be scrapped.

4.2. Soldering

In the actual manufacturing process, the reflow oven temperature profile setup needs to consider many factors. Besides the characteristics of the components themselves, factors such as the PCB material, component distribution density, and solder paste composition also need to be taken into account. Below is a reference reflow oven temperature profile for the GD32H75E series MCU.

Figure 4-1. Recommended Reflow Soldering Temperature Curve

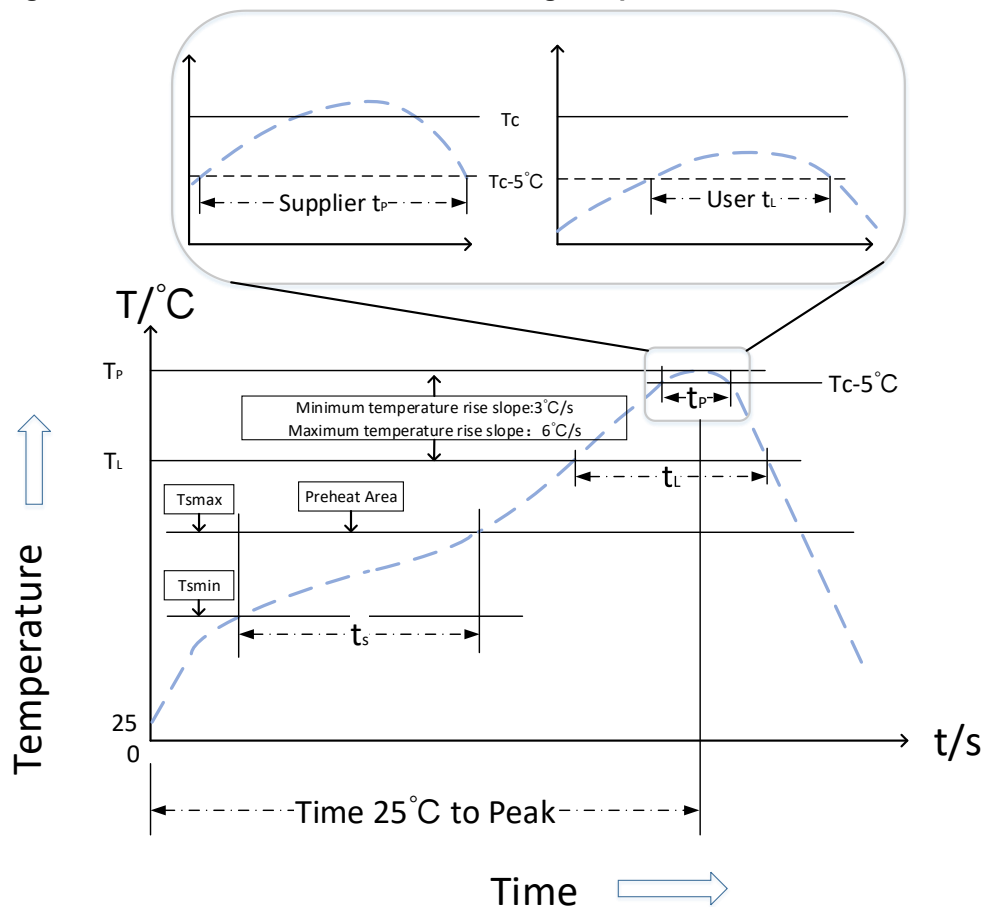


Table 4-2. Reflow soldering parameters

Characteristic parameter	Lead-free assembly
Average temperature rise slope from 217 °C to peak temperature	Maximum 3 °C / s
Preheating duration (150 °C to 200 °C)	60 s to 120 s
Duration for keeping the temperature above 217 °C	60 s to 150 s
Peak temperature	260 + 5 / - 0 °C
Duration for true peak temperature of below 5 °C	30 s
Temperature drop slope	Maximum 6 °C / s
Duration for temperature rising from 25 °C to peak temperature	Maximum 8 min

5. Package Description

The GD32H75E series has one package type, BGA240.

Table 5-1. Package Description

Ordering code	Package
GD32H75EYMJ7	BGA240 (14x14, 0.8 pitch)

(Original dimensions are in millimeters)

6. Revision History

Table 6-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Jan.24, 2026

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