GigaDevice Semiconductor Inc.

GD32H73x_75x 14-bit ADC User Guide

Application Note

AN180

Revision 1.3

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1 Introduction

This document is specifically designed for engineers developing with the GD32H73x_75x, focusing on the usage methods and precautions regarding the GD32H73x_75x 14-bit ADC. The accuracy of the ADC is influenced not only by its design, packaging, and manufacturing factors but also by various external factors. To achieve the specified accuracy in practical applications, sufficient attention must be given to both software configuration and the design of peripheral circuits.

The applicable products are as shown in ***Table 1-1. Applicable product***.

Table 1-1. Applicable product

Product series	Model
GD32H73x	GD32H737 series
GD32H75x	GD32H757, GD32H759 series

Note: This application note is for reference only. In case of any conflict with the user manual or datasheet, the user manual or datasheet shall prevail.

2 Introduction to the High-Precision ADC of the GD32H73x_75x

The GD32H73x_75x integrates 14/12-bit successive approximation analog-to-digital converter modules (ADC). Among them, ADC0 and ADC1 are 14-bit ADC that can be configured to 14-bit, 12-bit, 10-bit, or 8-bit resolution; ADC2 is a 12-bit ADC that can be configured to 12-bit, 10-bit, 8-bit, or 6-bit resolution.

ADC0 has 20 external channels, 1 internal channel (DAC0_OUT0 channel), ADC1 has 18 external channels, 3 internal channels (the battery voltage, V_{REFINT} inputs channel and DAC0_OUT1 channel), ADC2 has 17 external channels, 4 internal channels (the battery voltage, V_{REFINT} inputs channel, tempeture sensor and high-precision tempeture sensor). ADC sampling channels support multiple operating modes. After sampling and conversion, the conversion results can be stored in the corresponding data registers either aligned to the least significant bit (LSB) or the most significant bit (MSB). (ADC0/1 utilize 32-bit data registers, while ADC2 uses a 16-bit data register).

This document focuses on the implementation methods and usage precautions of the GD32H73x_75x 14-bit ADC (ADC0 / 1). For more details about GD32 ADC, please refer to the reference manual ***AN059 Improving GD32 ADC Sampling Accuracy***.

3 Software Design Considerations

3.1 Basic Configuration

The basic configuration of the GD32H73x_75x 14-bit ADC includes clock, sampling time, sampling rate, resolution, operating mode, and trigger source, among others.

- Clock: Synchronous clock AHB, asynchronous clocks CK_PLL1P, CK_PLL2R, or CK_PER.
- Sampling Time: The sampling time can be flexibly configured, ranging from 3.5 to 810.5 clock cycles.
- Resolution: Configurable to 14-bit, 12-bit, 10-bit, or 8-bit resolution.
- Operating Mode:
  1) Converts a single channel or scans a sequence of channels.
  2) Single operation mode converts selected inputs once per trigger.
  3) Continuous operation mode converts selected inputs continuously.
  4) Discontinuous operation mode.
  5) SYNC mode.
- Trigger Source:
  1) By software.
  2) By TRIGSEL.

After completing the basic configuration, the customer can further configure features such as watchdog, single-ended or differential mode, HPDF processing, hardware oversampling, DMA requests, and more as needed.

3.2 Internal Channel Configuration

The ADC has four types of internal channels: internal temperature sensor channel, high-precision temperature sensor channel, internal reference voltage input channel, and external battery monitoring channel.

When the TSVEN1 bit of ADC_CTL1 register is set, the temperature sensor channel (ADC2_CH18) is enabled. The output voltage of the internal temperature sensor exhibits a linear variation with temperature. Due to variations in the manufacturing process, deviations in the temperature response curve may differ between chips (up to ±45°C). The internal temperature sensor is more suitable for monitoring temperature changes rather than measuring absolute temperatures. When it is used to detect accurate temperature, an external temperature sensor part should be used to calibrate the offset error.

When the TSVEN2 bit of ADC_CTL1 register is set, the high-precison temperature sensor channel (ADC2_CH20) is enabled. The high-precision temperature sensor requires at least three ADC sampling cycles. The data from the first three conversions should be discarded.

Additionally, when the high-precision temperature sensor is configured, the ADC clock frequency must not exceed 5 MHz.

When the INREFEN bit of ADC_CTL1 register is set, the VREFINT channel is enabled. The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators.

When the VBATEN bit in ADC_CTL1 register is set, V_{BAT} channel is enabled and a bridge divider by 4 integrated on the V_{BAT} pin is also enabled automatically with it. As V_{BAT} may be higher than V_{DDA}, this bridge is used to ensure the ADC correct operation. The converted digital value is V_{BAT} / 4. In order to prevent unnecessary battery energy consumption, it is recommended that the bridge will be enabled only when it is required.

3.3 ADC Calibration

The GD32H73x_75x series 14-bit ADC features a pre-calibration function. When the ADC operating conditions change (e.g., VDDA, VREFP, temperature, etc.), it is recommended to perform the calibration operation again.

3.3.1 Introduction to ADC Calibration

The GD32H73x_75x 14-bit ADC's built-in calibration feature offers two calibration modes: offset and mismatch calibration and offset calibration. Currently, users are recommended to use the offset standard mode (CALMOD = 1).

During calibration, the ADC calculates a calibration coefficient, which is applied internally to the ADC and remains effective until the ADC is powered down next time. During the calibration process, the application cannot use the ADC and must wait until the calibration is completed. Calibration should be performed before A/D conversion.

3.3.2 ADC Calibration Software Configuration

The user can initialize the calibration process by setting CLB = 1 through software. During calibration, the CLB bit remains set to 1 until the calibration is completed, at which point the hardware clears the bit to 0.

The offset and mismatch and offset calibration modes can be modified by setting the CALMOD bit in the ADC_CTL1 register.

Internal analog calibration can be reset by setting the RSTCLB bit in the ADC_CTL1 register.

Calibration software procedure:

1. Ensure that ADCON = 1.
2. Delay 14 CK_ADC to wait for ADC stability.
3. Set RSTCLB (optional).

4. Set CLB = 1.
5. Wait until CLB=0.

3.4 Configuration Methods for Increasing Sampling Speed

Under suitable conditions, sampling speed improvement is typically achieved by increasing the sampling clock rate and reducing the sampling period. For application scenarios with low precision requirements, reducing the resolution can be used to shorten the conversion time, as shown in ***Table 3-1. tCONV timings depending on resolution for ADC0 and ADC1***. Lower resolution can reduce the conversion time t_{ADC} required for the successive approximation steps, thereby increasing the sampling rate, as shown in ***Table 3-2. The relationship between the GD32H73x_75x 14-bit ADC resolution and maximum sampling rate***.

Table 3-1. t_{CONV} timings depending on resolution for ADC0 and ADC1

DRES[1:0] bits	t_{CONV} (ADC clock cycles)	t_{CONV}(ns) at f_{ADC} = 72MHz	t_{SMPL}(min) (ADC clock cycles)	t_{ADC} (ADC clock cycles)	t_{ADC}(ns) at f_{ADC} = 72MHz
14	14.5	201.39 ns	3.5	18	250 ns
12	12.5	173.61 ns	3.5	16	222.22 ns
10	10.5	145.83 ns	3.5	14	194.44 ns
8	8.5	118.06 ns	3.5	12	166.67 ns

Table 3-2. The relationship between the GD32H73x_75x 14-bit ADC resolution and maximum sampling rate

Resolution (bit)	Maximum Sampling Rate (MSPs)
14	4
12	4.5
10	5.14
8	6

3.5 Configuration Methods for Improving Sampling Accuracy

To improve ADC sampling accuracy, hardware oversampling is typically used. The hardware oversampling unit performs data preprocessing to reduce CPU workload.

Oversampling rate $OSR = \frac{f_s}{2 \times f_{in\_max}}$, which is the ratio of the sampling rate to twice the maximum input signal bandwidth. For every 4x increase in the OSR, the signal-to-noise ratio (SNR) improves by 6dB, corresponding to a 1-bit increase in effective number of bits (ENOB).

It can handle multiple conversions and average them into a single data with increased data width, In the GD32H73x_75x 14-bit ADC, the maximum effective number of bits can reach up to 32 bits. The on-chip hardware oversampling circuit is enabled by OVSEN bit in the

ADC_OVSAMPCTL register. It provides a result with the following form, where N and M can be adjusted, and Dout(n) is the n-th output digital signal of the ADC:

$$\text{Result} = \frac{1}{M} * \sum_{n=0}^{N-1} D_{out}(n) \qquad (3\text{-}1)$$

For 14bit-ADC, the on-chip hardware oversampling circuit performs the following functions: summing and bit right shifting. The oversampling ratio N is defined by the OVSR[9:0] bits in the ADC_OVSAMPCTL register. It can range from 2x to1024x. The division coefficient M means bit right shifting up to 11-bit. It is configured through the OVSS[3:0] bits in the ADC_OVSAMPCTL register.

For 14bit-ADC, summation units can produce up to 24 bits (1024 x 14bit), which is first shifted right. Then store the data into register.

Figure 3-1. 14bit ADC oversampling with 10bits right shift

	23	19	15	11	7	3 0
Raw 24-bit data	d23 …	…	…	…	…	… d0

	23	19	15	11	7	3 0
Shifting(10 bit)	0	0	… d13	…	…	… d0

Figure 3-2. Numerical example for 14bit ADC oversampling with 10bits right shift

	23	19	15	11	7	3 0
Raw 24-bit data	3	2	A	C	D	6

	23	19	15	11	7	3 0
Shifting(10 bit)	0	0	0	C	A	B

When compared to standard conversion mode, the conversion timings of oversampling mode do not change, and the sampling time is maintained the same as that of standard conversion mode during the whole oversampling sequence. New data is supplied every N conversions, and the equivalent delay is equal to:

$$N*t_{ADC} = N*(t_{SMPL}+t_{CONV}) \qquad (3\text{-}2)$$

4 Precautions for Using ADC

The GD32H73x_75x ADC supports configurations such as resolution, sampling cycles, on-chip hardware oversampling, and supports both single-ended and differential input modes. Different ADC configurations, chip packages, etc., can affect the dynamic and static characteristics, sampling accuracy, and sampling rate of the ADC.

4.1 Improve 14-bit ADC dynamic and static characteristics using differential input.

The GD32H73x_75x 14-bit ADC supports both single-ended and differential input modes. Single-ended input mode uses only one pin, making external circuits and wiring relatively simple. In contrast, differential input mode offers better dynamic and static characteristics compared to single-ended mode, including lower noise levels and distortion, enabling high-precision measurements. However, differential input requires two pins. Therefore, if sufficient pins are available, users are recommended to use the differential input mode to achieve higher accuracy.

The pin allocation for differential channels is shown in ***Table 4-1. ADC differential channel pin matching***.

Table 4-1. ADC differential channel pin matching

Differential channel n number	ADC0		ADC1		ADC2	
	V_{INn}	V_{INm}	V_{INn}	V_{INm}	V_{INn}	V_{INm}
0	PA0_C	PA1_C	PA0_C	PA1_C	PC2_C	PC3_C
1	PA1_C	PA0_C	PA1_C	PA0_C	PC3_C	PC2_C
2	PF11	PF12	PF13	PF14	PF9	PF10
3	PA6	PA7	PA6	PA7	PF7	PF8
4	PC4	PC5	PC4	PC5	PF5	PF6
5	PB1	PB0	PB1	PB0	PF3	PF4
6	PF12	PF11	PF14	PF13	PF10	PF9
7	PA7	PA6	PA7	PA6	PF8	PF7
8	PC5	PC4	PC5	PC4	PF6	PF5
9	PB0	PB1	PB0	PB1	PF4	PF3
10	PC0	PC1	PC0	PC1	PC0	PC1
11	PC1	PC2	PC1	PC2	PC1	PC2
12	PC2	PC3	PC2	PC3	PC2	PC1
13	PC3	PC2	PC3	PC2	PH2	PH3
14	PA2	PA3	PA2	PA3	PH3	PH4
15	PA3	PA2	PA3	PA2	PH4	PH5
16	PA0	PA1	null	null	PH5	PH4

17	PA1	PA0	null	null	null	null
18	PA4	PA5	PA4	PA5	null	null
19	PA5	PA4	PA5	PA4	null	null
20	null	null	null	null	null	null
21	null	null	null	null	null	null

The dynamic and static characteristic data of the GD32H73x_75x 14-bit ADC in single-ended and differential modes are shown in ***Table 4-2. Dynamic and Static Characteristics of GD32H73x_75x 14-bit ADC in Single-ended Input Mode (1)*** and ***Table 4-3. Dynamic and Static Characteristics of GD32H73x_75x 14-bit ADC in Differential Input Mode (1)***.

Table 4-2. Dynamic and Static Characteristics of GD32H73x_75x 14-bit ADC in Single-ended Input Mode (1)

Symbol	Parameter	Test conditions	Typ	Unit
EO	Offset error	Single ended	±5.7	
DNL	Differential linearity error	Single ended	+1.3/-1.0	LSB
INL	Integral linearity error	Single ended	±1.9	
ENOB	Effective number of bits	Single ended	12.7	Bits
SNDR	Signal-to-noise and distortion ratio	Single ended	78.3	dB

(1) Test conditions: TA=25°C, BGA176 package, input pin is PC0; MODE1 power supply (LDO power supply mode), $V_{DD}=V_{DDA}=V_{REFP}=3.3$ V, external reference source; f_{ADC}=36MHz, SMP=3.5 CLK, uncalibrated.

Table 4-3. Dynamic and Static Characteristics of GD32H73x_75x 14-bit ADC in Differential Input Mode (1)

Symbol	Parameter	Test conditions	Typ	Unit
EO	Offset error	Differential	±0.1	
DNL	Differential linearity error	Differential	±1.0	LSB
INL	Integral linearity error	Differential	±1.6	
ENOB	Effective number of bits	Differential	13.4	Bits
SNDR	Signal-to-noise and distortion ratio	Differential	82.6	dB

(1) Test conditions: TA=25°C, BGA176 package, input pins are PC0 & PC1; MODE1 power supply (LDO power supply mode), $V_{DD}=V_{DDA}=V_{REFP}=3.3$ V, external reference source; f_{ADC}=36MHz, SMP=3.5 CLK, uncalibrated.

When comparing ADC static parameters in units of LSB, the relationship between LSB size and resolution must be considered. With a 3.3V reference voltage, "1 LSB" for a 14-bit resolution ADC equals $1\ \text{LSB} = \frac{3.3}{2^{14}}\ \text{V} \approx 0.2\ \text{mV}$, while "1 LSB" for a 12-bit resolution ADC equals $1\ \text{LSB} = \frac{3.3}{2^{12}}\ \text{V} \approx 0.8\ \text{mV}$, Therefore, 1 LSB (12-bit resolution) = 4 LSB (14-bit resolution).

4.2 Selection of Power Supply Mode for ADC Reference Source

The GD32H73x_75x integrates an internal reference circuit to provide reference voltage for ADC / DAC or to supply external circuits connected to the VREFP pin (external power supply: when using a 14-bit ADC, if V_{DDA} ≥ 2.4 V, then 2.4 V ≤ V_{REFP} ≤ V_{DDA}; if V_{DDA} < 2.4 V, then 1.8 V ≤ V_{REFP} ≤ V_{DDA}). The internal reference circuit can be configured to the following reference voltage levels: 1.5V, 1.8V, 2.048V, 2.5V.

Using an external high-precision reference source can further enhance ADC performance. The ADC performance with different reference sources is shown in *Table 4-4. Dynamic and Static Characteristics of GD32H73x_75x 14-bit ADC When Using Internal Reference Source (1)*, and *Table 4-5. Dynamic and Static Characteristics of GD32H73x_75x 14-bit ADC When Using External High-Precision Reference Source (1)*.

Table 4-4. Dynamic and Static Characteristics of GD32H73x_75x 14-bit ADC When Using Internal Reference Source (1)

Symbol	Parameter	Test conditions	Typ	Unit
EO	Offset error	Single ended	±5.2	LSB
	Differential linearity error	Differential	±1.3	
DNL	Integral linearity error	Single ended	+2.9/-1.0	
	Effective number of bits	Differential	+1.8/-1.0	
INL	Signal-to-noise and distortion ratio	Single ended	±4.0	
	Offset error	Differential	±1.8	
ENOB	Differential linearity error	Single ended	11.4	Bits
	Integral linearity error	Differential	12.6	
SNDR	Effective number of bits	Single ended	70.7	dB
		Differential	77.6	

(1) Test conditions: TA = 25°C, BGA176 package, single-ended input is PC0 pin, differential input is PC0 & PC1 pins; MODE1 power supply (LDO supply mode), V_{DD} = V_{DDA} = 3.3V, V_{REFP} = 2.5V, internal reference source; f_{ADC} = 36MHz, SMP = 3.5 CLK, uncalibrated.

Table 4-5. Dynamic and Static Characteristics of GD32H73x_75x 14-bit ADC When Using External High-Precision Reference Source (1)

Symbol	Parameter	Test conditions	Typ	Unit
EO	Offset error	Single ended	±5.7	LSB
	Differential linearity error	Differential	±0.1	
DNL	Integral linearity error	Single ended	+1.3/-1.0	
	Effective number of bits	Differential	±1	
INL	Signal-to-noise and distortion ratio	Single ended	±1.9	
	Offset error	Differential	±1.6	
ENOB	Differential linearity error	Single ended	12.7	Bits
	Integral linearity error	Differential	13.4	

Symbol	Parameter	Test conditions	Typ	Unit
SNDR	Effective number of bits	Single ended	78.3	dB
		Differential	82.6	

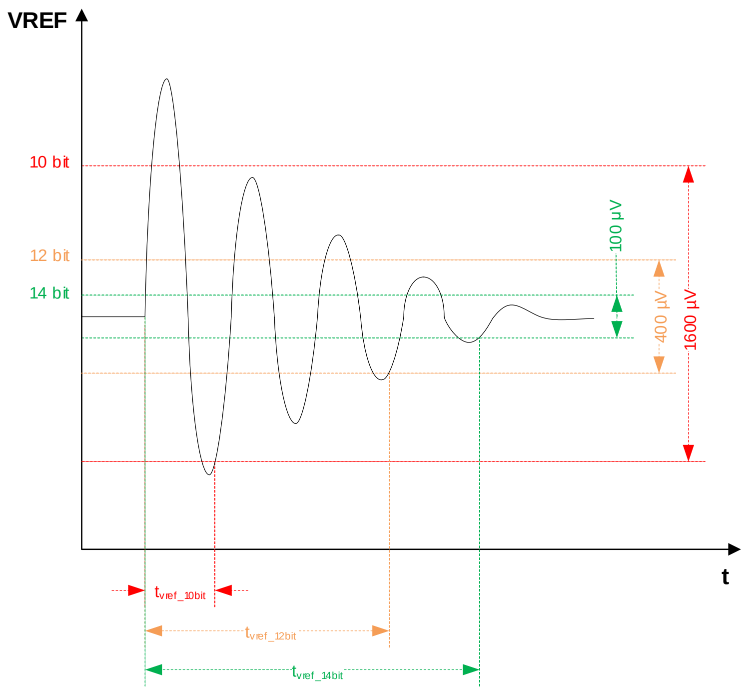
(1) Test conditions: TA = 25°C, BGA176 package, single-ended input is PC0 pin, differential input is PC0 & PC1 pins; MODE1 power supply (LDO supply mode), V_{DD} = V_{DDA} = V_{REFP} = 3.3V, external reference source; f_{ADC} = 36MHz, SMP = 3.5 CLK, uncalibrated.

4.3 The Impact of Resolution, Package, and Number of Simultaneously Used ADCs on Maximum ADC Frequency and Sampling Rate

During the conversion phase, the reference voltage input pin needs to respond to spike currents. To avoid conversion errors, sufficient time is required for the reference voltage to stabilize to ±1/4 LSB; otherwise, it may lead to reduced resolution and bit errors. The maximum ADC frequency decreases as the VREF stabilization time increases.

Figure 4-1. VREF Stabilization Time at Different Resolutions shows the time required for VREF to stabilize to ±1/4 LSB at different resolutions. It can be observed that the VREF in high-resolution mode requires a longer time to stabilize compared to low-resolution mode.

Figure 4-1. VREF Stabilization Time at Different Resolutions



The reference voltage stabilization time is also affected by the parasitic inductance of the package. Adding parasitic inductance to the VREF pin increases the stabilization time of VREF, thereby limiting the achievable ADC frequency. Therefore, package selection is critical to ADC performance and must be considered during the early design stages. BGA packages generally perform better than LQFP packages in this regard due to their lower pin inductance. In the GD32H73x_75x, the inductance of the VREFN and VREFP pins in the BGA176 package is approximately 2 nH, whereas the inductance of the VREFN and VREFP pins in the LQFP144 package exceeds 12 nH.

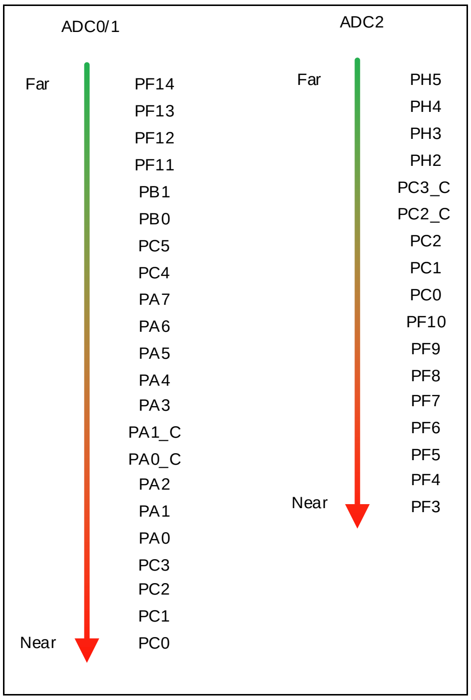
When multiple ADCs perform conversions simultaneously, the transient current on the VREFP pin increases, leading to an extended VREF stabilization time, which also reduces the maximum ADC frequency.

The impact of ADCs working simultaneously refers to ADCs with the same resolution operating synchronously with the same clock frequency and identical timing. If there is any delay in the timing, the VREF waveform becomes more complex, significantly degrading ADC performance.

4.4 The Impact of VCORE Power Supply Mode on ADC

The GD32H73x_75x integrates an internal SMPS module. When using the SMPS to supply power to VCORE, single-ended inputs may experience precision issues (with no impact on internal channels), while differential inputs are essentially unaffected. When using the GD32H73x_75x chip, if the SMPS module is employed, it is recommended to select ADC input pins located farther away from the SMPS module. The distance between ADC input pins and the SMPS module is illustrated in ***Figure 4-2. Diagram of ADC Input Pin Distance from SMPS Module***.

Figure 4-2. Diagram of ADC Input Pin Distance from SMPS Module

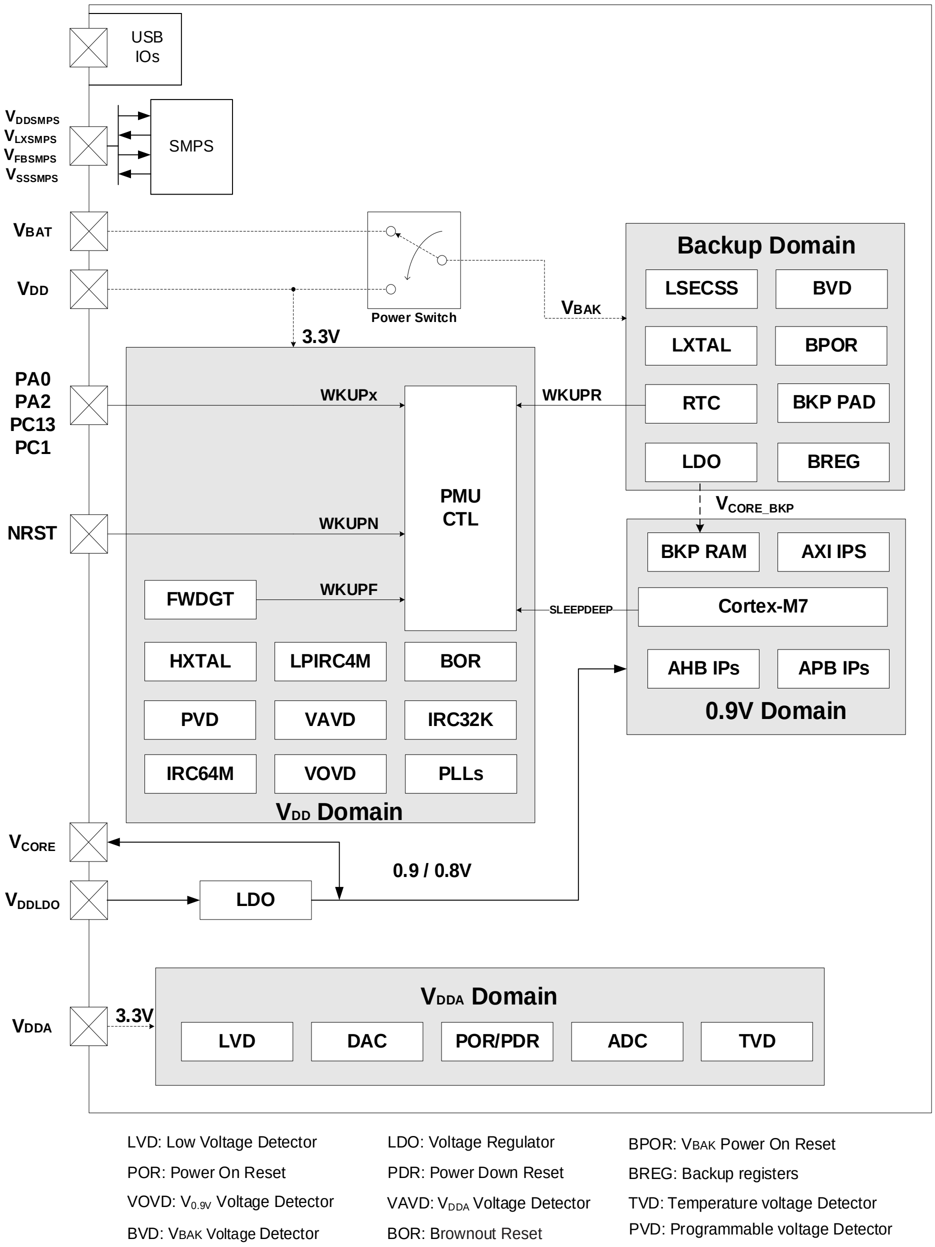


5 Hardware Design Considerations

5.1 Power Design

The GD32H73x_75x devices have three power domains, including the VDD domain, VDDA domain, 0.9 V domain, and backup domain. The VDD and VDDA domains are powered directly by the power supply, as shown in ***Figure 5-1. Power supply overview***.

Figure 5-1. Power supply overview



If VDDA is not equal to VDD, the voltage difference between them must not exceed 300mV. To avoid noise, VDDA can be connected to VDD through an external filter circuit.

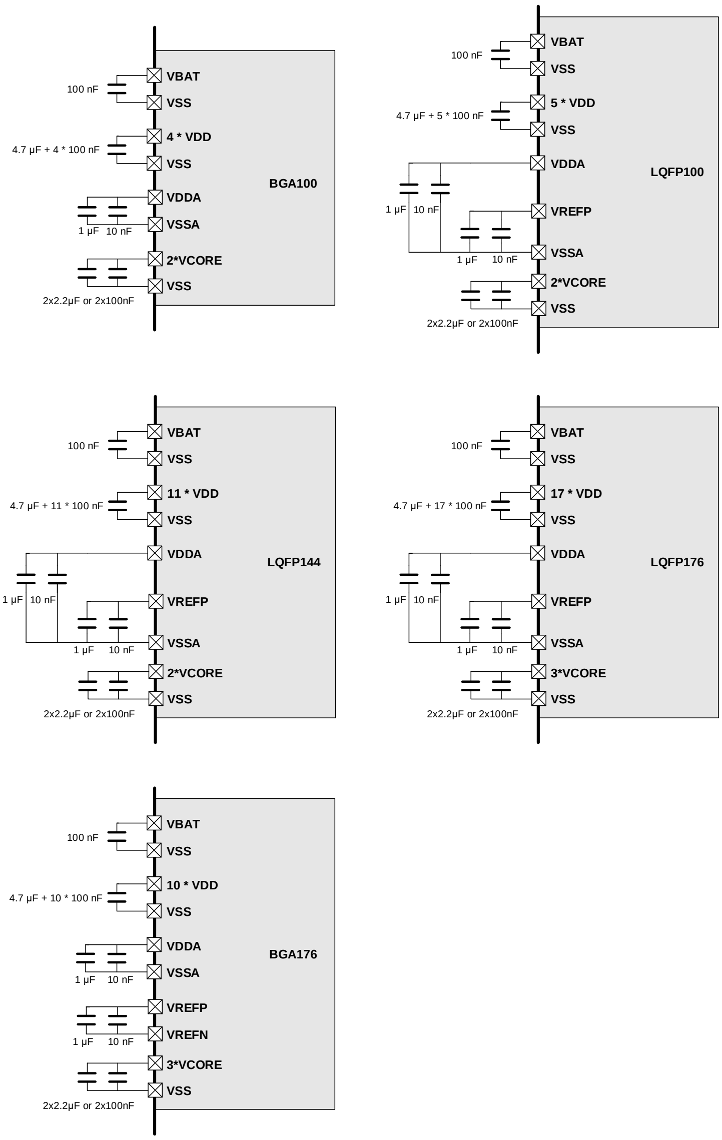
The BGA176 package includes VREFP and VREFN pins. VREFP can use an external reference power supply or be directly connected to VDDA, while VREFN must be connected to VSSA.

The LQFP package includes a VREFP pin, which can use an external reference power supply or be directly connected to VDDA.

Adding decoupling capacitors in the power network is essential. The recommended decoupling capacitors for different packages are shown in ***Figure 5-2. GD32H73x_75x Recommended Power Supply*** **Design**.

- The VDD pin must be connected with an external capacitor (N * 100 nF ceramic capacitor + not less than 4.7 uF tantalum capacitor, at least one V_{DD} needs to be connected to GND with a capacitor of not less than 4.7 uF, and other V_{DD} pins are connected to 100 nF).
- The V_{DDA} pin must be connected with an external capacitor (10 nF + 1 uF ceramic capacitor is recommended).
- The V_{REF} voltage can be generated internally or directly connected to V_{DDA}, and a 10 nF + 1 uF ceramic capacitor should be connected between the VREFP pin and ground.
- When using the internal LDO to supply power to VCORE, it is recommended to connect two 2.2 uF ceramic capacitors between VCORE and GND. When the internal LDO is bypassed, it is recommended to connect two 100nF ceramic capacitors between VCORE and GND.
- All capacitors must be placed close to the corresponding pins and directly connected to the ground plane.

Figure 5-2. GD32H73x_75x Recommended Power Supply Design



5.2 Peripheral circuit matching

To limit external noise, a small capacitor C_{IN} is placed at the ADC input pin, and a resistor is connected in between the signal source and the input pin. Together with C_{IN}, this forms an RC filter to achieve higher accuracy requirements, as shown in ***Figure 5-3. The ADC sampling block diagram with an external capacitor CIN added***. When configuring the sampling cycle, the external input impedance R_{AIN} (signal source impedance + RC filter impedance) must also be considered. For the GD32H73x_75x 14-bit ADC with f_{ADC} = 72 MHz, the sampling cycle and maximum input impedance are shown in ***Table 5-1. ADC RAIN max for fADC = 72 MHz (14-bit ADC) (1)(2)***.

Figure 5-3. The ADC sampling block diagram with an external capacitor CIN added

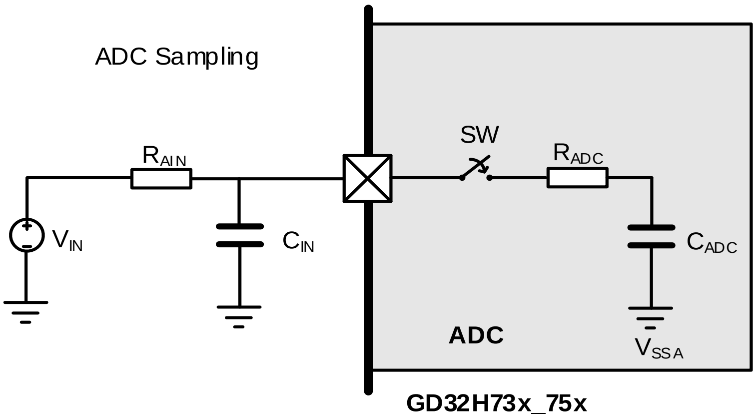


Table 5-1. ADC R_{AIN} max for f_{ADC} = 72 MHz (14-bit ADC) (1)(2)

Resolution	Sampling cycles @ 72 MHz	R_{AIN} max (kΩ)
14 bits	3.5	0.21
	6.5	0.52
	12.5	1.15
	24.5	2.40
	47.5	4.80
	92.5	9.50
	247.5	25.6
	810.5	84.4
12 bits	3.5	0.26
	6.5	0.62
	12.5	1.34
	24.5	2.77
	47.5	5.51
	92.5	10.8
	247.5	29.3
	810.5	96.5
10 bits	3.5	0.33
	6.5	0.75
	12.5	1.58
	24.5	3.25
	47.5	6.45
	92.5	12.7
	247.5	34.2
	810.5	112
8 bits	3.5	0.43
	6.5	0.93
	12.5	1.93
	24.5	3.94
	47.5	7.78

Resolution	Sampling cycles @ 72 MHz	R_{AIN} max (kΩ)
	92.5	15.2
	247.5	41.1
	810.5	135

(1) Value guaranteed by design, not 100% tested in production.

(2) The R_{AIN} value was calculated by theory and stray capacitance of actual pcb has not been taken into account.

5.3 Pin Selection

Due to capacitive coupling between I/O, traces, and internal bonding wires, the accuracy of the ADC can be affected by crosstalk from other signals. Therefore, it is recommended to avoid level-switching actions (such as PWM output) on pins adjacent to the ADC input pins. Additionally, pins that may switch and draw large currents should also be avoided, as this could lead to current surges causing voltage drops.

5.4 PCB Layout Considerations

1. Pay attention to the placement of components: digital modules and analog modules should be placed separately. Digital signals and their corresponding return current paths should be confined within the digital module section of the PCB and kept as far away as possible from analog signals.
2. The input path of ADC pins should be as short and straight as possible and should be kept as far away from digital signals as possible. In cases where ADC input signal paths and digital signal paths are not on the same layer, overlapping between the two should be avoided. It is recommended to add grounding shields around the ADC input signal paths, ensuring sufficient ground vias are placed for the grounding shield.
3. VSS / VSSA / VREFN pins should be grounded nearby, and the ground plane should be as complete as possible to ensure the return path has very low impedance.
4. It is recommended to connect VREFP / VDDA to a low-bias, low-noise, and low-drift voltage source. This voltage source should also have low impedance and sufficient bandwidth to respond to the transient current demands of the ADC.

6 Revision history

Table 6-1. Revision history

版本号.	说明	日期
1.0	Initial Release	Jan.31 2024
1.1	Delete the oversampling truncation table.	Mar.19 2024
1.2	Add the differential pin assignment for ADC2 channels to Table 4-1.	May,13 2025
1.3	Specify the chip series applicable to this Application Note, modify Important Notice page content.	Feb, 3 2026

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