

GigaDevice Semiconductor Inc.

GD32VW553K-START
User Guide

Rev1.3

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1. Summary

The GD32VW553K-START evaluation board is an RF performance evaluation board developed for the GD32VW553 series of dual-mode wireless microcontrollers. The GD32VW553K-START V5.0 evaluation board module supports the GD32VW553-MINI-I and GD32VW553-MINI-E wireless modules. The core device is the GD32VW553 wireless module, which contains a GD32VW553 series MCU. The GD32VW553 series MCU adopts a new open-source instruction set architecture RISC-V processor core with a main frequency of up to 160MHz. The integrated 2.4GHz Wi-Fi 6 and Bluetooth LE 5.2 RF module provides advanced baseband and RF performance, which is suitable for a wide range of wireless application scenarios, such as smart home appliances, industrial interconnection, and communication gateway.

Figure 1-1. GD32VW553K-START Appearance

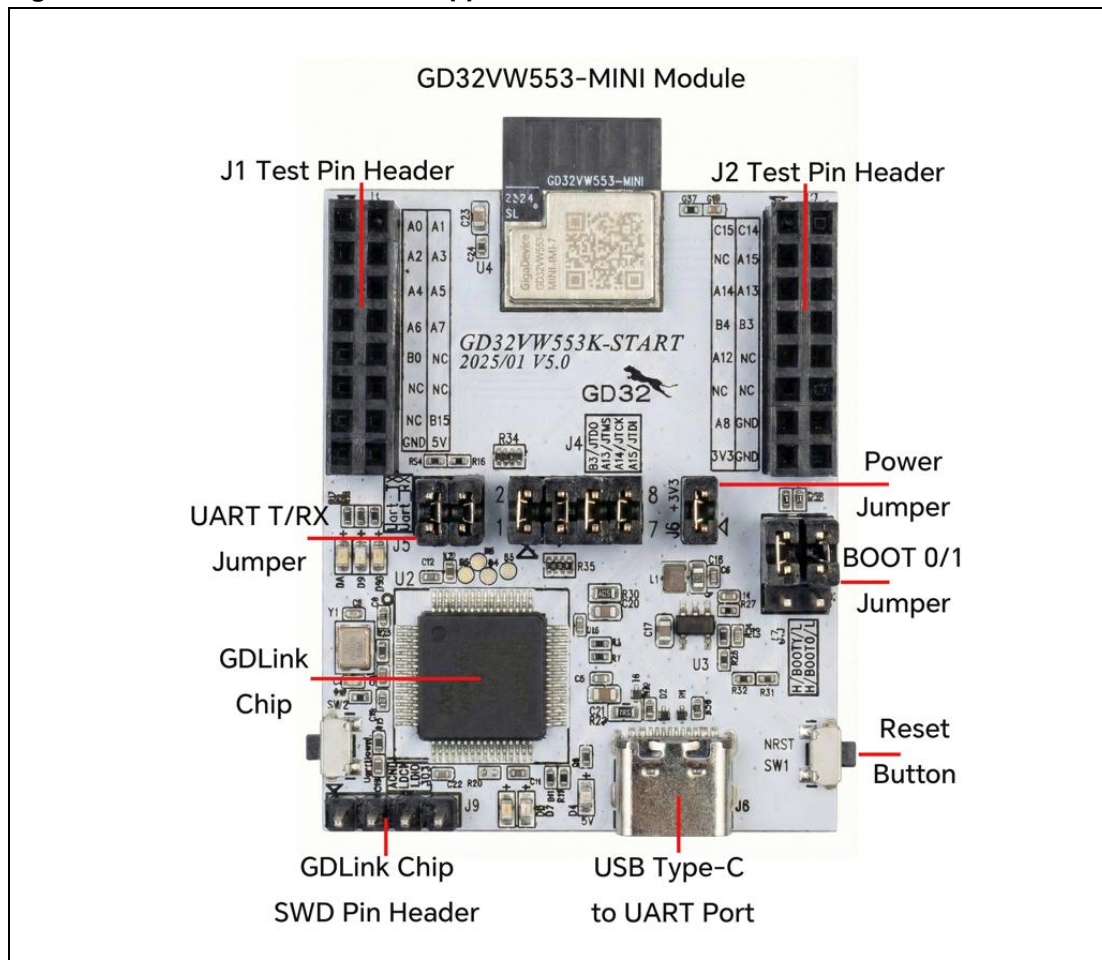
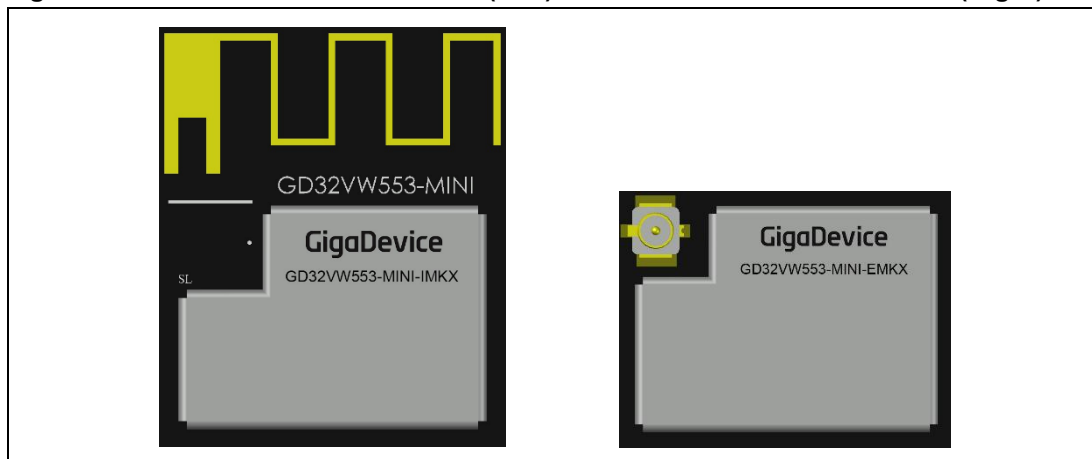


Figure 1-2. GD32VW553-MINI-I Module(Left)and GD32VW553-MINI-E Module(Right)


The GD32VW553K-START evaluation board uses a USB Type-C interface for power supply and serial communication. The DC-DC power supply chip on the board converts the 5V input from the USB to 3.3V, which powers either the GD32VW553-MINI-I / E wireless module and the GDLINK chip, depending on the configuration with the GD32E505. Alternatively, the system can be powered externally with a 5V input through pin J1.16.

The GD32VW553K-START provides test interfaces for all the GD32VW553-MINI-I / E wireless module's GPIO ports, as well as the main chip's NRST switches, the BOOT0 / 1 interface, the UART interface, the JTAG interface, and the GDLINK chip's burn-in interface.

Based on the START board, the tests that can be accomplished include but are not limited to: Non-signaling mode Wi-Fi & BLE transmitting and receiving RF indicators test, signaling mode Wi-Fi transmitting and receiving throughput indicators test, Wi-Fi & BLE power consumption indicators test in various scenarios, FCC / CE / SRRC certification regulations test, and other Wi-Fi and BLE hardware and software system function and performance test.

The GD32VW553K-START can also help developers to complete the compilation and debugging of applications developed based on the Wi-Fi and BLE APIs of the GD32VW553K series chips. For more details on the above test and use operation guide, please refer to the [Operation Guide](#) section of this document.

Table 1-1. GD32VW553K-START RF Characterization

Parameter Term	Instructions
Operation Frequency	2400-2483.5MHz
Wi-Fi Specification	IEEE 802.11b / g / n / ax
Data Transmission Rate	11b: 1,2,5.5,11(Mbps) 11g: 6,9,12,18,24,36,48,54(Mbps) 11n: HT20 MCS0-7. 11ax: HE20 MCS0-9. BLE 5.2: 125, 500(Kbps), 1, 2(Mbps)
Antenna Type	PCB Onboard Antenna, Gain 2-3dBi External Ipex Antenna

2. Function Pin Assign

This chapter describes each of the GD32VW553K-START connections and the main interfaces.

2.1. IO Connection

Table 2-1. GD32VW553K-START Connectors and Switch Functions

Interface	Description
J1	Interface to GPIO pins PA0~PA7 / PB0 / PB15 of the main chip, as well as +5V interface and GND interface.
J2	Interface to main chip PA8 / PA12~PA15 / PB3 / PB4 / PC14 / PC15 GPIO pins, as well as module +3.3V power supply test interface, GND interface.
J3	Connect to the main chip PC8 (BOOT0) and PB1 (BOOT1) pins, Boot mode selection needs to be configured accordingly. Default BOOT0 / 1 use shorting caps pull-down, that is, the chip default boot from Sip flash.
J4	Interface to the JTAG pins of PB3(JTDO) / PA13(JTMS) / PA14(JTCK) / PA15(JTDI) of the main chip, and interface to the JTAG pins of L_TDO / L_TMS / L_TCK / L_TDI of the GDLINK chip. By default, the above pins of the main chip and the GDLINK chip are connected by shorting caps, and the firmware can be burned into the main chip by the GDLINK chip.
J5	The interface to the UART TX / RX pins of the main chip PA6 (UART2_TX) and PA7 (UART2_RX), and the interface to the L_UART_RX, L_UART_TX and UART RX / TX pins of the GDLINK chip. By default, the above pins of the main chip and the GDLINK chip are connected via shorting caps, so that serial communication can be done between the GDLINK chip and the main chip.
J6	GD32VW553 module 3.3V power supply connection port, the default use of short-circuit cap connection. For power consumption test, external 3.3V power supply can be directly connected to J6.2.
J8	USB-C interface, default serial communication and +5V power supply interface.
J9	Interface to GDLINK chip L_SWIO / L_SWCK and other SWD pins, as well as GDLINK +3.3V power supply test interface and GND interface.
SW1	Connect the module to the NRST pin with GND via a 1K ohm resistor pull-up to 3.3 V. Press and release this switch to Reset the main chip.
SW2	Reserved button

2.2. Main Interfaces

Table 2-2. GD32VW553K-START Main Interfaces Description

Interface	Description
PA0	IO port that can be configured by the user.

Interface	Description
PA1	IO port that can be configured by the user.
PA2	IO port that can be configured by the user.
PA3	IO port that can be configured by the user.
PA4	IO port that can be configured by the user.
PA5	IO port that can be configured by the user.
PA6 / UART2_TX	IO port that can be configured by the user; UART TX。
PA7 / UART2_RX	IO port that can be configured by the user; UART RX。
PB0	IO port that can be configured by the user.
PB1 / BOOT1	IO port that can be configured by the user; Boot mode selection.
GND	Reference ground
PB15	IO port that can be configured by the user.
PA8	IO port that can be configured by the user.
PA12	IO port that can be configured by the user.
PB3 / JTDO	IO port that can be configured by the user; JTDO pin.
PB4 / JNTRST	IO port that can be configured by the user; JNTRST pin.
PA13 / JTMS	IO port that can be configured by the user; JTMS pin.
PA14 / JTCK	IO port that can be configured by the user; JTCK pin.
PC8 / BOOT0	IO port that can be configured by the user; Boot mode select.
PA15 / JTDI	IO port that can be configured by the user; JTDI pin.
PC14	IO port that can be configured by the user.
PC15	IO port that can be configured by the user.
NRST	Module reset pin, connect to 3.3V power supply to enable the module.
3V3	3.3V power supply pin
GND	Reference ground

3. Basic Operation

This chapter covers the GD32VW553K-START hardware configuration, software configuration and basic usage guidelines.

3.1. Hardware Configuration

The START evaluation board appearance is shown in [Figure 1-1. GD32VW553K-START Appearance](#) Among them:

- UART & JLINK functions: The communication function of USB to UART and the firmware burning function of USB to JLINK are realized through the GDLINK chip circuit on the bottom board, and PC is connected to the USB port of the bottom board through a USB cable.
- Serial port connection: Serial ports are connected to the bottom board J5.2 / 4 (main chip UART PIN) and J5.1 / 3 (GDLINK UART PIN)) respectively with shorting caps.
- JLINK connection: JLINK are connected to the bottom board J4.2 / 4 / 6 / 8 (main chip JLINK PIN) and J4.1 / 3 / 5 / 7 (GDLINK JLINK PIN)) respectively with shorting caps.
- Configuration of the main chip mode:
 - "BOOT0" of PIN should be at low level (boot from flash), which is realized by configuring the shorting caps J3.3 and J3.5 on the bottom board.
- Module power supply: The DC-DC circuit on the bottom board converts the 5V power input from the USB port into a 3V3 output, and the 3V3 output is connected to the 3V3 pad of the module through the shorting cap "J6". Disconnect this shorting cap (from external 3V3 output to J6.2) to test power consumption of the module.

3.2. Software Configuration

3.2.1. Driver Installation

It is recommended to use the START evaluation board on a PC with Win10, Win11 or future versions of Windows, as they come with the GDLINK driver. When the GDLINK driver is ready, and the evaluation board hardware and test system set up, the START evaluation board and the PC using USB cable connection, you can see the serial device and COM number in the PC "Device Manager" [Figure 3-1. Installation of serial port drive.](#)

Figure 3-1. Installation of serial port drive



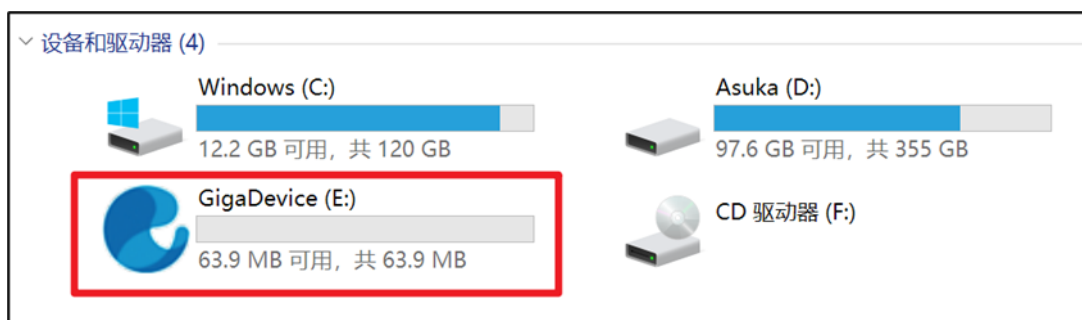
3.2.2. Firmware Download

The START evaluation board has an integrated GDLINK circuit (GD32E505) that can be used with OpenOCD. The GDLINK chip also integrates UART function, so only one USB Type-C cable is needed for power supply, debugging and log viewing at the same time.

Connect the pins JTCK, JTMS, JTDO and JTDI to the lower four pins via shorting caps, so that you can download and debug the code via GDLINK: After installing the GDLINK driver, you can find a new "GDLINK" diskette in the PC - "Explorer" ([Figure 3-2 GDLINK Folder](#)). After that, you can directly "drag and drop" (or copy and paste) the .bin format firmware provided by GigaDevice to this disk drive and wait for a moment to realize the firmware burning, and then press the "reset" button on the side of the evaluation board to reboot the chip after completion.

However, the above burning method is limited by the ability of the GDLINK chip, the debugging and downloading speed is relatively slow, so it is also recommended to connect an external GDLINK or JLINK debugger to the JTAG interface of the evaluation board for more efficient downloading and debugging.

Figure 3-2 GDLINK Folder



3.3. Operation Guide

The [GD32VW5 series MCU resource download page](#) provides complete test and application notes for the chip, most of the test and development descriptions in the notes are based on the GD32VW553K-START to complete, so this operation guide subsection will not repeat the description of the existing contents of the application notes, and will only make a brief

introduction of each test and application development guide, and prompt some of the matters that need attention.

3.3.1. AN154 GD32VW553 Quick Development Guide

[GD32VW553 Quick Development Guide](#) aims to guide developers to get started with Wi-Fi and BLE development on the corresponding evaluation boards for the GD32VW553 series chips. The main contents include the building of GD32Eclipse IDE development environment, SDK configuration, compiling and debugging SDK under GD32Eclipse IDE.

3.3.2. AN158 GD32VW553 Wi-Fi Development Guide

[GD32VW553 Wi-Fi Development Guide](#) aims to help developers familiarize themselves with the SDK and develop their own applications using the APIs. The main contents include the Wi-Fi SDK software framework, the startup process, and the introduction of Wi-Fi and related component APIs. The Development Guide is composed of three parts: OSAL API usage, Wi-Fi Netif API usage, and Wi-Fi management related API usage. It also uses a specific use case to introduce how to use the component API to scan wireless networks, connect to APs, start soft AP and connect to Alibaba Cloud and other operations.

3.3.3. AN152 GD32VW553 BLE Development Guide

[GD32VW553 BLE Development Guide](#) aims to help developers familiarize themselves with and develop their own applications using the BLE API. It describes in detail the BLE software framework and the related API interfaces, and introduces BLE Scanning, BLE Broadcasting, BLE GATT server application, and BLE Distribution Networking content with a specific use case.

3.3.4. AN153 GD32VW553 Basic Commands User Guide

[The GD32VW553 Basic Commands User Guide](#) aims to introduce the various basic UART-based commands required for Wi-Fi and BLE hardware and software system functionality and performance testing of the GD32VW553 series chips.

3.3.5. AN151 GD32VW553 AT Command User Guide

[The GD32VW553 AT Command User Guide](#) aims to guide developers in testing and developing the GD32VW553 series chips based on the AT command.

3.3.6. AN149 Test Guidelines for RF Performance and Transceiver Power Consumption of GD32VW553

[The Test Guidelines for RF Performance and Transceiver Power Consumption of](#)

[GD32VW553](#) aims to guide developers to evaluate the Wi-Fi & BLE transmit and receive RF performance and corresponding power consumption of the GD32VW553K-START in non-signaling mode. The Test Guidelines is about the three parts of the test method of RF performance using RF tools, using serial commands, and the test method of non-signaling RF transmitting and receiving power consumption. The Test Guidelines also introduces the configuration of the test system and the hardware and software of the START board, as well as common problems and solutions.

Note that this test requires burning the RF test firmware with keyword "rf_test".

3.3.7. **AN150 Test Guidelines for Throughput and Scenario-based Power Consumption of GD32VW553**

[Test Guidelines for Throughput and Scenario-based Power Consumption of GD32VW553](#) aims to guide developers to evaluate the Wi-Fi transmitting and receiving throughput performance and various scenario power consumption of GD32VW553K-START in signaling mode.

The Test Guidelines firstly introduces the test method of using serial tools and commands to evaluate the TCP TX / RX and UDP TX / RX throughput metrics in signaling mode, and testers can burn the signaling test firmware with keyword "wifi_signaling_test" for targeted testing. Secondly, it introduces the test methods of power consumption for four scenarios: Wi-Fi off, connecting AP+UDP TX, connecting AP+UDP RX, connecting AP+power saving & DTIM=1.

The Test Guidelines also introduces the configuration of the test system and the hardware and software of the START board, as well as common problems and solutions.

3.3.8. **AN146 GD32VW553 Certification Test Guidelines**

[The GD32VW553 Certification Test Guidelines](#) aims to guide developers to evaluate the START board's RF-related FCC / CE / SRRC certification regulations.

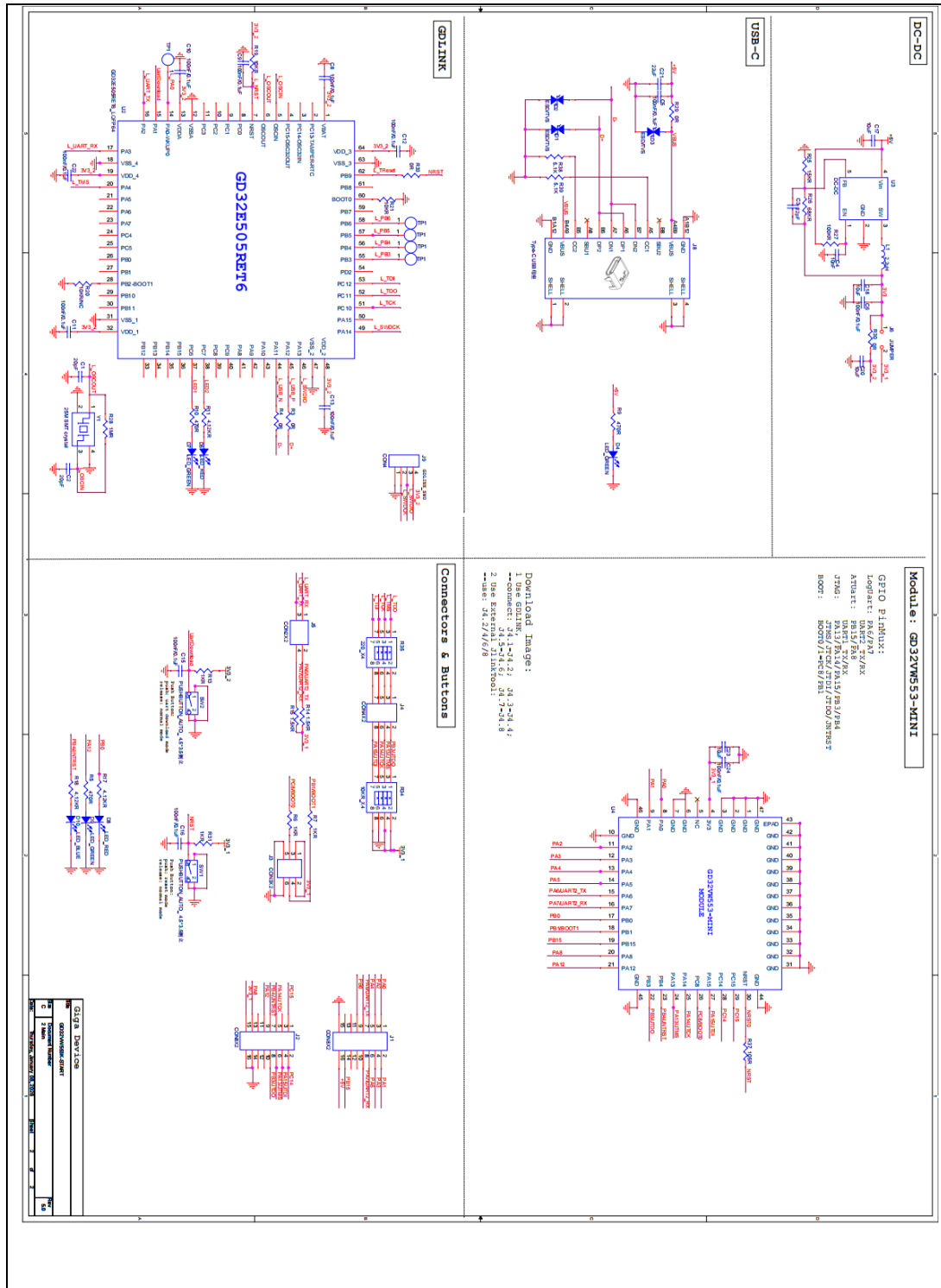
It introduces the methods of using RF tools and serial commands to evaluate the TX / RX indicators of non-signaling modes in each certification, as well as the methods of using serial commands to evaluate the "Blocking" and "Adaptivity" test items of signaling modes in CE certification.

Meanwhile, the article also introduces the configuration of the test system and the hardware and software of the START board, as well as the common problems and solutions.

It should be noted that this test requires burning the corresponding firmware according to the specific test items.

4. Schematic

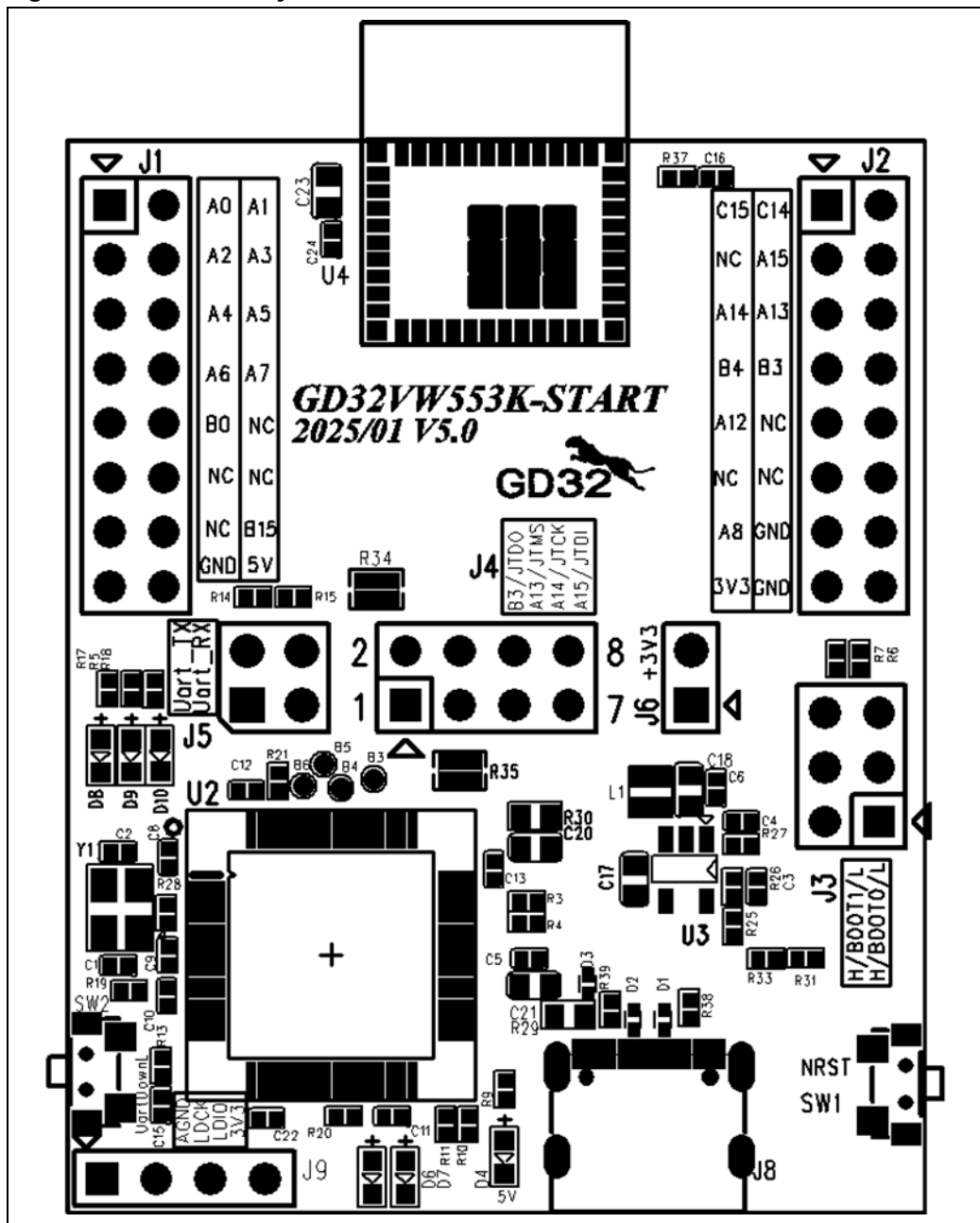
Figure 4-1 START Evaluation Board Schematic



5. Layout

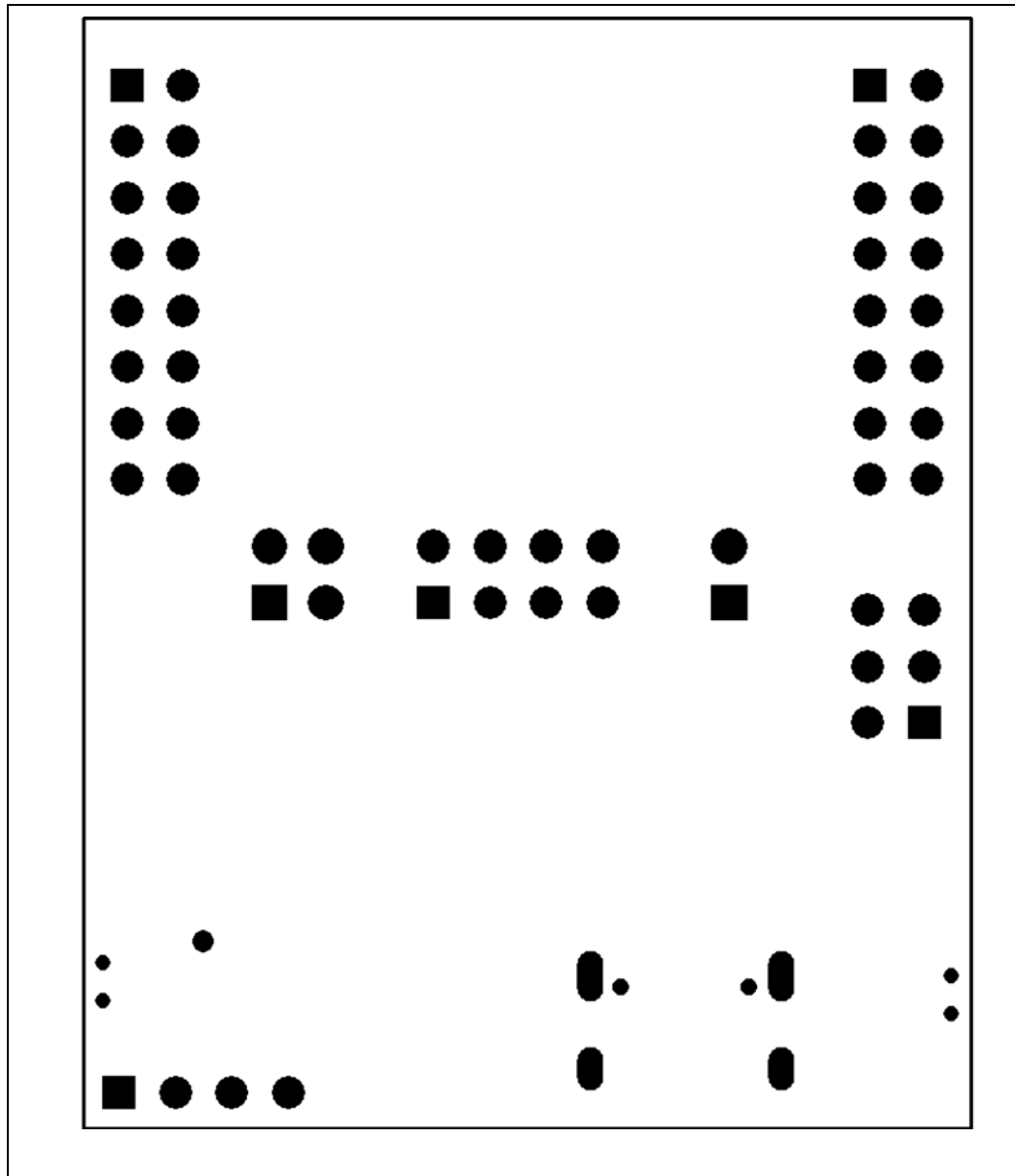
TOP Overlay

Figure 5-1. TOP Overlay



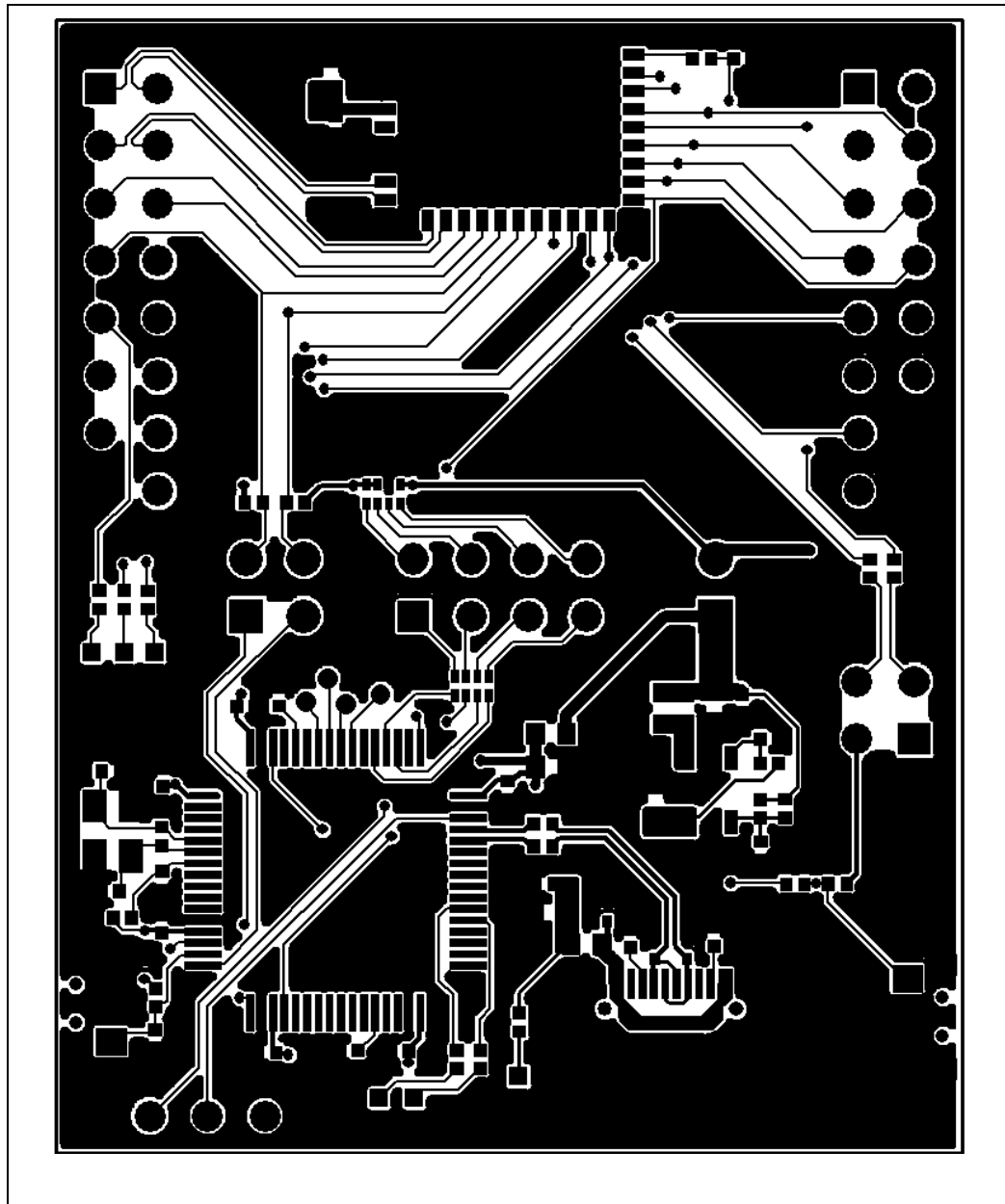
Bottom Overlay

Figure 5-2. Bottom Overlay



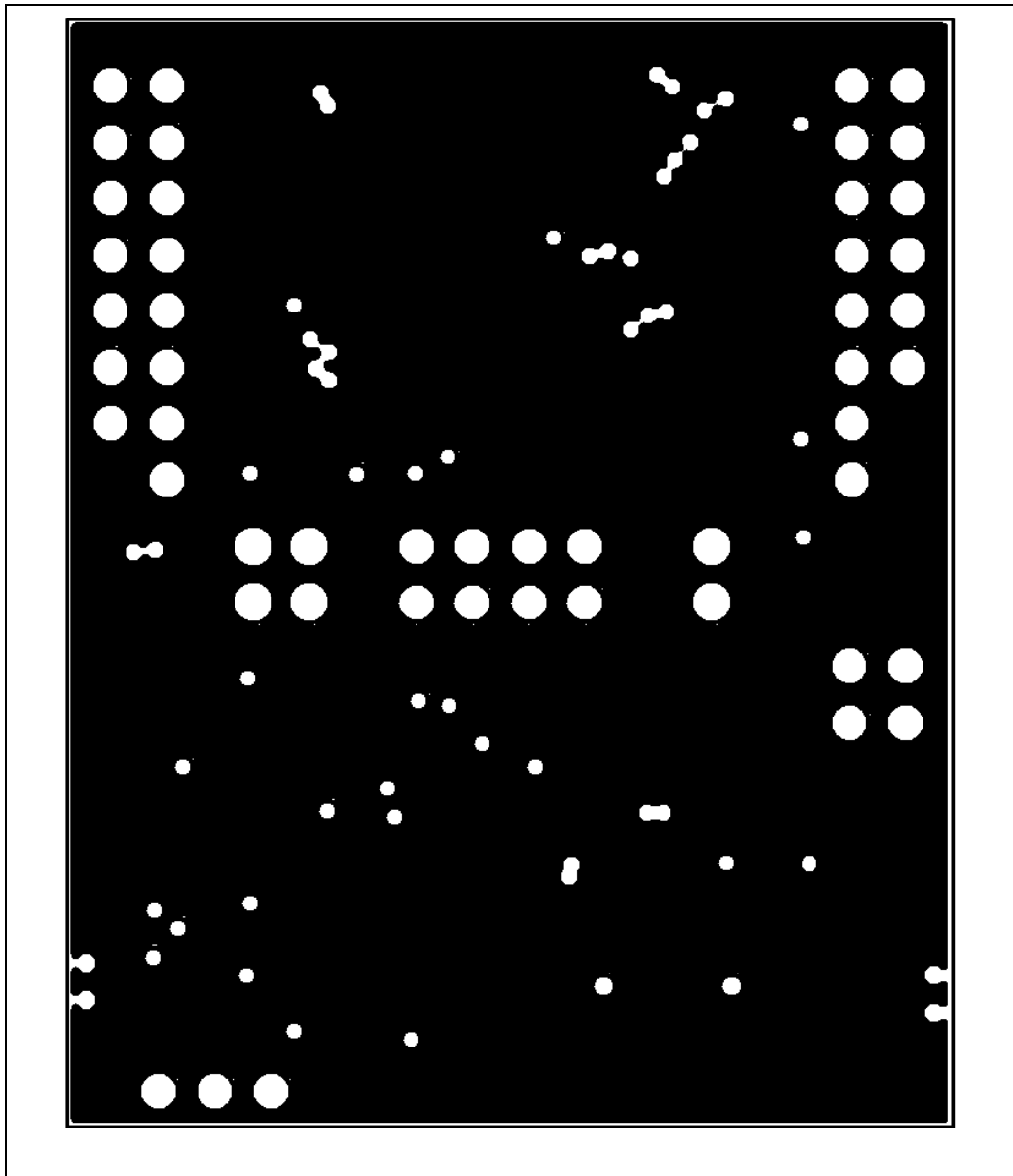
TOP Layer

Figure 5-3. TOP Layer



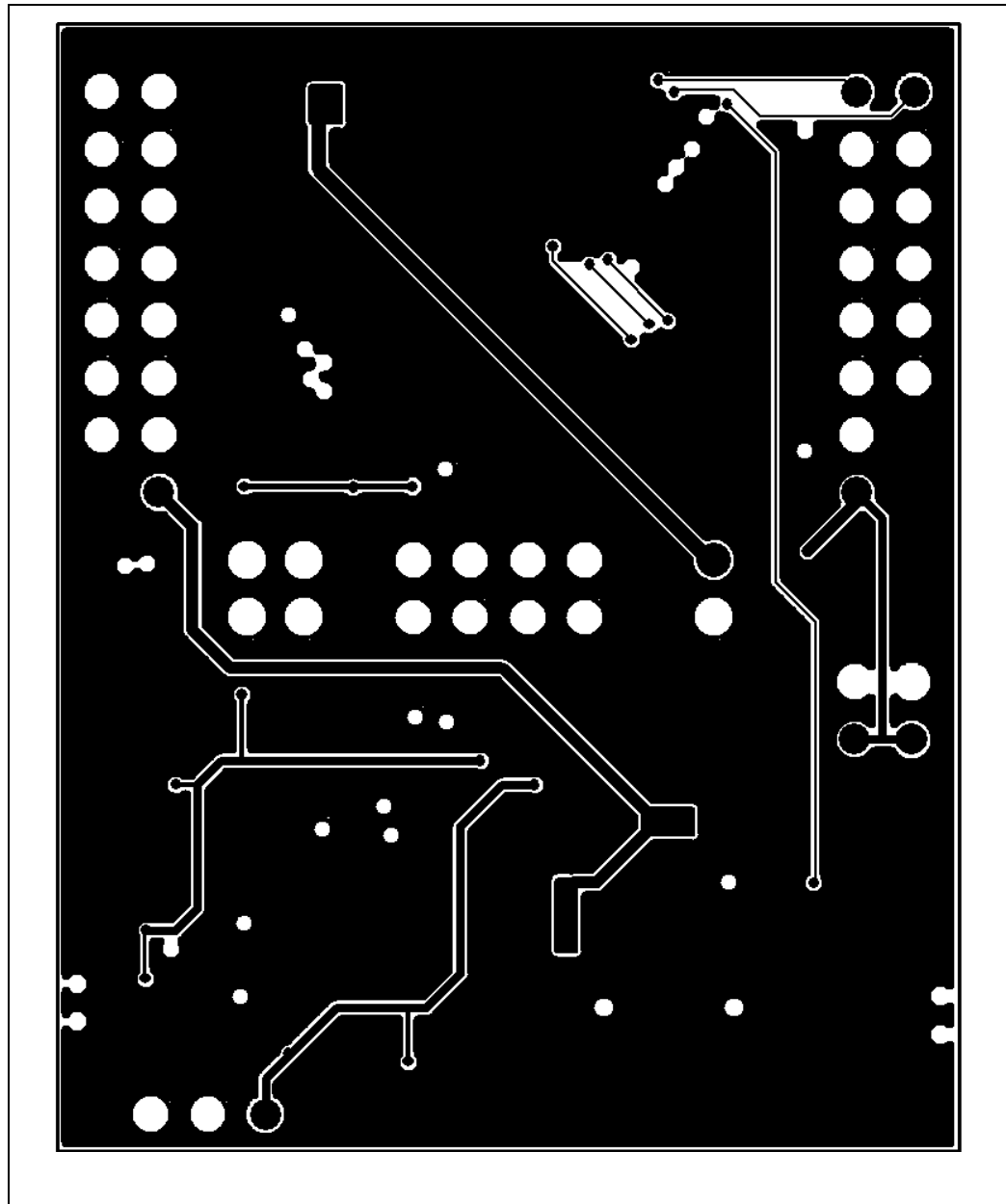
GND Layer

Figure 5-4. GND Layer



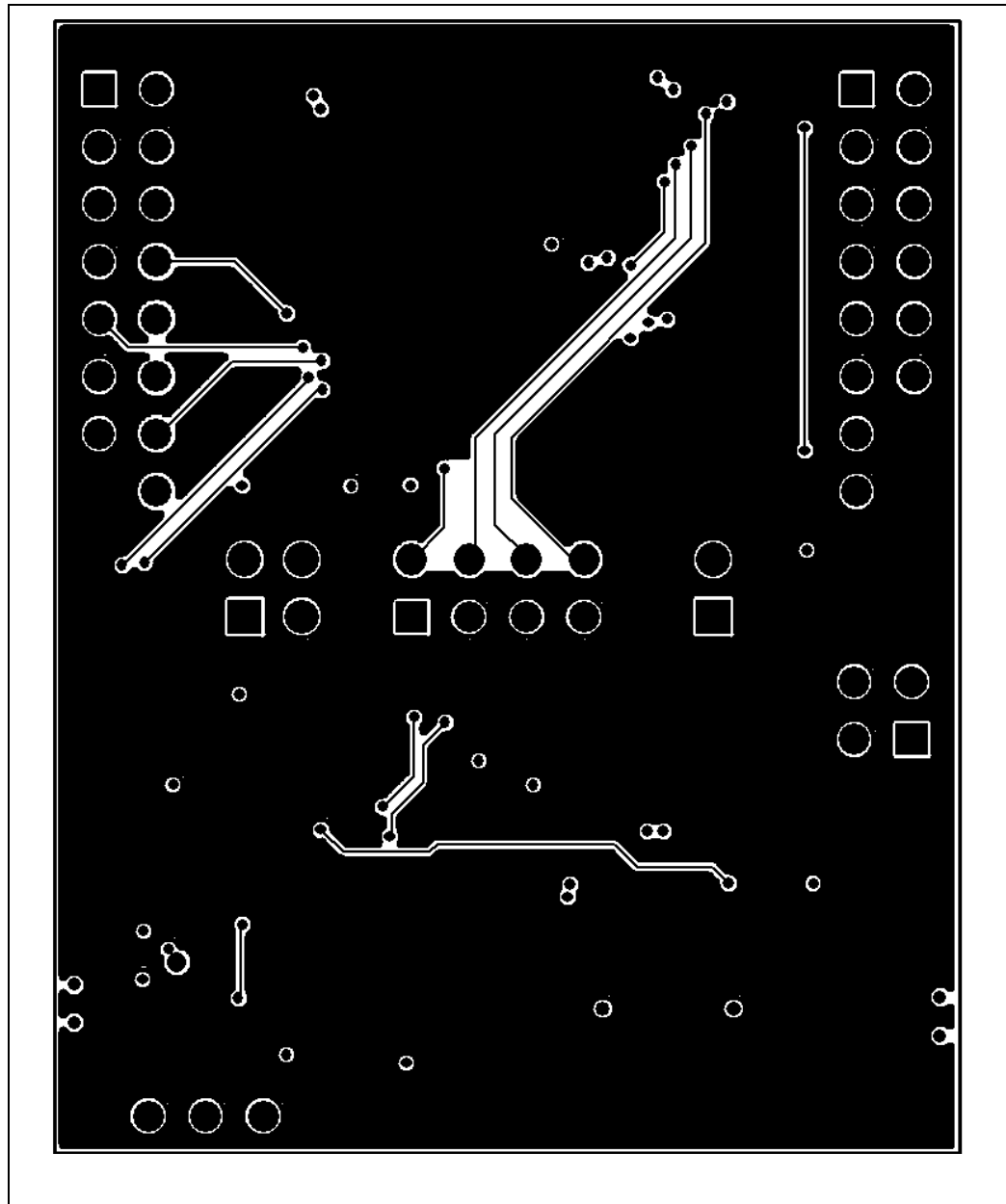
VCC Layer

Figure 5-5. VCC Layer



Bottom Layer

Figure 5-6. Bottom Layer



6. Revision History

Table 6-1 Revision History

Revision No.	Description	Date
1.0	Initial release	1/5/2024
1.1	Update partial GPIO descriptions	3/15/2024
1.2	Update the document content to adapt to the START development board Version V4.0	08/09/2025
1.3	Update the document content to adapt to the START development board Version V5.0	02/05/2026

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