GigaDevice Semiconductor Inc.

Device limitations of GD32E53x

Errata Sheet

Revision 1.0

(Nov. 2026)

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1. Introduction

This document applies to GD32E53x product series, as shown in Table 1-1. Applicable products. It offers technical guidance for using GD32MCU and provides workaround to current device limitations. This revision of the errata sheet applies only to devices with revision code B.

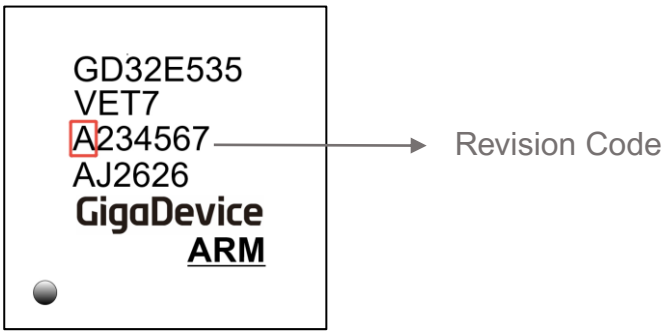
Table 1-1. Applicable products

Type	Part Numbers
MCU	GD32E533xx series
	GD32E535xx series
	GD32E537xx series
	GD32E53Pxx series

1.1. Revision identification

The device revision can be identified according to the mark on the top of the package. The 1st code on Line 3 of the mark is the product revision code, as shown in ***Figure 1-1. Device revision code of GD32E53x***.

Figure 1-1. Device revision code of GD32E53x



1.2. Summary of device limitations

The device limitations of GD32E53x are shown in ***Table 1-2. Device limitations***, please refer to Section 2 for more details.

Table 1-2. Device limitations

Module	Limitations	Workaround
		Rev. Code B
System	*The first 32 KB of SRAM is initialized after wake-up from Deep-sleep mode 1*	Y
FMC	*Entering Deep-sleep or Standby mode before Flash erase/program operations complete causes an abnormal system*	Y

Module	Limitations	Workaround
		Rev. Code B
	reset when nRST_STDBY and nRST_DPSLP are set to 0	
PMU	*FWDGTRSTF flag cannot be set in standby mode*	Y
	Enabling the wakeup function (WUPENx) will set WUF when WKUPx is configured for rising- or falling-edge wakeup	Y
USART	*In smartcard mode during data reception, a parity error detected during TX transmission is considered a retransmission, and FERR and RBNE cannot be set*	N
	In smartcard mode, RTF is set prematurely when the receive timeout threshold (RT) is configured as 0	Y
	In smartcard mode during data reception, EBF flag may fail to be set during retransmission	N
	The high baud rate of USART will cause data loss when using hardware flow control mode	N
	When the TX FIFO function is enabled, the TFNF flag is not cleared as expected	Y
	When DENR = 1, DDRE = 0, and HCM = 1, RTS remains asserted high	N
	In smartcard mode, the PERR flag is set abnormally	N
	In Deep-sleep mode, the parity error caused by wakeup frames will set PERR and EPERR bits	N
	In synchronous mode, the PERR flag is set abnormally	N
	In Deep-sleep mode, the parity error caused by wakeup frames will set PERR bit but not EPERR	N
I2C	*When I2C is operating as a master transmitter, if the slave responds with NACK to the last byte, a START condition cannot be correctly issued in the transfer complete interrupt*	Y
I2S	*When I2S is operating as a slave receiver, if the last frame of data is short and I2S_WS does not toggle after reception ends, the last data word is lost*	N
OSPI	*TERR error assertion*	Y
	Communication failure when switching to indirect mode after aborting memory-mapped mode with cache enabled	Y
CAN	*When TFO is set to 1, after sequentially enabling 3 mailboxes for transmission, aborting the lowest priority transmit mailbox will also cause the second priority transmit mailbox to be aborted*	Y
	Frequent switching between initialization mode and normal mode prevents recovery from the BUSOFF state	Y
Core	*Access permission faults are prioritized over unaligned Device memory faults*	N

Note:

Y = Limitation present, workaround available

N = Limitation present, no workaround available

'--' = Limitation fixed

2. Descriptions of device limitations

2.1. System

2.1.1. The first 32 KB of SRAM is initialized after wake-up from Deep-sleep mode 1

Description & impact

After waking up from Deep-sleep Mode 1, the first 32 KB of SRAM is hardware-initialized to 0.

Workarounds

Disable the SRAM hardware initialization function by configuring the SRAM_RST bit field in the option bytes register set. This function is disabled by default when the chip leaves the factory. During system power-up, use software-based SRAM initialization instead of hardware initialization.

2.2. FMC

2.2.1. Entering Deep-sleep or Standby mode before Flash erase/program operations complete causes an abnormal system reset when nRST_STDBY and nRST_DPSLP are set to 0

Description & impact

When nRST_STDBY and nRST_DPSLP are set to 0, the system is configured to reset rather than enter Standby or Deep-sleep mode. Under this configuration, attempting to enter either mode before Flash erase/program operations complete causes an abnormal system reset, compromising data integrity.

Workarounds

Ensure that all Flash erase/program operations are complete before the MCU attempts to enter Deep-sleep or Standby mode.

2.3. PMU

2.3.1. FWDGTRSTF flag cannot be set in standby mode

Description & impact

The FWDGTRSTF bit is not set by hardware when an FWDGT reset occurs while the MCU is in Standby mode.

Workarounds

The application programme can determine whether a FWDGT reset has occurred. For example, record whether a system reset has occurred and rule out other possible reset causes to determine whether the reset was caused by FWDGT.

2.3.2. Enabling the wakeup function (WUPENx) will set WUF when WKUPx is configured for rising- or falling-edge wakeup

Description & impact

For pins that support rising- or falling-edge wakeup from Standby mode, enabling the wakeup function (by setting WUPENx) will set WUF (the wakeup flag), even if the pin's pull-up or pull-down has been configured beforehand.

Workarounds

After enabling the wakeup function and before entering Standby mode, software must wait for WUF to be set and then clear it.

2.4. USART

2.4.1. In smartcard mode during data reception, a parity error detected during TX transmission is considered a retransmission, and FERR and RBNE cannot be set

Description & impact

In smartcard mode during data reception, a parity error detected during TX transmission is considered a retransmission, but the TX pin does not detect a NACK signal. The read data buffer not empty flag (RBNE) and the framing error flag (FERR) cannot be set.

Workarounds

Not available.

2.4.2. In smartcard mode, RTF is set prematurely when the receive timeout threshold (RT) is configured as 0

Description & impact

In smartcard mode, when the receive timeout threshold (RT) is set to 0, the receive timeout flag (RTF) is set at the START bit of the first data frame.

Workarounds

Configure the RT register with the desired receive timeout threshold value plus 11.

2.4.3. In smartcard mode during data reception, EBF flag may fail to be set during retransmission

Description & impact

In smartcard mode reception, if the retransmitted data frame satisfies the block count value = BL + 4, and the current retransmitted data frame remains with a parity error and is not moved into the data register, the block end flag (EBF) cannot be set. Additionally, the subsequent BL counter continues counting, causing counter runs out of control, and EBF remains reset.

Workarounds

Not available.

2.4.4. The high baud rate of USART will cause data loss when using hardware flow control mode

Description & impact

In the case of high baud rate of USART, when using the hardware flow control mode, the transmitter does not detect the RTS level in time due to the timing lag of the receiver RTS pulling up, resulting in one more data sent by the USART transmitter.

Workarounds

Not available.

2.4.5. When the TX FIFO function is enabled, the TFNF flag is not cleared as expected

Description & impact

When the TX FIFO function is enabled, continuously writing data until the FIFO is full results in TFNF = 0. If one data word is then transmitted, TFNF becomes 1. Subsequently, writing one data word into the FIFO fills it again, but TFNF remains 1 instead of being cleared to 0 as expected.

Note: The above issue applies only to USART5.

Workarounds

When using the TX FIFO function, use the TFF or TFT flag instead of the TFNF flag as the criterion when writing data.

2.4.6. When DENR = 1, DDRE = 0, and HCM = 1, RTS remains asserted high

Description & impact

When DENR = 1, DDRE = 0, and HCM = 1, the RTS signal remains asserted high, causing hardware flow control to fail.

Workarounds

Not available. If the application permits, ensure that the above three conditions are not all true at the same time during operation.

2.4.7. In smartcard mode, the PERR flag is set abnormally

Description & impact

In smartcard mode, when NACK is disabled (NKEN = 0) and SCRTNUM is configured to a non-zero value, the PERR bit fails to be set after the USART receives a frame with a parity error.

Workarounds

Not available.

2.4.8. In Deep-sleep mode, the parity error caused by wakeup frames will set PERR and EPERR bits

Description & impact

In Deep-sleep mode, parity errors caused by wake-up frames will set the PERR bit. For

example, when using USART address-match to wake up from Deep-sleep mode, if a frame with a parity error and a non-matching address is received first, followed by a frame with no parity error and a matching address, the PERR and EPERR bits will be set after wakeup.

Workarounds

Not available. The software ignores the parity error flag generated in this case.

2.4.9. In synchronous mode, the PERR flag is set abnormally

Description & impact

In synchronous mode, when the data bit inversion function is enabled (DINV = 1), the PERR bit will still be set even if the USART receives a frame with no parity error.

Workarounds

Not available. If the application permits, do not enable the data bit inversion feature in synchronous mode.

2.4.10. In Deep-sleep mode, the parity error caused by wakeup frames will set PERR bit but not EPERR

Description & impact

In Deep-sleep mode, parity errors caused by wake-up frames will set the PERR bit but not EPERR bit. For example, when using USART address-match to wake up from Deep-sleep mode, if a frame with a parity error and a non-matching address is received first, followed by a frame with parity error and a matching address, the PERR bit will be set after wakeup while the EPERR bit remains reset.

Workarounds

Not available. The software ignores the parity error flag generated in this case.

2.5. I2C

2.5.1. When I2C is operating as a master transmitter, if the slave responds with NACK to the last byte, a START condition cannot be correctly issued in the transfer complete interrupt

Description & impact

When I2C is operating as a master and has finished transmitting the last byte of data, if the

slave responds with a NACK signal, the master cannot correctly issue a START condition within the transfer complete (TC) interrupt, meaning the next transfer cannot be initiated.

Workarounds

Send a STOP condition in the NACK interrupt handler first, then initiate the next transfer.

2.6. I2S

2.6.1. When I2S is operating as a slave receiver, if the last frame of data is short and I2S_WS does not toggle after reception ends, the last data word is lost

Description & impact

When I2S is operating as a slave receiver, if the last frame of data is short and I2S_WS does not toggle after reception ends, the last data word is lost. If data transmission continues, an erroneous data word will be received; if data transmission stops, one data word will be missing at the end.

Workarounds

Not available. Evaluate the impact based on the specific application scenario. For example, when I2S is used for audio data communication, the impact of this issue on the application is minimal.

2.7. OSPI

2.7.1. TERR error assertion

Description & impact

When the configured data address plus data length exceeds the maximum device address range, TERR is asserted. If TERR is cleared and communication is initiated again, OSPI_ADDR and OSPI_DTLEN remain at their previous values. In this case, even when a write enable command is issued and address mode is disabled, TERR will still be triggered.

Workarounds

Before initiating communication again, reconfigure OSPI_DTLEN and OSPI_ADDR to ensure the new transaction uses updated address and length parameters.

2.7.2. Communication failure when switching to indirect mode after aborting memory-mapped mode with cache enabled

Description & impact

With cache enabled, after entering memory-mapped mode by configuring the wrap-related register group and then exiting that mode via Abort, any subsequent switch to indirect-mode communication requires synchronized configuration of both the tcfg register group and the wrap register group. Otherwise, indirect-mode communication cannot proceed unless the OSPI module is re-initialized first.

Workarounds

In the above mode-switching scenario, before entering indirect mode, configure the tcfg and wrap register groups synchronously.

2.8. CAN

2.8.1. When TFO is set to 1, after sequentially enabling 3 mailboxes for transmission, aborting the lowest priority transmit mailbox will also cause the second priority transmit mailbox to be aborted

Description & impact

When all pending transmit mailboxes are sent in first-in-first-out order (TFO=1), such as the transmission sequence is 0->1->2. When aborting mailbox 2 transmission, if mailbox 1 is still in pending status, mailbox 1 will also be aborted, meaning the data in transmit mailbox 1 will not be sent out.

Workarounds

Use one of the following solutions:

1) Before aborting the lowest priority transmit mailbox, ensure that the second priority transmit mailbox is not in pending status.
2) After aborting the lowest priority transmit mailbox, reconfigure and transmit the second priority and lowest priority transmit mailbox.

2.8.2. Frequent switching between initialization mode and normal mode prevents recovery from the BUSOFF state

Description & impact

When CAN frequently switches between initialization mode and normal mode, it may fail to recover either automatically or manually after entering the BUSOFF state, resulting in loss of CAN bus communication.

Workarounds

1) If automatic bus-off recovery is enabled, software does not need to switch modes to recover from the BUSOFF state.
2) If manual recovery is required, do not insert a delay between switching to initialization mode and switching back to normal mode. Enable the BUSOFF interrupt and perform the mode switching in the BUSOFF interrupt handler.

2.9. Core

About Cortex-M33 (r1p0) limitations, please refer to "Cortex-M33 AT623 and Cortex-M33 with FPU AT624 Software Developer Errata Notice". This document can be downloaded on ***ARM official website***.

2.9.1. Access permission faults are prioritized over unaligned Device memory faults

This limitation refers to Arm ID number 1080541 in "Cortex-M33 AT623 and Cortex-M33 with FPU AT624 Software Developer Errata Notice".

Description & impact

A load or store which causes an unaligned access to Device memory will result in an UNALIGNED UsageFault exception. However, if the region is not accessible because of the MPU access permissions (as specified in MPU_RBAR.AP), then the resulting MemManage fault will be prioritized over the UsageFault.

This erratum affects all configurations of the Cortex-M33 processor with the MPU enabled.

The failure occurring conditions are as follows:

The MPU is enabled and:

- A load/store access occurs to an address which is not aligned to the data type specified in the instruction.
- The memory access hits one region only.
- The region attributes (specified in the MAIR register) mark the location as Device memory.

- The region access permissions prevent the access (that is, unprivileged or write not allowed).

The implications of this limitation is that the MemManage fault caused by the access permission violation will be prioritized over the UNALIGNED UsageFault exception because of the memory attributes.

Workarounds

Not available. However, it is expected that no existing software is relying on this behavior since it was permitted in Armv7-M.(The CM33 is Armv8-M).

3. Revision history

Table 3-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Nov. 17, 2026

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