

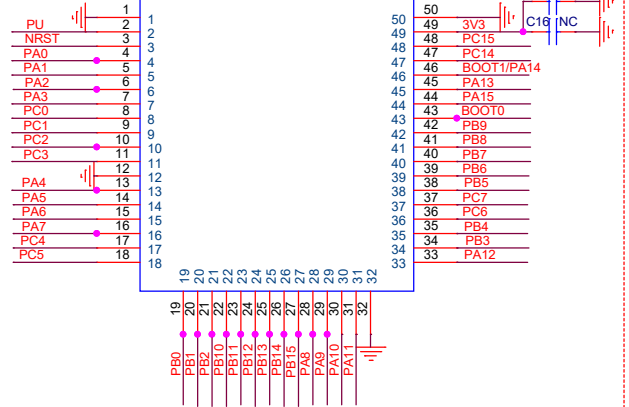
GD32W515PIQ6

QFN56 7X7

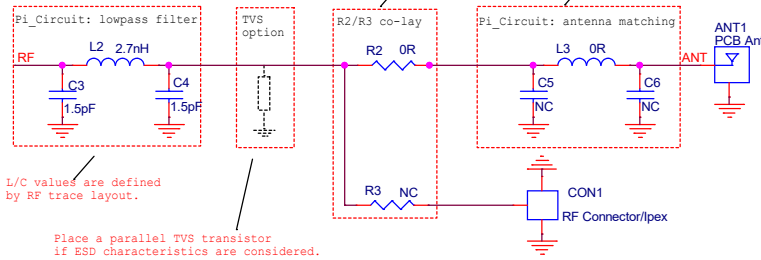
Module Pins

GPIO PINMUX: LogUart: PB15/PA8
UART1 TX/RX
JTAG: PA13/PA14/PA15/PB3/PB4
JTMS/JCLK/JTDI/JTDO/JNRST
BOOT: PC8/PA14
BOOT0/BOOT1
J1 Module_50pin

PCB ANTENNA

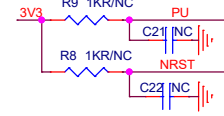


RF TRACE

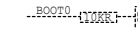


Latch-up pins

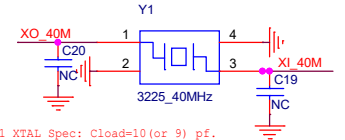
1 PU&NRST need to be pull-up on Module or MotherBoard (R9&R8).



2 BOOT0 pin need to be pull-down on Module or MotherBoard for the chip to boot from sip flash.



40MHz Crystal



1 XTAL Spec; Cload=10(or 9) pf.
2 C19&C20 default are "NC".

GIGA DEVICE

Title			
GD32W515_MD1_SP			
Size	Document Number	Rev	
Custom	Module	2.1	
Date:	Friday, December 15, 2023	Sheet	1 of 1