GigaDevice Semiconductor Inc.

GD32H73x_75x Hardware Development Guide

Application Note
AN109

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1. Introduction

The article is specially provided for developers of 32-bit general-purpose MCU GD32H73x_75x series based on Arm® Cortex®-M7 architecture. It provides an overall introduction to the hardware development of GD32H73x_75x series products, such as power supply, reset, clock, boot mode settings and download debugging. The purpose of this application notes is to allow developers to quickly get started and use GD32H73x_75x series products, and quickly develop and use product hardware, save the time of studying manuals, and speed up product development progress.

This application note is divided into seven parts to describe:

1. Power supply, mainly introduces the design of GD32H73x_75x series power management, power supply and reset functions.
2. Clock, mainly introduces the functional design of GD32H73x_75x series high and low speed clocks.
3. Boot configuration, mainly introduces the BOOT configuration and design of GD32H73x_75x series.
4. Typical peripheral modules, mainly introduces the hardware design of the main functional modules of the GD32H73x_75x series.
5. Download and debug circuit, mainly introduces the recommended typical download and debug circuit of GD32H73x_75x series.
6. Reference circuit and PCB Layout design, mainly introduces GD32H73x_75x series hardware circuit design and PCB Layout design notes.
7. Package description, mainly introduces the package forms and names included in the GD32H73x_75x series.

This document also satisfies the minimum system hardware resources used in application development based on GD32H73x_75x series products.

Table 1-1. Applicable Products

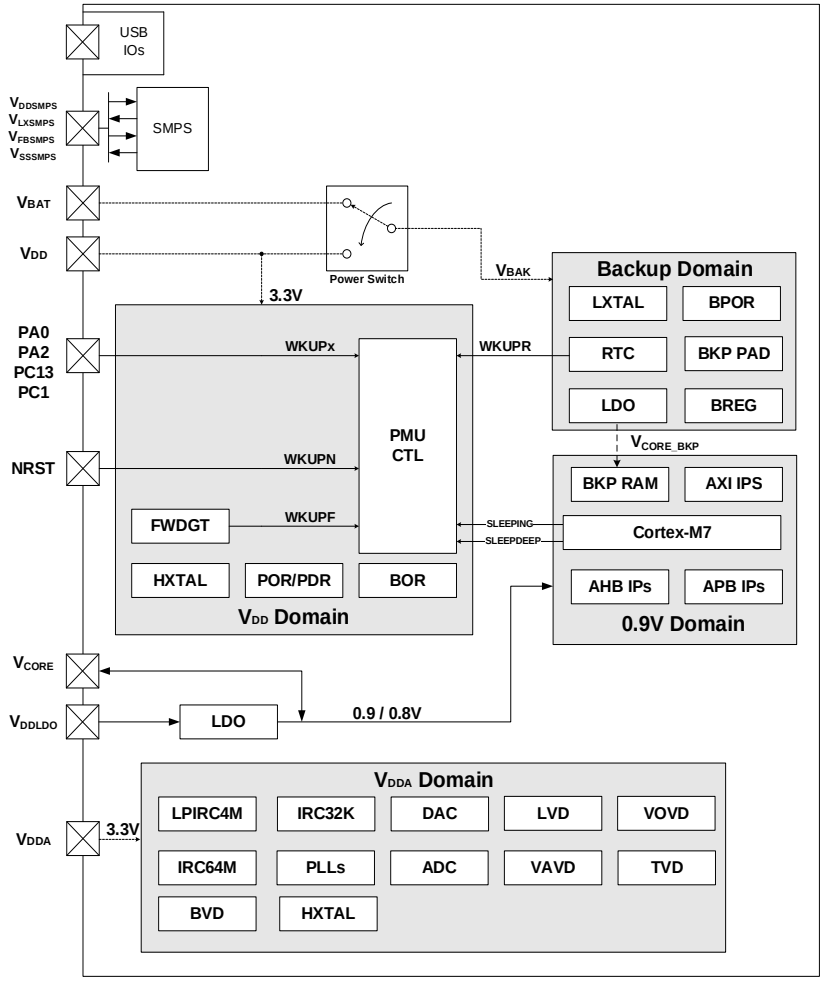
Type	Part Numbers
MCU	GD32H737xx series
	GD32H757xx series
	GD32H759xx series

2. Hardware design

2.1. Power supply

The V_{DD} / V_{DDA} operating voltage range of GD32H73x_75x series products is 1.71 V ~ 3.6 V. As shown in ***Figure 2-1. GD32H73x_75x series Power supply overview***, the GD32H73x_75x series device has three power domains, including the V_{DD} / V_{DDA} domain, 0.9V domain and backup domain. The V_{DD} / V_{DDA} domain is directly powered by the power supply. The GD32H73x_75x series is embedded with LDO and low-power switching power supply voltage regulator (SMPS voltage regulator) to supply power to the 0.9V domain. There is a power switch in the backup domain. When the V_{DD} power is turned off, the power switch can switch the power of the backup domain to the V_{BAT} pin. At this time, the backup domain is powered by the V_{BAT} pin (battery). The USB part has dedicated external power supply pins and voltage regulators, which can input 5 V power supply or 3.3 V power supply.

Figure 2-1. GD32H73x_75x series Power supply overview



LVD: Low Voltage Detector
LDO: Voltage Regulator
BPOR: V_{BAK} Power On Reset
POR: Power On Reset
PDR: Power Down Reset
BREG: Backup registers
VOVD: $V_{0.9V}$ Voltage Detector
VAVD: V_{DDA} Voltage Detector
TVD: Temperature voltage Detector
BVD: V_{BAK} Voltage Detector
BOR: Brownout Reset

2.1.1. Backup domain

The power supply voltage range of the backup domain is 1.71 V to 3.6 V. The internal power switch selects V_{DD} power supply or V_{BAT} (battery) power supply, and then V_{BAK} powers the backup domain. The backup domain includes RTC (real-time clock), LXTAL (low-speed external crystal oscillator), BPOR (backup domain power on reset), BREG, and a total of three BKP PAD from PC13 to PC15. To ensure the contents of the registers in the backup domain and the normal operation of the RTC, the V_{BAT} pin can be connected to the battery or other backup power supply when the V_{DD} is turned off. The power switch is controlled by the V_{DD} / V_{DDA} domain power-off reset circuit. For applications without external batteries, it is recommended to connect the V_{BAT} pin to the V_{DD} pin through a 100nF capacitor to ground.

The reset source of the backup domain includes power on reset and software reset of the backup domain. Before V_{BAK} is fully powered on, the BPOR signal forces the device to be in a reset state. The application software can be configured by setting the RCU_ The BDCTL register BKPRST bit triggers a backup domain software reset.

The clock source of RTC can be a low-speed internal 32kHz RC oscillator (IRC32K) or a low-speed external crystal oscillator (LXTAL), or a high-speed external crystal oscillator (HXTAL) clock divider controlled by the RTCDIV[5:0] (located in the RCU_CFG0 register) bit domain. When V_{DD} is turned off, RTC can only select LXTAL as the clock source. Before entering power-saving mode through WFI / WFE commands, Cortex®-M7 can achieve RTC timer wake-up events by setting the expected wake-up time in the RTC register and enabling wake-up function or based on EXTI. After entering the power saving mode for a certain period of time, when the elapsed time matches the preset wake-up time, the RTC will wake up the device.

When the backup domain is powered by V_{DD} (V_{BAK} connected to V_{DD}), the following functions are available:

- PC13 can be used as a universal I/O port or RTC function pin;
- PC14 and PC15 can be used as general-purpose I/O ports or LXTAL crystal oscillator pins.

When the backup domain is powered by V_{BAT} power (V_{BAK} connected to V_{BAT}), the following functions are available:

- PC13 can only be used as an RTC function pin;
- PC14 and PC15 can only be used as LXTAL crystal oscillator pins.

Note:

1. Since the PC13 to PC15 pins are powered through a power switch, which can only provide a small current, when the GPIO ports of PC13 to PC15 are in output mode, their operating speed must not exceed 2MHz (with a maximum load of 30pF).
2. The backup domain LDO can generate the V_{CORE_BKP} Voltage. When the V_{DD} / V_{DDA} is powered on, the BKP RAM in the 0.9V power domain is powered by V_{CORE}; when V_{DD} / V_{DDA} is powered off, the BKP RAM in the 0.9V power domain is powered by V_{CORE_BKP}.

V_{DD} can charge external batteries through an internal resistor. By configuring the VCRSEL bit in the PMU_CTL2 register, an internal resistance of 5K ohms or 1.5K ohms can be selected for external VBAT battery charging. Setting VCEN to 1 in the PMU_CTL2 register enables VBAT battery charging. In BKP only mode, V_{BAT} battery charging is not available.

Note: In BKP only mode, the V_{DD} loses power and the backup domain is powered by the V_{BAT} pin.

2.1.2. V_{DD} / V_{DDA} domain

The V_{DD} / V_{DDA} power domain includes two parts: V_{DD} domain and V_{DDA} domain. If V_{DDA} is not equal to V_{DD}, the voltage difference between the two should not exceed 300mV (the internal V_{DDA} and V_{DD} of the chip are connected through a back-to-back diode). To avoid noise, V_{DDA} can be connected to V_{DD} through an external filter circuit, and the corresponding V_{SSA} is connected to V_{SS} through a specific circuit (single-point grounding, through 0Ω resistors or magnetic beads, etc.).

In order to improve the conversion accuracy of the ADC, the independent power supply for V_{DDA} can make the analog circuit achieve better characteristics. GD32H73x_75x is internally integrated with V_{REFP} pin specially designed for independent power supply of ADC (External power supply: Using 12bit ADC, 1.71 V ≤ V_{REFP} ≤ V_{DDA}. Using 14bit ADC, when V_{DDA} ≥ 2.4 V, 2.4 V ≤ V_{REFP} ≤ V_{DDA}; when V_{DDA} < 2.4 V, 1.8 V ≤ V_{REFP} ≤ V_{DDA}).

- The BGA176 package contains V_{REFP} and V_{REFN}, V_{REFP} can use an external reference power supply or be directly connected to V_{DDA}. V_{REFN} must be connected to V_{SSA}.
- The LQFP package contains V_{REFP}, which can use an external reference power supply or be directly connected to V_{DDA}.
- The VREFP pin is connected to the VDDA pin through an internal diode. When V_{REFP} ≥ V_{DDA} + 0.3V, there will be leakage to the VDDA pin.
- The GD32H73x_75x series has a VREFBUF, which can generate four reference voltage levels ranging from 1.5V to 2.5V when the VREFP pin is not connected to an external reference power source. For details, please refer to the user guide and datasheet.

2.1.3. 0.9V domain

By using the SMPS voltage regulator and LDO, the power supply for the 0.9V power domain can be configured. Different configurations can provide four effective 0.9V power domain supply modes. The modes correspondence table is shown in ***Table 2-1. Power Supply Modes Correspondence Table***.

Table 2-1. Power Supply Modes Correspondence Table

Power supply mode
Unconfigured power supply mode (default power supply mode)
LDO power supply mode
SMPS power supply mode
Bypass mode

■ Unconfigured power supply mode (default power supply mode)

Unconfigured power supply mode is the initial transition mode. After the chip reset, if the software does not set any power mode, the chip will remain in this mode. At this time, all registers are at their reset values, and both SMPS and LDO are enabled. During this phase, if the hardware is set as follows, the following situations may occur:

1. When the hardware is set to LDO power supply mode, the LDO outputs 0.9V to power the $V_{0.9V}$ domain. This state is the same as the LDO power supply mode.
2. When the hardware is set to SMPS power supply mode, the SMPS outputs 1V to VCORE. However, the LDO is also enabled, and VDDLDO is shorted to VCORE, resulting in fluctuations in the VCORE voltage. Therefore, the software should configure the system to SMPS power supply mode after reset to ensure system reliability.
3. In BGA176 and LQFP176 packages, if the hardware is set to bypass mode, the LDO is enabled but forced to bypass by hardware, and the power is sourced from an external input, which may pose unknown risks. In LQFP144, LQFP100, and BGA100 packages, since the internal LDO input is connected to VDD by default, it will cause the internal LDO to output 0.9V, while the external power source also has an output, leading to voltage competition and potential risks. In summary, in this case, the software should immediately configure to bypass mode after reset to ensure safety.

In summary, this mode is the initial transition state during chip startup. Long-term use may pose unpredictable risks, so the software and hardware should be configured to other modes during normal chip operation.

The default state of the register is shown in ***Table 2-2. Default power supply mode register initial state***:

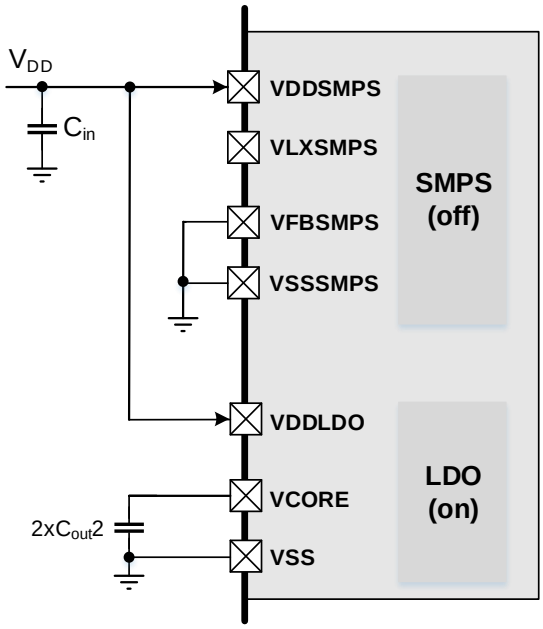
Table 2-2. Default power supply mode register initial state

Symbol	Description
DVSEN	1：SMPS enable
LDOEN	1：LDO enable
LDOVS[2:0]	010：LDO output 0.9V
BYPASS	0：BYPASS disable

■ LDO power supply mode

In this mode, the SMPS is turned off, and the LDO is turned on to supply power to the V0.9V domain. For the specific circuit, refer to ***Figure 2-2. The LDO power supply 0.9V power domain*** (when the SMPS module is off, the VDDSMPS pin must be connected to V_{DD} or V_{SS}). Using the internal LDO power supply can provide a stable power source for the system.

Figure 2-2. The LDO power supply 0.9V power domain



The configuration method for entering this power supply mode is as follows: the DVSEN bit is 0b0, the values of the DVSCFG and DVSVC[1:0] bit fields have no effect, and the SMPS step-down regulator is turned off; the LDOEN bit is 0b1, the LDO is in the on state and supplies power to the 0.9V power domain, with the supply voltage controlled by the LDOVS[2:0] bit field, and the operating mode of the LDO is consistent with the system's low-power mode; the BYPASS bit is 0b0. The register configuration for the SMPS and LDO output voltage is shown in ***Table 2-3. LDO Supply Register Configuration Table***:

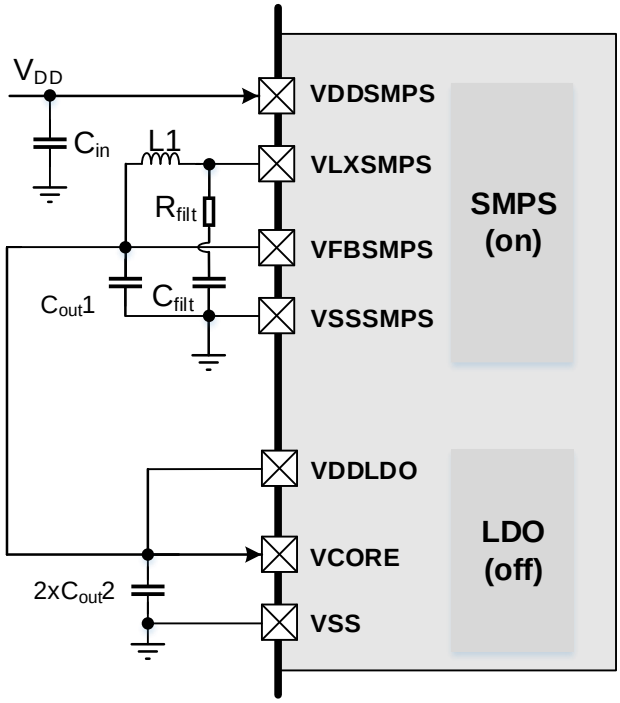
Table 2-3. LDO Supply Register Configuration Table

Symbol	Description
DVSEN	0：SMPS disable
LDOEN	1：LDO enable
LDOVS[2:0]	010：LDO output 0.9V
BYPASS	0：BYPASS disable

- SMPS power supply mode

In this mode, the SMPS is turned on and directly supplies power to the $V_{0.9V}$ domain, while the LDO is turned off. For the specific circuit, refer to ***Figure 2-3. The SMPS power supply 0.9V power domain***. Using SMPS power supply can effectively reduce chip heat and operational power consumption.

Figure 2-3. The SMPS power supply 0.9V power domain



The configuration method for entering this power supply mode is as follows: the DVSEN bit is 0b1, the DVSCFG bit is 0b1, the values of the DVSVC[1:0] bit field have no effect, the SMPS step-down regulator is turned on and supplies power to the 0.9V power domain, with the supply voltage controlled by the LDOVS[2:0] bit field, and the operating mode of the SMPS is consistent with the system's low-power mode; the LDOEN bit is 0b0, so the LDO is turned off; the BYPASS bit is 0b0. The register configuration for the SMPS and LDO output voltage is shown in ***Table 2-4. SMPS Supply Register Configuration Table***:

Table 2-4. SMPS Supply Register Configuration Table

Symbol	Description
DVSEN	1：SMPS enable
LDOEN	0：LDO disable
LDOVS[2:0]	010：SMPS output 0.9V
BYPASS	0：BYPASS disable

- Bypass mode

In this mode, the SMPS is turned off, and the LDO is turned off. The external circuit supplies power to the $V_{0.9V}$ domain through the VCORE pin. In the H7 series, the relevant SMPS pins may differ depending on the package. The BGA176 and LQFP176 packages include the SMPS module, with both the SMPS-related pins and VDDLDO pin exposed on the package; however, the LQFP144, LQFP100, and BGA100 packages do not include the SMPS module, and thus do not have relevant pins on the package. Therefore, the circuit connection in bypass mode is slightly different. For specific circuits, refer to ***Figure 2-4. Bypass mode (Include SMPS module)*** and ***Figure 2-5. Bypass mode (Does not include SMPS module)*** (when the SMPS module is off, the VDDSMPS pin must be connected to V_{DD} or V_{SS}).

Figure 2-4. Bypass mode (Include SMPS module)

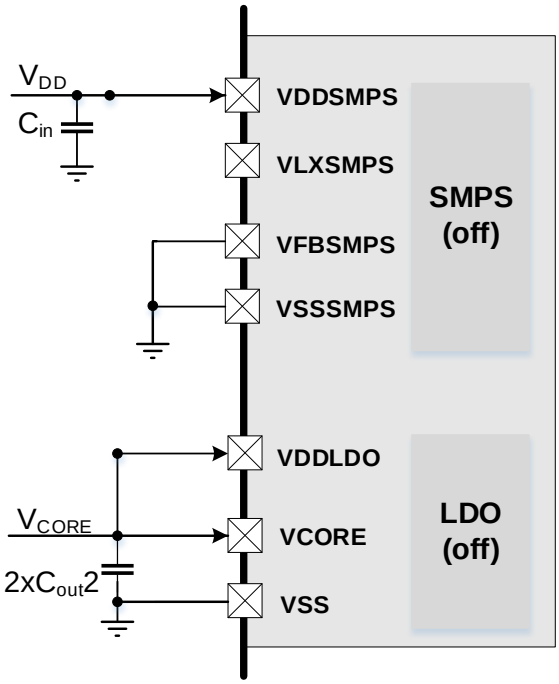
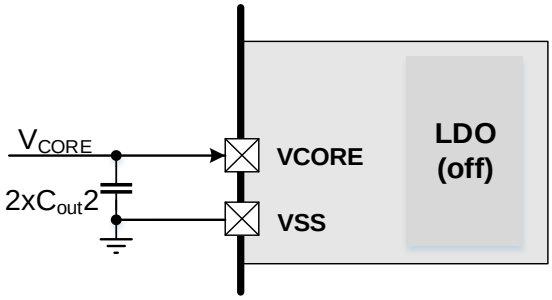
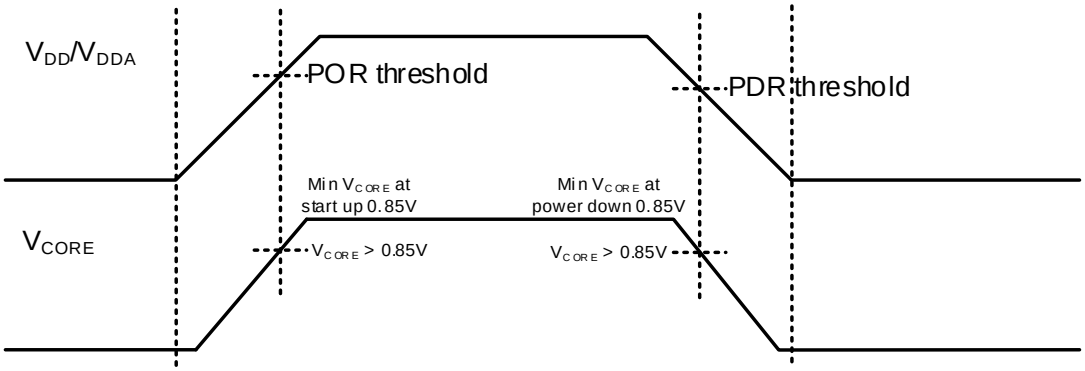


Figure 2-5. Bypass mode (Does not include SMPS module)



The power-up sequence diagram for the bypass mode is shown in ***Figure 2-6. Bypass Mode Power-Up and Power-Down Timing Diagram***. Before the MCU's V_{DD} / V_{DDA} voltage rises to the POR threshold, ensure that the V_{CORE} voltage is greater than 0.85V. Before the MCU's V_{DD} / V_{DDA} voltage falls to the PDR threshold, ensure that the V_{CORE} voltage is greater than 0.85V. Additionally, under any operating conditions, it is necessary to ensure that the V_{DD} / V_{DDA} voltage is greater than the V_{CORE} voltage.

Figure 2-6. Bypass Mode Power-Up and Power-Down Timing Diagram



The configuration method for entering this power supply mode is as follows: the DVSEN bit is 0b0, the values of the DVSCFG and DVSVC[1:0] have no effect, the SMPS step-down regulator is turned off; the LDOEN bit is 0b0, so the LDO is turned off; the BYPASS bit is 0b1, meaning the 0.9V power domain is powered through the VCORE pin. The register configuration for the SMPS and LDO output voltage is shown in ***Table 2-5. Bypass mode Register Configuration Table***:

Table 2-5. Bypass mode Register Configuration Table

Symbol	Description
DVSEN	0：SMPS disable
LDOEN	0：LDO disable
BYPASS	1：BYPASS enable

Note:

1. In bypass mode, when the external device outputs voltage to VCORE, ensure that its typical value is 0.9V, with a voltage range within 0.873V to 0.955V. Even in harsh application scenarios, ensure that the power fluctuation range is within 50mV.
2. Operating in bypass mode will cause relatively large current to flow into the $V_{0.9V}$ power domain from the external device through the VCORE pin (simulation and test results show this current can reach up to 400mA). Therefore, there are higher requirements for the external power supply devices. We recommend that the load capacity of the external device be greater than 600mA and the output voltage fluctuation range under different loads meets the aforementioned 50mV requirement. Considering power stability requirements, it is recommended to use an external LDO for power supply in bypass mode.
3. Considering the ESR effect and IR drop of large current on PCB traces, when routing the PCB, it is necessary to consider widening the trace width from the external power supply to the VCORE pin to reduce ESR and ensure that the voltage at the chip's VCORE pin meets the amplitude and fluctuation requirements.
4. It is recommended that multiple VCORE pins on the package be connected together externally through routing. Concerning decoupling and filter capacitors at the VCORE pin, when operating in bypass mode, it is recommended to place a 100nF capacitor near each VCORE pin. If there is a third VCORE pin on the package, it only needs to be connected to the other two VCORE pins without adding additional capacitors.
5. When using bypass mode to enter standby mode, first enter standby mode and then turn off the external V_{CORE} power; the external V_{CORE} power must be turned off. When exiting standby mode, first turn on the external V_{CORE} power and then exit standby mode.

Note: Except for the valid combinations mentioned above, all other configuration combinations of DVSEN, DVSCFG, DVSVC[1:0], LDOEN, BYPASS bits or bit values are invalid. The power state of the 0.9V power domain remains unchanged after reset (no configured power mode).

Note: When the SMPS voltage regulator supplies power to the 0.9V power domain and the DVSVC[1:0] is configured with an incorrect value, it will cause the SMPS voltage regulator to output high voltage to the 0.9V power domain. At this time, the 0.9V power domain will activate

hardware overvoltage protection, and the hardware will be set to DVSVC[1:0] 0b00.

Note: The maximum operating frequency is related to the power supply voltage, please refer to the data manual for details.

2.1.4. USB Power supply

The GD32H73x_75x series USB integrates a voltage regulator internally, which users can choose to enable. Connect the VDD50USB pin to a 5 V power supply to provide power for the USB module, as shown in ***Figure 2-7. Connection diagram of USB voltage regulator during power supply***; Alternatively, bypass the voltage regulator and connect the VDD33USB pin to a 3.3 V power supply to provide power to the USB module, as shown in ***Figure 2-8. Connection diagram for USB voltage regulator bypass***.

Figure 2-7. Connection diagram of USB voltage regulator during power supply

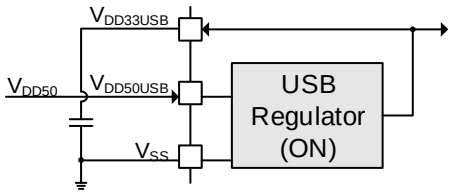
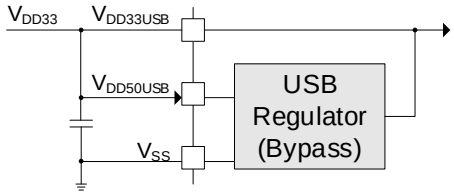


Figure 2-8. Connection diagram for USB voltage regulator bypass



Note:

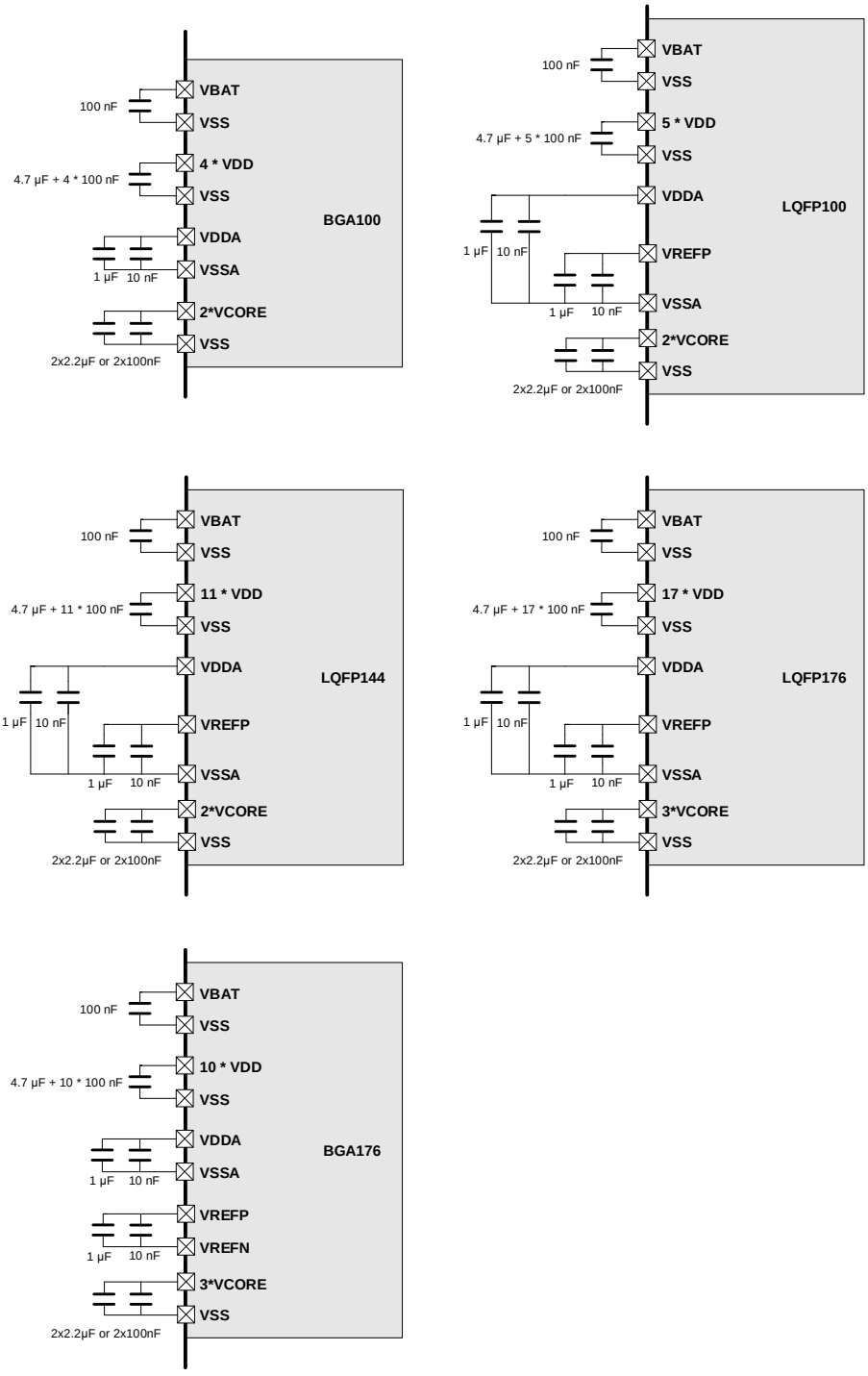
1. When VDD ≥ 3V, the USB power can use the USB regulator power supply mode or bypass mode; when VDD < 3V, the USB power can only use the USB regulator power supply mode.
2. When using the ISP download function, one of the two USB power supply methods mentioned above must be used to supply power to $V_{DD33USB}$.

2.1.5. Power supply design

The system needs a stable power supply. There are some important things to pay attention to when developing and using:

- The VDD pin must be connected with an external capacitor (N*100nF ceramic capacitor + not less than 4.7uF tantalum capacitor, at least one V_{DD} needs to be connected to GND with a capacitor of not less than 4.7uF, and other VDD pins are connected to 100nF).
- The VDDA pin must be connected with an external capacitor (10nF + 1uF ceramic capacitor is recommended).
- The V_{REF} voltage can be generated internally or directly connected to V_{DDA}, and a 10nF + 1uF ceramic capacitor should be connected between the VREFP pin and ground.

Figure 2-9. GD32H73x_75x Recommended Power Supply Design



Note:

1. All decoupling capacitors must be placed close to the corresponding VDD, VDDA, VBAT, VREFP, VCORE pins of the chip.
2. Regardless of whether LDO is enabled or not, all VCORE of the chip should be connected together.
3. When LDO is enabled, it is recommended that VCORE connect two 2.2uF ceramic capacitors to GND; When bypassing LDO, it is recommended that VCORE connect two 100nF ceramic capacitors to GND.

4. When the MCU power supply voltage is unstable or there is a risk of voltage drop, it is recommended to adjust the 4.7uF capacitor not less than 10uF.
5. BGA100: VREFP and VDDA are connected internally, VREFN and VSSA are connected internally.
6. LQFP100: VREFN and VSSA are connected internally.
7. LQFP144: VREFN and VSSA are connected internally.
8. LQFP176: VREFN and VSSA are connected internally.

The recommended design of the SMPS circuit is shown in ***Figure 2-10. GD32H73x_75x Recommended SMPS circuit Design***, and the typical value of the device are shown in ***Table 2-6. Characteristics of SMPS step-down converter external components***.

Figure 2-10. GD32H73x_75x Recommended SMPS circuit Design

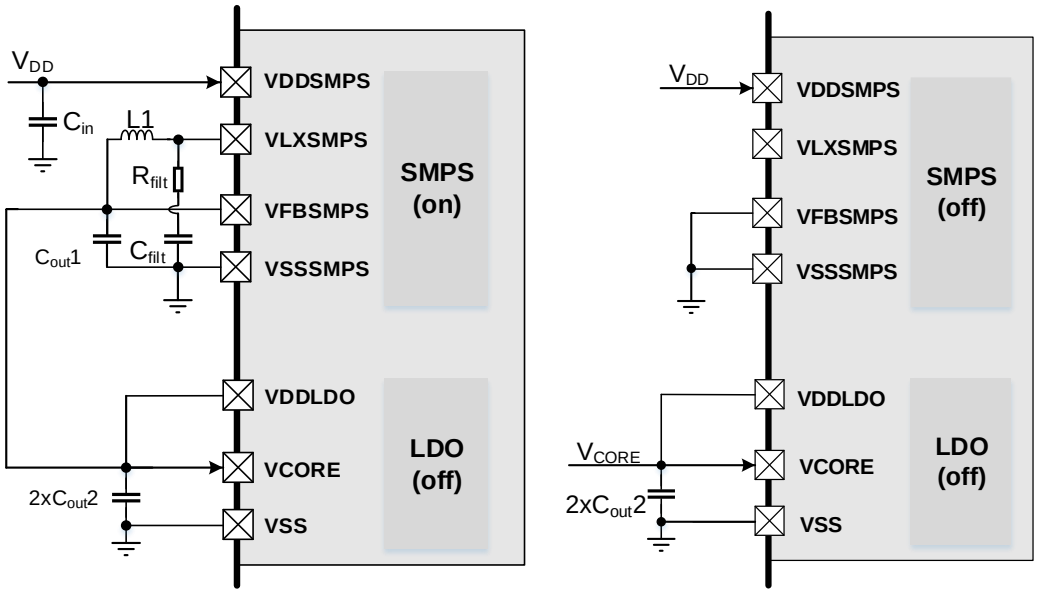


Table 2-6. Characteristics of SMPS step-down converter external components

Symbol	Parameter	Conditions	Package
C_{in}	Capacitance of external capacitor on VDDSMPS	10uF	0805
C_{filt}	Capacitance of external capacitor on VLXSMPS	220pF	0603
R_{filt}	Resistor of external capacitor on VLXSMPS	50Ω	0603
C_{OUT1}	Capacitance of external capacitor on VFBSMPS	10uF	0805
C_{OUT2}	Capacitance of external capacitor on VCORE	100nF / 2.2uF	0603 / 0805
L	Inductance of external Inductor on VLXSMPS	2.2uH	0806

2.2. Reset And Power Management

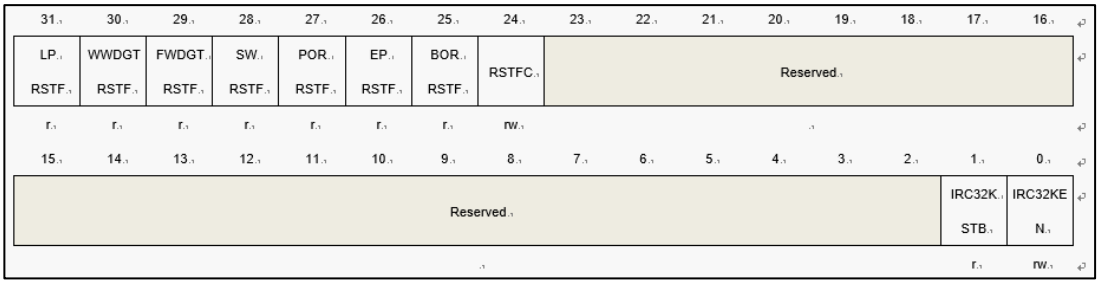
In this section, the default is that the VDD and VDDA pins remain connected and are powered by the same power source.

GD32H73x_75x series reset control includes three resets: power reset, system reset and backup domain reset. A power reset is a cold reset, which resets all systems except the

backup domain when the power is turned on.

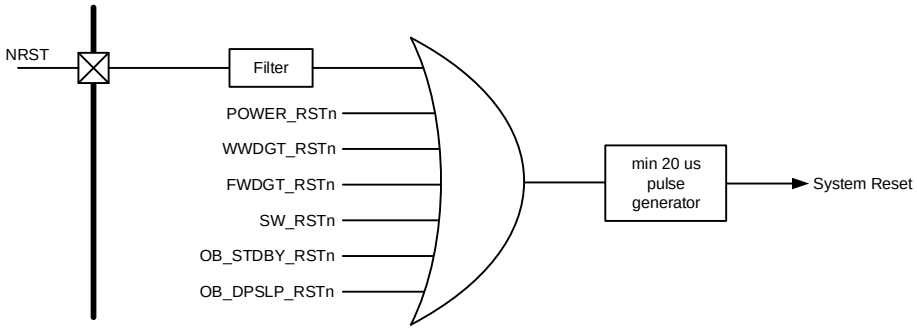
The MCU reset source can be searched by the register RCU_RSTSCK (0x40021024). This register can only clear the flag bit after power-on reset. Therefore, during use, after the reset source is obtained, the reset flag can be cleared through the RSTFC control bit, so that a watchdog reset or other reset events can be more accurately reflected in the RCU_RSTSCK register:

Figure 2-11. RCU_RSTSCK Register



MCU integrates a power-up / power-down reset circuit, when a reset occurs, the system reset pulse generator ensures that each reset source (external or internal) can have a low level pulse delay of at least 20μs.

Figure 2-12. System Reset Circuit

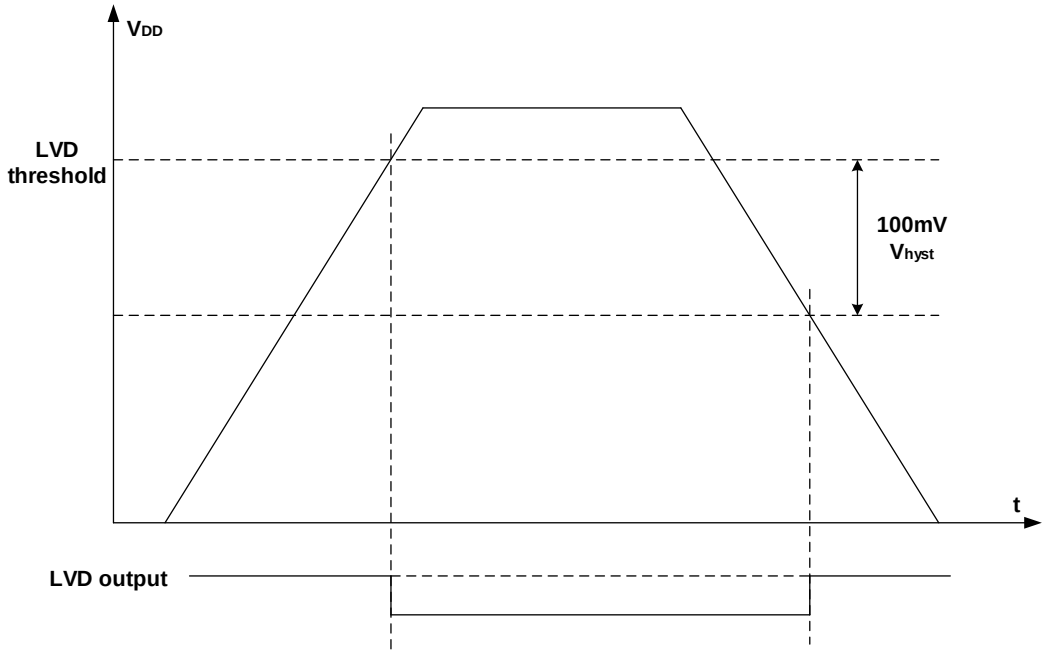


2.2.1. LVD

The function of LVD is to detect whether the V_{DD} supply voltage is lower than the low voltage detection threshold, which is configured by the LVDT[2:0] bit in the power control register 0 (PMU_CTL0). LVD is enabled by LVDEN setting. The LVDF bit in the power supply status register (PMU_CS) indicates whether a low voltage event occurs. This event is connected to the 16th line of EXTI. The user can generate a corresponding interrupt by configuring the 16th line of EXTI. ***Figure 2-13. Waveform of the LVD*** shows the relationship between V_{DD} supply voltage and LVD output signal. (LVD interrupt signal depends on the rising or falling edge configuration of EXTI line 16). The hysteresis voltage (V_{hyst}) is 100 mV.

LVD Application Scenario: When the MCU power supply is subject to external interference, such as a voltage drop, we can set a low voltage detection threshold with LVD (this threshold is greater than the PDR value). Once the voltage drops to this threshold, the LVD interrupt is triggered. In the interrupt function, operations such as a software reset can be set to prevent other anomalies from occurring in the MCU.

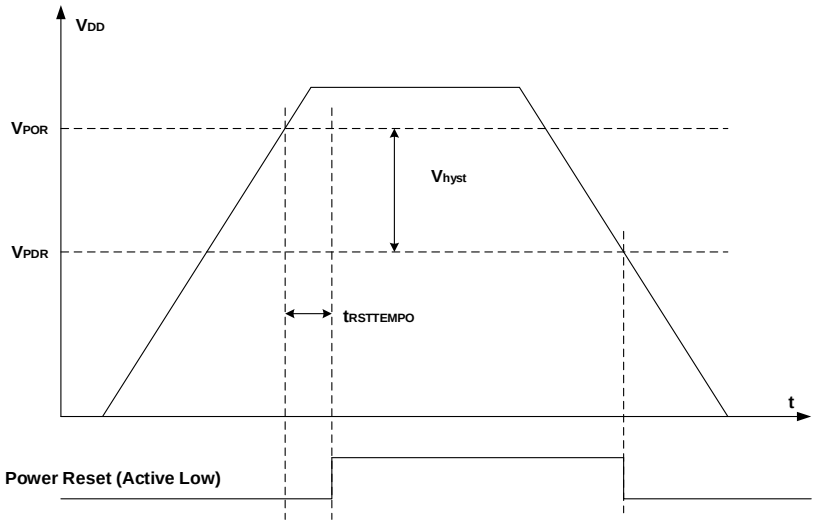
Figure 2-13. Waveform of the LVD



2.2.2. POR / PDR

The POR / PDR circuit monitors V_{DD} and generates a power reset signal to reset the entire chip except for the backup domain when the voltage falls below a specific threshold. ***Figure 2-14. Waveform of the POR / PDR*** shows the relationship between the power reset and V_{DD} when BOR is disabled. When BOR is enabled, the effect of BOR on the power reset level needs to be considered. Information related to BOR will be introduced in the next subsection. V_{POR} indicates the threshold voltage for power-on reset, while V_{PDR} indicates the threshold voltage for power-down reset. The hysteresis voltage Vhyst is approximately 50mV.

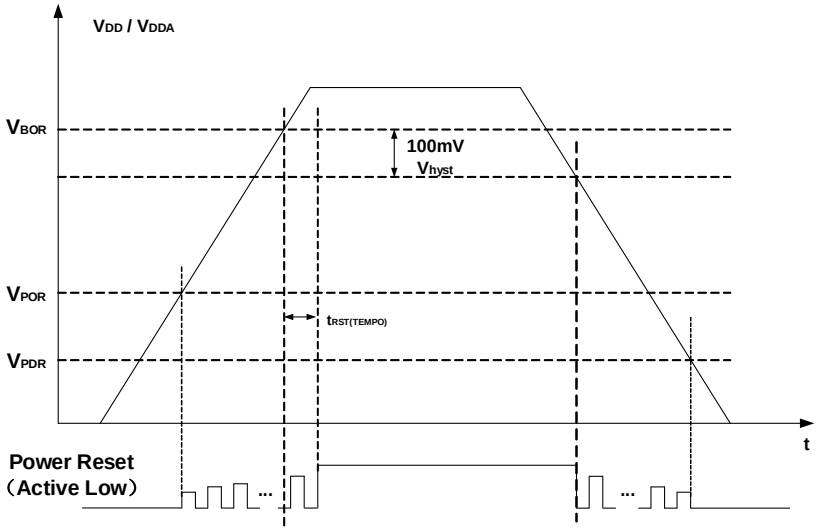
Figure 2-14. Waveform of the POR / PDR



2.2.3. BOR

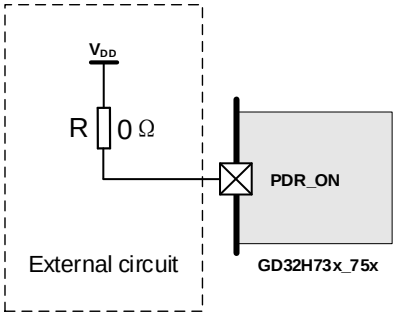
The BOR circuit monitors V_{DD} and generates a power reset signal to reset the entire chip, except for the backup domain, when BOR_TH is not 0b11 and the voltage falls below the threshold defined by the BOR_TH option byte. Regardless of whether BOR is enabled, the POR / PDR circuit is always in detection mode. Therefore, the power reset level will be pulled high when V_{DD} rises to V_{POR}, regardless of whether BOR is enabled. When BOR is enabled, it will quickly pull the elevated power reset level low. The POR / PDR circuit, upon detecting V_{DD} > V_{POR}, will pull the power reset level high again, and BOR will pull it low. This cycle continues, forming a square wave on the NRST pin. Only after the V_{DD} / V_{DDA} voltage exceeds V_{BOR} will BOR no longer pull the power reset level low, and the power reset will remain high. A square wave will only appear when V_{DD} / V_{DDA} voltage is greater than V_{POR} and less than V_{BOR}. ***Figure 2-15. Waveform of the BOR*** shows the relationship between the supply voltage and the BOR reset signal. V_{BOR} indicates the threshold voltage for BOR reset, which is defined in the option byte BOR_TH. The hysteresis voltage Vhyst is 100mV..

Figure 2-15. Waveform of the BOR



The internal power monitor of the GD32H73x_75x series can be enabled or disabled through the PDR_ON pin. To ensure the chip operates normally and to improve anti-interference capability, as well as to generate effective reset signals during power-up / power-down stages, the recommended circuit for PDR_ON is shown in ***Figure 2-16. Recommended PDR_ON Pin Circuit Design***.

Figure 2-16. Recommended PDR_ON Pin Circuit Design



Note： The PDR_ON pin must be kept at high level. The user can flexibly adjust the value of the pull-up resistor R according to the specific scenario for a better performance.

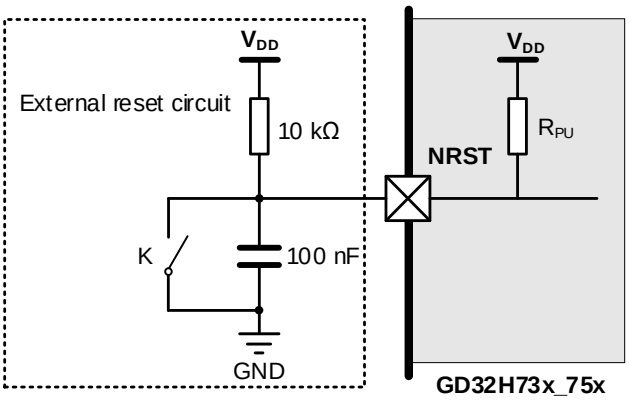
When PDR_ON is connected to GND, the following functions will be disabled:

1. Internal Power On Reset(POR) / Pwer Down Reset(PDR) disabled.
2. Internal Brown Out Reset(BOR) disabled.
3. Internal Low Voltage Detection(LVD) disabled.
4. V_{BAT} function disabled, VBAT pin should be connected to V_{DD}.

2.2.4. NRST Pin

For the MCU's NRST pin, to prevent false reset triggering, it is recommended to place a capacitor (typical value of 100nF) on the NRST pin.

Figure 2-17. Recommend External Reset Circuit



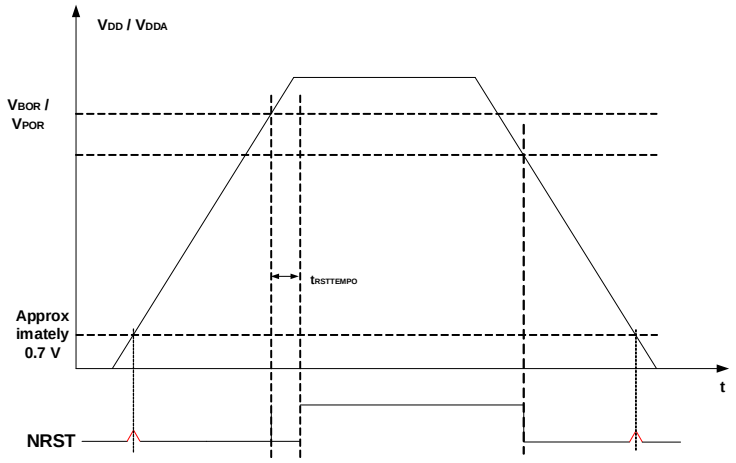
Note:

1. Internal pull-up resistance R_{PU} = 40 kΩ. You are advised to use an external pull-up resistance of 10 kΩ to ensure that voltage interference does not cause chip abnormalities
2. If the influence of static electricity is considered, an ESD protection diode can be placed at the NRST pin.
3. Although there is a hardware POR circuit inside the MCU, it is still recommended to add an external NRST reset resistor-capacitor circuit.
4. If the MCU starts abnormally (due to voltage fluctuations, etc.), the capacitance value of NRST to ground can be appropriately increased, and the MCU reset completion time can be extended to avoid the abnormal power-on sequence area.

Due to the threshold voltage characteristics of the MOS transistor, during the power-up and power-down process of the chip, when VDD / VDDA < 0.7 V, the internal pull-down MOS transistor of the chip will not pull down the NRST pin. Therefore, during the power-up and power-down process, when VDD / VDDA ≈ 0.7 V, a small pulse occurs, which does not affect the normal operation of the chip, as shown by the red pulse in ***Figure 2-18. The illustration of the pulse of the NRST pin power-up/down MOS transistor***.

Figure 2-18. The illustration of the pulse of the NRST pin power-up/down MOS

transistor



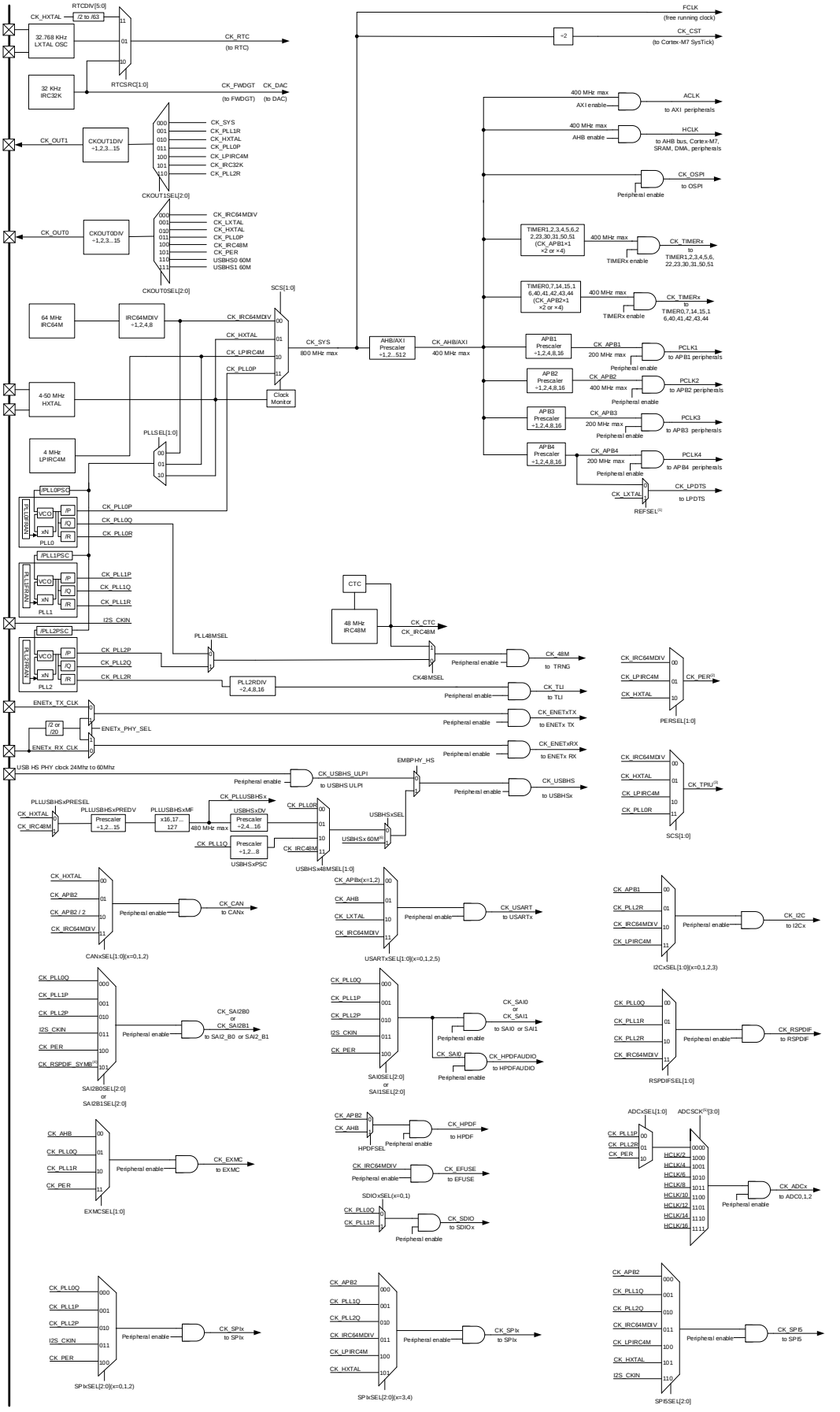
Due to the difference in charge and discharge speeds, the duration of the pulse on the falling edge is slightly longer than that on the rising edge, both of which are at the millisecond level.

2.3. Clock

GD32H73x_75x series has a complete clock system inside, and you can choose a suitable clock source according to different applications. The main features of the clock:

- 4 - 50 MHz external high-speed crystal oscillator (HXTAL)
- Internal 64 MHz RC oscillator (IRC64M)
- Internal 48 MHz RC oscillator (IRC48M)
- 32.768 kHz external low-speed crystal oscillator (LXTAL)
- Internal 32 kHz RC oscillator (IRC32K)
- Low power internal 4M RC oscillator (LPIRC4M)
- PLL clock source can be selected from HXTAL, LPIRC4M or IRC64M
- PLLs support integer and decimal multiplication factors
- The decimal frequency factor of PLLs can be modified at runtime
- The peripheral clock supports dynamic switching
- HXTAL clock monitor
- LXTAL clock monitor

Figure 2-19. GD32H73x_75x Clock Tree



Note:

1. REFSEL is the LPDTS reference clock selection bit, which can be selected as CK_PCLK4 or CK_LXTAL.
2. CK_PER is a peripheral clock, which can be a CK_LPIRC64MDIV，CK_LPIRC4M or CK_HXTAL.
3. CK_TPIU is the tracking port interface unit (TPIU) clock, which can be a CK_IRC64MDIV, CK_LPIRC4M，CK_HXTAL or CK_PLL0R.
4. CK_RSPDIF_SYMB is the RSPDIF symbol clock.
5. ADCSCK selects the bit for ADC synchronous clock.
6. USBHSx 60M is the internal PHY 60M input clock source of USBHSx.

2.3.1. External high-speed crystal oscillator clock (HXTAL)

An external high-speed crystal oscillator with a frequency range of 4 - 50MHz can provide a more accurate clock source for the system clock. Crystals with specific frequencies must be connected to the pins near the two HXTAL. The external resistance and capacitance connected to the crystal must be adjusted according to the selected oscillator.

Figure 2-20. HXTAL External Crystal Circuit

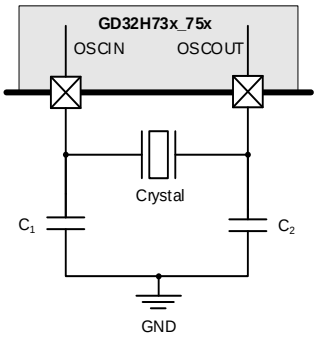
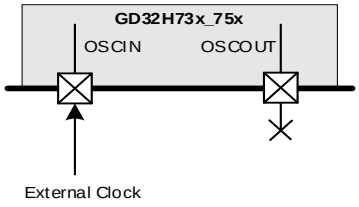


Figure 2-21. HXTAL External Clock Circuit



Note:

1. When using the bypass input, the signal is input from OSCIN, and OSCOUT remains floating.
2. For the size of the external matching capacitor, please refer to the formula: $C_1 = C_2 = 2*(C_{LOAD} - C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, with a typical value of 10pF. When it is recommended to use an external high-speed crystal, try to choose a crystal load capacitance of about 20pF, so that the external matching capacitors C_1 and C_2 can be 20pF, and the PCB layout should be as close to the crystal

pin as possible.

3. C_S is the parasitic capacitance on the PCB board traces and MCU pins. The closer the crystal is to the MCU, the smaller the C_S, and vice versa. Therefore, in practical applications, when the crystal is far away from the MCU, causing the crystal to work abnormally, the external matching capacitor can be appropriately reduced.
4. When using an external high-speed crystal, it is recommended to connect a 1MΩ resistor in parallel at both ends of the crystal to make the crystal easier to vibrate.
5. Accuracy: external active crystal oscillator > external passive crystal > internal crystal oscillator.
6. When the active crystal oscillator is used normally, Bypass will be turned on. At this time, the high level is required to be no less than 0.7 V_{DD}, and the low level is no more than 0.3 V_{DD}.
7. The traces connecting the resonator to the MCU clock pins may cause inconsistent lengths of the traces connected to the OSCOUT and OSCIN pins due to the space constraints of the PCB layout. This will make the stray capacitances introduced by the two PCB traces inconsistent, so that the load capacitances on both sides of the resonator cannot be equal in value, and there needs to be a difference to match the actual PCB board. In this case, it is recommended to contact the resonator manufacturer to calculate the actual value.

2.3.2. External low-speed crystal oscillator clock (LXTAL)

LXTAL is an external low-speed crystal or ceramic resonator with a frequency of 32.768kHz. It provides a low-power and high-precision clock source for real-time clock circuits. The LXTAL oscillator can be turned on and off by setting the LXTALEN bit in the backup domain control register (RCU_BDCTL). The LXTALSTB bit in the backup domain control register RCU_BDCTL is used to indicate whether the LXTAL clock is stable. If the corresponding interrupt enable bit LXTALSTBIE in the interrupt register RCU_INT is set to '1', an interrupt will be generated after LXTAL stabilizes.

The external clock bypass mode can be selected by setting the LXTALBPS and LXTALEN to 1 'of the backup domain control register RCU_BDCTL. CK_LXTAL is consistent with the external clock signal connected to the OSC32IN pin.

Figure 2-22. LXTAL External Crystal Circuit

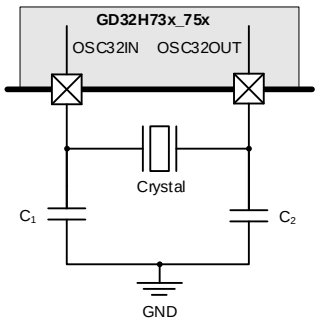
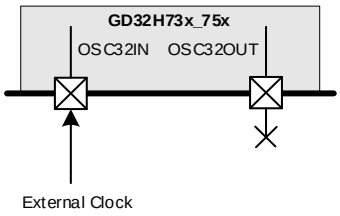


Figure 2-23. LXTAL External Clock Circuit



Note:

1. When using the bypass input, the signal is input from OSC32IN, and OSC32OUT remains floating.
2. For the size of the external matching capacitor, please refer to the formula: $C_1 = C_2 = 2*(C_{LOAD} - C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, the empirical value is between 2pF ~ 7pF, and 5pF is recommended as a reference value calculation. When it is recommended to use an external crystal, try to choose a crystal load capacitance of about 10pF, so that the externally connected matching capacitors C_1 and C_2 can be 10pF, and the PCB layout should be as close to the crystal pin as possible.
3. When the RTC selects IRC32K as the clock source and uses VBAT external independent power supply, if the MCU loses power at this time, the RTC will stop counting. After re powering on, the RTC will continue to accumulate timing based on the previous count value. If the application needs to use VBAT to power the RTC, and the RTC can still clock normally, the RTC must choose LXTAL as the clock source.
4. MCU can set the driving capacity of LXTAL. If during actual debugging, it is found that external low-speed crystals are difficult to vibrate, try adjusting the driving capacity of LXTAL to high.
5. The traces connecting the resonator to the MCU clock pins may cause inconsistent lengths of the traces connected to the OSCOUT and OSCIN pins due to the space constraints of the PCB layout. This will make the stray capacitances introduced by the two PCB traces inconsistent, so that the load capacitances on both sides of the resonator cannot be equal in value, and there needs to be a difference to match the actual PCB board. In this case, it is recommended to contact the resonator manufacturer to calculate the actual value.

2.3.3. Clock Output Capability (CKOUT)

GD32H73x_75x series can output internal related clock signals, and different clock signals can be selected by setting the CK_OUT0 clock source selection bit field CKOUT0SEL in the clock configuration register 0 (RCU_CFG2). The corresponding GPIO pin should be configured as a backup function I/O (AFIO) mode to output the selected clock signal. The selection of CK_OUT1 clock output source is achieved by setting the CKOUT1SEL bit field in the clock configuration register RCU_CFG2.

Table 2-7. Clock source selection for clock output 0

CKOUT0SEL[2:0]	Clock source
000	CK_IRC64MDIV
001	CK_LXTAL
010	CK_HXTAL
011	CK_PLL0P
100	CK_IRC48M
101	CK_PER
110	USBHS0 60M
111	USBHS1 60M

Table 2-8. Clock source selection for clock output 1

CKOUT1SEL[2:0]	Clock source
000	CK_SYS
001	CK_PLL1R
010	CK_HXTAL
011	CK_PLL0P
100	CK_LPIRC4M
101	CK_IRC32K
110	CK_PLL2R

By configuring the CKOUT0DIV bit field of the RCU_CFG2 register, the frequency of the CK_OUT0 output clock can be proportionally divided, thereby reducing the output frequency of CK_OUT0.

By configuring the CKOUT1DIV bit field of the RCU_CFG0 register, the frequency of the CK_OUT1 output clock can be proportionally divided, thereby reducing the output frequency of CK_OUT1.

2.3.4. HXTAL Clock Monitor (CKM)

Set the HXTAL clock monitoring enable bit CKMEN in the control register RCU_CTL, which enables the clock monitoring function. This function must be enabled after the delay of HXTAL start is completed, and disabled after HXTAL stop. Once an HXTAL fault is detected, HXTAL will automatically be disabled, and the HXTAL clock blocking interrupt flag bit CKMIF in the interrupt register RCU_INT will be set to '1', generating an HXTAL fault event. The interrupt caused by this fault is connected to the non maskable interrupt NMI of Cortex®-M7. If HXTAL is selected as the clock source for the system or PLL0, a HXTAL fault will prompt the selection of IRC64M as the system clock source and PLL0 will be automatically disabled. If HXTAL is selected as the clock source for PLLs, a HXTAL fault will cause the PLL to be automatically disabled.

2.3.5. LXTAL Clock Montior (LCKM)

Set the LXTAL clock monitoring enable bit LCKMEN in the clock control register RCU_BDCTL,

which enables the clock monitoring function. This function must be enabled after the LXTAL start delay is completed. The clock monitor on LXTAL operates in all modes except V_{BAT}. If a fault is detected on an external 32 kHz oscillator, an interrupt can be sent to the CPU. Then the software must disable the LCKMEN bit, stop the defective 32 kHz oscillator, and change the RTC clock source, or take any necessary measures to protect the application.

When LCKMEN is enabled, a 4-bit plus a counter will operate in the IRC32K domain. If the LXTAL clock gets stuck at 0 / 1 error or slows down by about 20KHz, the counter will overflow. LXTAL clock fault will be detected. Once an LXTAL fault is detected, the LXTAL clock blocking interrupt flag bit LCKMIF in the interrupt register RCU_INT will be set to '1', generating an LXTAL fault event. This interrupt is connected to the EXTI 18 interrupt line and can be used to wake up from sleep or deep sleep mode. LXTAL fault events can also wake up the system from standby mode.

2.4. Startup Configuration

The GD32H73x_75x series MCU provides different boot sources, which can be selected through the boot pin and boot address 0/1 [15:0] in the Arm® Cortex®-M7 core register (FMCBTADDRMDF) boot address. Details can be found in ***Table 2-9. BOOT mode selection*** and ***Table 2-10. Details of BOOT mode*** The level state of the BOOT pin will be latched on the rising edge of the fourth CKSYS (system clock) after reset. Users can choose the desired boot source by setting the pin level of the BOOT after power on reset and system reset.

The BOOT_ADDR0[15:0] and BOOT_ADDR1[15:0] addresses allow the boot memory address to be configured to any address between 0x0000 0000 and 0x9000 0000. The boot mode can be obtained from the BOOT_MODE [2:0] bit field of the SYSCFG_USERCFG0 register.

Table 2-9. BOOT mode selection

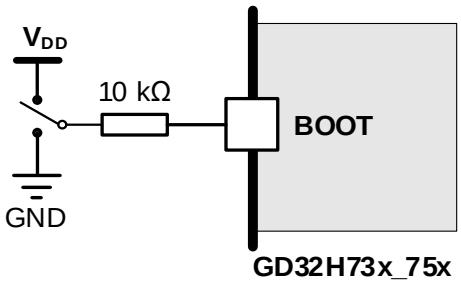
Boot source address	Boot mode selection pin
	BOOT
MSB of the boot address: defined by BOOT_ADDR0[15:0] LSB of the boot address: 0x0000	0
MSB of the boot address: defined by BOOT_ADDR1[15:0] LSB of the boot address: 0x0000	1

Table 2-10. Details of BOOT mode

SCR	SPC[7:0]	BOOT_ADDRESS (configured in BOOT_ADDRx(x = 0,1))	BOOT_MODE	Boot from
1	x	XXXX	SECURITY BOOT	ROM
0	Protection level high	0x9000_0000	USER BOOT	OSPI0
		0x7000_0000	USER BOOT	OSPI1
		0x0800_0000~max user flash	USER BOOT	BOOT_ADDRESS

SCR	SPC[7:0]	BOOT_ADDRESS (configured in BOOT_ADDRx(x = 0,1))	BOOT_MODE	Boot from
		other	USER BOOT	0x0800_0000
	No protection / Protection level low	0x9000_0000	USER BOOT	OSPI0
		0x7000_0000	USER BOOT	OSPI1
		0x2408_0000~ max RAM shared(ITCM/DTCM/AXI)	SRAM BOOT(RAM shared)	BOOT_ADDRESS
		0x2400_0000~ max AXI SRAM	SRAM BOOT(AXI SRAM)	BOOT_ADDRESS
		0x2000_0000	SRAM BOOT(DTCM)	0x2000_0000
		0x0800_0000~max user flash	USER BOOT	BOOT_ADDRESS
		0x0000_0000	SRAM BOOT(ITCM)	0x0000_0000
		0x1FF0_0000	SYSTEM BOOT	BootLoader
		Other	USER BOOT	0x0800_0000 (BOOT Pin = 0)
			SYSTEM BOOT	BootLoader (BOOT Pin = 1)

Figure 2-24. Recommend BOOT Circuit Design



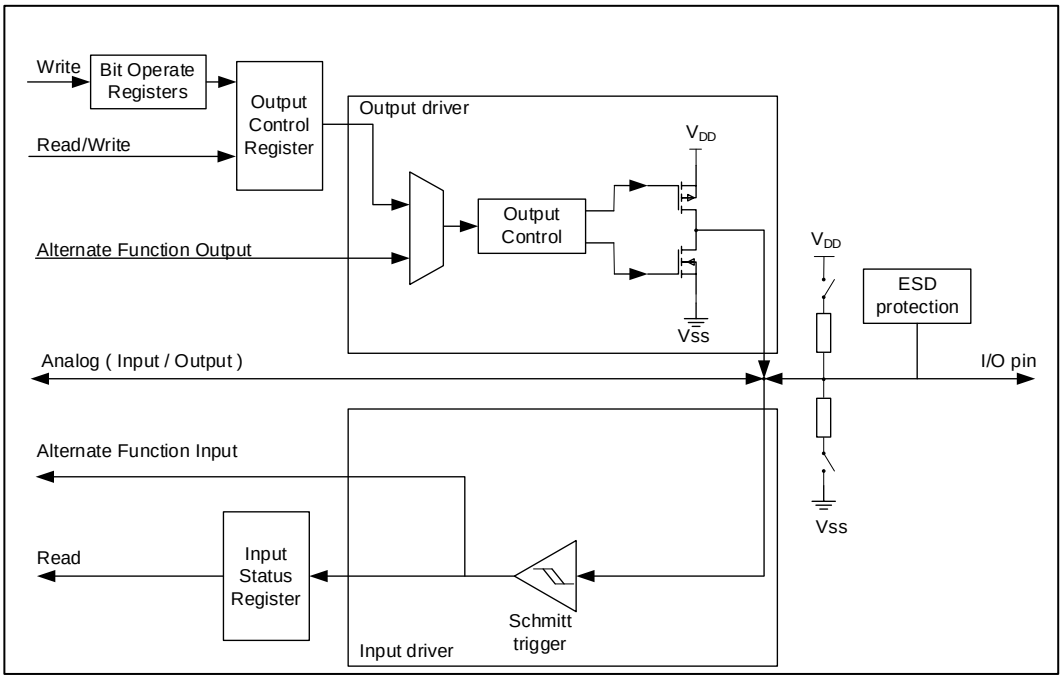
Note: After the MCU is running, if the BOOT state is changed, it will take effect after the system is reset. MCU.

2.5. Typical Peripheral Modules

2.5.1. GPIO Circuit

GD32H73x_75x can support up to 135 universal I/O pins (GPIO), including PA0 ~ PA15, PB0 ~ PB15, PC0 ~ PC15, PD0 ~ PD15, PE0 ~ PE15, PF0 ~ PF15, PG0 ~ PG15, PH0 ~ PH15, PJ8 ~ PJ11, PK0 ~ PK2. Each on-chip device uses it to implement logical input / output functions. Each GPIO port has relevant control and configuration registers to meet the specific application requirements. The external interrupt of the GPIO pin of the on-chip device is controlled and configured by the register of the EXTI module. The basic structure of the GPIO port is shown in ***Figure 2-25. Basic structure of standard IO***:

Figure 2-25. Basic structure of standard IO



Note:

1. The IO port is divided into 5V tolerant and non-5V tolerant. When using, pay attention to distinguish the IO port withstand voltage, refer to the datasheet for details.
2. When the 5V-tolerant IO port is configured as an open drain output or input mode, a 5V voltage can be connected. When configured as a push-pull output mode, it is prohibited to connect a 5V voltage.
3. To improve EMC performance, it is recommended to pull up or pull down the unused IO pins by hardware.
4. The three IO ports of PC13, PC14, PC15 have weak drive capability and limited output current capability(about 3mA). When configured in output mode, their working speed cannot exceed 2MHz(Maximum load is 30pF).
5. The same label PIN in multiple groups can only configure one port as an external interrupt. For example, PA0, PB0, and PC0 only support one of the three IO ports to generate external interrupts, and do not support three external interrupt modes.
6. Non-5V tolerance I/O, external voltage over V_{DD}, may generate perfusion current.

2.5.2. ADC Circuit

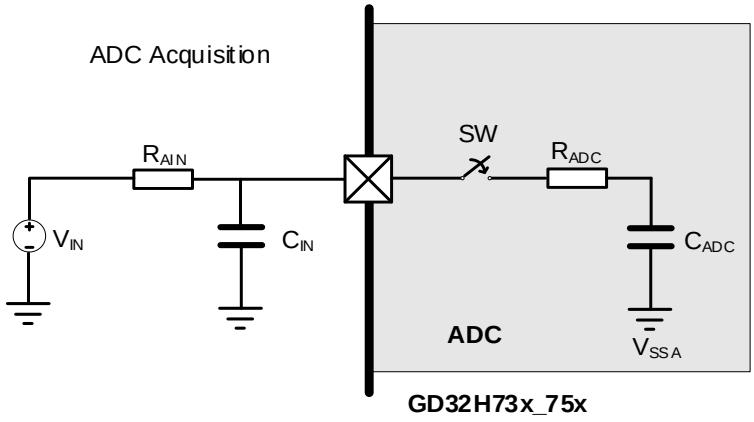
GD32H73x_75x integrates a 12/14 bit successive approximation analog-to-digital converter module (ADC) internally. ADC0 has 20 external channels, 1 internal channel (DAC_OUT0 channel), ADC1 has 18 external channels, 3 internal channels (battery voltage (V_{BAT}) channel, reference voltage input channel (V_{REFINT}), and DAC_OUT0 channel), ADC2 has 17 external channels, 4 internal channels (battery voltage (V_{BAT}) channel, reference voltage input channel (V_{REFINT}), internal temperature sensing channel (V_{SENSE}) and high-precision temperature sensor channel (V_{SENSE2})). ADC sampling channels support multiple operation modes. After sampling conversion, conversion results can be stored in the corresponding data register in

the least significant bit alignment or most significant bit alignment (ADC0/1 is a 32-bit data register, and ADC2 is a 16 bit data register). The on-chip hardware oversampling mechanism can improve performance by reducing the related computing burden from MCU.

If the ADC collects the external input voltage during use, if the sampled data fluctuates greatly, it may be due to the interference caused by power supply fluctuations. You can calibrate by sampling the internal V_{REFINT} and then calculate the externally sampled voltage.

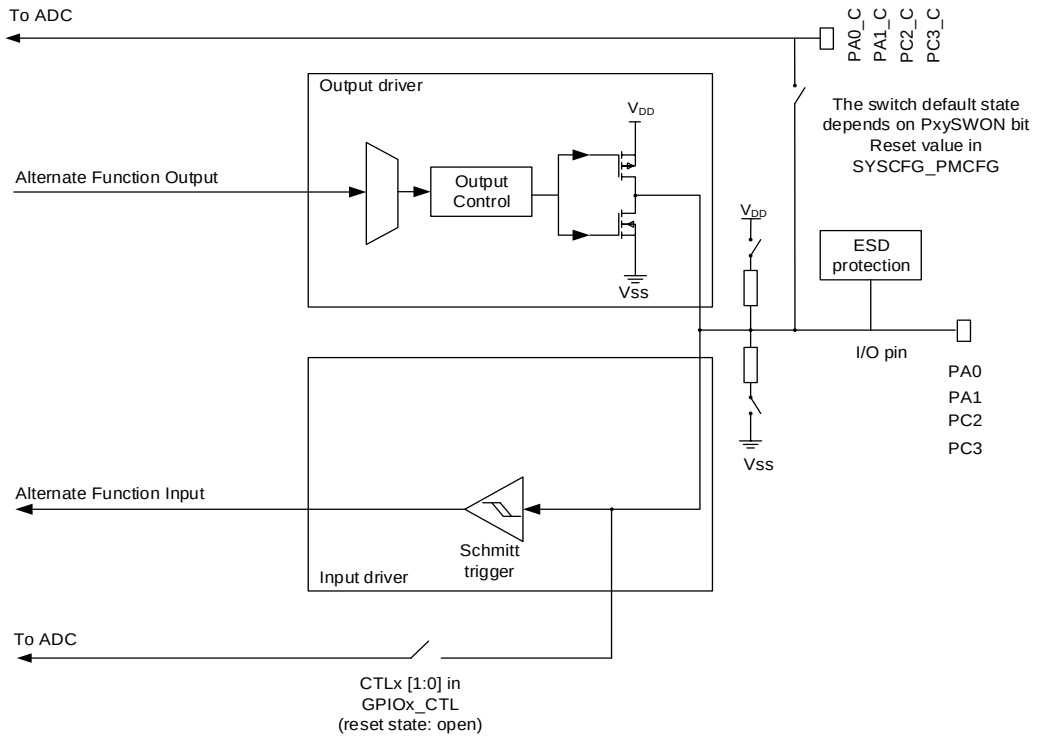
When designing the ADC circuit, it is recommended to place a small capacitor at the ADC input pin, as shown in ***Figure 2-26. ADC Acquisition Circuit Design***.

Figure 2-26. ADC Acquisition Circuit Design



Some pins are directly connected to PA0_C, PA1_C, PC2_C and PC3_C ADC analog input terminal (as shown in ***Figure 2-27. Analog configuration of ADC***): The Pxy_C and Pxy pins are directly connected through analog switches.

Figure 2-27. Analog configuration of ADC



2.5.3. Internal temperature sensor calibration

The GD32H73x_75x series MCU is internally integrated with a temperature sensor (ADC2_CH18), a high-precision temperature sensor (ADC2_CH20) and a low power digital temperature sensor (LPDTS), with an effective temperature measurement range of -40 °C to 105 °C. The output voltage of the temperature sensor varies linearly with temperature. To ensure the accuracy of temperature measurement, it is necessary to provide an accurate and low-temperature drift reference voltage V_{REFP} for the ADC.

The output voltage of the temperature sensor varies linearly with temperature. Due to the diversity of chip production processes, the deviation of the temperature change curve may vary between chips (up to 45 °C difference). Internal temperature sensors are more suitable for detecting temperature changes than for measuring absolute temperature. If precise temperature measurement is required, an external temperature sensor should be used to calibrate this offset error.

The internal voltage reference (V_{REFINT}) provides a stable (bandgap reference) voltage output to the ADC and comparator. V_{REFINT} internal connection to ADC1_CH17 / ADC2_CH19 input channel.

Using temperature sensors:

1. Configure the conversion sequence and sampling time of the temperature sensor channel (ADC1_CH18) to ts_temp us;
2. Set the TSVEN1 bit in the ADC_CTL1 register to enable the temperature sensor;
3. Set the ADCON bit of the ADC_CTL1 register, or trigger ADC conversion externally;
4. Read and calculate the temperature sensor data $V_{temperature}$ from the ADC data register, and calculate the actual temperature using the following formula:

   $$Temperature(°C) = \{(V_{25} - V_{temperature}) / Avg\_Slope\} + 25$$

   V_{25}: The voltage of the internal temperature sensor at 25 °C, please refer to the datasheet for typical values.

   Avg_Slope: The average slope of the temperature and internal temperature sensor voltage curve, please refer to the datasheet for typical values.

Using high-precision temperature sensors:

1. Configure the conversion sequence and sampling time of the temperature sensor channel (ADC2_CH20) to ts_ temp us；
2. Set the TSVEN2 bit in the ADC_CTL1 register to enable the temperature sensor;
3. Set the ADCON bit of the ADC_CTL1 register, or trigger ADC conversion externally;
4. Read and calculate the temperature sensor data $V_{temperature}$ from the ADC data register, and calculate the actual temperature using the following formula:

   $$Temperature(°C) = \{(V_{temperature} – V_{25}) / Avg\_Slope\} + 25$$

   V_{25}: The voltage of the internal temperature sensor at 25 °C, please refer to the datasheet for typical values.

   Avg_Slope: The average slope of the temperature and internal temperature sensor voltage curve, please refer to the datasheet for typical values.

Note:

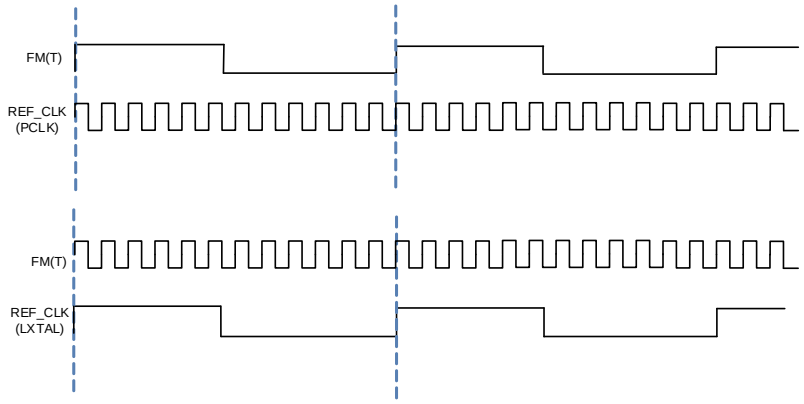
1. When a high-precision temperature sensor is enabled, it is necessary to wait for at least 3 ADC sampling cycles, and the first three converted data should be discarded;
2. The accuracy of high-precision temperature sensor can be improved by oversampling and software averaging (50 point averaging is generally recommended).

Low power digital tempearature sensor(LPDTS) is used to transmit square wave,which is converted by temperature and the frequency is proportional to the absolute temperature. The frequency measurement is based on the PCLK or the LXTAL clock.

A signal is output, which FM(T) frequency (typically 641 kHz) is related to temperature, by the analog part of temperature sensor. Two counters are embedded in the temperature sensor block, which makes the counting mode relevant to the reference clock frequency. The counting result is stored in the LPDTS_DATA register.

- When the reference clock is PCLK, the measurement method is to sample one or multiple FM(T) cycles and count at the rising edge and falling edge of PCLK.
- When the reference clock is LXTAL, the measurement method is to sample one or multiple LXTAL cycles and count at the rising edge and falling edge of FM(T).

Figure 2-28. Measurement method



The Temperature calculation formula When PCLK is used:

$$T=T0+((2\times F_{PCLK}/COVAL)\times SPT-100\times FREQ)/RF\_CF$$

The Temperature calculation formula When LXTAL is used:

$$T=T0+(((F_{LXTAL}\times COVAL)/(2\times SPT))-(100\times FREQ))/RF\_CF$$

T0: T0 equal to 25 °C.

COVAL: COVAL is the value of the counter output value for temperature sensor which measured and stored in the LPDTS_DATA register.

SPT: SPT is Sampling time for temperature sensor.

FREQ: FREQ is engineering value of the frequency measured at T0 for temperature sensor which measured and stored in the LPDTS_SDATA register. It is expressed in hundreds of Hertz.

RF_CF: RF_CF is the engineering value of the ramp coefficient for the temperature

sensor.

2.5.4. USB Circuit

The GD32H73x_75x series MCU has an embedded USBHS interface, providing a USB interconnection solution for portable devices. USBHS not only supports host mode and device mode, but also supports OTG mode that follows HNP (Host Negotiation Protocol) and SRP (Session Request Protocol). The USBHS includes an internal USB PHY that can be configured to either full speed or high speed, and no longer requires an external PHY chip. USBHS can support all four transmission methods defined by the USB 2.0 protocol (control transmission, batch transmission, interrupt transmission, and synchronous transmission). In addition, there is a DMA engine operation inside the USBHS that can act as an AHB bus host to accelerate data transmission between the USBHS and the system. For the operation of full speed devices, it also supports Battery Charge Detection (BCD), Additional Detection Protocol (ADP), and Link Layer Power Management (LPM).

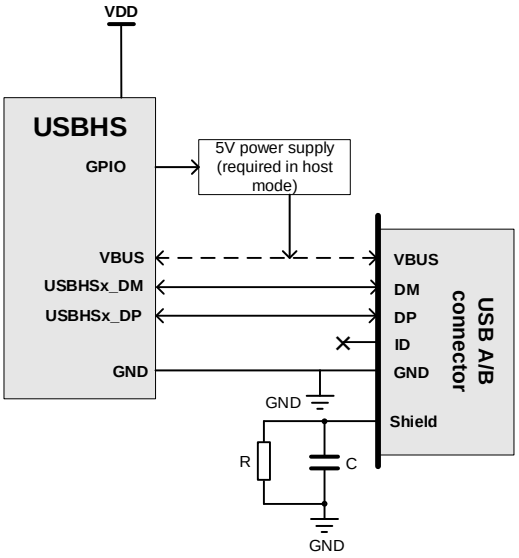
The USB protocol requires a clock accuracy of no less than 500ppm, and internal clocks may not be able to achieve such accuracy. Therefore, it is recommended to use external crystals or active crystal oscillators as the clock source for the USB module when using the USB function. When designing the circuit, in order to improve the ESD performance of USB, it is recommended to design a resistance capacitance discharge isolation circuit for the USB shell. The description of the USBHS signal line is shown in ***Table 2-11. USBHS signal line description***.

Table 2-11. USBHS signal line description

I/0 port	Type	Description	Note
VBUS	Input	Bus power port	For internal PHY only
DM	Input/Output	Differential data line - port	For internal PHY only
DP	Input/Output	Differential data line + port	For internal PHY only
ID	Input	USB identification: Mini connector identification port	For internal PHY only
ULPI_D[7:0]	Input/Output	ULPI Data line	For external ULPI PHY
ULPI_NXT	Input	ULPI next line	For external ULPI PHY
ULPI_DIR	Input	ULPI Direction	For external ULPI PHY
ULPI_STP	Output	ULPI Stop	For external ULPI PHY
ULPI_CLK	Input	ULPI Clock	For external ULPI PHY

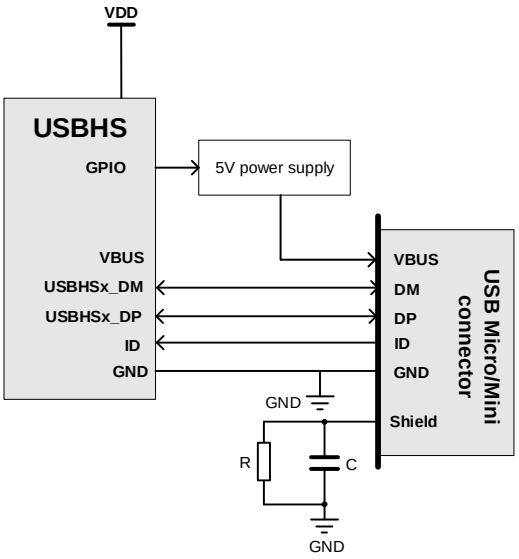
USBHS includes an internal embedded PHY that supports high, full, and low speeds in host mode, high and full speeds in device mode, and OTG protocols with HNP and SRP. The pull-up or pull-down resistors are already integrated into the internal full speed PHY, and the USBHS can automatically control based on the current mode (host, device, or OTG mode) and connection status. Connection diagram using internal PHY is shown in ***Figure 2-29. Connection diagram in host or device mode***. The connection diagram of OTG mode is shown in ***Figure 2-30. Connection diagram of using internal embedded PHY in OTG mode***.

Figure 2-29. Connection diagram in host or device mode



Recommended: R=1 MΩ, C=4700 pF.

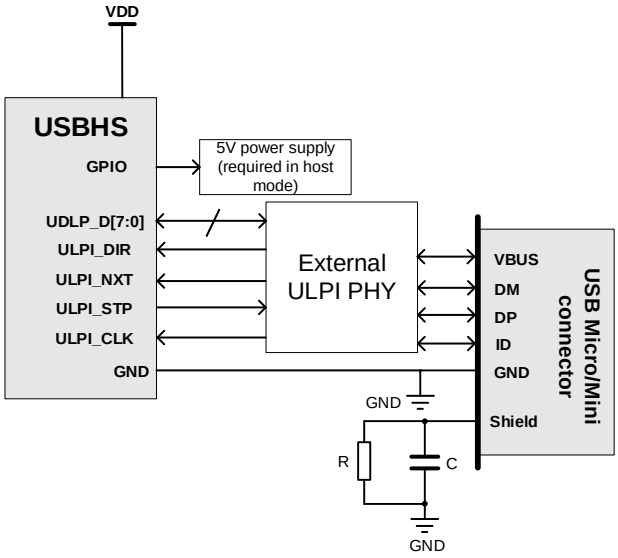
Figure 2-30. Connection diagram of using internal embedded PHY in OTG mode



Recommended: R=1 MΩ, C=4700 pF.

USBHS provides an ULPI interface for external PHYs. If a USBHS module is required to complete high-speed USB applications, then an external high-speed ULPI PHY is required. Combined with external ULPI PHY, USBHS supports high-speed hosts and devices, as well as all modes described in the previous article for internal embedded full speed PHY. The connection diagram of using external ULPI PHY is shown in ***Figure 2-31. Connection diagram of using external ULPI PHY***.

Figure 2-31. Connection diagram of using external ULPI PHY

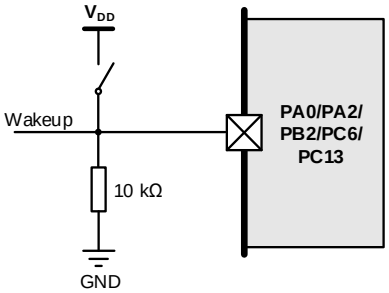


2.6. Thermal management and low power consumption mode

GD32H73x_75x series has a high power consumption when using more peripherals, and users should ensure that T_J < 125 °C under any working condition when using it. For external circuits, refer to “AN060 Thermal management manual for GD32 MCU” and choose the appropriate heat dissipation method. There are three ways to achieve lower power consumption in internal control: slow down the system clock (HCLK, PCLK1, and PCLK2), turn off the clock of unused peripherals, or configure the output voltage of LDO through the LDOVS[2:0] bit of the PMU_CTL3 register. LDOVS[2:0] can only be configured when PLL is not enabled.

In addition, three power-saving modes can achieve lower power consumption, namely sleep mode, deep sleep mode, and standby mode. The standby mode has the lowest power consumption, and this low-power mode also requires the longest wake-up time. Wake up from Standby mode can be achieved through the rising edge of the WKUP pin, totaling 5 WKUP pins. At this time, there is no need to configure the corresponding GPIO, only the WUPENx bit in the PMU_CS register needs to be configured. The corresponding WKUP wake-up pin reference circuit design is shown in ***Figure 2-32. Recommend Standby external wake-up pin circuit design***.

Figure 2-32. Recommend Standby external wake-up pin circuit design



Note: In this mode, attention should be paid to the circuit design. If there is a series resistance between the WKUP pin and V_{DD}, additional power consumption may be added.

2.7. Download the debug circuit

The GD32H73x_75x series supports both JTAG debugging interface and SWD debugging interface. By default it supports SWD interface and can be modified to JTAG mode through effuse. It also supports secure JTAG, but cannot be rolled back to SWD mode, refer to “AN111 GD32H73x_75x Software Development Guide” for details. The JTAG interface standard is a 20 pin interface, with 5 signal interfaces, and the SWD interface standard is a 5 pin interface, with 2 signal interfaces.

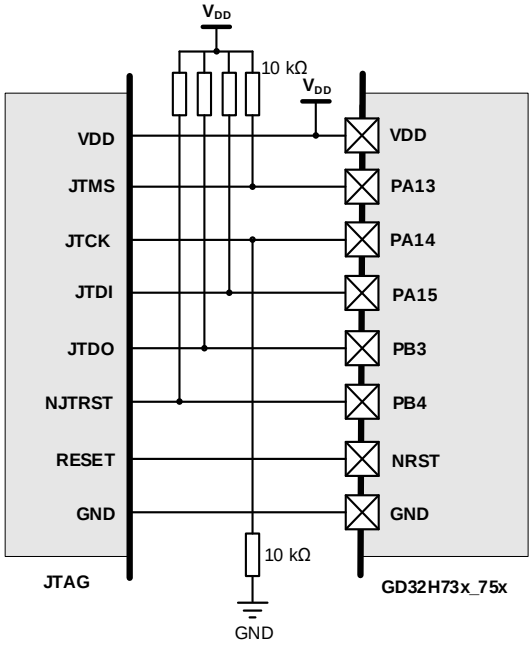
Note: After reset, the debug related ports are in input pull-up / pull-down mode, where:

PA15: JTDI in pull-up mode.
PA14: JTCK / SWCLK in pull-down mode
PA13: JTMS / SWDIO in pull-up mode
PB4: NJTRST in pull-up mode
PB3: JTDO in floating mode.

Table 2-12. JTAG download debug interface assignment

Alternate function	GPIO port
JTMS	PA13
JTCK	PA14
JTDI	PA15
JTDO	PB3
NJRST	PB4

Figure 2-33. Recommend JTAG wiring reference design



Note: After reset, the debug related ports are in input pull-up / pull-down mode, where:

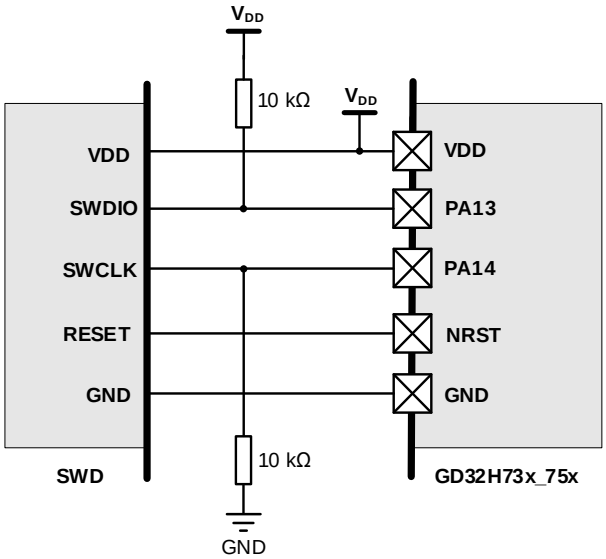
PA13: SWDIO in pull-up mode.

PA14: SWCLK in pull-down mode

Table 2-13. SWD download debug interface assignment

Alternate function	GPIO port
SWDIO	PA13
SWCLK	PA14

Figure 2-34. Recommend SWD Wiring Reference Design

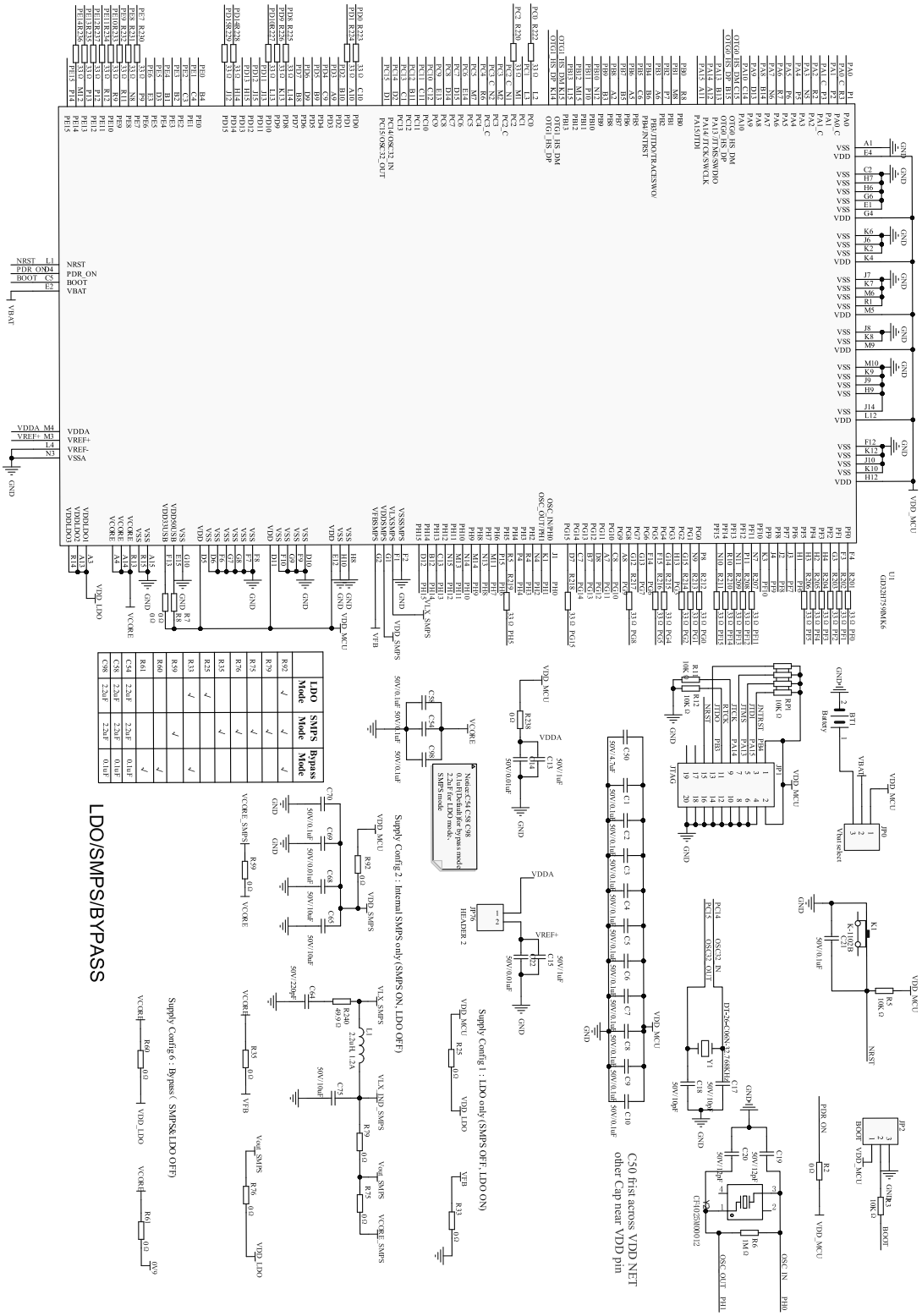


There are several ways to improve the reliability of SWD download and debugging communication and enhance the anti-interference ability of download and debugging.

1. Shorten the length of the two SWD signal lines, preferably within 15 cm.
2. Weave the two SWD wires and the GND wire into a twist and twist them together.
3. Connect separately tens of pF small capacitors in parallel between the two signal lines of the SWD and the ground.
4. Any IO of the two signal lines of SWD is connected in series with a 100 Ω ~ 1 kΩ resistor.

2.8. Reference Schematic Design

Figure 2-35. GD32H73x_75x Recommend Reference Schematic Design



3. PCB Layout Design

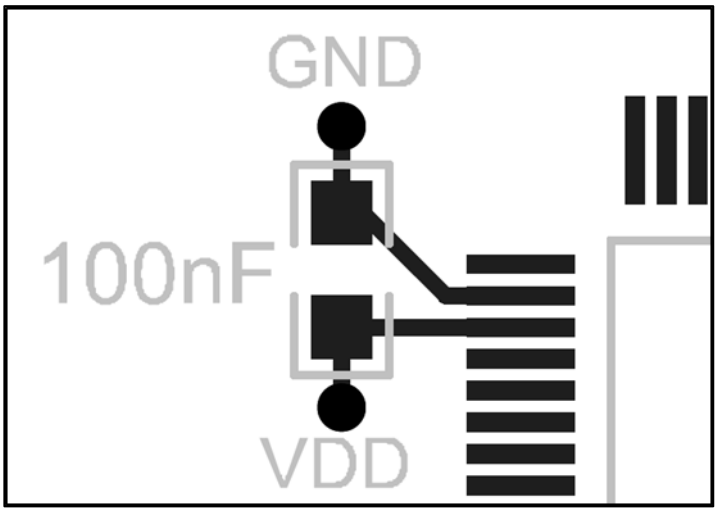
In order to enhance the functional stability and EMC performance of the MCU, it is not only necessary to consider the performance of the supporting peripheral components, but also the PCB Layout. In addition, when conditions permit, try to choose a PCB design solution with an independent GND layer and an independent power supply layer, which can provide better EMC performance. If conditions do not allow, independent GND layer and power supply layer cannot be provided, then it is also necessary to ensure a good power supply and grounding design, such as making the GND plane under the MCU as complete as possible. For packages with EPAD, it is recommended that EPAD be grounded on the PCB Layout.

In applications with high power or strong interference, it is necessary to consider keeping the MCU away from these strong interference sources.

3.1. Power Supply Decoupling Capacitors

The GD32H73x_75x series power supply has V_{DD}, V_{DDA}, V_{REFP} and other power supply pins. Ceramic MLCC can be used for the 100nF decoupling capacitor, and the position should be as close to the power pin as possible. The power cable should be routed through the capacitor before reaching the MCU power pin. It is recommended to lay out a Layout in the form of Via near the capacitor PAD

Figure 3-1. Recommend Power Pin Decoupling Layout Design



3.2. 0.9V Power Domain Circuit

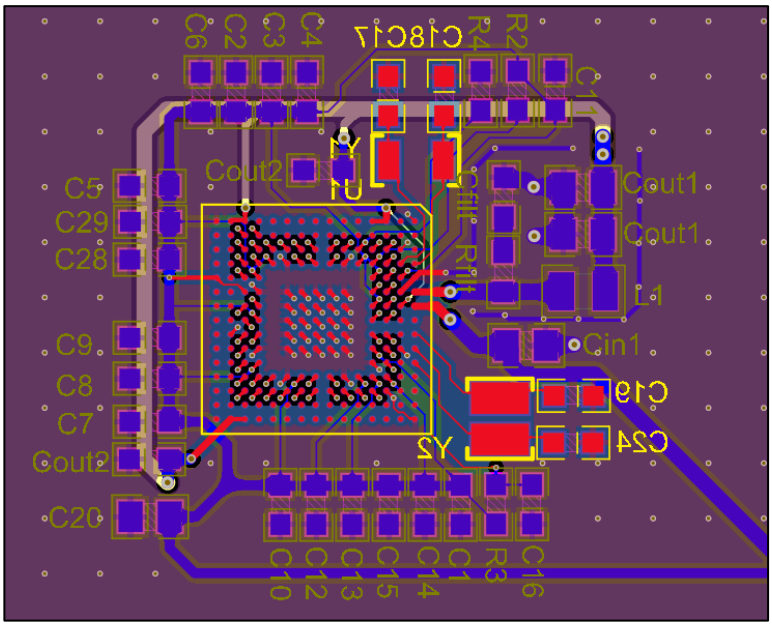
The current 0.9V power domain is recommended to use either the SMPS (Switched-Mode Power Supply) mode or bypass mode. To enhance the functional stability and EMC (Electromagnetic Compatibility) performance of the MCU (Microcontroller Unit), the power circuit design should consider not only the performance of peripheral components but also the PCB (Printed Circuit Board) layout.

The PCB layout for the SMPS power supply mode should adhere to the following requirements:

1. The VLXSMPS of the SMPS is a 2MHz voltage switching signal, whose amplitude may exceed VDD or fall below VSS. Based on system-level EMC protection design, it should be shielded from other signals as much as possible.
2. All traces for this module and peripheral components should be placed on the same layer as much as possible, with adjacent layers kept as complete ground planes. Clock lines, VFBSMPS, and other analog lines should maintain distance from the module and line layer, with proper grounding treatment.
3. To increase overcurrent capacity, the trace widths for VDDSMPS and VLXSMPS should be as wide as possible, at least 20 to 30 mil or more.
4. The placement and routing of peripheral components should follow the shortest di/dt principle for the output current loop.
5. To ensure output stability, the VFBSMPS feedback line of the SMPS should return from the load end.
6. Whether the LDO (Low-Dropout Regulator) is enabled or not, all VDDLDO pins and VCORE pins of the chip must be connected together.

The recommended layout for the SMPS power supply mode in the BGA176 package is shown in ***Figure 3-2. Recommend layout diagram for the BGA176 package SMPS power supply mode***.

Figure 3-2. Recommend layout diagram for the BGA176 package SMPS power supply mode



The PCB layout for bypass mode should adhere to the following requirements:

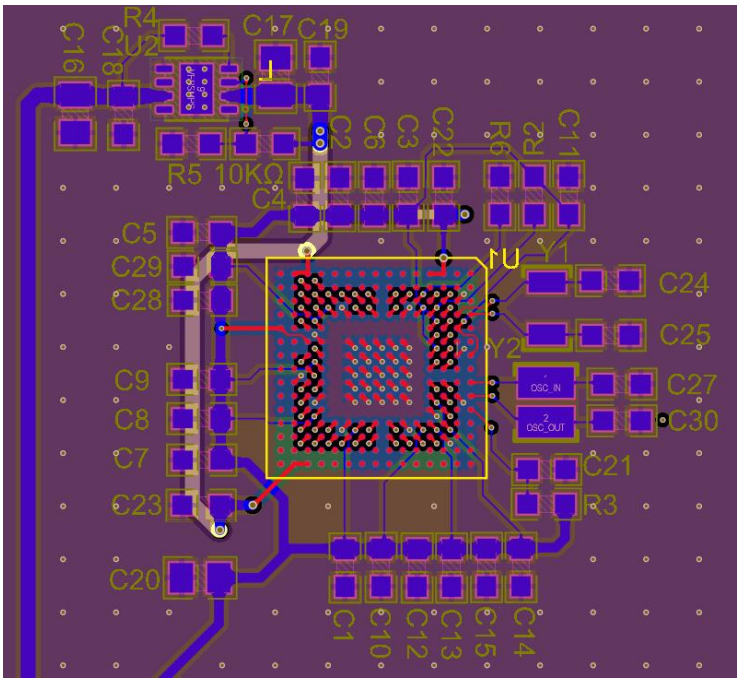
1. When using an external power supply for the VCORE, attention should be paid to the line loss caused by line resistance under high current output conditions, to avoid the terminal voltage falling below the specified requirements.
2. Heat dissipation measures should be taken to prevent the heat generation of the external

power supply from affecting the heat dissipation and performance of the MCU.

3. All VDDLDO pins and VCORE pins of the chip must be connected together and connected to the output terminal of the external power supply.

The recommended layout for the bypass mode in the BGA176 package is shown in ***Figure 3-3. Recommend layout diagram for the BGA176 package bypass mode***.

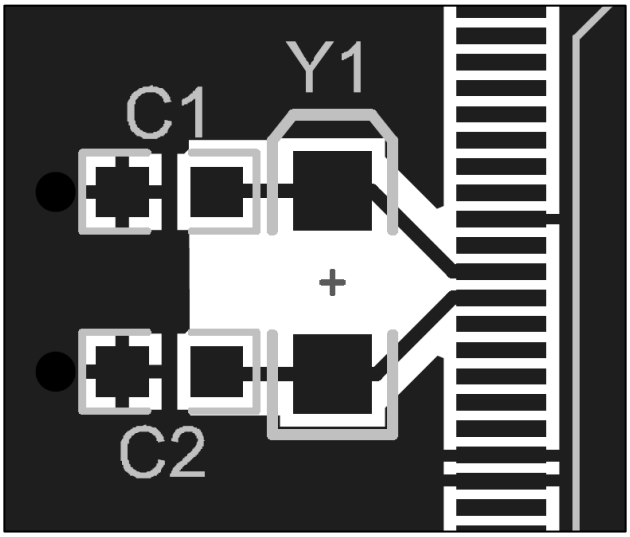
Figure 3-3. Recommend layout diagram for the BGA176 package bypass mode



3.3. Clock Circuit

GD32H73x_75x series clocks have HXTAL and LXTAL, and the clock circuit (including crystal or crystal oscillator and capacitor, etc.) is required to be placed close to the MCU clock pin, and the clock trace should be wrapped by GND as much as possible.

Figure 3-4. Recommend Clock Pin Layout Design (passive crystal)



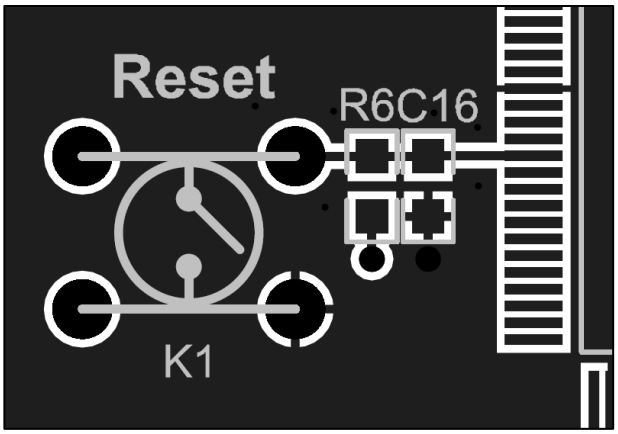
Note:

1. The crystal should be as close to the MCU clock pin as possible, and the matching capacitor should be as close as possible to the crystal.
2. The whole circuit should be on the same layer as the MCU, and the wiring should not go through the layer as much as possible.
3. The PCB area of the clock circuit should be kept as empty as possible, and no traces unrelated to the clock should be taken.
4. High-power, high-interference risk devices and high-speed wiring should be kept away from the clock crystal circuit as far as possible.
5. The clock line is grounded to achieve a shielding effect.

3.4. Reset Circuit

NRST trace PCB Layout reference is as follows:

Figure 3-5. Recommend NRST Trace Layout Design

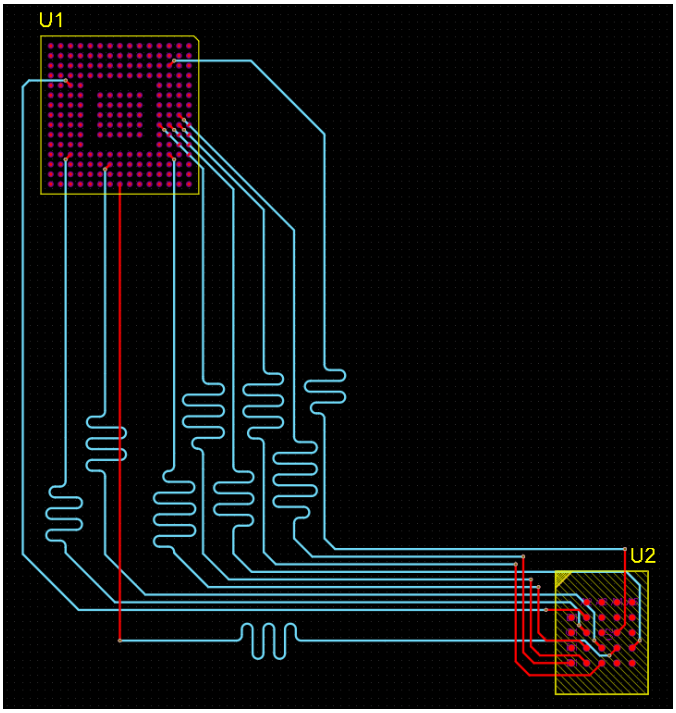


Note: The resistance and capacitance of the reset circuit should be as close as possible to the NRST pin of the MCU, and the NRST trace should be kept away from devices with strong interference risk and high-speed traces as far as possible. If conditions permit, it had better to wrap the NRST traces for better shielding effect.

3.5. OSPI Circuit

The GD32H73x_75x series MCU OSPI module supports single-line, dual-line, quad-line, and octal-line SPI memory (PSRAM, NAND, NOR flash, etc.). The PCB layout guidelines for OSPI routing are as follows:

Figure 3-6. Recommend OSPI routing layout design



Note:

1. Avoid signal traces crossing power plane divisions and maintain a complete reference plane for signals.
2. The signal lines and clock lines of the OSPI should be routed on the top layer with ground shielding as much as possible, with equal lengths controlled within 300 mil (the spacing for serpentine microstrip lines is recommended to be 7H, and for stripline is recommended to be 5H, where H is the distance from the signal trace to the reference plane; if there are vias, generally one via adds 50-100 mil to the trace length, depending on the via length).
3. The OSPI chip should be placed as close to the MCU as possible, and away from power sources and power devices that act as sources of interference.
4. If the quality of the signal lines or clock line signals is poor, consider adding termination resistors at the memory end.

3.6. USB Circuit

For the GD32H73x_75x series MCU USB FS module, there are two differential signal lines DM and DP. For the USB HS module, after the external high-speed PHY is connected, the PHY chip will also lead out two differential signal lines DM and DP. It is recommended that the PCB wiring requires a characteristic impedance of 90Ω. The differential wiring should be strictly in accordance with the equal length isometric gauge, and the wiring should be as short as possible. If the two differential lines are not equal in length, a serpentine wire can be used at the terminal to compensate for the short line.It is recommended to connect DM and DP directly without matching resistors in series.

DM and DP differential wiring reference is as follows:

1. Reasonably arrange the layout to shorten the differential routing distance.
2. Give priority to drawing differential lines, try not to exceed two pairs of vias on a pair of differential lines, and place them symmetrically.
3. Symmetrical parallel wiring ensures close coupling between two wires, avoiding 90°, arc or 45° wiring methods.
4. Devices such as resistors, capacitors, EMC, or test points connected to the differential wiring should also adhere to the principle of symmetry.

For the USB HS module, the data and signal control lines between the MCU and the external HS PHY should also be kept as short as possible. It is necessary to use serpentine wires for equal length processing, and the following precautions should be taken:

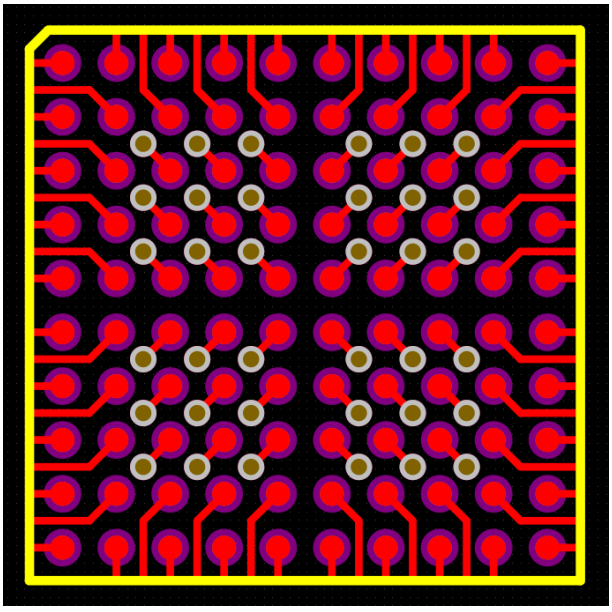
1. The layout should be arranged reasonably, and the USB HS-PHY chip should be as compact as possible between the MCU.
2. When wiring, take the longest signal wire as the target length and compensate for other signal wires through a serpentine routing.

3.7. BGA Circuit

For some models of the GD32H73x_75x series MCU with BGA100 (0.8mm Pitch) and BGA176 (0.65mm Pitch) packaging, we recommend the following wiring rules and fanout methods.

For BGA100 package with a 0.8 mm pitch, it is recommended to use a rule setting of 5 mil line width and line spacing. Use 10 / 16 mil through holes for fanout. After fanout, as shown in *Figure 3-7. Fan out method for BGA100 package*.

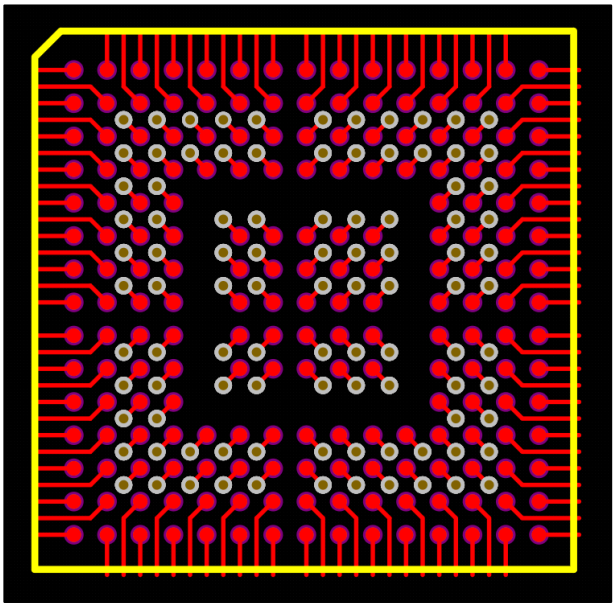
Figure 3-7. Fan out method for BGA100 package



For BGA176 package with a 0.65 mm pitch, it is recommended to use a rule setting of 4 mil

line width and line spacing. Use 8/12 mil (if the current is large, 8/13 mil can also be used, but larger than 8/13 mil size, 4 mil line width and line spacing cannot be used) through holes for fanout. After fanout, as shown in ***Figure 3-8. Fan out method for BGA176 package***.

Figure 3-8. Fan out method for BGA176 package



4. Package Description

The GD32H73x_75x series comes in five packaging forms, LQFP100, LQFP144, LQFP176, BGA100 and BGA176.

Table 4-1. Package Description

Ordering code	Package
GD32H737VxT6	LQFP100(14x14, 0.5 pitch)
GD32H757VxT6	
GD332H737ZxT6	LQFP144(20x20, 0.5 pitch)
GD32H757ZxT6	
GD32H737IxT6	LQFP176(24x24, 0.5 pitch)
GD32H759IxT6	
GD32H757VxJ6	BGA100(8x8, 0.8 pitch)
GD32H737VxJ6	BGA176(10x10, 0.65 pitch)
GD32H759IxK6	

(Original dimensions are in millimeters)

5. Revision history

Table 5-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Apr.14, 2023
1.1	1. Add section 2.1.4. 2. Update section 2.1.5 to provide all packaging power supply design drawings, explaining the connection of relevant pins within the chip.	Jun.21, 2023
1.2	1. Update Section 2.1.3 to add configuration tables for registers in each mode and update the recommended circuit design for each mode. 2. Update Section 2.8 with the design of the reference schematic. 3. Add a new Section 3.5.	Dec.19, 2023
1.3	1. Update Figure 2-1 to add descriptions related to the backup domain LDO. 2. Update Section 2.1.2 to include descriptions of VREFP and VDDA. 3. Update Section 2.1.3 with the configuration of registers for each mode; add descriptions of VDDSMPS pins when the SMPS module is disabled; add power-up sequences and related explanations for bypass mode. 4. Update Section 2.1.4 to add precautions. 5. Update the descriptions related to Cin, COUT1, and COUT2 in Figure 2-10 and Table 2-6. 6. Update the description of the reset circuit in Section 2.2. 7. Update Section 3.2 to add Figure 3-3.	Aug.13, 2024
1.4	1. Update Figure 2-4. 2. Update Figure 2-6. 3. Update the description of the 0.9V power domain configuration.	Nov.19, 2024
1.5	1. Update the description of the 0.9V power domain configuration. 2. Refine the content related to power detection and reset, adding Section 2.2.	Dec.15, 2024
1.6	1. Rename the document to	Mar.06, 2026

	"GD32H73x_75x Series Hardware Development Guide". 2. In the document content, change all GD32H7xx-related content to GD32H73x_H75x-related content. 3. Update Figure 2-8 in Section 2.1.4 and add Note 2	

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