GigaDevice Semiconductor Inc.

PWM-DAC Technology Guide Based on GD32 MCU

Application Note
AN320

Revision 1.0

(Mar. 2026)

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1. Introduction

In modern embedded systems, Digital-to-Analog Conversion (DAC) serves as a critical interface bridging digital processing and analog signal domains. DACs are widely utilized in applications such as audio signal generation, sensor excitation, voltage regulation, signal modulation, and motor control. However, in resource-constrained or cost-sensitive embedded designs, not all microcontrollers (MCUs) integrate dedicated hardware DAC modules. To achieve analog signal generation while maintaining system simplicity and cost-effective, Pulse Width Modulation (PWM)-based DAC technology has emerged as an effective and flexible alternative.

This Application Note (AN) presents a comprehensive guide to implementing and utilizing PWM-DAC technology on the GD32 MCU. It covers the fundamental principles of PWM-DAC operation, resolution analysis, filter circuit design, and test results. Through this document, engineers can quickly learn how to leverage the GD32 MCU's timer resources to generate high-quality analog signals, providing a cost-effective and flexible solution for modern embedded system designs.

Table 1-1. Applicable product

Type	Model
MCU	GD32 MCU Family

Note: This application note is for reference only. In case of any conflict with the user manual or datasheet, the user manual or datasheet shall prevail.

2. Theoretical Analysis of PWM-DAC Fundamentals

2.1. Fourier and Spectrum Analysis of PWM Signals

According to Fourier analysis, any periodic signal can be represented as the superposition of infinitely many sinusoidal components with distinct frequencies. For a signal $f(t)$ with a period T, it can be expressed in the form:

$$f(t) = a_0 + \sum_{n=1}^{\infty} a_n \cos(n\omega_0 t) + \sum_{n=1}^{\infty} b_n \sin(n\omega_0 t) \tag{2-1}$$

where, ω_0 = the fundamental angular frequency, it is given by:

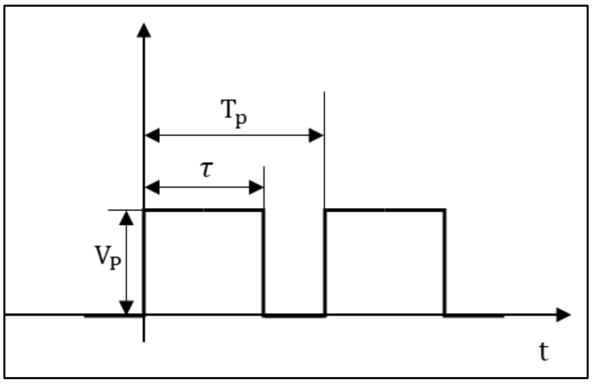
$$\omega_0 = \frac{2\pi}{\mathrm{T}} \tag{2-2}$$

As shown in ***Figure 2-1. Time-domain waveform of the PWM signal***, a PWM signal is a periodic square wave whose high-level duration is determined by the duty cycle *D*, which typically ranges from 0 to 1. The duty cycle defines the ratio of the high-level time to the total period of the waveform, as expressed by:

$$D = \frac{\tau}{\mathrm{T_p}} \tag{2-3}$$

where, $\mathrm{T_p}$ = the period of the PWM signal, and τ = the duration of the high level.

Figure 2-1. Time-domain waveform of the PWM signal



Expand the PWM signal into a Fourier series:

$$v_{\mathrm{PWM}}(t) = A_0 + \sum_{n=1}^{\infty} A_n \cos(2n\pi f_{\mathrm{PWM}} t) \tag{2-4}$$

where, A_0 = the amplitude of the DC component, A_n = the amplitude of the harmonic components, and f_{PWM} = the frequency of the PWM signal.

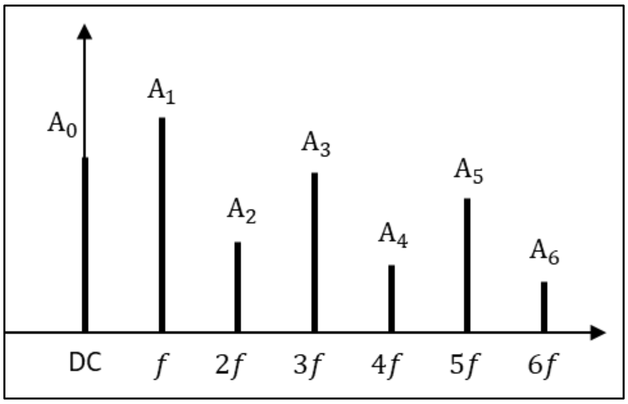
Expand A_0 and A_n respectively, then:

$$A_0 = D\mathrm{V_p} \tag{2-5}$$

$$A_n = \frac{\mathrm{V_p}}{n\pi}\left\{\sin(n\pi D) - \sin\left[2n\pi\left(1-\frac{D}{2}\right)\right]\right\} \tag{2-6}$$

Figure 2-2. Frequency-domain waveform of the PWM signal illustrates the amplitude distribution of various harmonics in the PWM signal. According to Equations (2-5) and (2-6), both the amplitudes of the DC component and the harmonic components are dependent on the duty cycle *D*, while being unaffected by the frequency of the PWM signal f_{PWM}.

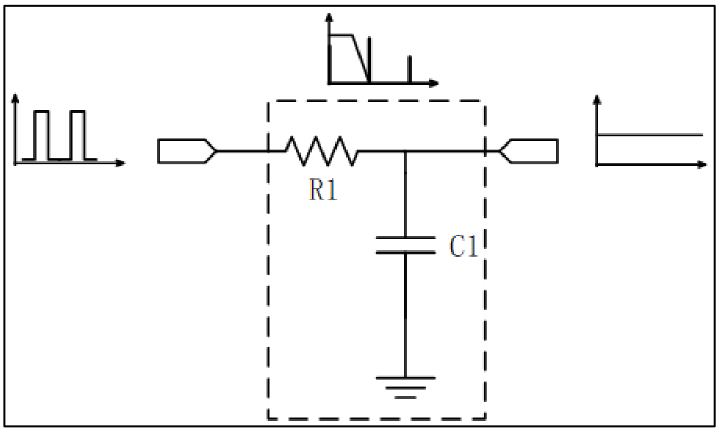
Figure 2-2. Frequency-domain waveform of the PWM signal



2.2. Conversion from PWM Input to DAC Output

As described in Section ***Fourier and Spectrum Analysis of PWM Signals***, the DC component of the PWM signal is directly proportional to its duty cycle *D*. The PWM-DAC technology operates in the frequency domain, where a filtering process removes the harmonic components of the PWM signal while preserving the essential DC component. This enables the conversion from a digital to an analog signal. The schematic diagram of the implementation is presented in ***Figure 2-3. Filtering of PWM Signal for DC Voltage Generation***.

Figure 2-3. Filtering of PWM Signal for DC Voltage Generation



In most cases, a first-order passive RC filter is sufficient to meet the implementation requirements of PWM-DAC conversion, making it suitable for applications with relatively low output resolution. However, to achieve higher output resolution, higher-order RC filter networks can be employed.

To maintain high input impedance, minimize loading effects, and further enhance filtering performance, an active filter configuration using operational amplifier (Op-Amp) is recommended. Active filters not only provide signal buffering but also allow designers to realize specific frequency responses—such as Butterworth or Chebyshev characteristics—according to design requirements. This approach helps optimize the system's dynamic behavior and accuracy performance. Further discussion on filtering design considerations is provided in Section ***Trade-off Between PWM-DAC Resolution and Filtering Requirements***.

3. PWM-DAC Resolution: Modeling and Theoretical Analysis

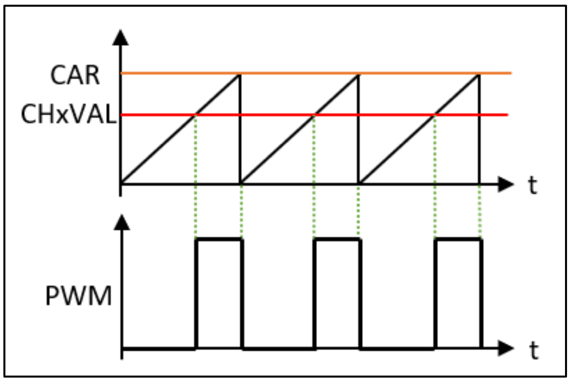
3.1. Conversion Resolution of PWM-DAC

As illustrated in *Figure 3-1. MCU PWM Generation Principle*, for a PWM signal operating with a fixed period (constant CAR), the duty cycle is defined by the CHxVAL register. The smallest step in duty cycle, as given by Equation (3-1), is linearly proportional to the minimum resolution of the DAC.

$$D_0 = \frac{1}{2^{\mathrm{N}}} \quad (3\text{-}1)$$

where, N = the depth of the counter (in bits).

Figure 3-1. MCU PWM Generation Principle



The minimum step can also be expressed as a function of the counter clock frequency and the PWM signal frequency.

$$D_0 = \frac{f_{\mathrm{PWM}}}{f_{\mathrm{C}}} \quad (3\text{-}2)$$

where, f_{PWM} = the PWM signal frequency, and f_C = the counter clock frequency.

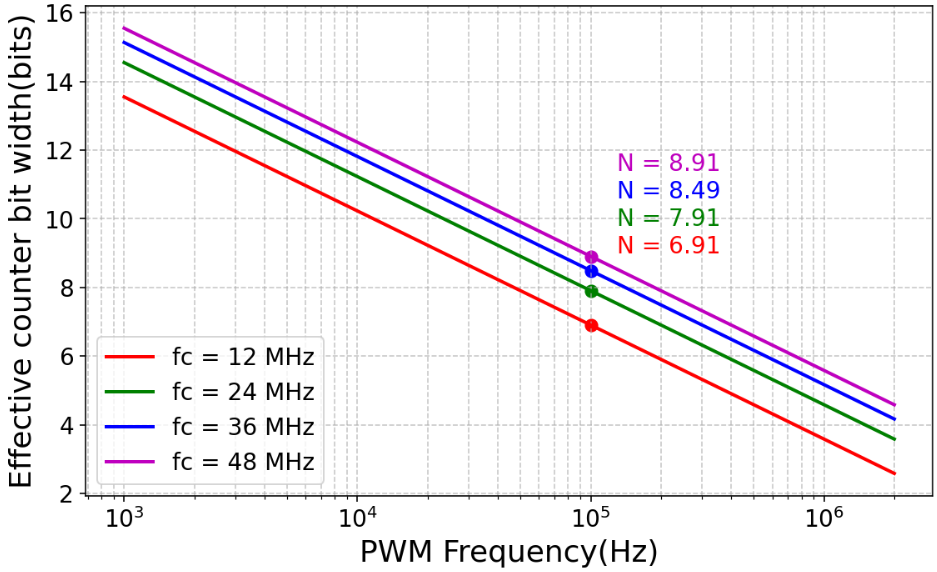
The theoretical minimum output voltage corresponding to the PWM-DAC is:

$$V_{min} = \mathrm{V_p} * D_0 \quad (3\text{-}3)$$

From Equations (3-2), it can be observed that a smaller D_0 can be obtained either by decreasing f_{PWM} or by increasing f_C, thereby enhancing the resolution of the PWM-DAC. However, lowering f_{PWM} necessitates a lower cutoff frequency for the output filter, which significantly increases circuit complexity and component cost—contradicting the cost-effective nature of PWM-DAC technology. Consequently, the most practical and efficient way to improve PWM-DAC resolution is to increase f_C.

Taking GD32C231xx as an example, the maximum counter clock frequency is 48 MHz. The relationship between the PWM-DAC resolution and the PWM signal frequency was simulated at four counter frequencies—12 MHz, 24 MHz, 36 MHz, and 48 MHz—as illustrated in ***Figure 3-2. PWM-DAC Resolution vs PWM Signal Frequency***. Under different counter frequencies, when f_{PWM} = 100 kHz, the effective counter bit width N of the PWM-DAC is approximately 8.9 bits.

Figure 3-2. PWM-DAC Resolution vs PWM Signal Frequency



3.2. Trade-off Between PWM-DAC Resolution and Filtering Requirements

As previously discussed, improving the PWM-DAC resolution by lowering f_{PWM} inevitably increases the complexity and cost of the filtering circuit. The following section presents a design approach to achieve a practical balance between these two factors, enabling the PWM-DAC to attain an optimal resolution within system constraints.

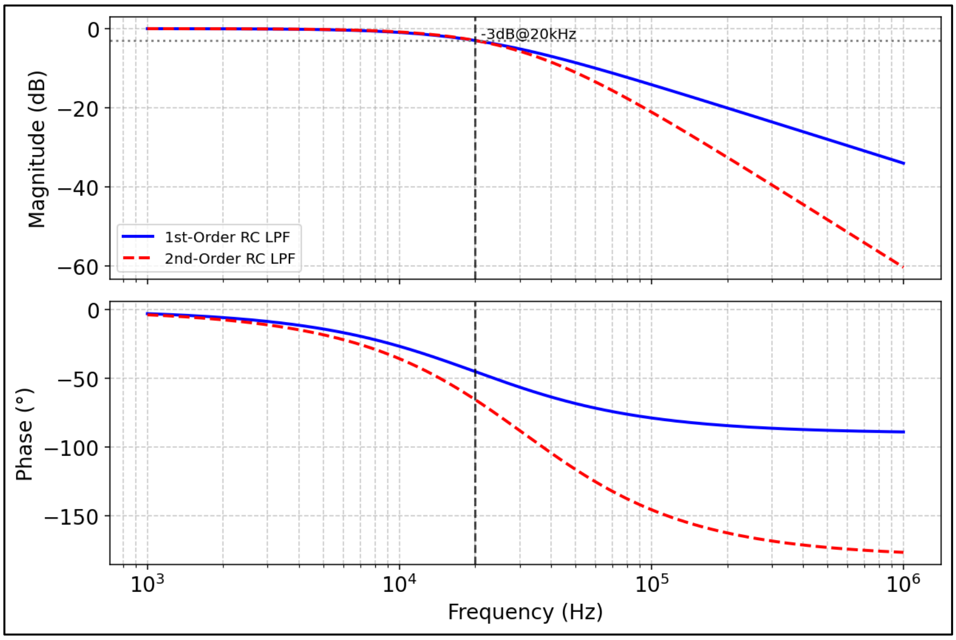
Passive RC filter networks are widely used due to their simplicity and ease of implementation. A comparative analysis is performed between first-order and second-order passive RC filters, and their corresponding transfer functions are given in Equations (3-4) and (3-5).

$$H_1(s) = \frac{1}{1 + sRC} \tag{3-4}$$

$$H_2(s) = \frac{1}{s^2 R_1 R_2 C_1 C_2 + sR_1C_1 + sR_2C_2 + 1} \tag{3-5}$$

To provide a clearer comparison between the two filter orders, the amplitude-frequency and phase-frequency responses of the first-order and second-order passive RC networks at a cutoff frequency of 20 kHz are illustrated in ***Figure 3-3. Bode Plot of 1st & 2nd Order RC Low Pass Filters***. As shown in the figure, second-order filter exhibits a steeper roll-off rate (-40 dB/decade) and a longer phase delay compared with first-order filter (-20 dB/decade), thereby achieving more effective suppression of harmonic components.

Figure 3-3. Bode Plot of 1st & 2nd Order RC Low Pass Filters



It can be seen from Equation (3-2) that the lower the first-harmonic frequency is, the higher the resolution the PWM-DAC can achieve. But when the filter network fails to effectively suppress the harmonic, the residual harmonic components inevitably superimpose on the DC output, thereby degrading the resolution of the PWM-DAC. The amplitude-frequency characteristics vary significantly with the filter order. As shown in ***Figure 3-3. Bode Plot of 1st & 2nd Order RC Low Pass Filters***, a second-order passive RC filter, featuring a steeper roll-off rate, provides superior attenuation of the first-harmonic and thus achieves a higher effective number of bits (ENOB). However, as the PWM frequency increases, the minimum step size of the PWM-DAC deteriorates, leading to a rapid decline in achievable resolution. To obtain higher resolution from the PWM-DAC, the roll-off rate of the filter network should be optimized, and it is recommended that the attenuation at the first-harmonic be between -60 dB and -40 dB.

In practical PWM-DAC applications, a simple RC low-pass filter can smooth the PWM waveform but exhibits limited load-driving capability. To enhance the output drive and ensure voltage stability under varying load conditions, an additional Op-Amp stage is typically introduced as a voltage follower, providing low output impedance and improved load capacity for subsequent circuits.

4. PWM-DAC Test Results

The PA1 pin of the GD32C231xx is configured as an output, with the counter clock frequency f_C set to 48 MHz, generating a PWM signal with a frequency of 100 kHz. And a first-order passive RC filter is connected at the output to extract the DC component, where R = 4.7 kΩ and C = 100 nF. Under this configuration, the attenuation of the first-harmonic component is approximately -49 dB, which meets the recommended range of between -60 dB and -40 dB. Detailed test data are provided in ***Table 4-1. Test Results at 100 kHz***.

Table 4-1. Test Results at 100 kHz

CHxVAL	Theoretical Voltage（mV）	Measured Voltage（mV）	Error（mV）
48	332.8	331.9	-0.9
96	665.6	663.6	-2.0
144	998.4	995.4	-3.0
192	1331.2	1327.2	-4.0
240	1664	1659	-5.0
288	1996.8	1990.9	-5.9
336	2329.6	2322.8	-6.8
384	2662.4	2654.8	-7.6
386	2676.3	2668.8	-7.5
388	2690.1	2682.6	-7.5
390	2704	2696.5	-7.5
392	2717.9	2710.3	-7.6
394	2731.7	2724.2	-7.5
395	2738.7	2731.1	-7.6
396	2745.6	2738	-7.6
397	2752.5	2744.9	-7.6
398	2759.5	2751.8	-7.7
432	2995.2	2986.9	-8.3
480	3328	3319.1	-8.9

According to the results shown in ***Table 4-1. Test Results at 100 kHz***, the minimum resolution of the DAC is approximately 6.9 mV, which is consistent with the theoretical value derived from Equation (3-3). However, this resolution does not take into account the influence of the residual first-harmonic component. In practice, most commonly used voltage measurement instruments adopt Op-Amp, which integrate the output of the first-order passive RC filter, leading to an apparent improvement in the measured resolution. Therefore, when evaluating the ENOB, the impact of the residual first-harmonic component should also be considered comprehensively.

5. Conclusion

This application note verifies that PWM-DAC technology can effectively generate stable analog voltages using a timer output and a simple RC filter. The approach provides a cost-effective and flexible solution for embedded systems without dedicated DAC hardware. By optimizing PWM parameters and filter design, this approach can achieve stable and predictable output performance across different GD32 MCU products.

6. Revision history

Table 6-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Mar.30, 2026

Important Notice