GigaDevice Semiconductor Inc.

GDSCN832xx Hardware Development Guide

Application Notes
AN241

Revision 1.0

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1. Introduction

This article is for developers of GDSCN832xx series based on EtherCAT sub-device controllers (ESCs), and provides a general introduction to the hardware development of GDSCN832xx series products, such as power supply, reset, clock, etc. The purpose of this application note is to allow developers to quickly get started with GDSCN832xx series of products and quickly develop and use product hardware, saving time on studying manuals and speeding up product development progress.

This app development guide is divided into six parts:

1. Power supply, mainly introducing the design of GDSCN832xx series power management and power supply functions.
2. Reset, mainly introducing the design of GDSCN832xx series reset function.
3. clock, mainly introducing the functional design of GDSCN832xx series of clocks.
4. typical peripheral modules, mainly introducing the hardware design of the main functional modules of the GDSCN832xx series.
5. Refer to the circuit and PCB layout design, mainly introduce the GDSCN832xx series hardware circuit design and PCB layout design precautions.
6. The package description mainly introduces the package form and naming included in the GDSCN832xx series.

This document also satisfies the minimum system hardware resources used in application development based on the GDSCN832xx family of products.

Table 1-1. Applicable products

Type	Model
ESC	GDSCN832xxxx series

2. Hardware design

2.1. Power supply

The GDSCN832xx series VDD33 / VDD3Ax has an operating voltage range of 3.0 V ~ 3.6 V and VDDIO operating voltage range of 1.8 V ~ 3.6 V. GDSCN832xx series devices have three power domains, including V_{DD33} / VDD3Ax, VDDIO domain, and 1.1 V domain. The VDD / VDD33 / VDD3Ax and VDDIO domains are directly powered by the power supply. GDSCN832xx series has an embedded LDO to power the 1.1 V domain.

2.1.1. VDD33 / VDD3Ax power domain

The VDD33 / VDD3Ax power domain includes two parts: the VDD33 domain and the VDD3Ax domain. To avoid noise, the VDD3Ax can be connected to the VDD33 via an external filtering circuit.

2.1.2. VDDIO power domain

The VDDIO power domain is the power pin that powers the GPIO. To avoid noise, it can be connected to the VDD33 via an external filtering circuit.

2.1.3. 1.1 V power domain

The 1.1 V power domain includes VDDCR and VDD1Ax. By using an internal voltage regulator, the power supply for the 1.1 V power domain can be set, and VDD1Ax can be connected to VDDCR through an external filter circuit. Different configurations can provide two effective power supply modes for the 1.1 V power domain, the mode corresponds to the table as follows ***Table 2-1. Power supply mode mapping table*** shown.

Table 2-1. Power supply mode mapping table

REG_EN pins	Supply Configuration
High	LDO power supply mode
Low	Bypass mode

The power supply mode is set by the hardware and when the pin REG_EN is set high, the internal LDO outputs 1.1 V to supply power to the $V_{1.1V}$ domain. When the pin REG_EN is low, 1.1 V must be brought in externally to supply power to the $V_{1.1V}$ domain.

2.1.4. Crystal power supply

To improve the stability of the clock circuit, a voltage regulator is integrated inside the GDSCN832xx series crystal that provides 1.1 V to the crystal circuit. The user can set the REG_EN pin high to enable OSC_LDO regulator and connect the VDD33 pin to a 3.3 V power

supply to power the crystal module. Placing the REG_EN low does not enable the regulator, and the OSCVDD11 pin is connected to an external 1.1 V power supply to provide power to the crystal module. Note: The OSCVSS pin must be grounded.

Table 2-2. Corresponding table of power supply mode of crystal oscillator power supply

REG_EN pins	Supply Configuration
High	OSC_LDO power supply mode
Low	Bypass mode

2.1.5. Power supply design

The system needs a stable power supply, and there are some important things to pay attention to when developing and using:

- VDD33 pin must be connected to an external capacitor (100 nF ceramic capacitor + 4.7 uF tantalum capacitor)
- VDDIO pins must be connected to external capacitors (N * 100 nF ceramic capacitors)
- VDDCR pins must be external capacitors (N * 100 nF ceramic capacitors + 1 uF ceramic capacitors + 470 pF ceramic capacitors)
- VDD3Ax pins must be external capacitors (100 nF + 4.7 uF ceramic capacitors recommended)
- The VDD1Ax pin must have an external capacitor (N * 100 nF ceramic capacitor)

Figure 2-1. GDSCN832xx series is recommended for power supply design(Enable internal voltage regulator)

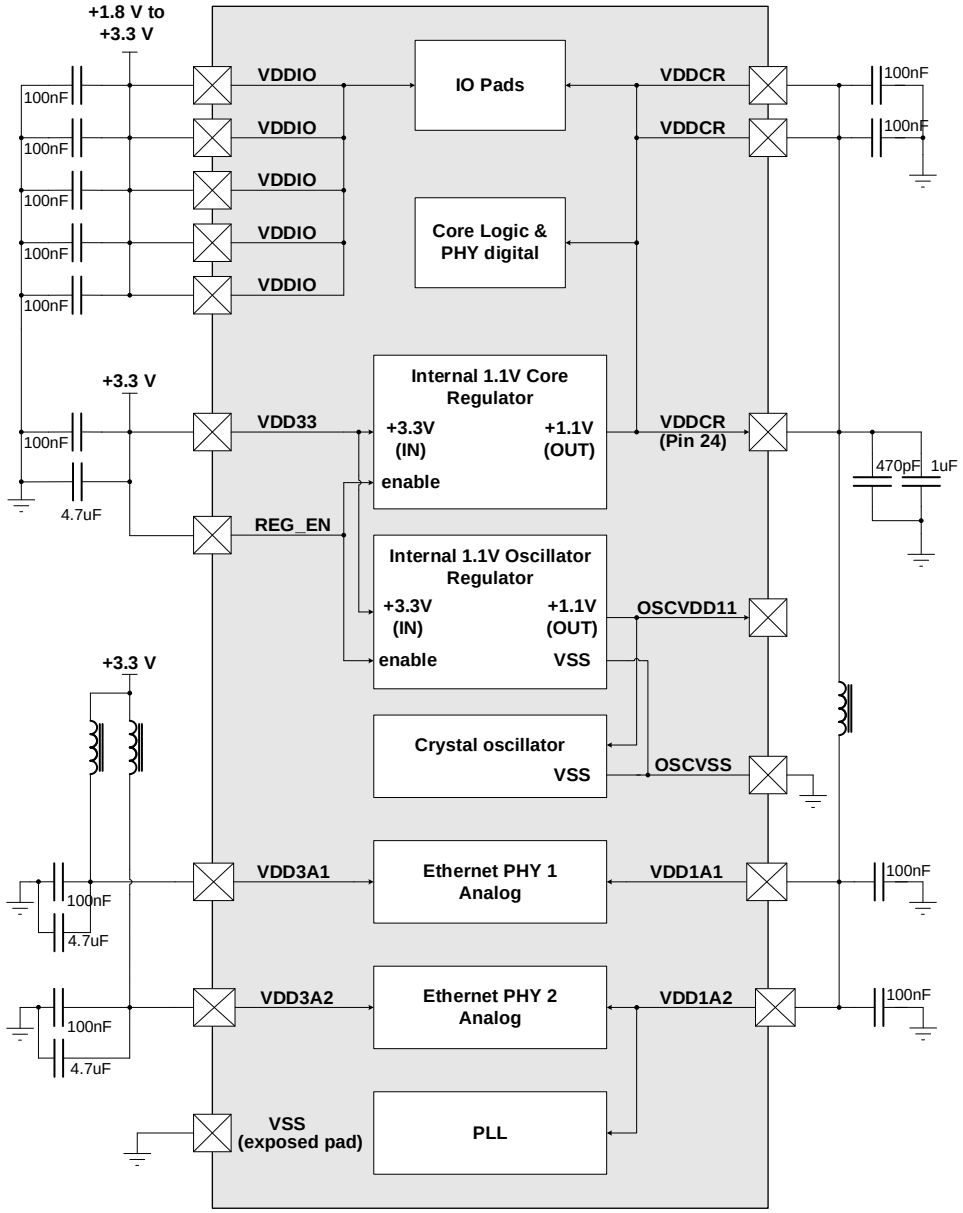
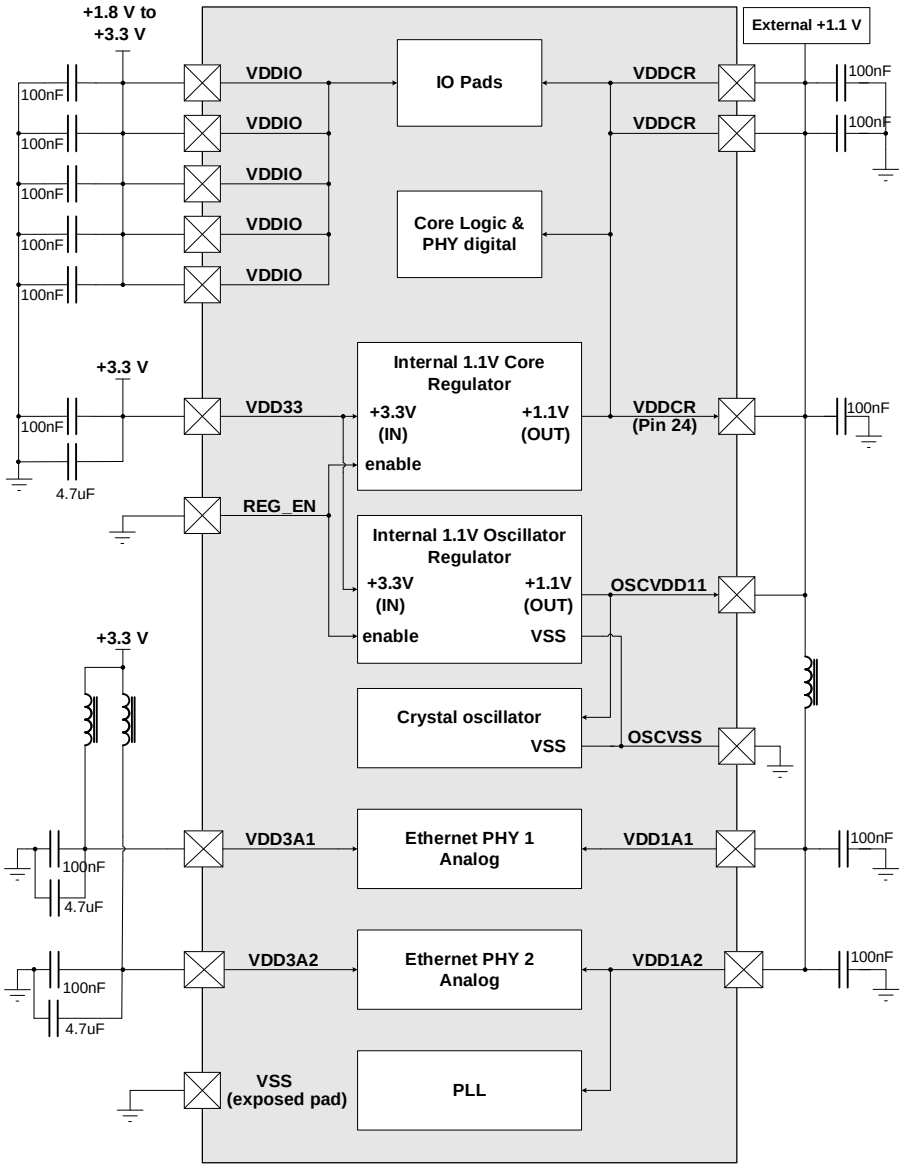


Figure 2-2. GDSCN832xx series is recommended for power supply design(Internal regulator not enabled)



Note:

1、 All decoupling capacitors must be placed close to the corresponding pins of VDD33, VDDIO, VDD3Ax, VDD1Ax, and VDDCR on the chip.

2、 All VDDCRs of the chip should be connected together, regardless of whether the internal regulator is enabled or not.

2.2. Reposition

The GDSCN832xx series reset control includes two types of reset: system reset and module reset. System reset includes power-on reset (POR), external pin reset (RSTN), and EtherCAT system reset to reset all circuits in the device. Module reset includes digital reset, PHY reset and EtherCAT kernel reset, which can reset the corresponding module.

POR (Power-On Reset) is a power-on reset that occurs when the device is powered on or re-powered after the power supply is disconnected. RSTN pin reset is an external pin reset that drives the RSTN input pin to a low level. The EtherCAT system reset is initiated by three consecutive sequences of special frames/commands.

Multi-Module Reset: Perform a digital reset by setting the DRST bits of the configuration register (RCU_RSTCFG). Digital reset resets all device submodules except the PHY.

Single-module reset: Single-module reset only the specified module. Single-module reset does not lock configuration pins, including PHY reset on port A, PHY reset on port B, and EtherCAT controller reset. The single-module reset description is as follows:

The PHY reset of port A can be achieved by using the PYARST bit in the Placement Reset Configuration Register (RCU_RSTCFG) or the MR_MAIN_REST bit in the Positioning PHY Control Register (PHY_MII_CTL). After the PHY reset of port A, the PHYRST bit and the soft reset bit are automatically cleared. This reset does not affect other modules of the device. The PHY reset of port A can be checked if the PHY reset is complete by resetting the PYAR bit in the configuration register (RCU_RSTCFG) or the MR_MAIN_REST bit in the PHY control register (PHY_MII_CTL).

The PHY reset of port B can be achieved by using the PHYBRST bit in the Placement Reset Configuration Register (RCU_RSTCFG) or the MR_MAIN_REST bit in the Placement PHY Control Register (PHY_MII_CTL). After the PHY reset of port B, the PHYBRST bit and the soft reset bit are automatically cleared. This reset does not affect other modules of the device. The PHY reset of port B can be checked if the PHY reset is complete by clearing the PHYBRST bit in the reset configuration register (RCU_RSTCFG) or the MR_MAIN_REST bit in the PHY control register (PHY_MII_CTL).

A separate reset of the EtherCAT controller can be achieved by clearing the ESCRST bits in the configuration register (RCU_RSTCFG), which will reset the EtherCAT core and its registers.

Figure 2-3. RCU_RSTCFG register

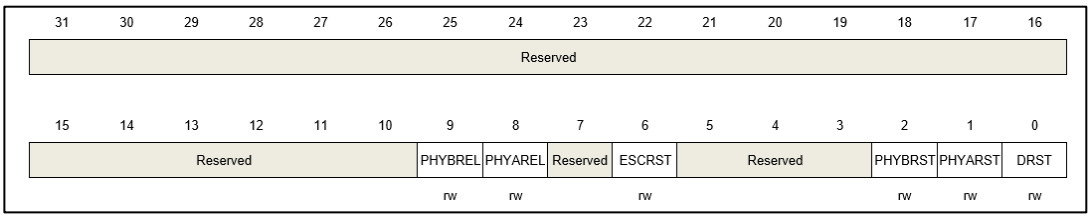
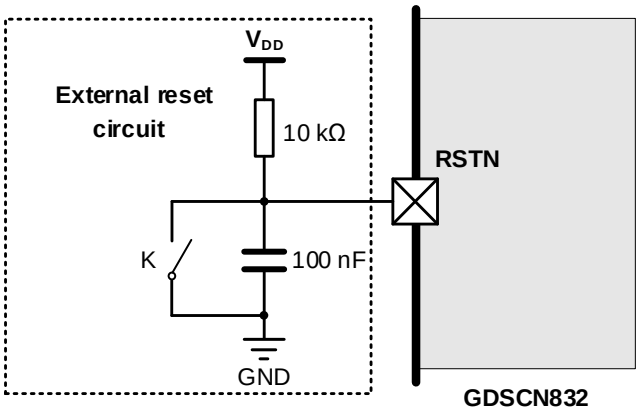


Figure 2-4. An external reset circuit is recommended



Note:

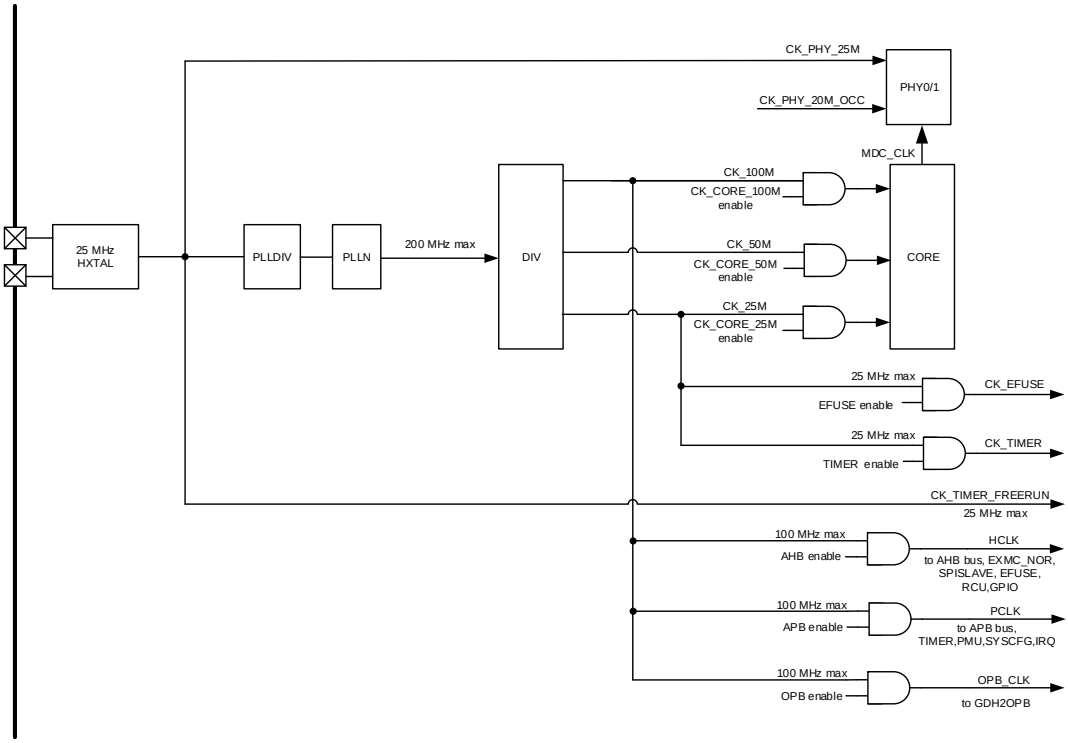
1. Externally connected pull-up resistor 10 kΩ.
2. If the influence of static electricity is considered, ESD protection diodes can be placed at the NRST pin.
3. Although the ESC has a hardware POR circuit inside, it is still recommended to add an external NRST reset resistor circuit.
4. If the ESC starts abnormally (due to voltage fluctuations, etc.), the capacitance value of NRST to ground can be appropriately increased to prolong the completion time of OSC reset and avoid the abnormal timing area of power-up.

2.3. Clock

GDSCN832xx series has a complete clock system inside, and the clock control unit is mainly composed of an external high-speed crystal oscillator (HXTAL) and a phase-locked loop (PLL). The clock is typically provided by the OSCIN and OSCOUT of the 25 MHz passive crystal oscillator, or by the OSCIN pin of the single-ended 25 MHz clock source driver. Clock main features:

- 25 MHz high-speed crystal oscillator (HXTAL)
- Phase-locked loop (PLL)

Figure 2-5. GDSCN832xx series clock tree



2.3.1. External high-speed crystal oscillation clock (HXTAL)

An external high-speed crystal oscillator at 25 MHz provides a more accurate clock source for the system clock. Crystals with specific frequencies must be connected with pins close to two HXTALs. The external resistance and capacitance connected to the crystal must be adjusted according to the oscillator chosen.

Figure 2-6. HXTAL external crystal circuit

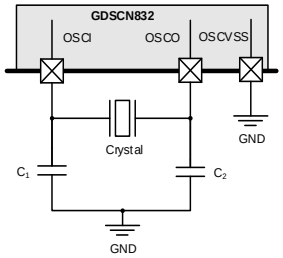
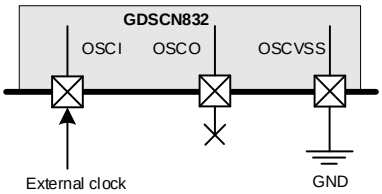


Figure 2-7. HXTAL external clock circuit



Note:

1. When using an active crystal oscillator, the signal is input from the OSCI and the OSCO remains in a suspended state.
2. For the size of the external matching capacitance, you can refer to the formula: $C_1 = C_2 = 2 * (C_{LOAD} - C_S)$, where C_S is the stray capacitance of the PCB and OSC pins, and the typical value is 10 pF. It is recommended to choose an external high-speed crystal, try to choose a crystal load capacitance of about 20 pF, so that the external matching capacitors C_1 and C_2 capacitors can be 20 pF, and the PCB layout is as close as possible to the crystal pins. For more content on resonator-based oscillator circuit design, please refer to《AN052 GD32 MCU Resonator-Based Clock Circuits》.
3. C_S is the parasitic capacitance on the PCB board traces and ESC pins, and the closer the crystal is to the ESC, the smaller the C_S and vice versa. Therefore, in practical application, when the crystal is far away from the OSC and the crystal works abnormally, the external matching capacitance can be appropriately reduced.
4. Accuracy: external active crystal oscillator> external passive crystal.
5. When the active crystal oscillator is used normally, Bypass will be turned on. At this time, the high level is required to be no less than 0.7VDD, and the low level should not exceed 0.3VDD.
6. The traces connected to the OSC clock pins of the resonator may be inconsistent in the length of the traces connected to the OSCO and OSCI pins due to space constraints in the PCB layout routing. This will cause the stray capacitance introduced by the two PCB traces to be inconsistent, resulting in the load capacitance on both sides of the resonator not being equal at the value, and there needs to be a difference to match the actual PCB board. For this case, it is recommended to contact the resonator manufacturer to measure the actual value.

2.3.2. Clock output test mode

In order to debug the system and observe the clock situation, the IRQ pin output crystal clock can be realized by setting the IRQCKOUT bit of the INTC_CTL register to 1. In this case, the IRQ pin must be configured in push-pull output mode (IRQMODE = 1) for the best results.

2.4. Typical peripheral modules

2.4.1. GPIO circuit

Supports mode configurations with up to 35 general-purpose input/output pins (GPIOs). Each GPIO port will determine the current functionality of that port, including input/output modes, based on the chip's current operating mode. Each GPIO pin can be configured to pull up/down or float. When the pins are in output mode, the pins can be configured as push-pull/open-drain/open-source outputs.

- Each pin has a weak pull-up / pull-down function
- Push and pull / drain open / source output enable control
- configure the functions of the selected pins according to the chip pattern

When the chip is in different modes, each pin has a different function.

Digital IO mode: When PDI_TYPE = 0x04, AFIO is adjusted to Digital IO mode.

When PDI_TYPE = 0x80 and the MCU_PDI_TYPE pin is 1, AFIO adjusts to EXMC mode.

SPI Mode: When the PDI_TYPE is equal to 0x80 and the pin of the MCU_PDI_TYPE is equal to 0, AFIO adjusts to SPI mode.

Table 2-3. GPIO configuration table

Schema name	Register / signal	Description

EXMC	pdi_type / mcu_pdi_type / sip_mode	pdi_type == 0x80;
		mcu_pdi_type == 1'b1;
		sip_mode == 1'b0

GAVE	pdi_type / sip_mode	pdi_type == 0x04; sip_mode == 1'b0

spi8w_gpio	pdi_type / mcu_pdi_type / spi_ext_mode / sip_mode / line_mode	pdi_type == 0x80;
		mcu_pdi_type == 1'b0;
		sip_mode == 1'b0;
		line_mode == 2'b11;
		LINKACTLED1 pin must be pulled down externally

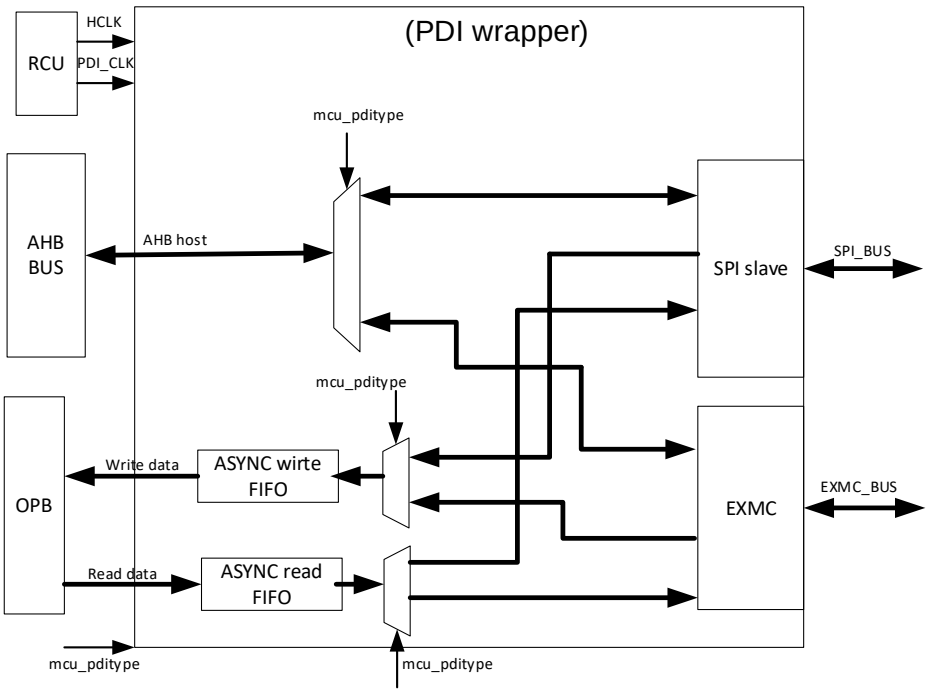
spi4w_mii_down	pdi_type / mcu_pdi_type / spi_ext_mode / sip_mode / line_mode / chip_mode	pdi_type == 0x80;
		mcu_pdi_type == 1'b0;
		sip_mode == 1'b0;
		line_mode == 2'b10;
		chip_mode == 2'b10
		LINKACTLED1 pin must be pulled up on the outside

spi4w_mii_up	pdi_type / mcu_pdi_type / spi_ext_mode / sip_mode / line_mode / chip_mode	pdi_type == 0x80;
		mcu_pdi_type == 1'b0;
		sip_mode == 1'b0;
		line_mode == 2'b10;
		chip_mode == 2'b11;
		LINKACTLED1 pin must be pulled up on the outside

2.4.2. Bus interface (PDI Wrapper) circuit

In GDSCN, EXMC and SPI SLAVE are encapsulated as a wrapper for system integration. The PDI Wrapper is used to select data between SPI and EXMC. Two asynchronous FIFOs are integrated inside, each 16 x 32-bit. SPI SLAVE and EXMC can only work one at a time, selected by the MCU_PDITYPE (IO16) pin.

Figure 2-8. PDI Wrapper block diagram



SPI slave and EXMC cannot be valid at the same time. The SPI slave or EXMC accesses the registers via the AHB channel and the kernel RAM data via asynchronous read FIFO and asynchronous write FIFO. The data path of EXMC is the same as that of the SPI slave. MCU_PDITYPE pin selection of the working access interface module. When the MCU_PDITYPE pin is 0, only the SPI slave can access the internal data. When the MCU_PDITYPE pin is 1, only EXMC can access the internal data. PDI_CLK provides clocks for SPI_SLAVE, EXMC, and ASYNC_FIFO. When the pin of the MCU_PDITYPE is 0, the PDI_CLK is from SPI_SCK. When the pin of the MCU_PDITYPE is 1, the PDI_CLK is from EXMC_CLK. HCLK is a 100MHz system clock that provides clocks for ASYNC_FIFO, SPI_SLAVE, and EXMC.

2.4.3. Ethernet PHYS

GDSCN contains two voltage PHYs A and B, which are functionally identical. PHY A is connected to EtherCAT port 0 or 2. PHY B is connected to EtherCAT port 1. These PHYs interface with their respective MACs via internal MII interfaces. Can be configured for full-duplex 100 Mbps (100BASE-TX) Ethernet operation. All PHY registers follow IEEE 802.3 regulations for MII management registers and are fully configurable.

- Fully compliant with IEEE 802.3 100 Base-TX standard and supports EEE
- Auto-negotiation and parallel detection capabilities for automatic speed and duplex selection
- Support MII interface
- Holds plug-and-play Auto-MDIX functionality

- Programmable loopback mode for diagnostics
- Support programmable LED output for different applications, power on self-test LED
- Supports WOL(WAKE-UP on-Lan) function

Figure 2-9. PHY function module diagram

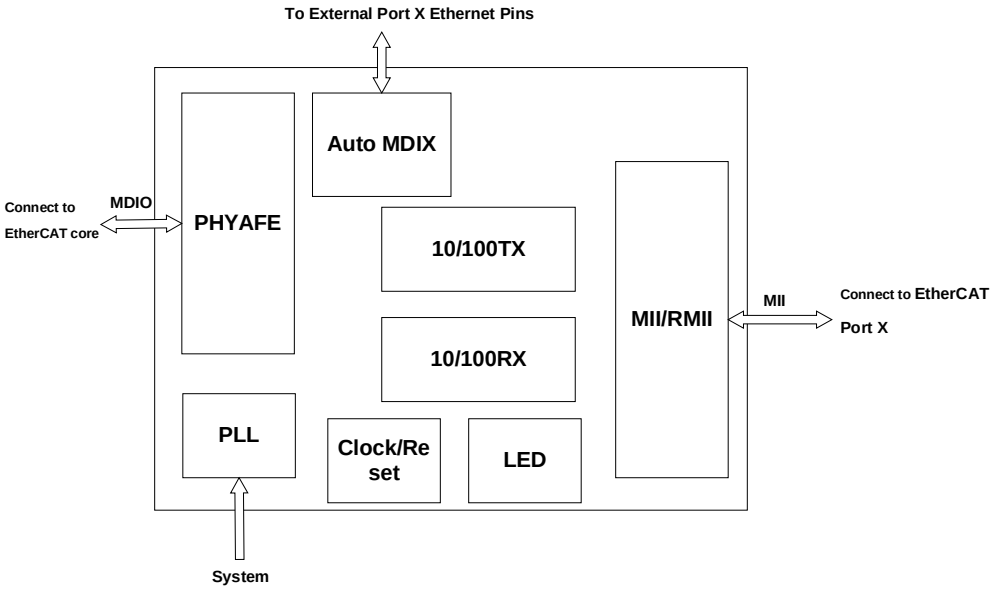
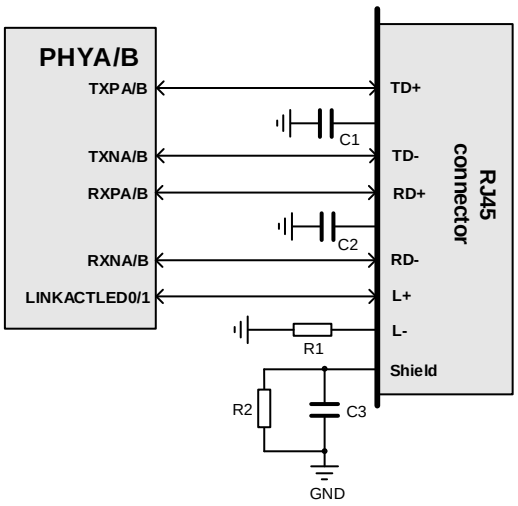


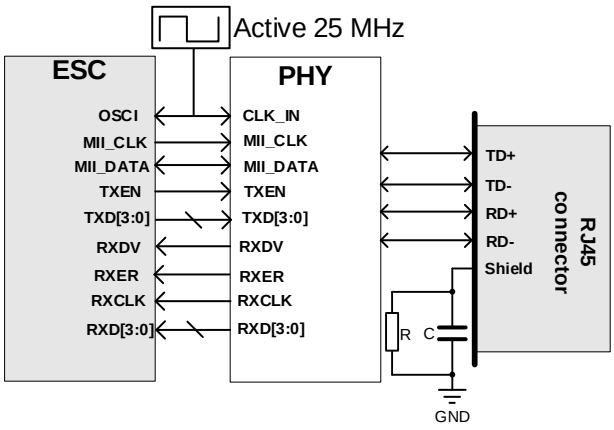
Figure 2-10. Built-in PHY and RJ45 network port (with transformer inside.)) connection diagram



Recommend：R1 = 470 Ω，R2 = 1 MΩ，C1 = 0.1 uF，C2 = 0.1 uF，C3 = 4.7 nF。

GDSCN provides a MII interface for external PHYs. Schematic diagram using external PHY connections is shown below ***Figure 2-11. Schematic diagram of connection using an external PHY*** shown.

Figure 2-11. Schematic diagram of connection using an external PHY



Note: When using an external PHY to connect with the OSC chip, the same active clock needs to be used.

2.5. Low power mode type

Power consumption design is one of the issues that GDSCN832xx series of products pay more attention to. The power management unit (PMU) offers four device-level energy-saving modes and three module-level energy-saving modes, including MOD0, MOD1, MOD2, and MOD3 at the device level, and EtherCAT clock management, PHY power management, and LED pin power management. These modes reduce power consumption and allow applications to achieve the best trade-off between conflicting requirements between device uptime, speed, and power consumption. The PMU also supports wake-up event detection and power management event (PME) notification.

The PME module handles latching functions for EDWOLASTAT and EDWOLBSTAT bits in PMU_CTL registers. You can refer to it ***Figure 2-12. PME outage pending*** to understand the logic of PME interrupt control. If EDWOLAEN or EDWOLBEN is placedWhen an energy detection/WoL event occurs in the PHY of port A or B, the PMEIF bit in the interrupt status register will be placed. When the PMWUPCFG is placed, the PME event can automatically wake up the system in some device-level energy-saving modes.

Figure 2-12. PME outage pending

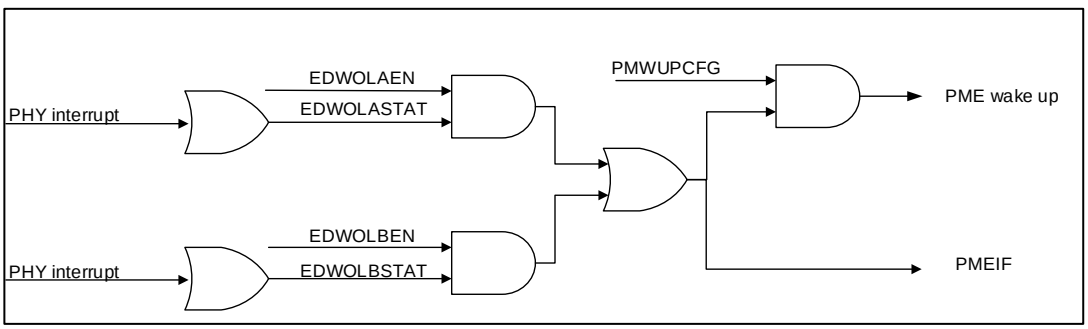
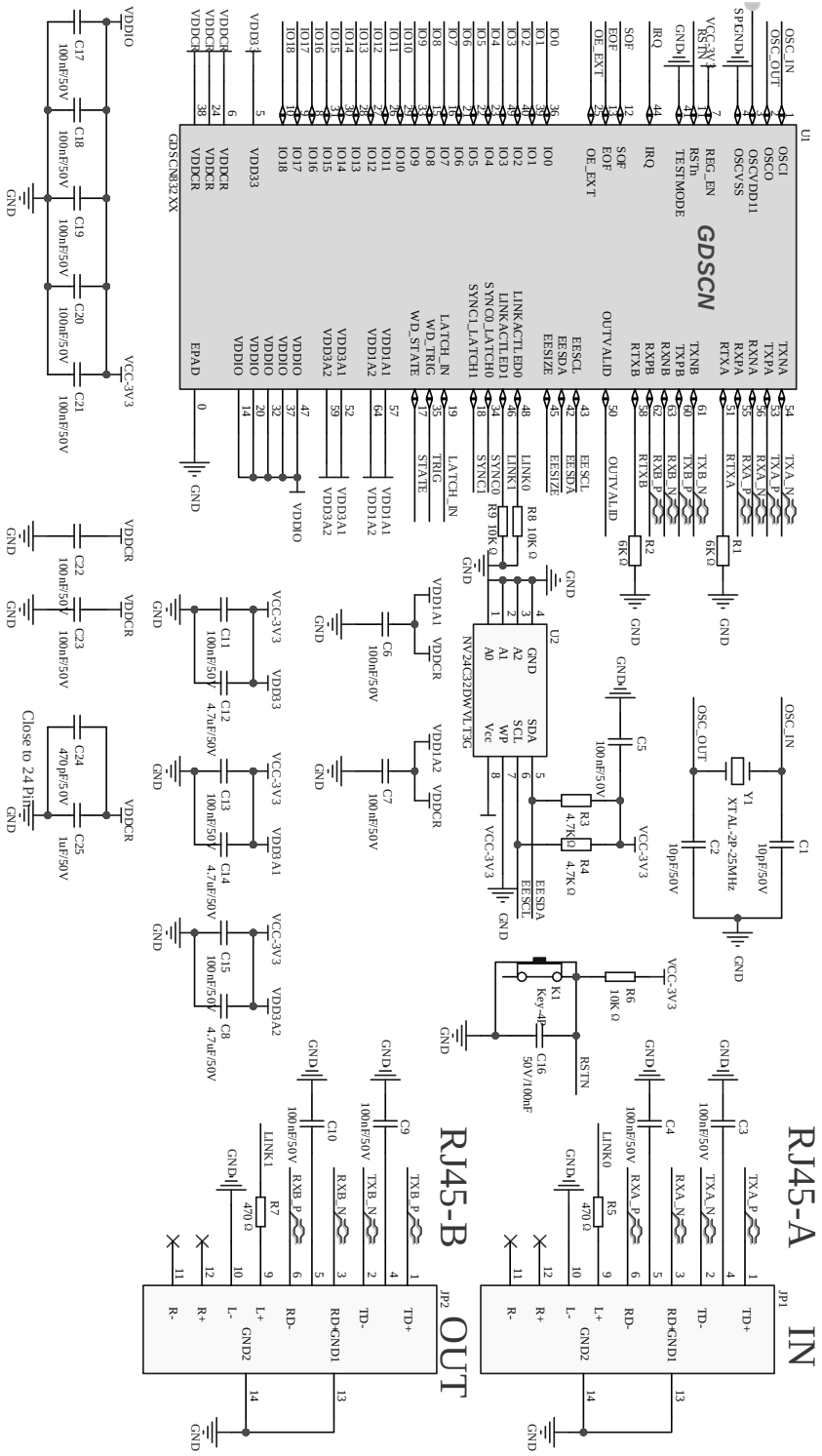


Table 2-4. Summary of energy-saving mode

Mode	PLL	System clocks	Network clocks	XTAL
MOD0	ON	ON	usable	ON
MOD1	ON	OFF	usable	ON
MOD2	OFF	OFF	usable	ON
MOD3	OFF	OFF	OFF	OFF

2.6. Refer to the schematic design

Figure 2-13. GDSCN832xx recommend referring to the schematic design



3. PCB Layout design

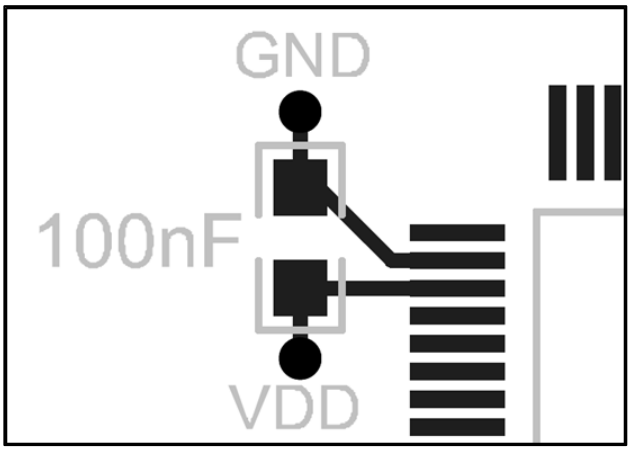
In order to enhance the functional stability and EMC performance of OSC, it is necessary to consider not only the performance of supporting peripheral components, but also the PCB layout. In addition, if conditions permit, try to choose a PCB design scheme with independent GND layer and independent power layer, which can provide better EMC performance. If conditions do not allow it, it is not possible to provide independent GND layer and power supply layer, then it is also necessary to ensure a good power supply and grounding design, such as trying to make the integrity of the GND plane under the OSC as much as possible, with EPAD packaging, PCB layout recommends EPAD grounding, etc.

In applications with high power or strong interference, consider keeping the OSC away from these sources of interference.

3.1. Power supply decoupling capacitors

GDSCN832xx series power supply has VDD33, VDD3Ax, VDDIO, VDD1Ax, VDDCR and other power supply pins, and the 100 nF decoupling capacitor can be used as a ceramic MLCC, and the position needs to be as close to the power pin as possible. The power supply trace should be as much as possible so that it passes through the capacitor before reaching the OSC power pin, and it is recommended to punch holes near the capacitor PAD.

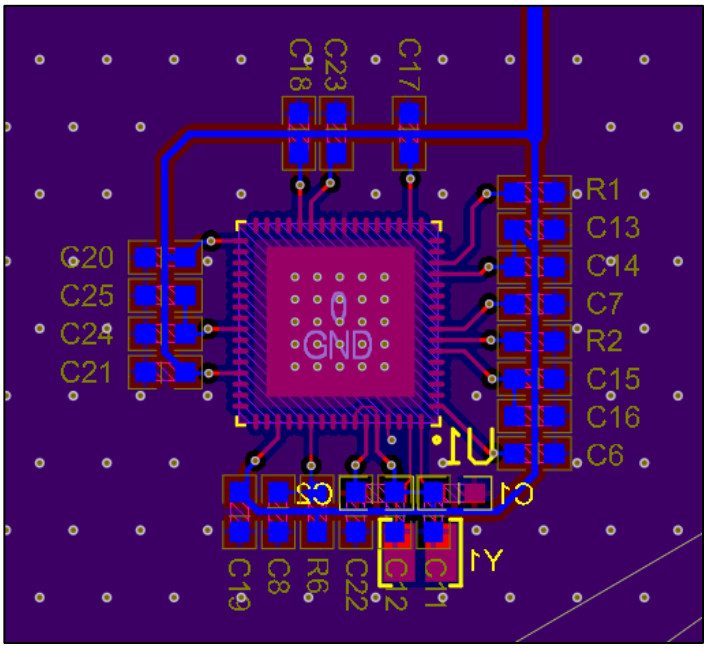
Figure 3-1. Power pin decoupling Layout design is recommended



3.2. 1.1V power domain circuit

The current 1.1V supply domain recommends SMPS power supply mode or bypass mode. In order to enhance the functional stability and EMC performance of OSC, power supply circuits need to consider not only the performance of supporting peripheral components, but also the PCB layout.

Figure 3-2. Internal LDO power supply mode recommended layout diagram



PCB layout in bypass mode needs to follow the following requirements:

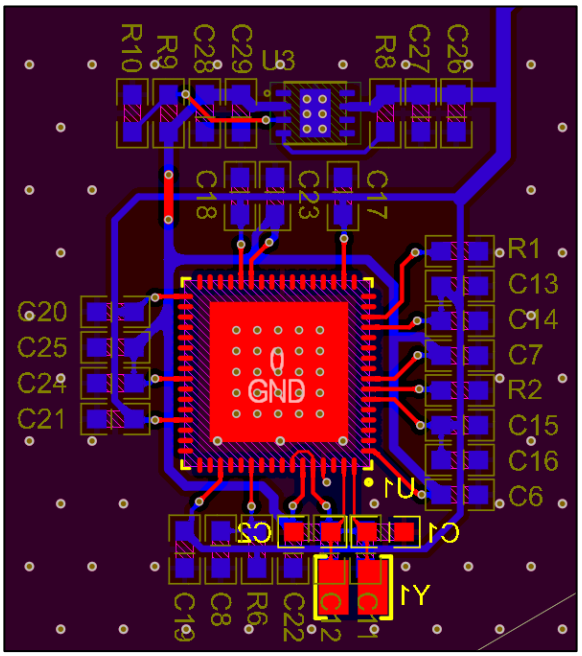
1、 When using an external power supply to power VDDCR, it is necessary to pay attention to the line loss caused by the line resistance in the case of high output current to avoid the terminal voltage being lower than the specified requirements.

2、 Heat dissipation measures need to be taken to avoid heat generation from the external power supply affecting the heat dissipation and its own performance.

3、 Be sure to connect the VDDCR pins of the chip to the external power output.

Bypass mode recommended layout such as ***Figure 3-3. Bypass mode recommends layout diagrams*** shown:

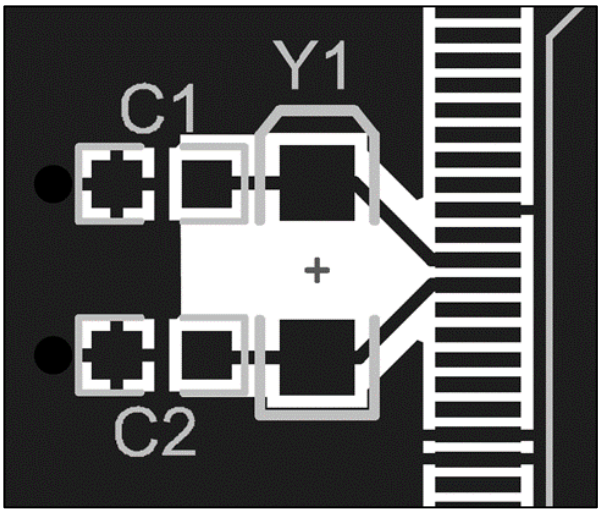
Figure 3-3. Bypass mode recommends layout diagrams



3.3. Clock circuit

GDSCN832xx series clocks have XTAL, which requires the clock circuit (including crystals, crystal oscillators, capacitors, etc.) to be placed close to the OSC clock pins, and the clock traces are wrapped in GND as much as possible.

Figure 3-4. Recommended Clock Pin Layout Design (Passive Crystal)



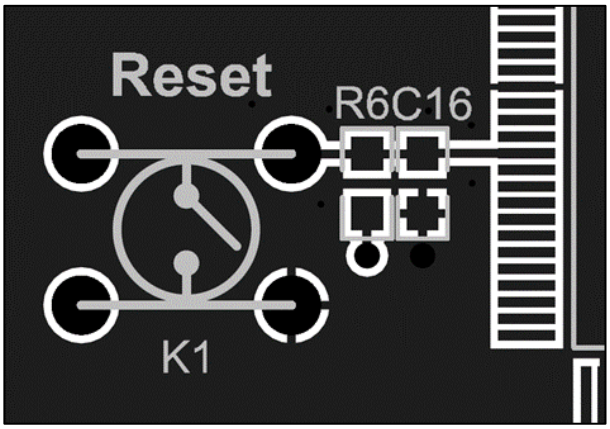
Note:

1. The crystal should be as close to the OSC clock pin as possible, and the matching capacitor should be as close to the crystal as possible.
2. The whole circuit should be on the same layer as the OSC as much as possible, and the wiring should not be passed through the layer.
3. The PCB area of the clock circuit should be empty as much as possible, and no traces unrelated to the clock should be taken.
4. high-power, strong interference risk devices and high-speed traces should be kept away from clock crystal circuits as much as possible.
5. The clock line is covered with ground to play a shielding effect.

3.4. Reset circuit

RSTN Routing PCB Layout is as follows:

Figure 3-5. RSTN Layout design is recommended

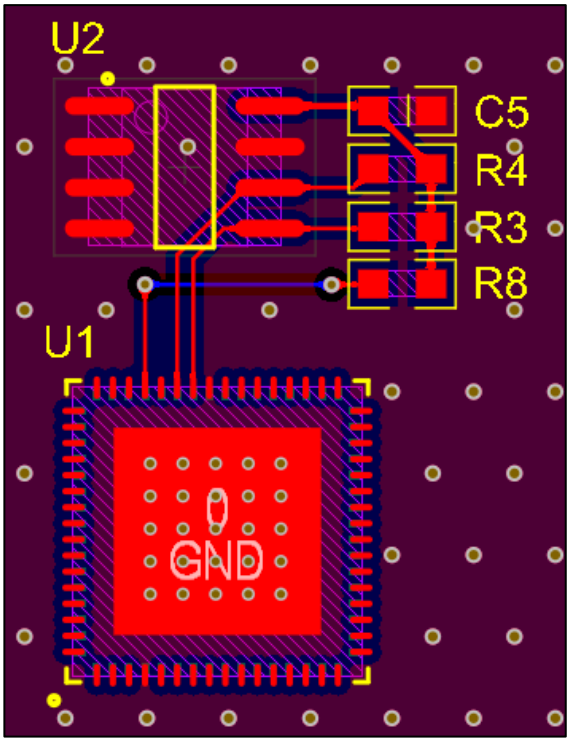


Note: The reset circuit resistor should be as close to the RSTN pin as possible, and the RSTN trace should be as far away as possible from strong interference risk devices and high-speed traces.

3.5. I2C circuit

For the GDSCN832xx series I2C module, there are two signal lines, EESCL and EESDA, which need to be connected to the resistor and pulled up to the power supply VDD33. When the capacity of the EEPEOM chip is greater than 16K, the EESIZE pin needs to be pulled up to the power supply VDD33 through the resistor, otherwise it needs to be pulled down to GND.

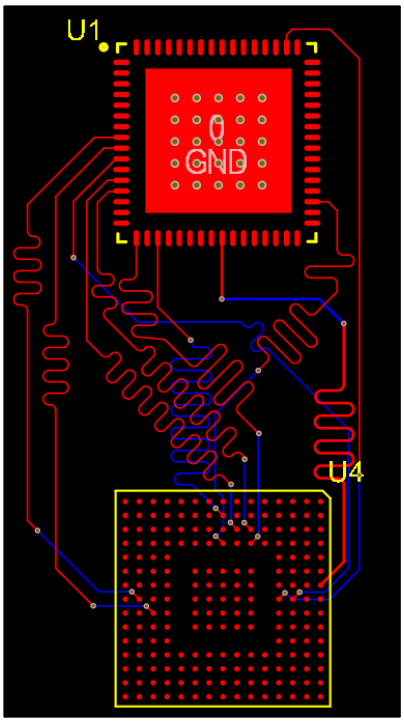
Figure 3-6. Recommended I2C Trace Layout design



3.6. OSPI circuit

The GDSCNxx series OSPI modules support two-wire, four-wire, and eight-wire SPI. When using OSPI communication, the IO16 pin needs to be pulled down to GND through the resistor, and the OSPI trace PCB layout is as follows:

Figure 3-7. OSPI Layout design is recommended



Note:

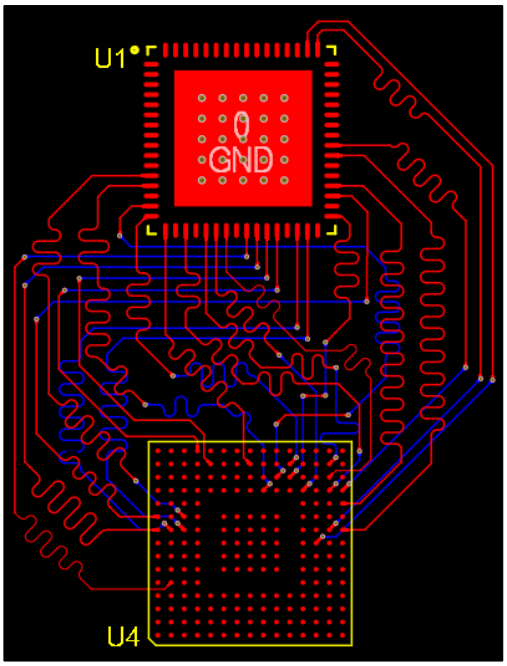
1. Avoid signal traces from crossing the power supply segmentation area and keep the signal reference plane intact.
2. The signal line and clock line of OSPI should be traced on the surface layer as much as possible and cover the ground, and the equal length should be controlled within 300 mil (the serpentine trace spacing of the microstrip line is recommended to be 7H, and the serpentine trace spacing of the ribbon line is recommended to be 5H, and H is the distance from the signal trace to the reference plane; If there are vias in the trace, generally a via is counted as 50 ~ 100 mil line length, which is determined by the length of the via).
3. OSPI chips should be placed as close to the ESC as possible, away from interference sources such as power supplies and power devices.
4. If the signal line or clock line signal is poor, consider adding a termination resistor on the memory side.

3.7. EXMC circuit

When the GDSCNxx series uses EXMC communication, the IO16 pin needs to be pulled up

to VDD33 through the resistor, and the EXMC trace PCB layout is as follows:

Figure 3-8. EXMC Layout design is recommended



Note:

1. Avoid signal traces from crossing the power supply segmentation area and keep the signal reference plane intact.
2. The signal line and clock line of EXMC should be traced on the surface layer as much as possible and cover the ground, and the equal length should be controlled within 300 mil (the serpentine trace spacing of the microstrip line is recommended to be 7H, and the serpentine trace spacing of the ribbon line is recommended to be 5H, and H is the distance from the signal trace to the reference plane; If there are vias in the trace, generally a via is counted as 50 ~ 100 mil line length, which is determined by the length of the via).
3. EXMC chips should be placed as close to the ESC as possible, away from interference sources such as power supply and power devices.
4. If the signal line or clock line signal is poor, consider adding a termination resistor on the memory side.

3.8. Ethernet interface circuit

GDSCN832xx series integrates two voltage PHYs, each PHY module has TXPx, TXNx, RXPx, RXNx two pairs of differential signal lines, if connected to an external PHY, the PHY chip will also lead to TXPx, TXNx and RXPx, RXNx two pairs of differential signal linesIt is recommended that the PCB routing requires a characteristic impedance of 100 Ω, and the differential routing is strictly in accordance with the rules of equal distance and equidistant, and the trace is as short as possible. If the two differential lines are of unequal length, the short line can be compensated for by a serpentine line at the end.

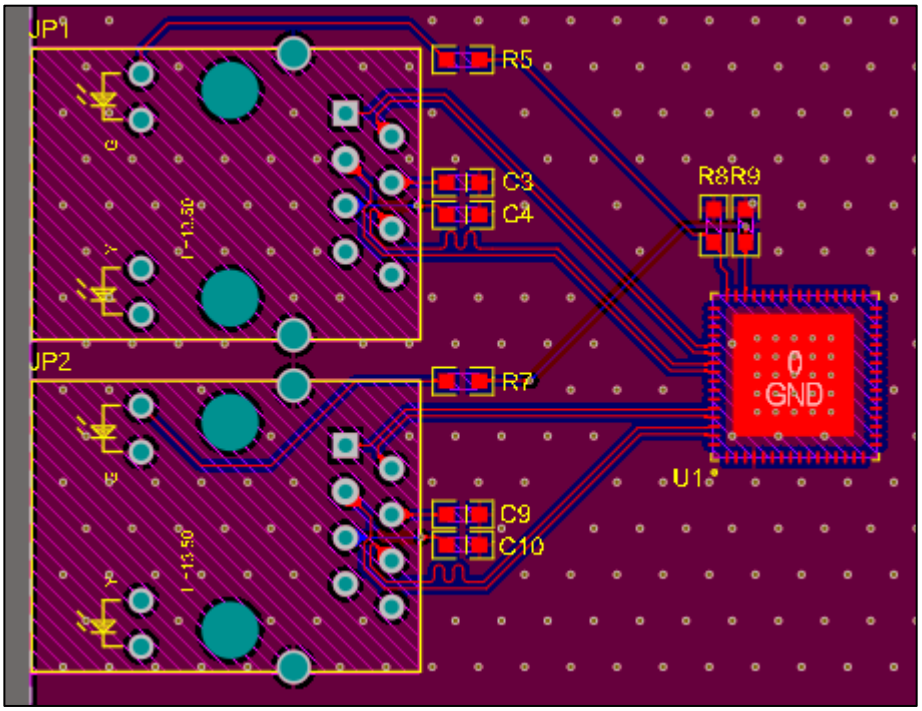
The precautions for TXPx, TXNx, and RXPx, RXNx differential traces are as follows:

1. The layout is reasonably placed to shorten the differential trace distance.
2. Priority should be given to drawing differential lines, and there should be no more than two pairs of vias on a pair of differential lines, and they need to be placed symmetrically.
3. Symmetrical parallel traces ensure that the two wires are closely coupled, avoiding 90°, arc or 45° traces.
4. The resistive capacitance, EMC and other devices or test points connected on the differential trace should also be symmetrical.

For external PHY chip modules, the data line and signal control line between the ESC and the external PHY should also be shortened as much as possible, and the serpentine wire needs to be treated with equal length, and the precautions are as follows:

1. The layout is reasonable, and the PHY chip and ESC are as compact as possible.
2. When routing, the length of the longest wire in the signal line is targeted, and the other signal wires can be compensated by serpentine traces.

Figure 3-9. Ethernet interface circuit routing layout design is recommended



4. Package Description

The GDSCN832xxxx series is available in one package, QFN64.

Table 4-1. Package Description

Product model	Package
GDSCN832xxR2U6	QFN64(9x9, 0.5 pitch)

(Dimensions in mm)

5. Revision history

Table 5-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Sep 22, 2025

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