GigaDevice Semiconductor Inc.

GD32MCU EMC

Application Note
AN062

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1. Introduction

As semiconductor process nodes shrink and performance improves, MCUs face increasingly complex electromagnetic environments. This means that both immunity to external noise and electromagnetic radiation become more intricate. This article specifically introduces the principles and characteristics of EMC for GD32 MCU products and provides corresponding recommendations based on experience gained from various applications.

2. Scope of EMC

2.1. EMC

EMC (electromagnetic compatibility) refers to the ability of a system to function fully and normally (without performance degradation). In a standard environment, electromagnetic compatibility requires that a device or system neither malfunctions due to interference from surrounding electromagnetic fields nor generates electromagnetic interference that affects other devices.

2.2. EMS

EMS (electromagnetic susceptibility) refers to the ability of a device or system to resist noise interference. A higher EMS level indicates better immunity to interference, whereas devices with lower EMS levels are extremely sensitive to electromagnetic environments, with their operational state being influenced by surrounding electromagnetic conditions. (Although "electromagnetic susceptibility" is often translated as "electromagnetic sensitivity" in many contexts, considering the difference between "susceptibility" and "sensitivity," we adopt the term "electromagnetic susceptibility.")

EMS primarily includes fast transient burst EFT/FTB and system-level electrostatic discharge ESD, which are measured to determine the reliability level of a device operating in non-ideal electromagnetic environments.

2.3. EMI

EMI (electromagnetic interference) refers to the level at which a device acts as a source of interference, emitting electromagnetic waves into the surrounding environment. The emitted electromagnetic waves are categorized into conducted emissions and radiated emissions. Conducted emissions propagate along cables or interconnect lines, while radiated emissions propagate through free space.

2.4. EMS&EMI test standard

Table 2-1. International Electrotechnical Commission standard table

Standard	Description
IEC61000-4-2	Electrostatic Discharge (ESD) Immunity Test
ISO10605	Road Vehicles - Test Methods for Electrical Disturbances from Electrostatic Discharge
IEC61000-4-4	Electrical Fast Transient (EFT) Immunity Test

IEC61967-2	Integrated Circuit Radiated Emission Test - TEM Cell Method
IEC61967-4	Integrated Circuit Conducted Emission Test - 1Ω/150Ω Direct Coupling Method
IEC61967-8	Integrated Circuit Radiated Emission Test - Stripline Method

According to IEC62132-1, the system-level ESD and EFT failure modes for MCUs can be classified into five levels. Among them:

Level A: No issues observed.

Levels B, C, D: Represent various types of soft failures.

Level E: Hard failure occurs.

Table 2-2. IEC62132-1 MCU failure mode levels

Level	Description
A	Unaffected: During and after pulse injection, ESD interference does not affect the chip.
B	Automatic Recovery: During pulse injection, the chip operates abnormally, but returns to normal after the pulse injection ends.
C	Manual Recovery: During pulse injection, the chip operates abnormally and does not automatically return to normal after the pulse injection ends. However, with manual intervention (reset), the chip resumes normal operation.
D	Power Cycling Required: During and after pulse injection, the chip cannot operate normally (reset is ineffective). Only by power cycling the chip can it return to normal operation, typically due to latch-up phenomena.
E	Hard Failure: ESD pulse injection causes physical damage to the chip.

3. EMS Theory

3.1. EMS (electromagnetic susceptibility)

EMS primarily includes system-level Electrostatic Discharge (ESD) and Electrical Fast Transient/Burst (EFT/FTB). The EMC characteristics in the GD32 MCU Datasheet encompass system-level EMS electromagnetic immunity and absolute electrical sensitivity test results.

Figure 3-1. EMS Parameters in the Datasheet

System level ESD (Electrostatic discharge, according to IEC 61000-4-2) and EFT (Electrical Fast Transient/burst, according to IEC 61000-4-4) testing result is given in the ***Table 4-12. System level ESD and EFT characteristics***(1). System level ESD is for end-customer operation, it includes ESD field events on system level occur in an unprotected area (outside EPA). System level ESD protection necessary to satisfy higher ESD levels.

Table 4-12. System level ESD and EFT characteristics(1)

Symbol	Description	Conditions	Package	Class	Level
V_{ESD}	Contact / Air mode high voltage stressed on few special I/O pins	V_{DD} = 3.3 V, T_J = 25 °C, f_{HCLK} = 600 MHz IEC 61000-4-2	BGA176	CD 8kV AD 15kV	4A
			LQFP176	CD 8kV AD 15kV	4A
V_{EFT}	Fast transient high voltage burst stressed on Power and GND	V_{DD} = 3.3 V, T_J = 25 °C, f_{HCLK} = 600 MHz IEC 61000-4-4	BGA176	4kV	4A
			LQFP176	4kV	4A

(1) Value guaranteed by characterization, not 100% tested in production.

System-level EMS testing involves powering up the minimal system and running the GD32 MCU to evaluate system robustness in application scenarios. The program logic is represented by two LEDs performing sequential switching to indicate normal operation. By applying system-level ESD or EFT to the running MCU, the system is monitored in real-time during interference testing to determine whether soft failures (system disturbances) or hard failures occur.

Absolute electrical sensitivity includes chip-level ESD (HBM/CDM) and latch-up (LU). Chip-level ESD (HBM/CDM) and LU testing are conducted on unpowered devices. After the test, functional and integrity checks of MCU pins are performed through FT testing.

3.2. System-level ESD test

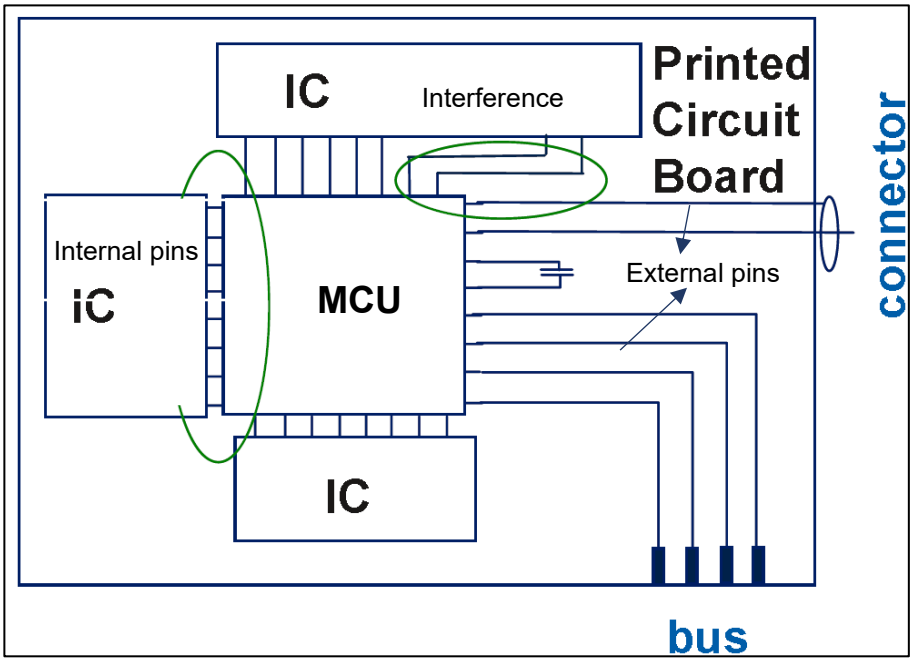
This test is performed on all GD32 series MCUs, where each test pin is subjected to 10 positive/negative voltage pulses at each level, progressing from lower to higher levels until

abnormal phenomena occur. This allows for internal fault investigation of the chip, but does not provide additional application protection circuits to safeguard sensitive MCU pins from ESD effects.

Two test pins are selected to cover both 5VT and non-5VT pins, positioned centrally between the two power pins (VDD and GND). Additionally, the test pins are preferably chosen from external pins. As the MCU serves as the control core, it inevitably needs to connect with external ports, where connectors or buses introduce a higher risk of ESD. We define MCU pins directly connected to external systems as external pins. Furthermore, pins with layout traces adjacent to external pin traces are also at risk of interference. Pins not connected to external systems and not at risk of crosstalk from external pins are defined as internal pins. Generally, internal pins are less susceptible to system-level ESD risks. Therefore, external pin protection is crucial for system-level ESD defense.

The schematic diagram of external and internal pins is shown in ***Figure 3-2.***

Figure 3-2. External and internal pins

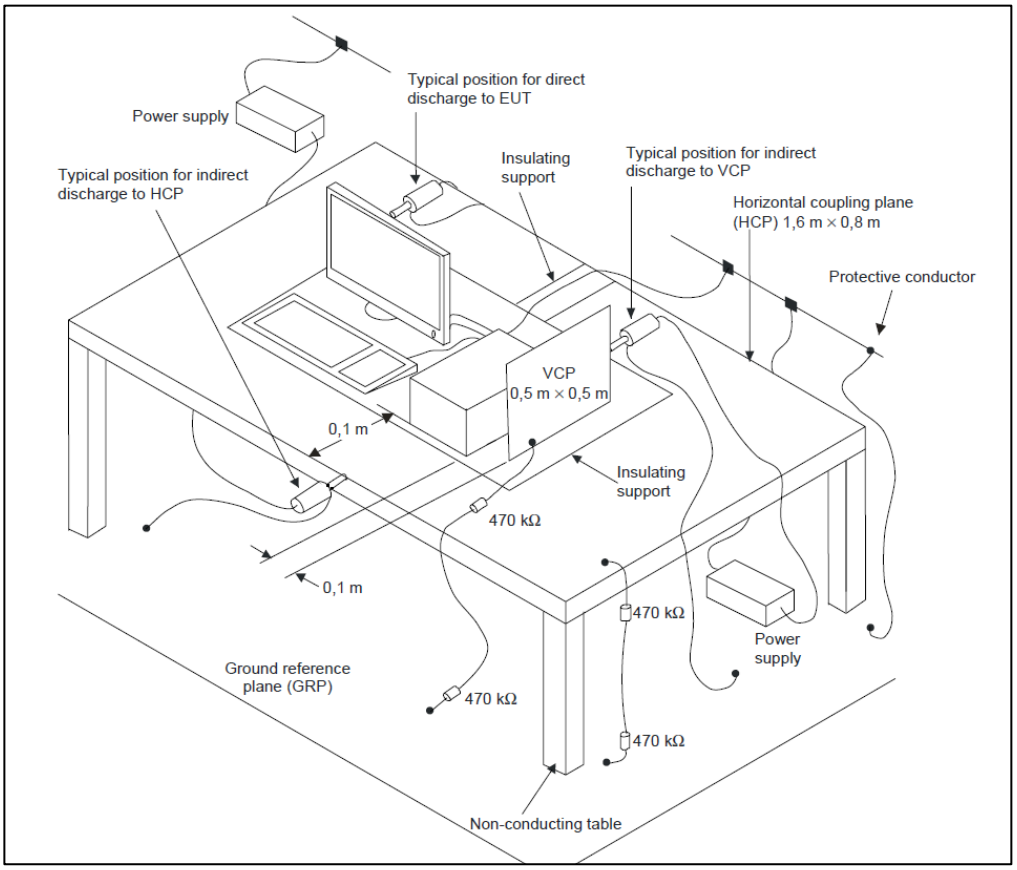


3.2.1. System-level ESD test setup

The equipment used for performing system-level ESD testing is an ESD generator compliant with the IEC 61000-4-2 standard, which directly applies discharge to the test pins of the MCU. Both contact discharge and air discharge are tested, with the test levels progressing from low to high. At each level, more than 10 positive and negative voltage static discharges are applied until system operation abnormalities occur.

The setup of the ESD workstation and grounding requirements are shown in ***Figure 3-3. IEC61000-4-2 Test setup and grounding requirements***.

Figure 3-3. IEC61000-4-2 Test setup and grounding requirements



3.2.2. System-level ESD test levels

System-level ESD test includes contact discharge (CD) and air discharge (AD). In contact discharge, the tip of the ESD gun directly contacts the metallic parts of the EUT (Equipment Under Test) to give static electricity. In air discharge, the rounded tip of the ESD gun is used to give static electricity onto non-metallic parts of the EUT, such as gaps, screens, and buttons. Both CD and AD are direct contact tests.

In addition to direct contact tests, there are indirect contact tests, where the ESD gun gives static electricity onto a horizontal coupling plane (HCP) and a vertical coupling plane (VCP). The coupling planes then indirectly radiate ESD to the EUT.

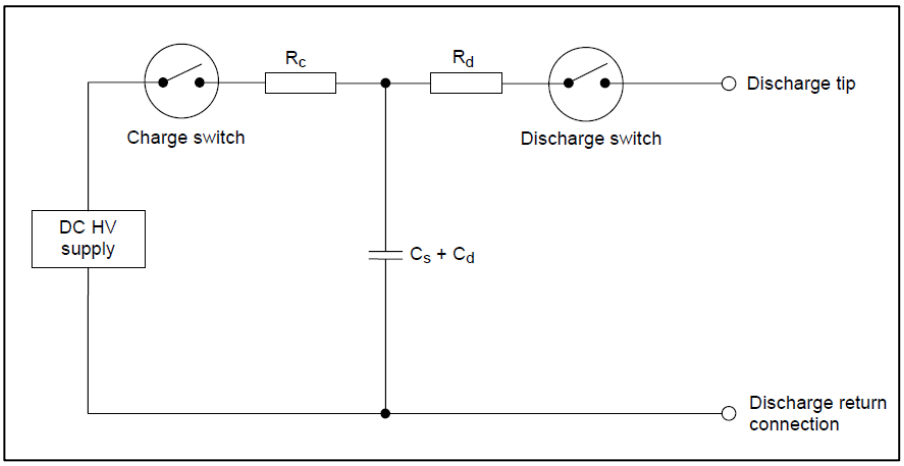
Table 3-1. System-level ESD test levels

Contact discharge		Air discharge	
Level	Test voltage(kV)	Level	Test voltage(kV)
1	2	1	2
2	4	2	4
3	6	3	8
4	8	4	15
Special(1)	Customization	Special	Customization
(1). Special refers to any level of voltage, whether higher, lower, or in between. The Special level is determined based on the specific application environment required for the particular equipment under test.			

3.2.3. System-Level ESD discharge waveform

The ideal discharge model of a system-level ESD generator is shown in ***Figure 3-4. The ideal discharge model of the system-level ESD generator***.

Figure 3-4. The ideal discharge model of the system-level ESD generator



The typical value of Cs+Cd is 150pF, and the typical value of Rd is 330 ohms. According to ISO10605, for automotive systems, the typical values of Cs+Cd are 150pF/330pF, and the typical values of Rd are 330 ohms/2000 ohms.

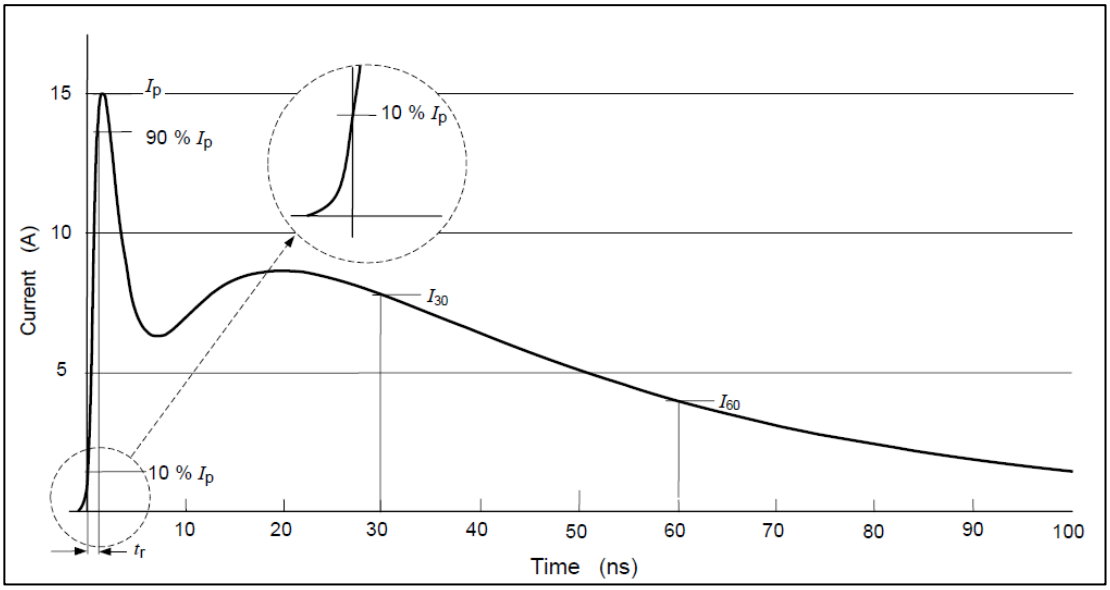
The parameters of the current waveform for contact discharge are shown in ***Figure 3-5. System-level ESD contact discharge current waveform parameters***.

Figure 3-5. System-level ESD contact discharge current waveform parameters

Level	Indicated voltage kV	First peak current of discharge ±15 % A	Rise time t_r (±25 %) ns	Current (±30 %) at 30 ns A	Current (±30 %) at 60 ns A
1 2 3 4	2 4 6 8	7,5 15 22,5 30	0,8 0,8 0,8 0,8	4 8 12 16	2 4 6 8
The reference point for measuring the time for the current at 30 ns and 60 ns is the instant when the current first reaches 10 % of the 1st peak of the discharge current. NOTE The rise time, t_r, is the time interval between 10 % and 90 % value of 1st peak current.					

The ideal 4kV contact discharge current waveform is shown in ***Figure 3-6. Ideal 4kV contact discharge current waveform***.

Figure 3-6. Ideal 4kV contact discharge current waveform



3.3. Electrical fast transient (EFT) test

When inductive loads (such as relays, motors, or encoders) are powered off, short-duration high-frequency transient pulses are generated on the power distribution system. Transient pulses can also occur when power is connected or disconnected. A common cause of power line transients is electrical arcing, which happens when an AC power line is connected, equipment is turned off, or circuit breakers are opened or closed. Transient noise in the power system can couple into terminal equipment through power lines.

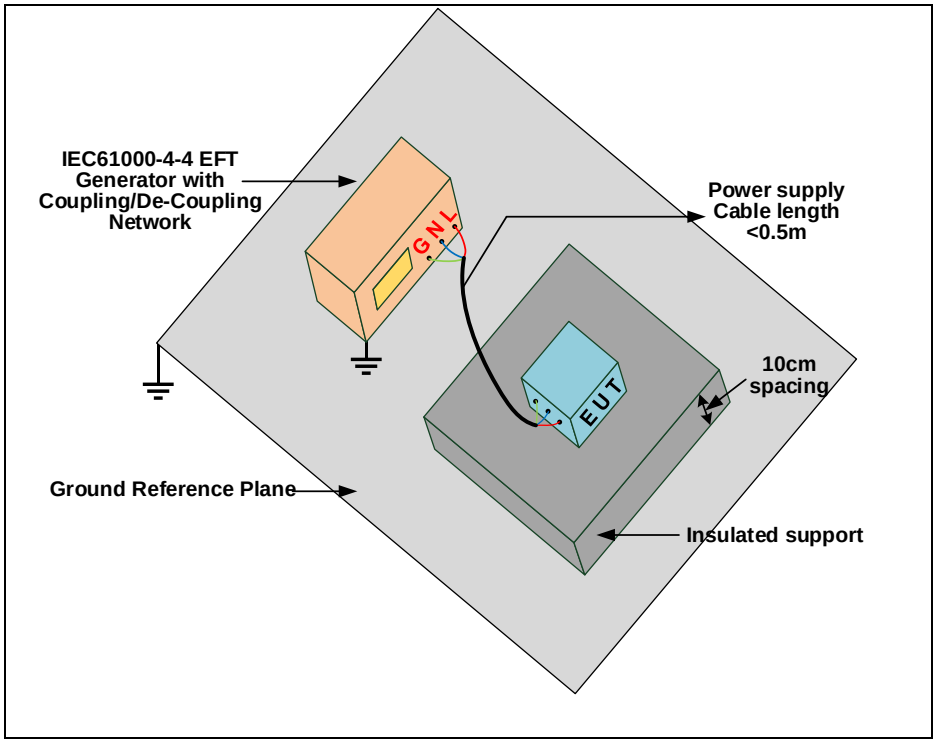
IEC 61000-4-4 specifies the test voltage waveform used to simulate transients caused by switching inductive loads on AC power lines. This standard also defines the immunity requirements for repetitive electrical fast transients and the testing methods required for systems.

Manufacturers use the EFT waveform defined by IEC 61000-4-4 to test the performance of equipment after exposure to fast transients. This test injects EFT pulses into the power lines, signal lines, control lines, and grounding connections of the equipment to simulate the coupling of transient noise on these lines. The pulse waveform is characterized by high amplitude (0.5 ~ 4 kV), short rise time, high repetition rate, and low energy.

There are multiple international standards specifying the transient immunity performance requirements for specific types of equipment. For example, the European Union's EN 55024 outlines the testing requirements and performance standards for information technology equipment. IEC 61547 specifies the testing requirements and performance standards for lighting equipment. All these standards derive their requirements and testing methods from IEC 61000-4-4.

3.3.1. EFT test setup

Figure 3-7. IEC 61000-4-2 Test setup and grounding requirements



The EFT test for GD32MCU uses the same test board as the ESD test. A DC current source is connected to the coupling front end of the EFT generator, and the power line is applied to the MCU through the coupling network.

Tests are conducted with 5kHz and 100kHz repetition frequencies, positive and negative polarities, as well as synchronous and asynchronous injection modes. The coupling methods include L1, N, and L1+N. Each level is tested sequentially from low to high, with each level tested for at least 60 seconds.

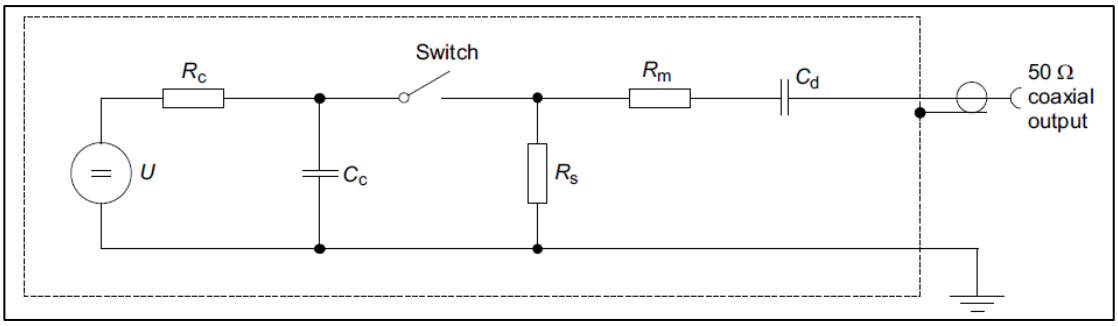
3.3.2. EFT test levels

Table 3-2. EFT test levels

Open circuit output test voltage and repetition frequency of the impulses				
Level	Power ports, earth port (PE)		Signal and control ports	
	Voltage peak kV	Repetition frequency kHz	Voltage peak kV	Repetition frequency kHz
1	0,5	5 or 100	0,25	5 or 100
2	1	5 or 100	0,5	5 or 100
3	2	5 or 100	1	5 or 100
4	4	5 or 100	2	5 or 100
X [a]	Special	Special	Special	Special
The use of 5 kHz repetition frequency is traditional, however, 100 kHz is closer to reality. Product committees should determine which frequencies are relevant for specific products or product types. With some products, there may be no clear distinction between power ports and signal ports, in which case it is up to product committees to make this determination for test purposes.				
[a] "X" can be any level, above, below or in between the others. The level shall be specified in the dedicated equipment specification.				

3.3.3. EFT waveform

Figure 3-8. The ideal discharge model of EFT generator



U: High-voltage source

Rc: Charging resistor

Cc: Energy storage resistor

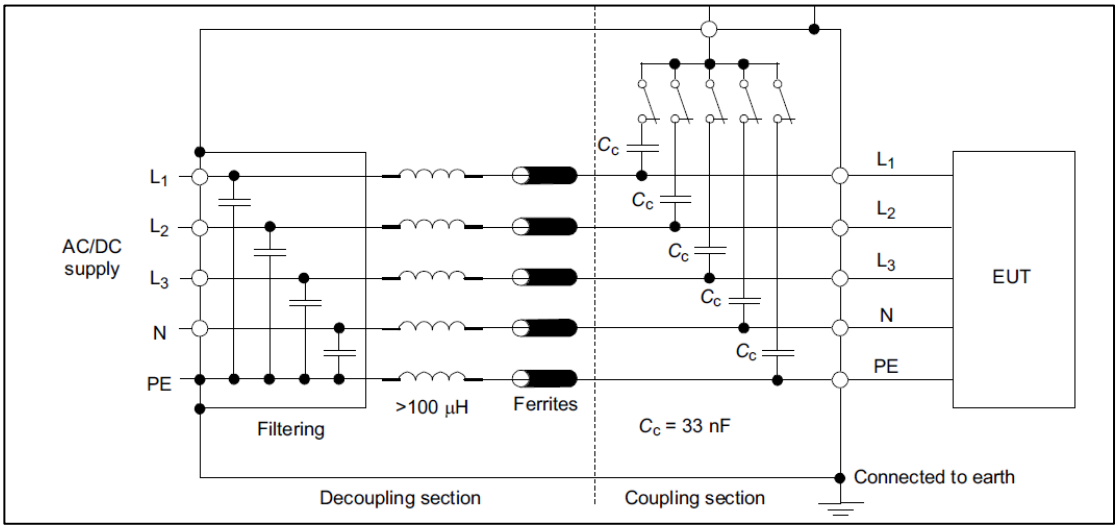
Rs: pulse secondary resistor

Rm: impedance matching resistor

Cd: DC limit capacitor

Switch: Hight voltage switch

Figure 3-9. EFT generator decoupling network model



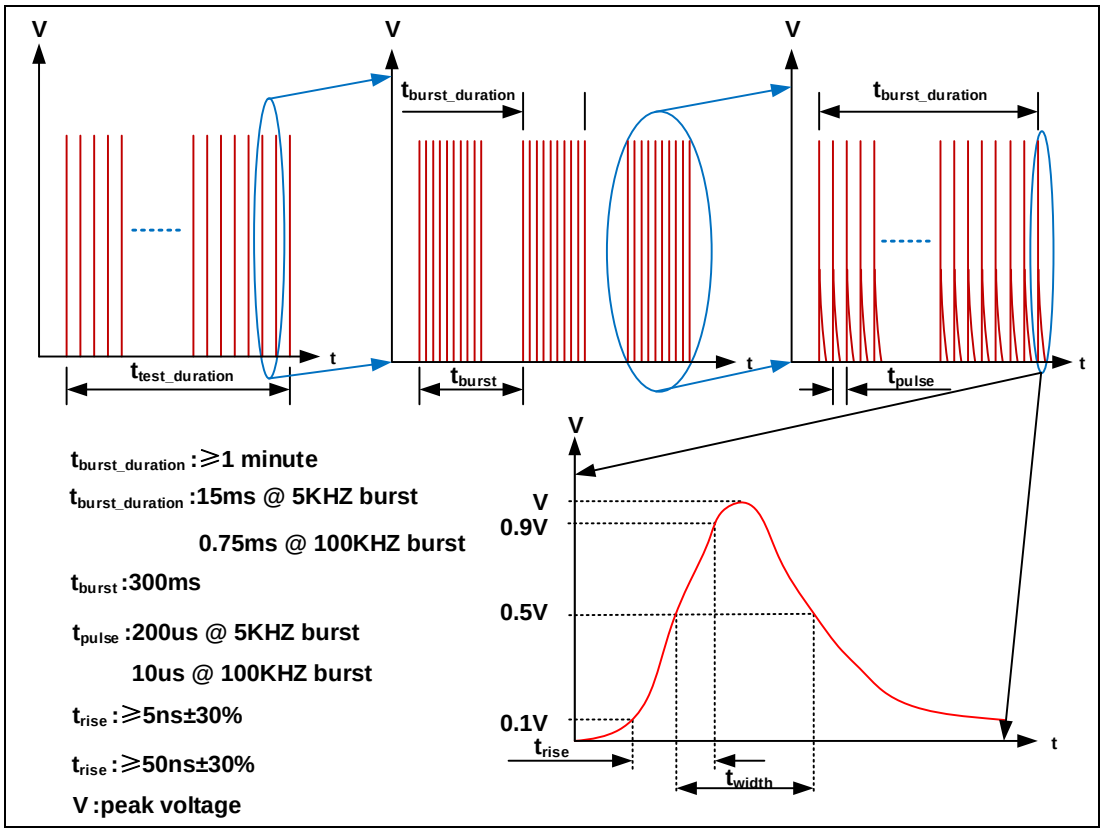
L1/L2/L3: Three-phase lines

N: Neutral line

PE: Protection earth

Cc: Coupling capacitor

Figure 3-10. EFT burst waveform parameters



4. Electrical Parameters

Discharges during manual operations may cause irreversible damage to integrated circuits, while discharges during automated mechanical operations can destroy even more integrated circuits. The chip-level ESD (Electrostatic Discharge) mechanisms differ in their discharge methods and causes when applied to integrated circuits or system devices. Based on different discharge scenarios, ESD discharge models are primarily categorized into three types: Human Body Model (HBM), Charged Device Model (CDM), and Machine Model (MM).

The failure characteristics we are usually concerned with include junction leakage, short circuits, gate oxide breakdown, and thermal damage. Since most current testing instruments have comprehensive protective measures for the MM model, the risk associated with the MM model has become relatively low. Each series of GD32 MCUs undergoes HBM and CDM testing, with the results documented in the datasheet.

The purpose of chip-level ESD testing is to evaluate the anti-static performance of the chip during processes such as wafer dicing, packaging, pre-shipment testing, transportation, PCB assembly, and mounting. Chip-level ESD occurs during non-powered operations within the ESD Protected Area (EPA). System-level ESD testing, on the other hand, measures the chip's performance in complex static environments encountered during actual use, which are outside the ESD-controlled area and mostly occur when the MCU is powered and the system is in operation.

The data in the datasheet is shown in ***Figure 4-1. Representation of electrical parameters in the datasheet***.

Figure 4-1. Representation of electrical parameters in the datasheet

Table 4-14. Component level ESD characteristics(1)

Symbol	Description	Conditions	Package	Max	Unit	Level
V_{HBM}	Human body model electrostatic discharge voltage (Any pin combination)	T_J = 25 °C; JS-001-2017	BGA176	2000	V	2
V_{CDM}	Charge device model electrostatic discharge voltage (All pins)	T_J = 25 °C; JS-002-2018	BGA176	500	V	C2a

(1) Value guaranteed by characterization, not 100% tested in production.

Table 4-15. Latch-up characteristics(1)

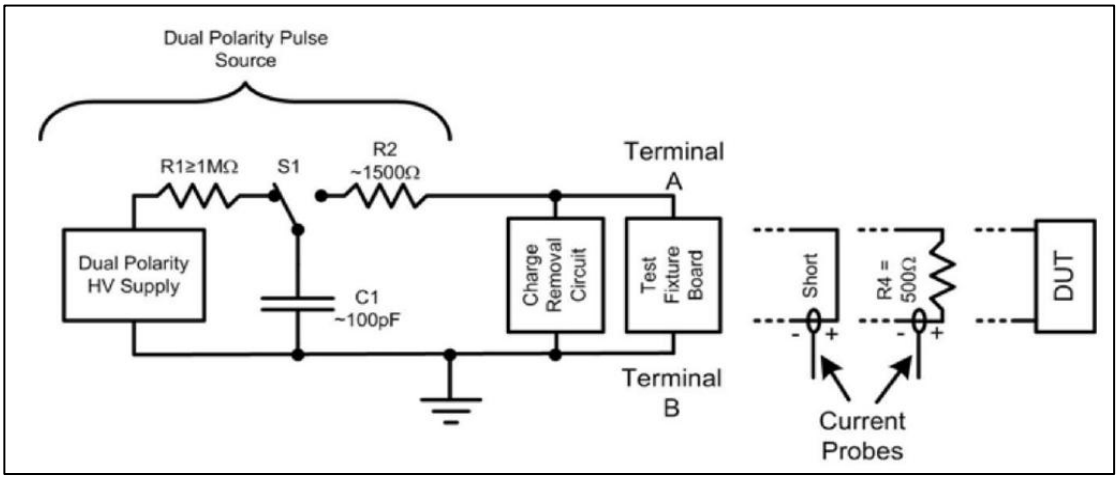
Symbol	Description	Conditions	Package	Class
LU	I-test	T_A = 125 °C, JESD78F	BGA176	II Level A
	V_{supply} over voltage			

(1) Value guaranteed by characterization, not 100% tested in production.

4.1. Chip-level ESD human body model (HBM)

HBM ESD pulses simulate the direct transfer of static electricity from the human body to the device under test. A 100pF capacitor discharges through a switching element and a 1.5kΩ series resistor. This is currently the most widely used industrial model for classifying the ESD sensitivity of devices. This test complies with the ESDA/JEDEC JS-001-2017/AEC_Q100-002 Rev-E standards.

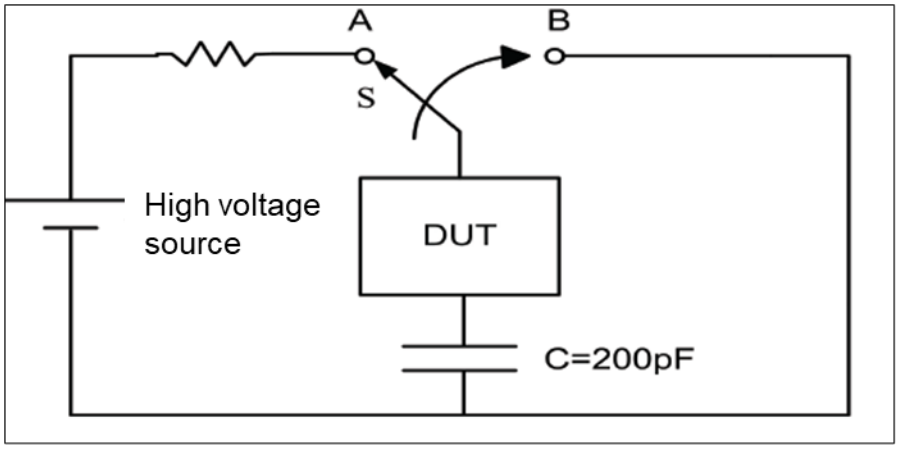
Figure 4-2. Ideal discharge model of chip-level ESD HBM generator



4.2. Chip-Level ESD charged device model (CDM)

The Charged Device Model simulates the discharge of static electricity from the IC itself. In this model, the charge is initially stored within the IC, and if one of its pins comes into contact with a grounded object, it discharges automatically. Factors such as the placement angle of the integrated circuit chip, its position, packaging type, and the accumulation of static charge within the chip can all lead to variations in its equivalent capacitance. This test complies with the ESDA/JEDEC JS-002-2018/AEC_Q100-011 Rev-D standards.

Figure 4-3. Ideal discharge model of chip-level ESD CDM generator



4.3. Latch-up (LU)

Latch-up refers to the phenomenon in CMOS circuits where a low-impedance path is formed between the power supply (VDD) and ground (GND/VSS) due to the mutual influence of parasitic PNP and NPN bipolar BJTs. This phenomenon can lead to an overload, causing high current consumption. In such cases, the power supply must be disconnected to restore the initial state. Overload can result from voltage or current surges, excessive rates of change in current or voltage, or any other abnormal condition that triggers the parasitic BJTs to enter a self-sustaining state. If the amplitude or duration of the current through the low-impedance path is sufficiently limited, latch-up will not damage the device. This test complies with JESD78E/AEC-Q100-004 Rev-D standards.

To evaluate latch-up performance, two complementary latch-up tests must be performed:

- Power Supply Overvoltage (applied to each power pin): Simulates scenarios where transient overvoltage is applied to the power supply by the user.
- Current Injection (applied to each input, output, and configurable I/O pin): Simulates situations where the voltage applied to a pin exceeds the maximum rated value due to application conditions, such as overshoot/ringing causing an input voltage to significantly exceed VDD or drop below ground.

5. EMI Theory

EMI (electromagnetic interference) refers to the level at which a device, as a source of interference, emits electromagnetic waves into the surrounding environment. The emitted electromagnetic waves are categorized into conducted emissions and radiated emissions. Conducted emissions propagate along cables or interconnects, while radiated emissions propagate through free space. When the distance between the interference source and the victim is typically greater than one wavelength (λ), this type of EMI coupling is commonly encountered.

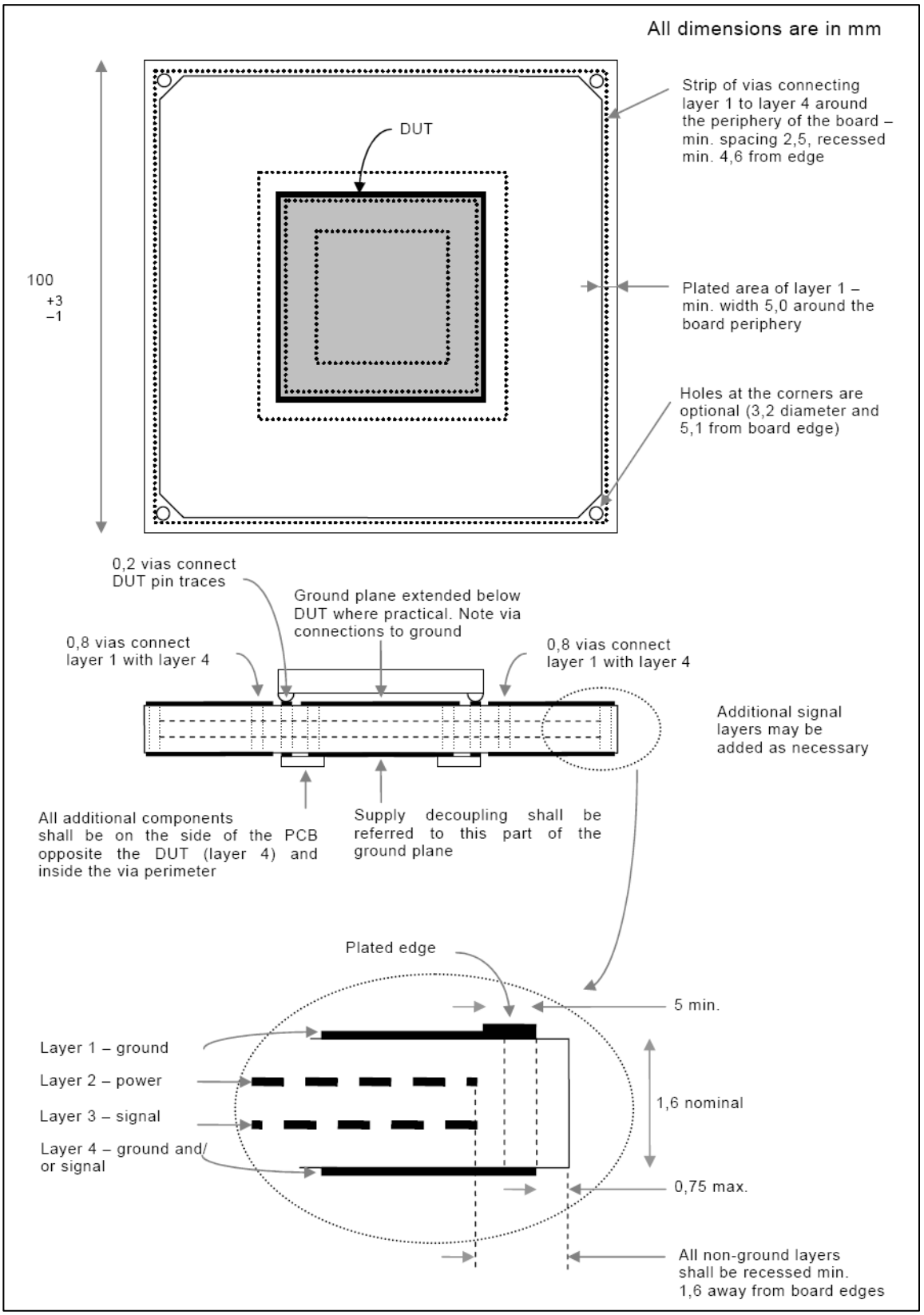
5.1. Test hardware and relevant standards

The main guidelines for test hardware in the IEC61967-1 standard are shown in ***Table 5-1. Recommended IC Pin Loads*** and ***Figure 5-1. Standard PCB design reference according to IEC61967-1***.

Table 5-1. Recommended IC Pin Loads

IC pin type	PIN load
Analog	
— Power	As specified by the manufacturer (or as required) (1)
— Input	Grounded (Vss) through a 10kΩ resistor unless internally terminated within the IC
— Output signal	Grounded (Vss) through a 10kΩ resistor unless internally terminated within the IC
— Output power	Rated load as specified by the manufacturer
Digital	
— Power	As specified by the manufacturer (or as required) (1)
— Input	Grounded (Vss); if grounding is not possible, connected to power (Vdd) through a 10kΩ resistor unless internally terminated within the IC
— Output	Grounded (Vss) through a 47pF capacitor
Control	
— Input	Grounded (Vss); if grounding is not possible, connected to power (Vdd) through a 10kΩ resistor unless internally terminated within the IC
— Output	As specified by the manufacturer
—Bidirectional	Grounded (Vss) through a 47pF capacitor
— Analog	As specified by the manufacturer (or as required) (1)
(1). The actual pin load should be specified in the report.	

Figure 5-1. Standard PCB design reference according to IEC61967-1



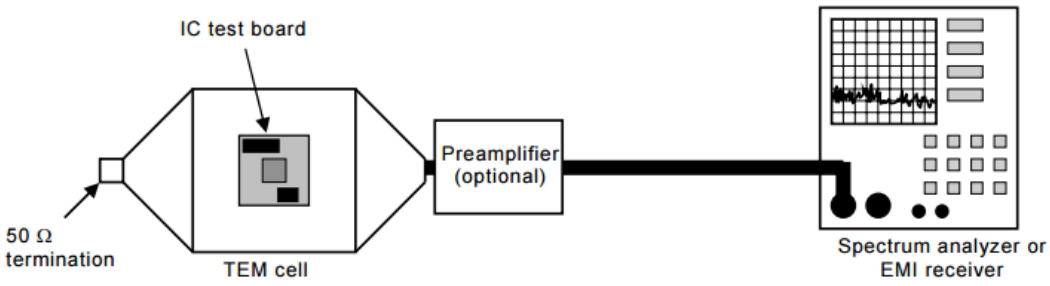
5.2. EMI radiation TEM cell method

5.2.1. Test setup

The test complies with the SAE J1752-3:2017 (IEC61967-2) standard and is conducted using the TEM cell method. By rotating the test board to 0°, 90°, 180°, and 270°, the radiated noise in four directions is measured. This method effectively evaluates the level of radiated noise emitted by the MCU in application environments.

The radiated noise is influenced by the MCU chip and its packaging. The crystal oscillator, MCU system clock and its harmonic multiples typically manifest as EMI noise spikes. The test is based on a simple application firmware. Two LEDs are toggled via the I/O ports.

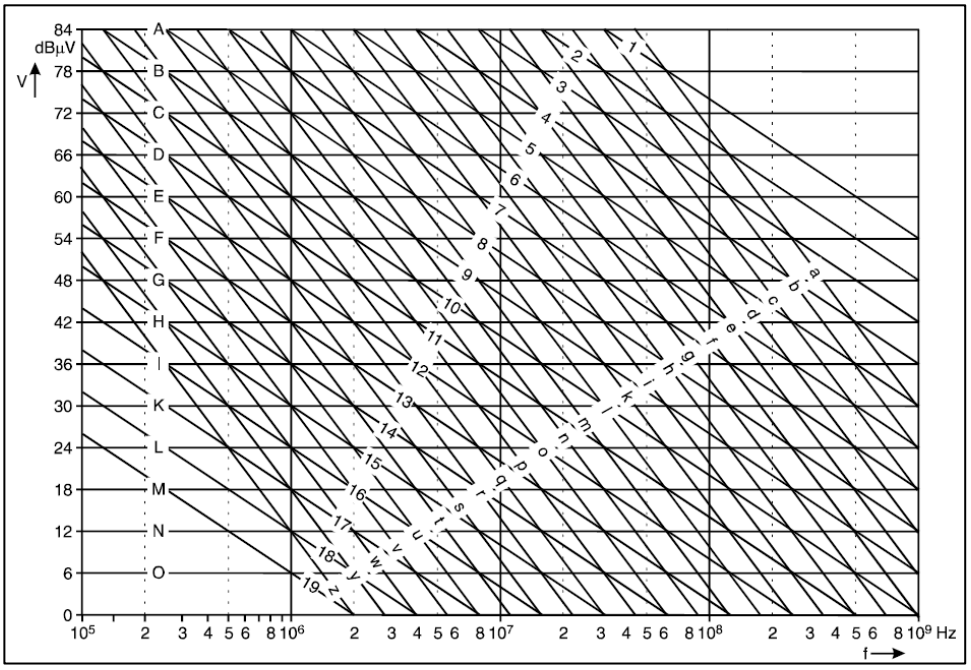
Figure 5-2. Setup of TEM test method



5.2.2. EMI classification

The EMI level classification is based on the IEC61967-2 international standard.

Figure 5-3. EMI radiation characteristic level curve



The data in the datasheet is shown as in ***Figure 5-4. IEC61967-2 radiation levels***.

Figure 5-4. IEC61967-2 radiation levels

EMI (Electromagnetic Interference) emission test result is given in the ***Table 4-10. EMI characteristics***(1), The electromagnetic field emitted by the device are monitored while an application, executing EEMBC code, is running. The test is compliant with SAE J1752-3:2017 standard which specifies the test board and the pin loading.

Table 4-10. EMI characteristics(1)

Symbol	Parameter	Conditions	Tested frequency band	Max vs. [f_{HXTAL}/f_{HCLK}] 8/168 MHz	Unit
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = +23 °C, LQFP144, f_{HCLK} = 168 MHz, conforms to SAE J1752-3:2017	0.15 MHz to 30 MHz	3.49	dBµV
			30 MHz to 130 MHz	8.04	
			130 MHz to 1 GHz	16.70	

(1) Based on characterization, not tested in production.

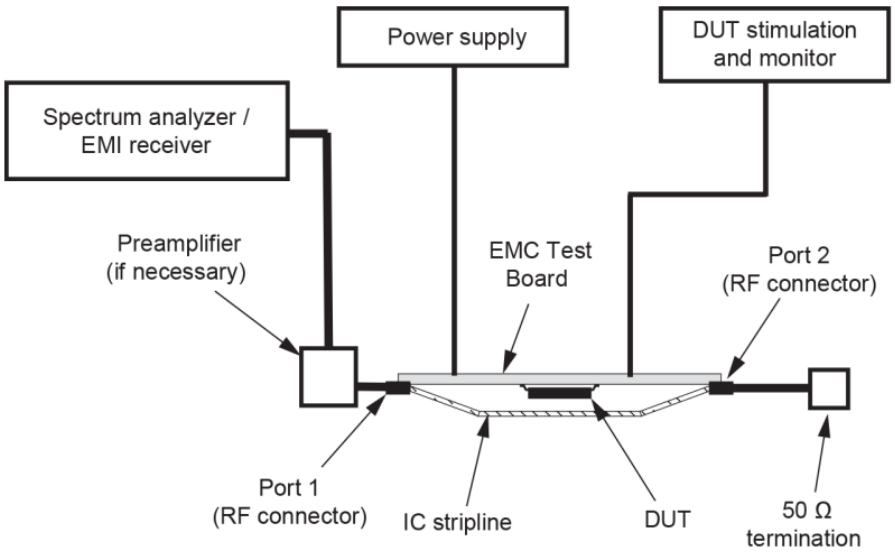
5.3. EMI radiation stripline method

5.3.1. Test setup

The test complies with the IEC61967-8:2023 standard and is conducted using the stripline method. By rotating the test board to 0°, 90°, 180°, and 270°, the radiated noise in four directions is measured. This method effectively evaluates the level of radiated noise emitted by the MCU in application environments.

The radiated noise is influenced by the MCU chip and its packaging. The crystal oscillator, MCU system clock and its harmonic multiples typically manifest as EMI noise spikes. The test is based on a simple application firmware. Two LEDs are toggled via the I/O ports.

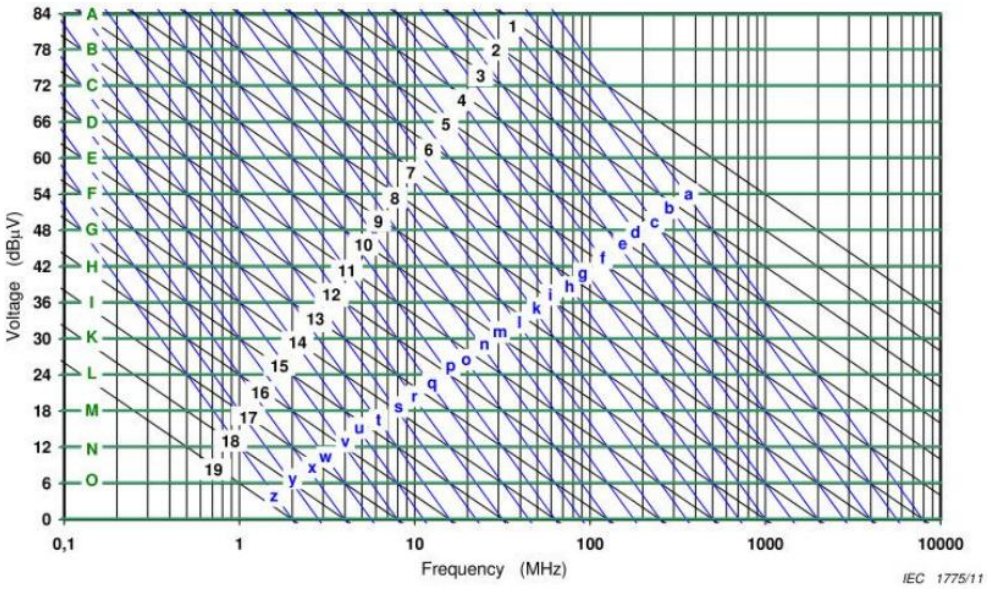
Figure 5-5. Setup diagram for EMI testing using the stripline method



5.3.2. EMI classification

The EMI level classification is based on the IEC61967-8 international standard.

Figure 5-6. EMI radiation characteristic level curve

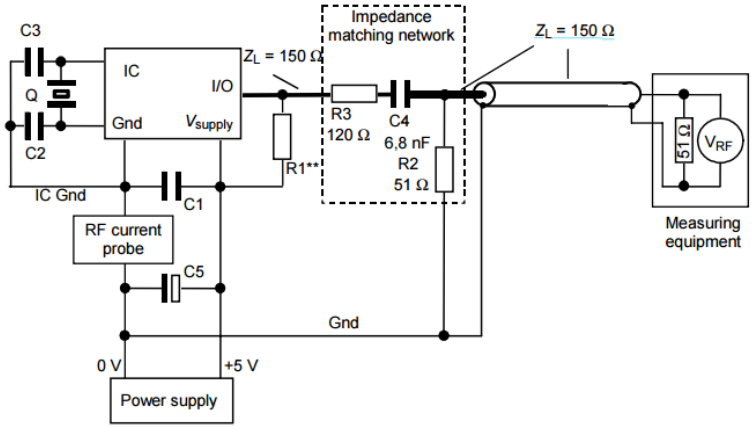


5.4. EMI conducted emission

5.4.1. Test setup

The test complies with the IEC61967-4:2021 standard and conducts conducted emission testing on MCU ports. This test uses a 150Ω test network to measure RF noise conducted through IC pins. The 150Ω test method is primarily used to measure interference voltage at output ports. This method effectively evaluates the level of conducted noise emitted from MCU pins, especially noise on power pins. The test is based on a simple application firmware. Two LEDs are toggled via the I/O ports.

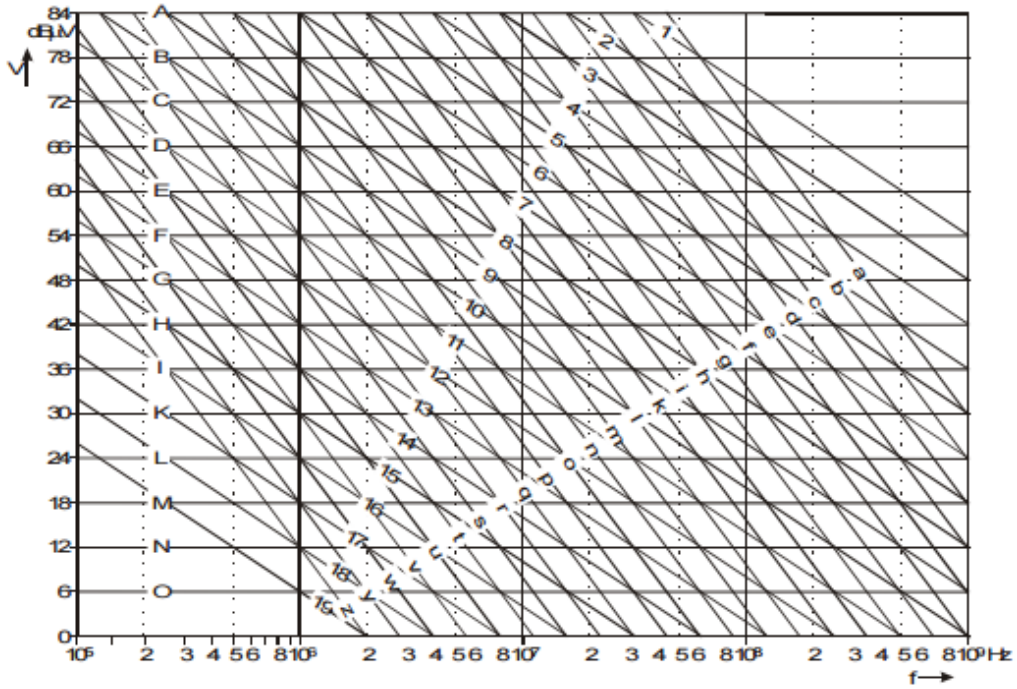
Figure 5-7. Setup diagram for EMI conducted emission



5.4.2. EMI classification

The EMI level classification is based on the IEC61967-4 international standard.

Figure 5-8. EMI characteristic level curve of conducted emission



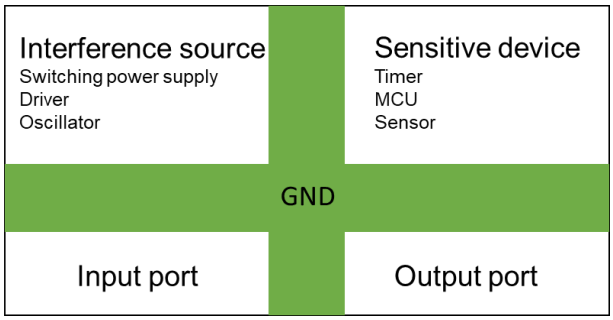
6. GD32 MCU EMC Hardware Strategies

6.1. Segmentation and layer stack-up

6.1.1. PCB segmentation

EMC involves three key elements: interference sources, coupling paths, and sensitive devices. Switching power supplies and switching signals are the primary noise sources, while PCB traces can act as both noise radiation antennas and receiving antennas. Noise suppression is closely related to PCB layout as well as the design of power and ground planes. Therefore, it is recommended to segment interference sources from sensitive devices in the PCB layout to reduce coupling paths. A recommended layout is shown in ***Figure 6-1. Recommended PCB segmentation***.

Figure 6-1. Recommended PCB segmentation



MCUs typically include clock circuits and high-speed interface outputs, which can easily generate high-frequency noise along PCB traces. Meanwhile, pins such as the reset pin are relatively sensitive to external environments. It is advised to place the MCU near the central area of the PCB.

6.1.2. PCB layer stack-up

Before designing a four-layer PCB, it is essential to determine the total thickness required for the product, the type of dielectric material to be used, and the impedance types on the board. A typical four-layer stack-up consists of two signal layers and two reference layers. During the design process, it is recommended to ensure that Layer 2 is a complete GND layer and to minimize power and sensitive signal traces on the Bottom Layer. The recommended four-layer PCB stack-up is shown in ***Table 6-1. Recommended four-layer PCB stack-up***.

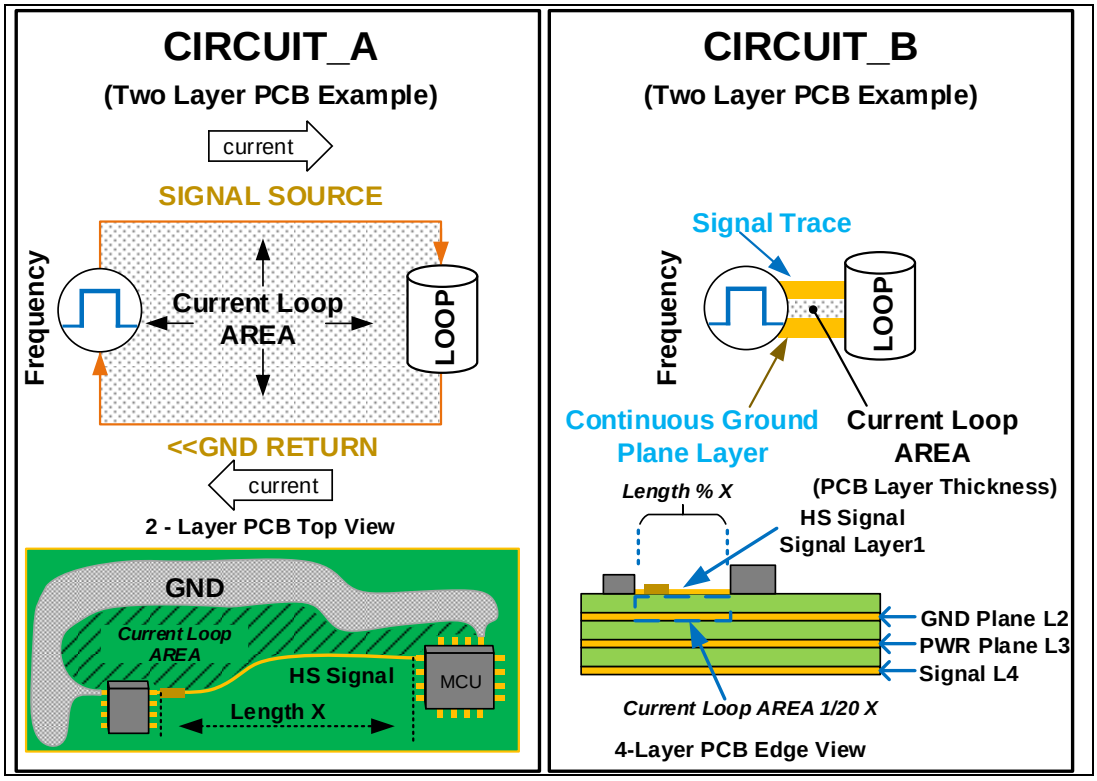
Table 6-1. Recommended four-layer PCB stack-up

PCB layer	Recommended routing
Layer1	Signal1
PP	PP
Layer2	GND
Core	Core

Layer3	Power
PP	PP
Layer4	Signal2

Figure 6-2. The return area comparison between two-layer and four-layer PCBs shows that the return area of a four-layer PCB is only 1/20 of a two-layer PCB. This results in less radiated EMI and is more conducive to noise dissipation.

Figure 6-2. The return area comparison between two-layer and four-layer PCBs



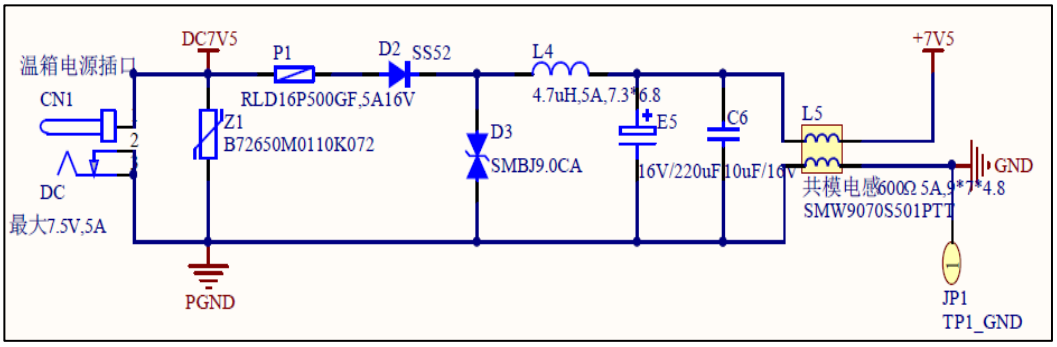
6.2. Power/ground design

6.2.1. Power design

Each power supply must have a filter. If the filter is located on the board, it must be placed close to the regulator. If it is an external regulator, it must be placed near the PCB entry point. The filter should be designed based on the ripple characteristics of the regulator and the power requirements of the integrated circuit. It should include at least two capacitors: a large capacitor (μF) for low-frequency filtering and a small capacitor (nF) for high-frequency filtering. Integrated circuits requiring clean power should be equipped with an additional LC filter to prevent noise coupling with other modules in the circuit.

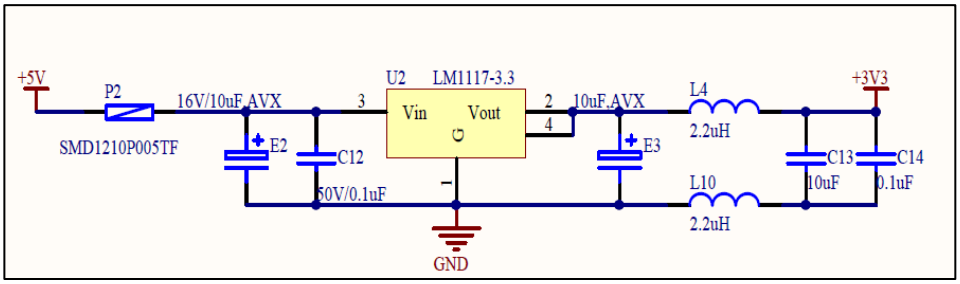
Example of power design:

Figure 6-3. Recommended power protection design



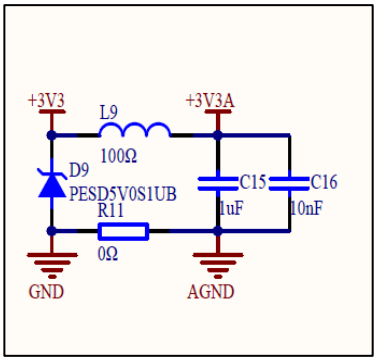
Example of LDO design:

Figure 6-4. Recommended LDO design



The design between the MCU power domains VDD and VDDA is shown in ***Figure 6-5. Recommended VDD&VDDA design***.

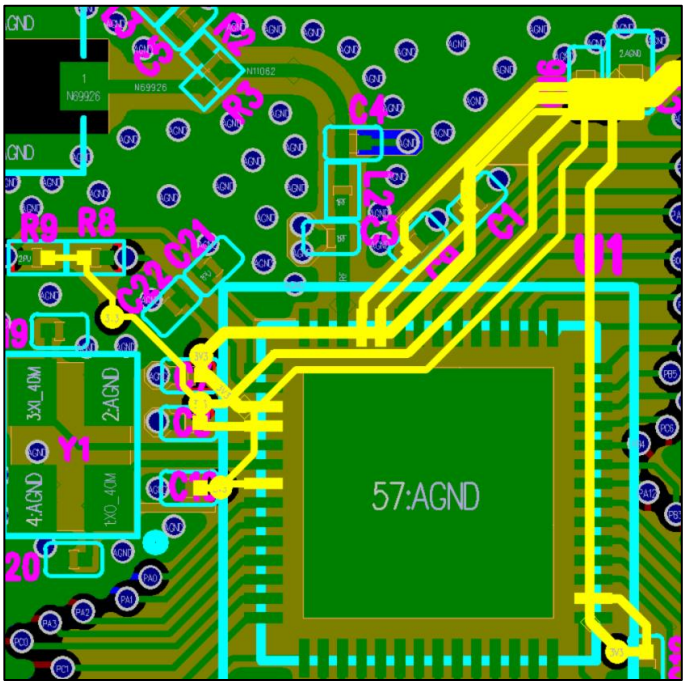
Figure 6-5. Recommended VDD&VDDA design



6.2.2. Power Topology

It is recommended to use a "star" power supply method for the 5V/3.3V power traces of the MCU. Each power pin's trace should be routed individually from the 5V/3.3V source to the chip pin, with large capacitors placed at the 5V/3.3V source.

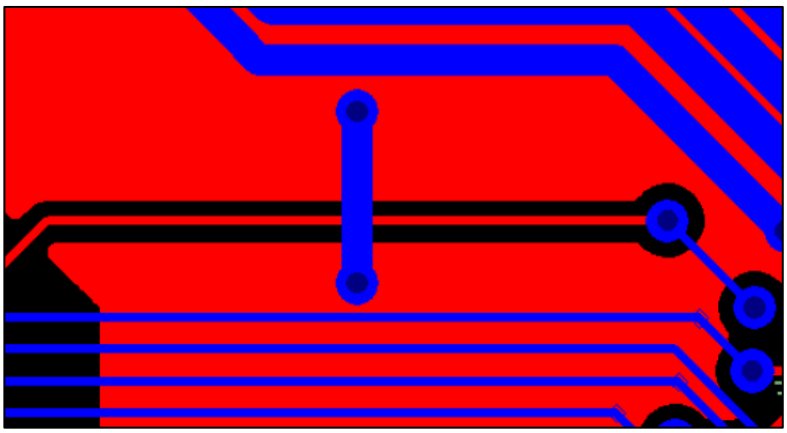
Figure 6-6. Recommended MCU star power supply network



6.2.3. GND Integrity and copper pouring

In addition to the reference layers for GND and Power, it is recommended to pour copper on the signal layer as part of the GND network to avoid dead copper and ensure GND integrity. The GND copper on the signal layer should have multiple VIAs connected to the GND plane to reduce return path area of high-frequency noise. It is also recommended to add more VIAs on the signal layer beneath the MCU to facilitate heat dissipation and signal return. Dead copper and isolated islands can be bridged, as shown in ***Figure 6-7. Recommended bridging***.

Figure 6-7. Recommended bridging

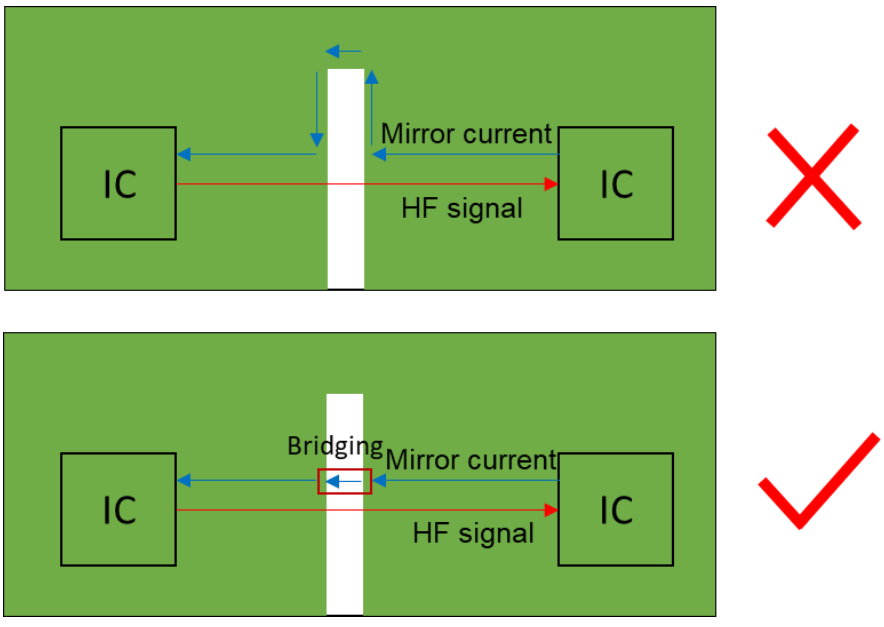


Slotting and Boundaries: The analog ground (AGND) and digital ground (DGND) on the GND layer should be separated by slotting, dividing the digital and analog grounds on the same ground plane. The power ground does not need to be as strictly separated. Since the noise

and current generated by analog circuits are several orders smaller than those of digital circuits, analog ground is generally isolated from digital ground to avoid introducing noise and current from the digital ground. This is typically achieved by slotting between the digital and analog circuits, as shown in ***Figure 6-7. Recommended bridging***. In the reference ground plane, high-frequency signals will automatically seek the path with the lowest impedance (more precisely, the lowest inductance) and the shortest distance. However, when connecting analog and digital domain logic or other low-speed digital circuits, it is usually necessary to bridge the slot with a resistor in the range of 1k-5k Ohm. When connecting high-speed signals between the analog and digital domains, such as the main clock of an audio decoder, a direct connection should be used instead of slotting. As shown in ***Figure 6-7. Recommended bridging***. In practical applications, a 50-Ohm termination resistor is typically placed at the clock source for impedance matching.

When high-frequency current flows from the output terminal of an IC through a signal line into the input terminal of another IC, there is always a mirror current on the nearest plane, flowing in the opposite direction to its input path. This mirror current and the current on the signal line form a closed loop. The smaller this loop, the lower the noise radiation it generates. Since clock signals and high-speed signals have higher frequencies, they are particularly susceptible to electromagnetic interference and generate high-frequency noise. To enhance the anti-interference capability of clock and high-speed signals and reduce the radiation interference they produce, it is necessary to ensure that all clock and high-speed signal traces have a complete reference ground plane or the smallest and most unobstructed current return path. Therefore, high-speed clock and high-speed signal traces need to be surrounded by ground as closely as possible, and crossing segmented ground planes is strictly prohibited. If routing across two segmented ground planes is necessary, it is recommended to design bridging points or solder resistors and capacitors as bridging points between the two ground planes. As shown in ***Figure 6-8. Routing method across segmented ground planes***.

Figure 6-8. Routing method across segmented ground planes

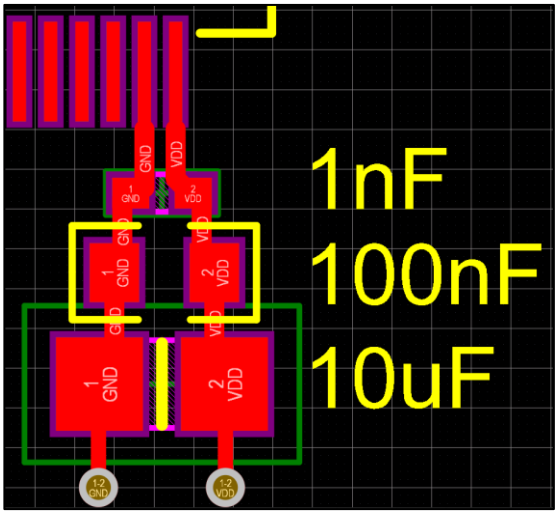


6.3. Decoupling capacitor design

Each power pin of the MCU should have at least one decoupling capacitor. Decoupling capacitors can to provide the transient current needed by the CMOS switching devices in the MCU, offsetting the effects of output inductance and interconnect inductance of the power IC. To ensure the effectiveness of decoupling capacitors, design and layout should follow the principles below:

- Recommended Decoupling Capacitor Combination: It is recommended to place 10uF + 100nF + 1nF capacitors on each pin of the VDD/VBAT power domain of the MCU, and 1uF + 10nF capacitors on each pin of the VDDA power domain. These capacitor values are empirical. Please refer to the product datasheet and hardware development guide for specific capacitor combinations.
- Placement of Decoupling Capacitors: Decoupling capacitors should be placed as close to the MCU as possible. When there are multiple decoupling capacitors, the smaller value the capacitance has, the closer it should be to the MCU. Typically, the 1nF capacitor is closest to the MCU pin, followed by the 100nF capacitor, and the 10uF capacitor is placed furthest away.
- Ensure Current Flow: Ensure that the power current flows to the capacitor first and then to the MCU. If the power pin and GND pin are relatively far apart, it is recommended to place the capacitor near the GND pin, as signals generally use GND as a reference.
- Dedicated VIA for Each Capacitor: Each capacitor should have its own VIA, and multiple capacitors sharing a single VIA is strictly prohibited. The trace between the decoupling capacitor and the MCU pin should be as wide and short as possible to reduce the impedance between the decoupling capacitor and the MCU power pin. The trace between the power network and the decoupling capacitor should be as narrow and long as possible, or isolated using VIA, to provide high impedance against potential power noise and ripple.

Figure 6-9. Recommended decoupling capacitor combination

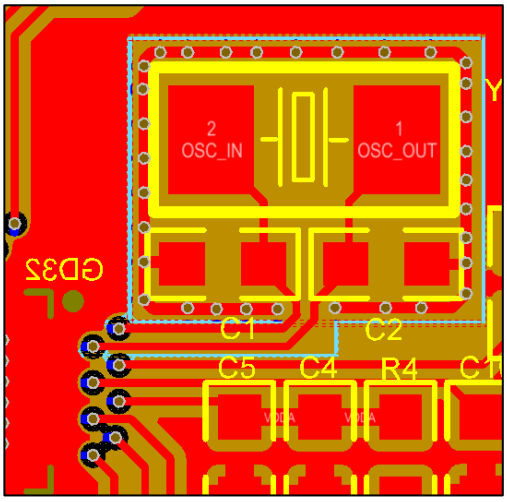


6.4. Design of sensitive peripheral circuits for MCU

6.4.1. Crystal OSC circuit

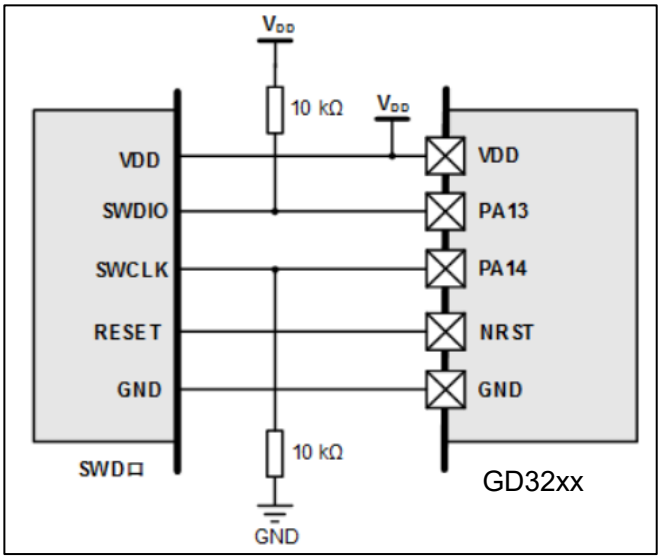
The crystal should be placed as close as possible to the chip pin, away from magnetic induction devices such as power inductors and radiation devices such as antennas. Use GND copper and VIA to isolate it from other signal traces on the same layer. The input and output traces of the crystal should be as short as possible with minimal bends, and should not cross layers or intersect other traces. The load capacitors on both sides and the GND PAD of the crystal can be connected, and multiple GND VIAs should be placed to enhance heat dissipation and stability. No transmission lines should be routed under the crystal. Instead, a complete GND copper pour should be maintained. The crystal circuit traces and matching capacitors should be on the same side as the crystal, avoiding layer transitions as much as possible. The crystal should be placed close to the MCU, and the crystal circuit traces should not be too long, ideally not exceeding 12mm. On the same layer as the crystal and the layer below, the crystal circuit should be separated from other circuits and use grounding VIAs around to form a protective ring.

Figure 6-10. Recommended crystal layout design



SWD Programming Port: The SWD programming port traces of the MCU should be kept as short as possible and should be at least 12mm away from the edge of the board.

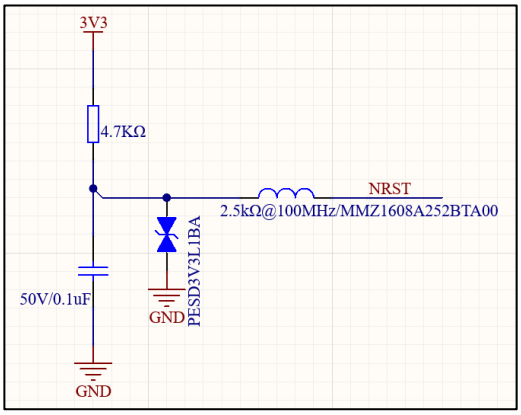
Figure 6-11. Recommended SWD programming port design



The following methods can improve the reliability of SWD download and debugging communication and enhance the anti-interference capability during download and debugging: Shorten the length of the two SWD signal lines, preferably within 15cm; Twist the two SWD lines together with the GND line into a braid; Connect small capacitors of several tens of pF in parallel to ground on each of the two SWD signal lines; insert resistors of 100Ω to 1kΩ in series on any IO of the two SWD signal lines.

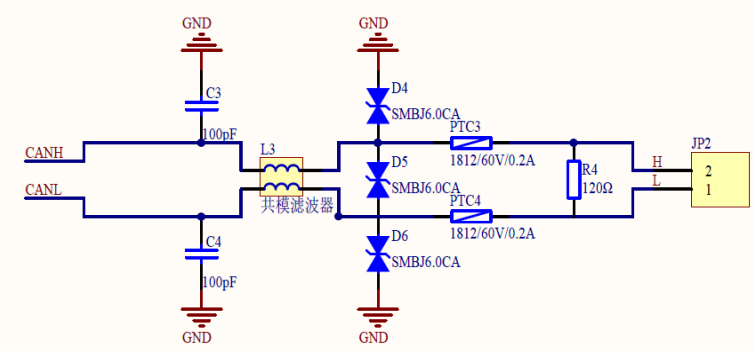
6.4.2. Reset circuit NRST

Figure 6-12. Recommended reset circuit design



6.4.3. Typical CAN circuit design

Figure 6-13. Recommended CAN bus circuit design



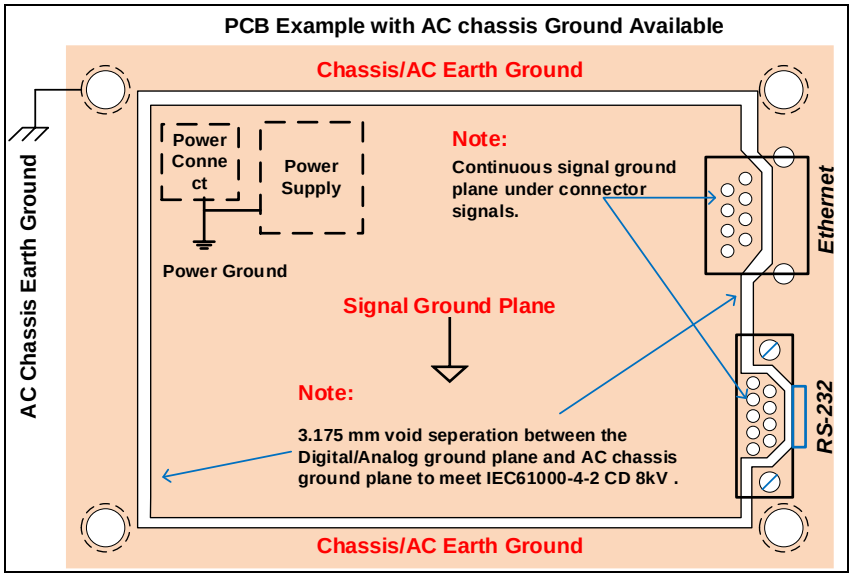
6.5. Hardware protection circuit design

The relevant design of hardware protection circuits can refer to document "AN163 GD32 MCU EMC Hardware Protection Design Reference" and the product hardware development guide.

6.6. PCB Layout

The chassis AC protective ground, card holder, connector housing of peripherals as RS232 and CAN should be electrically isolated from signal ground. The chassis should be connected to the AC rack ground (i.e., earth ground) as much as possible to divert high-voltage discharge to the protective earth, avoiding entry into digital or analog grounding circuits. Note that the grounding plane remains continuous under all high-speed signal connections of peripheral connectors, but the connector housing is isolated from the external AC chassis plane.

Figure 6-14. Recommended layout for chassis protective ground



In applications with chassis ground (protective earth/AC rack ground), it is strongly recommended not to connect digital signal ground and AC rack ground directly. Maintain a minimum distance of >3.175mm (0.125 inches) between the two for 11-12 kV spark gap isolation to meet IEC61000-4-2 Level-4 8 kV contact discharge requirements.

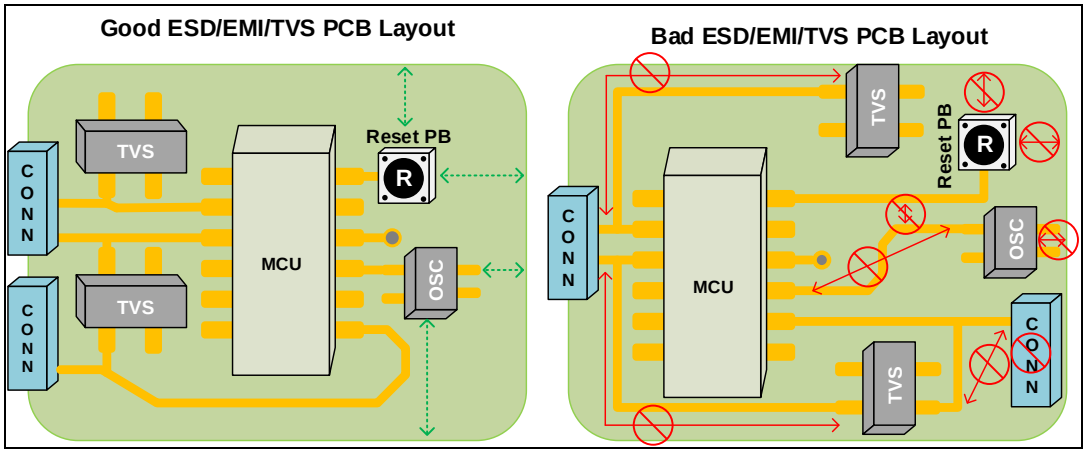
Place the TVS as close as possible to the external signal connector, and connect the TVS ground directly to the ground plane to avoid ground traces.

High-speed or sensitive analog/digital traces should be routed at least 2x away from the edge of the circuit board, where "x" is the distance between the trace and its return current path. Traces very close to the edge of the board have lower containment of electric and magnetic field lines. These traces are more prone to crosstalk and coupling with antennas, making them more susceptible to ESD, EMI, and EFT events.

High-speed clock and high-speed signal traces need to be isolated from each other. For example, USB/EMMC/Ethernet signal lines should be isolated from other signal lines using ground lines. SPI/QSPI/I2C/system clock and other strong interference signals should be isolated from general GPIOs as much as possible using ground lines. Sensitive signals and surrounding interference signals should also be isolated with ground lines. The ground lines used for isolation should be as wide as possible and connected to the main ground through vias.

Susceptible components/circuits should be kept away from the PCB edges. Ideally, they should be placed in the center of the board. If this is not possible and an external protective earth ring is not used, try to place them more than 12 mm away from the edge. During high-voltage discharge events, high-frequency energy tends to accumulate at the outer edges, especially at the corners of the PCB body with right angles (use rounded PCB corners).

Figure 6-15. Recommended layout for protective devices



Components connected to external should be kept near the edge of the PCB. Other components should be placed away from the PCB edge to reduce environmental impacts (e.g., ESD).

If common-mode chokes or transient suppressor devices (e.g., TVS, MOV) are used for power filtering, they should be placed at the PCB entry point. In circuits protected by TVS,

external signals from the connector should first be routed to the TVS, then to the ferrite or common-mode choke, and finally to the protected components.

Hardware layout-related designs can refer to the document "AN191 GD32 MCU Hardware Layout Design Reference."

6.7. Other EMC Application Solutions

6.7.1. IO Configuration

Floating pins pose potential threats to circuits. To improve EMC performance, unused IO pins are recommended to be pulled up or pulled down in hardware.

Overshoot during IO high-to-low level transitions increases with IO speed. Reducing IO speed can help minimize overshoot. The main noise sources of MCU are high-speed clocks and high-speed communication interfaces, such as SPI, I2C clocks, and USB. The rise/fall time of these interfaces is a critical factor affecting EMI. Therefore, RC low-pass filters are typically added in designs.

GD32 MCU provides adjustable IO drive capability. By controlling the rise and fall slopes and drive strength of IO, the di/dt of IO can be reduced, thereby lowering the noise intensity of output clock signals. GPIO drive capability needs to match the signal frequency in actual applications. The selected drive capability must ensure that the signal waveform's setup and hold times meet the signal sampling requirements of peripheral devices.

6.7.2. Spread Spectrum SSC

High-speed clock is a typical source of high-speed noise. But conventional EMI improvement measures such as shielding and filtering have limited effectiveness against high-frequency interference. Clock spreading can significantly reduce EMI emission intensity. The energy of clock signals is concentrated at their carrier, resulting in high energy at the fundamental frequency and harmonics. Spread spectrum modulates the peak clock, dispersing the energy concentrated in a narrow frequency band across a set wide frequency range, thereby reducing peak energy and suppressing EMI.

GD32 MCU products include SSC (Spread Spectrum Clocking) functionality for clock. Spread spectrum modulation is only applicable to the main PLL clock. Specific output pins need to be selected through software configuration, and the clock source for the pins can be referenced in the GD32 MCU user manual. To enable clock spreading, the clock spreading control register value of the GD32 MCU should be modified. By configuring MODSTEP and MODCNT, the amplitude and frequency of the PLL spread spectrum modulation curve can be adjusted. Simply modifying the MODSTEP and MODCNT values in the code allows spread spectrum under different conditions. Detailed settings can be found in the chip user manual.

Compared to non-spread spectrum, configuring PLL spread spectrum by setting MODSTEP and MODCNT values can reduce clock peak energy by up to approximately 20dBm.

Spread spectrum expands the jitter range of the clock based on the original clock frequency. Increasing spread spectrum depth can enhance noise attenuation. But excessive spread

spectrum depth may cause the clock jitter range to exceed the system frequency tolerance, affecting system performance. Therefore, spread spectrum depth is generally recommended to be between 0.5% and 2.5%. For example, if the PLL output frequency of the chip is 200MHz, the typical expanded bandwidth would be 1MHz-5MHz. Ultimately, the most suitable spread spectrum parameters should be chosen based on the actual tolerance of the system.

7. Version History

Table 7-1. Version history

Version	Description	Date
1.0	Initial Release	August 17, 2022
2.0	Add EMI radiation stripline method and conducted emission testing, revise MCU EMC hardware strategy	June 27, 2025

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