GigaDevice Semiconductor Inc.

Methods to improve ADC sampling accuracy

Application Note
AN059

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1. Introduction

GD32 MCU embeds several SAR ADCs (the number depends on the device selection). Through this module, analog signals can be converted into digital signals flexibly and conveniently. The accuracy of ADC is not only affected by the chip design and process factors, but also by a variety of external factors. If user want to achieve nominal accuracy in practical application, enough attention should be paid to the design of software configuration and peripheral circuit. This application note gives the basic working principle and common index parameters of SAR ADC, several directions and means to improve ADC sampling accuracy, to obtain the best accuracy of ADC.

1.1. The introduction of ADC

ADC conversion includes four steps: sampling, holding, quantization and coding. In the sampling phase, the voltage of the external signal shall be sampled to the sampling capacitor of ADC within the specified sampling time, that is, during the closing of the sampling switch, the external input signal shall charge the sampling capacitor C_{ADC} through the external input resistance R_{AIN} and ADC sampling resistance R_{ADC}. As shown in ***Figure 1-1. The basic block of ADC sampling***. Each sampling process can be simplified as external signal charging the sampling capacitor through input impedance and sampling resistance (i.e. unit step response of the sampling capacitor in zero state), as shown in ***Figure 1-2. Unit step response in ADC sampling phase***. When the sampling time is over, the sampling error is expressed as the difference between the voltage on the sampling capacitor and the voltage on the signal source. In an ideal sampling process, the voltage difference should be kept within 0.5LSB (LSB is the minimum voltage resolution of SAR ADC, and 0.5LSB is the quantization error of SAR ADC).

In the quantization phase, the sampling switch SW is turned on firstly, and then driven by the ADC clock. Based on the switching capacitor technology, the voltage on the ADC sampling capacitor is compared with the reference voltage with different weights step by step, and the value on each bit of the n-bit data is determined bit by bit (n is the resolution of the ADC), and then the digital code value is coded and output. In the quantization process, the reference voltage V_{REF+} needs to charge the switched capacitor network. V_{REF+} benchmarks need to be stable during quantification.

Figure 1-1. The basic block of ADC sampling

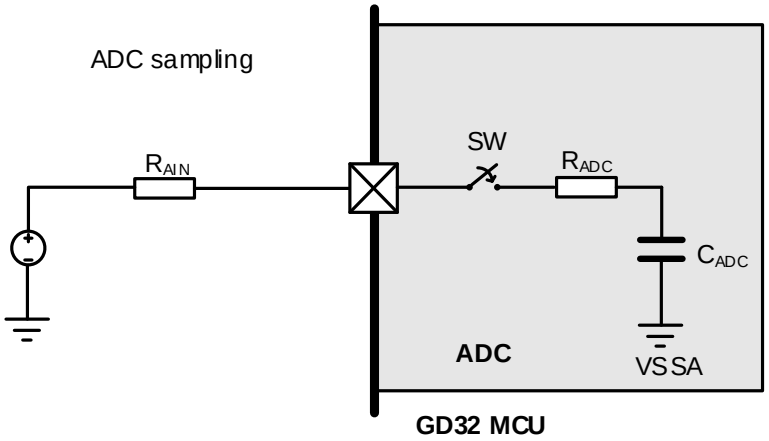
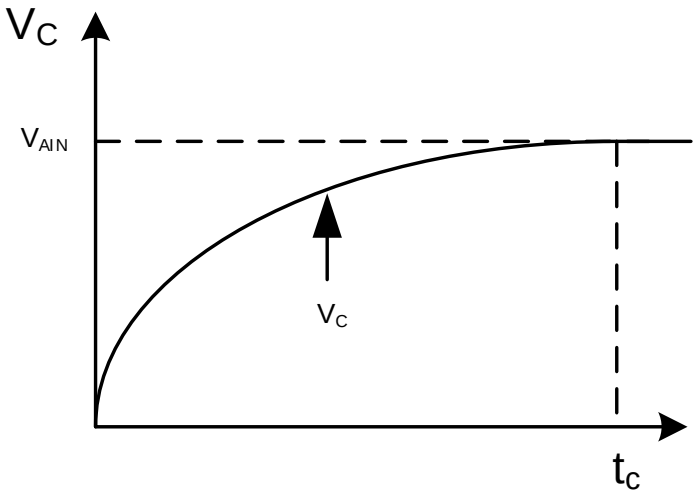


Figure 1-2. Unit step response in ADC sampling phase



1.2. Index of ADC performance

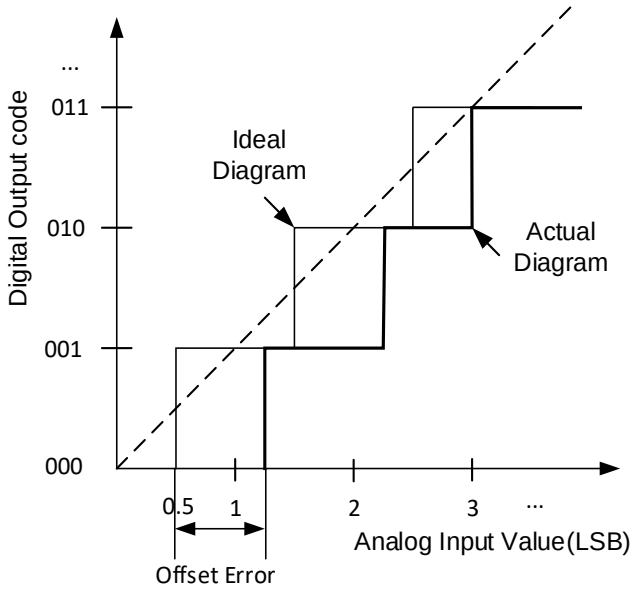
There are usually two kinds of indicators to evaluate ADC performance, one is static performance parameter, the other is dynamic performance parameter. Here we first introduce the definitions of these parameters.

The static performance parameters mainly include the following:

- Offset error

The offset error of ADC is defined as the difference between the actual voltage corresponding to the first code conversion (from 0x00 to 0x01) and the ideal voltage position. As shown in *Figure 1-3. Diagram of Offset Error*

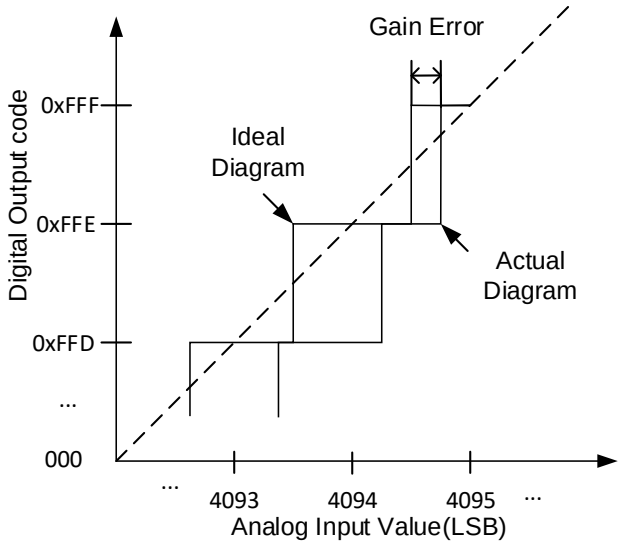
Figure 1-3. Diagram of Offset Error



■ Gain Error

The gain error of ADC refers to the difference between the actual conversion and the ideal conversion point voltage (from 0xffe to 0xfff for 12bit ADC) in the last conversion. As shown in ***Figure 1-4. Diagram of Gain Error.***

Figure 1-4. Diagram of Gain Error

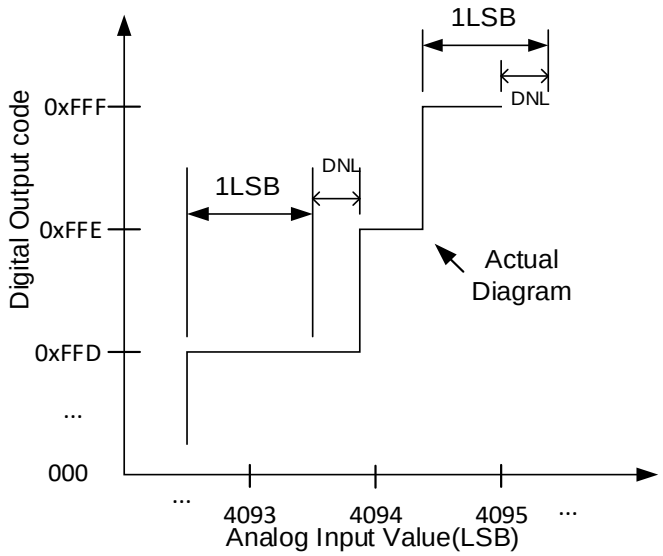


■ DNL

The differential nonlinear error is defined as the difference between the actual quantization step width and the ideal voltage corresponding to 1 LSB. It refers to the degree that the width of each code deviates from the ideal 1 LSB. The calculation method is to subtract one LSB

value from the width of each actual code. When the actual code width is greater than 1 LSB width, the value of DNL is positive, otherwise, DNL is negative. As shown in ***Figure 1-5. Diagram of DNL.***

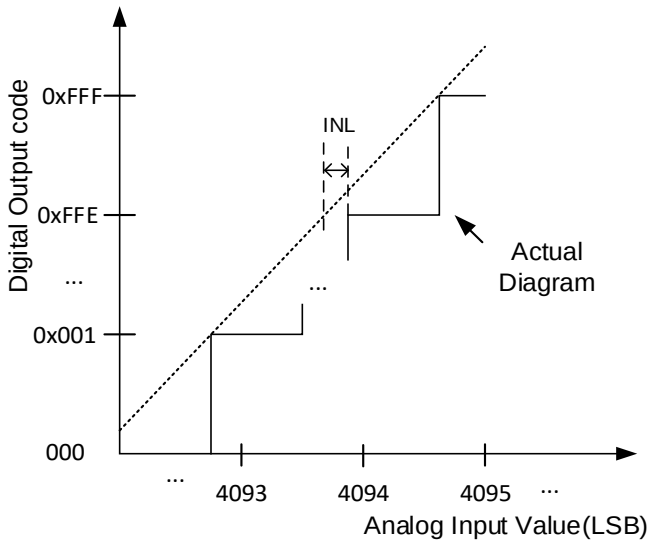
Figure 1-5. Diagram of DNL



- INL

Integral nonlinear error refers to the offset between the actual position of a code and the ideal position on the transmission function line. The transfer function line can be defined as the line connected between the first actual conversion and the last actual conversion, that is, a straight line between the offset and gain error points of ADC. As shown in ***Figure 1-6. Diagram of INL***.

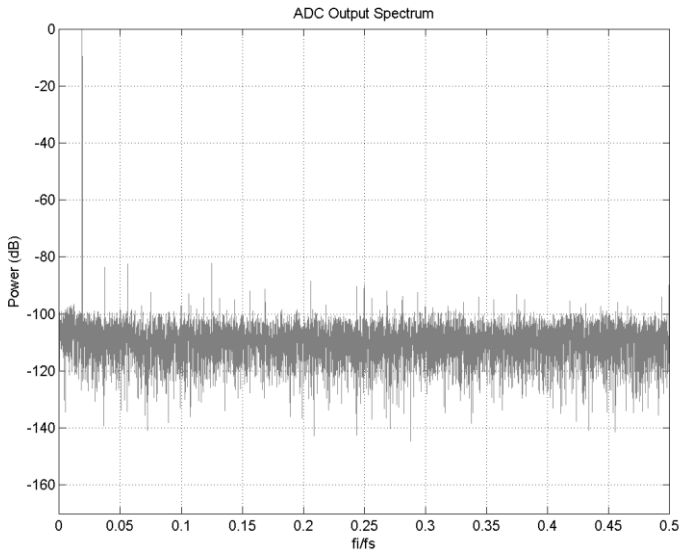
Figure 1-6. Diagram of INL



In the precision signal link system, the static characteristic parameters of ADC are often concerned. However, SAR ADCs with sampling rate up to MSPs are sometimes used for AC

signals with fast sampling frequency. Therefore, it is particularly important for the real reproduction of AC input signals. In this scenario, we pay more attention to the frequency domain characteristics of signals. Some dynamic characteristic parameters also need to be paid attention to, mainly including the following. It is usually necessary to analyze the frequency domain characteristics with the help of FFT transformation of the sampled signal. The following is the typical spectrum of ADC sampling a group of periodic signals and FFT analysis, as shown in ***Figure 1-7. FFT spectrum of ADC sampling signal.***

Figure 1-7. FFT spectrum of ADC sampling signal



- SNR

SNR represents the ratio between the effective value of signal and the effective value of noise in the spectrum. Then take the logarithm and multiply by 20 to get the SNR value in dB form.

- SNDR

The SNDR represents the sum of the RMS ratio of signal power in the spectrum plus noise plus all harmonic components. Therefore, by definition, the SNDR is bound to be lower than the SNR.

- ENOB

In many applications, it is customary to use ENOB to describe ADC performance. ENOB is usually calculated using the SNR. The index of ENOB can be calculated by following formula (1-1):

$$ENOB=\frac{(SNDR-1.76)}{6.02} \quad (1\text{-}1)$$

- THD

The total harmonic coefficient represents the ratio of the effective value of the fundamental wave signal to the sum of the effective values of all harmonics.

1.3. Theoretical analysis of ADC sampling process

According to the working model of SAR ADC, the unit step response of the system in zero state is calculated according to the circuit theory. See the following formula (1-2):

$$V_{C(t)=}V_{AIN}*\left(1-e^{-\frac{t}{\tau}}\right) \quad (1\text{-}2)$$

τ is the time constant in the above circuit, and the value is $(R_{AIN}+R_{ADC})*C_{ADC}$. R_{ADC} and C_{ADC} can be found in the datasheet;

For the sampling error of ADC, we give an ideal maximum error value of 0.5lsb according to the quantization error. Therefore, if we need to meet the requirements of sampling error within a given sampling period, we have certain requirements for the input impedance of the signal. See the following formula (1-3):

$$V_{AIN}-V_{C(t)}=\frac{LSB}{2}=\frac{1}{2}*\frac{V_{REF}}{2^N} \quad (1\text{-}3)$$

In formula (1-3), N is the conversion bit of ADC and VREF is the full-scale voltage. Bring formula (1-2) into formula (1-3) to obtain formula (1-4):

$$R_{AINmax}=\frac{T_S}{f_{ADC}*C_{ADC}*\ln\left(2^{N+1}\right)}-R_{ADC} \quad (1\text{-}4)$$

Where T_S is the ADC sampling period configured in the software.

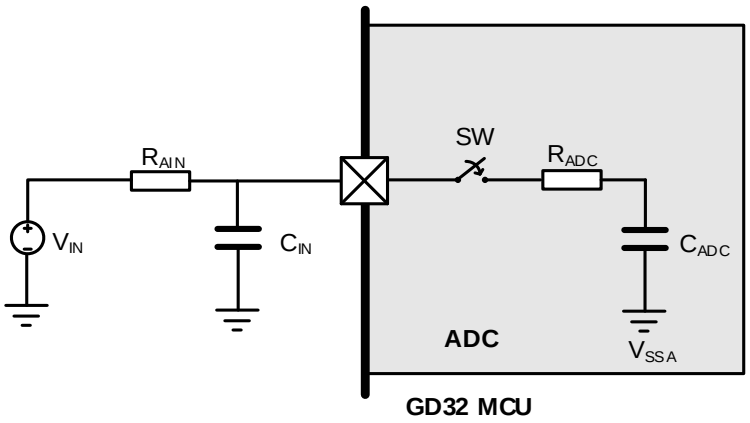
Obviously, when the ADC clock frequency f_{ADC} is determined, different sampling periods will correspond to a R_{AINmax}, and the output impedance of the external input signal must also be less than this R_{AINmax}, otherwise the sampling accuracy error will be greater than 0.5LSB.

Based on the above discussion, for SAR ADC, the sampling time and external signal source impedance are first considered when designing its circuit. If these basic parameters are ignored, the sampling results are difficult to achieve ideal accuracy.

The above discussion is about the basic operation of SAR ADC.

However, in practice, we usually add an RC filter between the signal source and the ADC interface to limit the out of band noise of the signal to obtain more accurate sampling results. Before entering the ADC channel, the signal source passes through an equivalent input impedance (taking the signal source impedance and RC filter resistance as R_{AIN}), and then passes through a capacitance C_{IN}, as shown in ***Figure 1-8. ADC sampling block diagram with external capacitance CIN***.

Figure 1-8. ADC sampling block diagram with external capacitance CIN

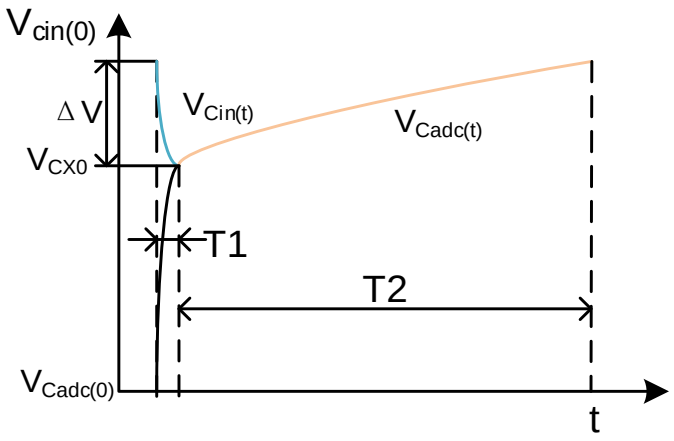


The premise of the above circuit formula is that the circuit responds from the zero state, that is, the initial voltage of C_{ADC} is 0, but the initial voltage on the sampling capacitor is not 0 in the actual sampling process. The value of this voltage is related to the specific ADC input structure. In the charge redistribution structure of SAR ADC, if a pre sampling circuit is used, the value of this voltage may be equal to V_{REF+} or GND. In some special cases. In order to reduce the voltage stress on the capacitor, through special design, the initial voltage can be set to 1/2 V_{REF+}. During continuous and scanning mode sampling, the initial voltage may be equal to the signal voltage of the previous sampling channel.

Generally speaking, the input impedance R_{AIN} of the signal will be significantly greater than the sampling resistance R_{ADC} of the ADC. Therefore, when the sampling switch of the ADC is closed, the relationship between the voltage and time on the input capacitance and the sampling capacitance can be shown in ***Figure 1-9. Voltage diagram during sampling.***

The time period after switch SW is closed can be simplified into two parts, namely T1 time period and T2 time period.

Figure 1-9. Voltage diagram during sampling



Set up α Is the ratio of input capacitance C_{IN} and C_{ADC}.

Assuming that the initial voltage of the sampling capacitor C_{ADC} is $C_{ADC(0)}$, in the T1 time period,

the charge of the input capacitor flows through the ADC sampling resistor to the ADC sampling capacitor, and finally reaches a stable value. And then there is no energy transfer.

According to the charge redistribution, the voltage after the balance of C_{IN} and C_{ADC} after T1 time period can be obtained as formula (1-5) and the voltage change as formula (1-6):

$$V_{CX0}=\left(\frac{\alpha}{\alpha+1}V_{Cin(0)}+\frac{1}{\alpha+1}V_{Cadc(0)}\right) \quad (1\text{-}5)$$

$$\Delta V=\frac{1}{\alpha+1}\left(V_{Cin(0)}-V_{Cadc(0)}\right) \quad (1\text{-}6)$$

It is easy to conclude that the larger the ratio of the input capacitance to the sampling capacitance, the smaller the amplitude of the voltage drop (or voltage spike, depending on the initial voltage on the sampling capacitance and the voltage on the external input capacitance before the sampling switch is closed).

In the T2 time period, the voltage on the input capacitor and the sampling capacitor has been equal. In fact, the circuit can be equivalent to the charging of the sampling capacitor and the input capacitor in parallel by the input signal source through the output impedance of the signal.

According to knowledge of circuit theory:

In the T2 time period, the voltage on the sampling capacitor is shown in formula (1-7):

$$V_{Cadc(t)}=V_{cin(t)}=(V_{IN}-V_{CX0})\left(1-e^{-\frac{t}{\tau 2}}\right)+V_{CX0} \quad (1\text{-}7)$$

$\tau 2$ is the time constant of T2 phase, the value is $(R_{AIN}+R_{ADC})*(C_{ADC}+C_{IN})$.

At the end of sampling, we also need the difference between the actual voltage on the sampling capacitor and the input signal voltage to be less than 1/2LSB, and bring it into the relevant formula to obtain the following result formula (1-8):

$$R_{AINmax}=\frac{T_S}{f_{ADC}*(C_{ADC}+C_{IN})*\ln\left(\frac{(V_{IN}-V_{Cadc(0)})}{(1+\alpha)*V_{REF}}*2^{N+1}\right)}-R_{ADC} \quad (1\text{-}8)$$

From the formula, we can find that when $V_{IN}=V_{REF}$, $C_{IN}=0$, $V_{CADC}=0$, the input impedance requirements are consistent with the simple case above. After adding RC filter between signal and ADC input, the requirements for sampling time and signal input resistance will be higher.

2. Several methods to improve the accuracy of ADC

Based on the several process of SAR ADC, it is necessary to ensure that the possibility of causing errors is not introduced into each process. We discuss the methods to improve ADC sampling accuracy from the following aspects

2.1. MCU power supply

In different series or packages of GD32 MCU, V_{REF+} pins are led out separately, or V_{REF+} pins are not led out separately, but are connected with V_{DDA} inside the chip. For details, please refer to the datasheet.

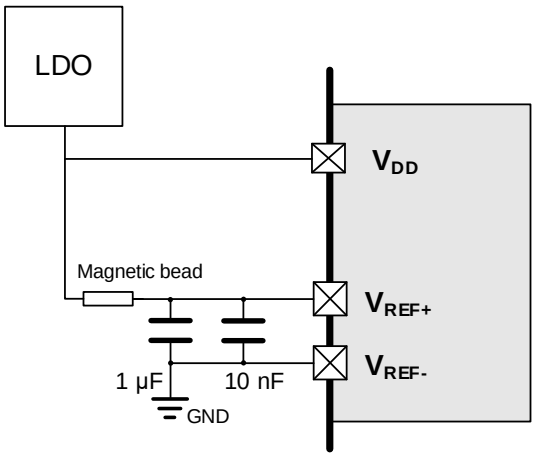
In some series of GD32 MCU, there is an accurate internal reference (typical voltage 2.5V), which can be used as the reference voltage for ADC. The internal reference voltage can be connected to the V_{REF} pin. However, it should be noted that the load capacity of the internal reference source is not strong, and the load size should be carefully selected.

In the process of quantization and coding, V_{REF+} needs to charge the conversion capacitor network. In the process of quantization, there will also be the action of extracting charge from the reference source. Therefore, if there are no other decoupling measures, a robust and clean V_{REF+} reference will significantly affect the accuracy of ADC quantization. We recommend that LDO with smaller ripple noise coefficient be used for this power supply. For V_{REF+} reference source, we suggest that an uF level and an nF level decoupling capacitor be connected in parallel near the pin. On the one hand, it can filter out the external low-frequency and high-frequency noise. On the other hand, it can also make the reference source more stable in the process of quantization and coding.

In the layout process, for the routing of relevant power lines, we recommend widening the power trace to reduce the ESR of the trace, and in the quantization stage, to reduce the impact of instantaneous charging of the conversion capacitor network on the input reference.

In the same case, in some scenarios, V_{DD} and V_{REF+} come from the same LDO, and then a magnetic bead is connected in series between the LDO and V_{REF+}, as shown in ***Figure 2-1. Diagram of VREF+ series with magnetic bead*** to shield the influence of external power supply on V_{REF+}. Attention should be paid to the R_{DC} (DC resistance) parameter of the magnetic bead when selecting the magnetic bead. The model with small R_{DC} should be selected first to reduce the DC voltage drop on the magnetic bead. If the DC resistance is small, the impedance at high frequency of the magnetic bead will be small, so this is also a trade-off process between anti-interference and sampling accuracy. In addition, it is generally not recommended to replace the magnetic beads with inductors here. Because there will be high-frequency pulse current in the quantization and coding process, if the decoupling capacitor near the V_{REF+} pin is not set properly, it is easy to cause V_{REF+} voltage oscillation and affect the accuracy of ADC.

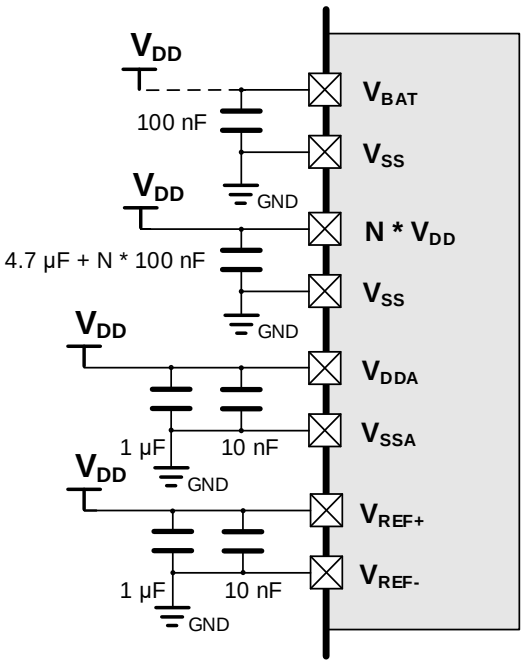
Figure 2-1. Diagram of V_{REF+} series with magnetic bead



2.2. Decoupling capacitor setting

The decoupling capacitor setting of the power supply is particularly important for improving the sampling accuracy, as shown in ***Figure 2-2. Diagram of decoupling capacitor setting***. For the analog power pin, it is recommended to place a 1uF and a 10nF ceramic capacitor nearby (ESR is low). For other V_{DD} pins of digital power supply, place a 100nF ceramic capacitor nearby. For the MCU grounding pin, it is recommended to connect analog ground and digital ground with 0 ohm resistance or magnetic bead to shield the interference of digital ground to analog ground.

Figure 2-2. Diagram of decoupling capacitor setting



2.3. Influence of ADC reference voltage setting

ADC input signal amplitude ranges from V_{SSA} to V_{REF+}. For some MCU with small package, V_{REF+} and V_{DDA} are connected together inside the chip. The setting of V_{REF+} voltage shall strictly refer to the specified range in datasheet. The amplitude of sampling signal shall not exceed the amplitude of V_{REF+}. For MCU without V_{REF+} pin, the amplitude of sampling signal shall not exceed the amplitude of V_{DDA}. Otherwise, analog power leakage may be caused and ADC performance may be seriously affected.

In addition, we can think about how to choose a reasonable V_{REF+} according to the ADC input signal amplitude range, or set a reasonable ADC signal input range according to the V_{REF+}.

For instance:

When the input signal voltage range is 0-2.6 V, if V_{REF+} is set to 3.6 V, on the premise of ignoring the sampling error, the digital code range of the sampling result is 0-2958, and the sampling result can distinguish the voltage of 0.9 mV. However, the digital code values between 2759-4095 do not appear. If the hardware is modified so that V_{REF+} is 2.6 V, the digital code range of sampling results is 0-4095, and the minimum voltage that ADC can distinguish is 0.6 mV. Obviously, the latter has higher sampling accuracy.

Therefore, at the beginning of hardware design, if there are requirements for sampling accuracy, we need to evaluate the voltage range of ADC input signal and configure the maximum value of input signal voltage to be slightly less than V_{REF+} to improve sampling accuracy.

2.4. Influence of over voltage introduced to IO pin

If there is a negative voltage less than GND on any analog pin (or the adjacent digital input pin) (a negative voltage not greater than -200 mV can be considered safe), the negative current from the IO port will be introduced. In this case, the ADC sampling results will be significantly affected. In order to obtain high accuracy, it is necessary to ensure that there is no negative voltage on the relevant IO port during ADC operation.

Do not introduce voltage higher than V_{DDA} at the IO channel of ADC sampling during non-working time, which may cause leakage to the ADC core and poor sampling accuracy.

2.5. Influence of input resistance of signal source

From the previous theoretical analysis, it can be seen that SAR ADC sampling has clear requirements for the input resistance of the signal. For a specific ADC, the sampling resistance R_{ADC} and the sampling capacitance C_{ADC} cannot be changed. When the configurable parameters of ADC such as sampling clock and sampling period are configured, the input impedance of the external signal has a maximum requirement, that is, formula (1-

4):

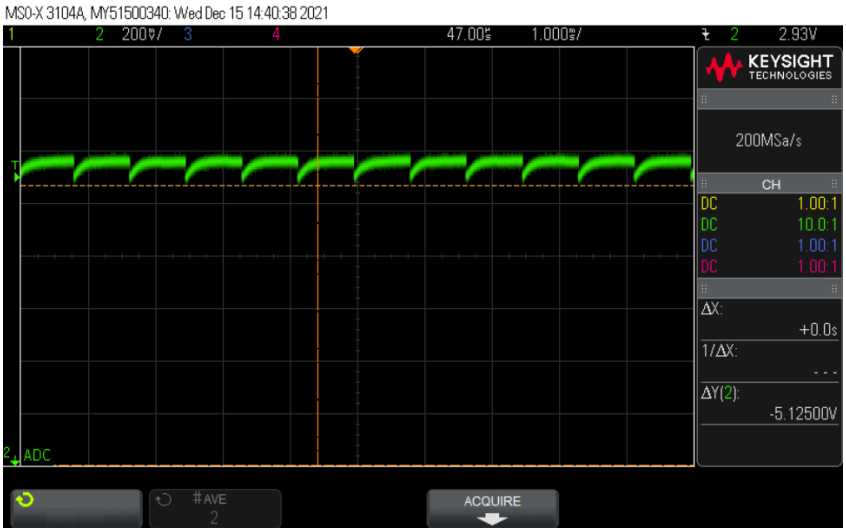
$$R_{AINmax}=\frac{T_S}{f_{ADC}*C_{ADC}*\ln(2^{N+1})}-R_{ADC}$$

The maximum input resistance corresponding to different configured sampling periods will be given in the datasheet of the corresponding MCU device. The user can also calculate it by himself according to the formula and the actual situation.

Figure 2-3. Voltage waveform on CIN show the voltage signal waveform collected on the input capacitor CIN during ADC sampling process in GD32 MCU.

It can be seen that after the sampling switch SW is closed, the voltage will drop significantly. However, as long as the sampling time and signal input impedance meet the requirements of our datasheet, the voltage on sampling capacitor can be restored to within 0.5LSB between the actual signal voltage after the sampling time is met.

Figure 2-3. Voltage waveform on C_{IN}

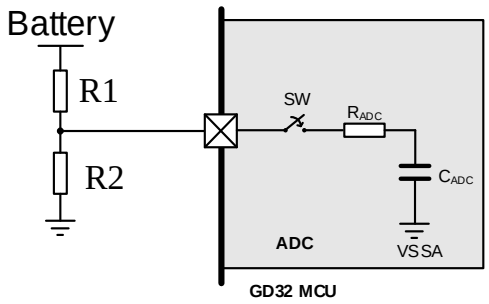


Next, we will consider an extreme case. When the input resistance of the signal source obviously do not meet the requirements of the datasheet, what methods can we use?

For instance:

In practical use, it is a common requirement to sample the voltage of lithium battery. Since the voltage of lithium battery is often higher than the voltage allowed by ADC (the sampling range of ADC is V_{SSA} to V_{REF+}), users often use two resistors to divide the voltage, and then send the voltage division results to ADC channel for sampling. For lithium battery powered applications, customers often have strict requirements for power consumption. Therefore, as shown in *Figure 2-4. Voltage Sampling circuit of lithium battery* voltage sampling circuit are often set very large to reduce unnecessary power consumption.

Figure 2-4. Voltage Sampling circuit of lithium battery



In the above figure, assuming that the lithium battery voltage is 24V, R2 = 1M ohm, R1 = 9M ohm, the voltage entering the ADC channel is 2.4V. The value is within the sampling range of ADC. At this time, the wasted additional unnecessary power consumption is only 2.4uA. it looks very ideal. But let's calculate the output impedance of this circuit. The output impedance of this circuit is the parallel connection of R1 and R2 resistors, and the result is 0.9M ohm. Refer to the following table about R_{AIN} and sampling period in the GD32F150x MCU datasheet:

Table 2-1. ADC RAIN max for f_{ADC} = 14 MHz

T_s(cycles)	t_s(us)	R_{AINmax} (kΩ)
1.5	0.107	0.88
7.5	0.536	6.4
13.5	0.964	11.95
28.5	2.036	25.72
41.5	2.964	37.68
55.5	3.964	50.57
71.5	5.107	65.29
239.5	17.107	219.86

Obviously, when the ADC sampling clock is 14MHz, and the sampling period is set to a maximum of 239.5 cycles, the maximum allowable input impedance is 219.9k ohms. 0.9M ohm is far greater than 219.9k. Therefore, since the sampling time cannot be configured to be larger, the ADC sampling of MCU cannot achieve accurate sampling at this time.

At this point, we have several methods to improve ADC sampling accuracy in this case:

If the circuit can still be modified, it is suggested to add an op amp circuit to realize good impedance matching;

If high sampling rate is not required, we can reduce the sampling clock of ADC and increase the sampling time to charge the sampling capacitor to the correct level;

If higher power consumption is acceptable, we can reduce the two resistors R1 and R2 in the same proportion. For example, R1 = 900k and R2 = 100k. At this time, the output impedance of the voltage divider circuit becomes 90k. Configuring an appropriate sampling period can

meet the impedance requirements of ADC;

If the above methods cannot be realized due to various conditions. When the output impedance of the external circuit has exceeded the maximum input impedance requirements of the ADC circuit, we consider another way to ensure the ADC sampling accuracy and successfully complete the ADC sampling.

According to the above theoretical analysis, if an input capacitor C_{IN} is connected in parallel on the ADC input channel, the charge on the sampling capacitor will be transferred to the external input capacitor through the sampling resistance within T1 time period after the ADC sampling switch is closed, causing the voltage drop or spike on the input capacitor (depending on the voltage on the sampling capacitor). If the voltage drop or spike is less than the quantization error, i.e. 0.5LSB, the ADC sampling accuracy will not be affected.

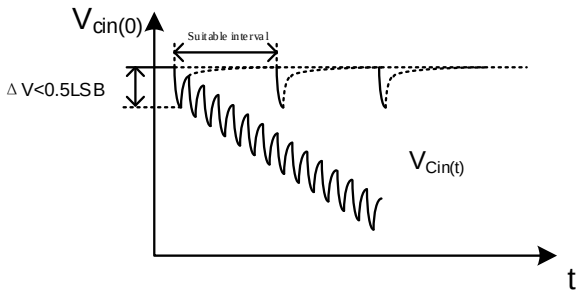
From formula (1-6), when $V_{Cin(0)} = V_{max} = V_{REF+}$, $V_{Cadc(0)} = 0$, the voltage drop is taken to the maximum value.

$$\Delta V = \frac{1}{\alpha+1} * V_{REF+} < \frac{LSB}{2}$$

We can get results α≥8191, so when $C_{IN} > 8191 * C_{ADC}$, we can meet the ADC sampling accuracy requirements.

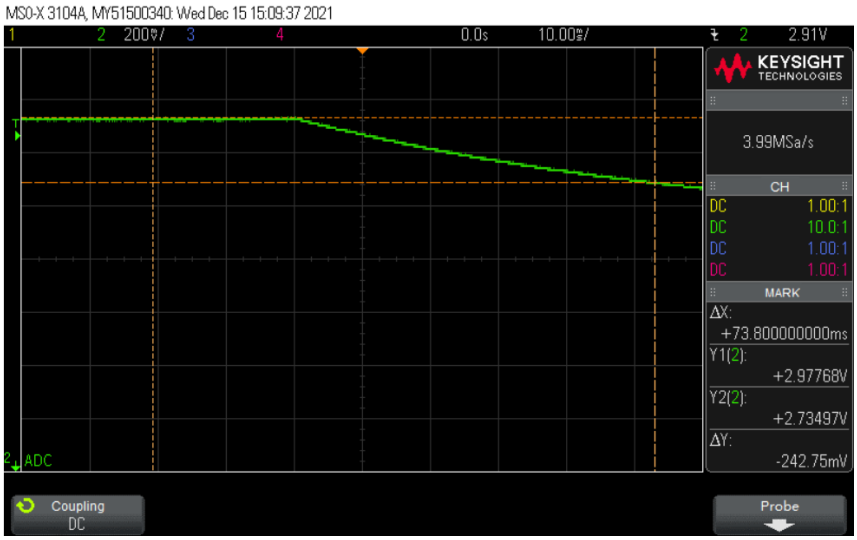
It is easy to find that in this case, the sampling frequency of ADC needs to be paid special attention, because when voltage drops or voltage pulse occur on the input capacitor, the signal source needs to supplement these charges through the input resistance R_{IN} (or release them, depending on the voltage on the sampling capacitor and the input voltage). Therefore, we need to ensure that a certain delay is required between sampling, Otherwise, the input capacitor will continuously charge the sampling capacitor, resulting in the voltage on the input capacitor being continuously pulled down, which will exceed the accuracy requirement of 0.5LSB error. As shown in ***Figure 2-5. Theoretical diagram of sampling with insufficient interval***:

Figure 2-5. Theoretical diagram of sampling with insufficient interval



As shown in ***Figure 2-6. Ideal diagram of sampling with insufficient interval***. In the actual sampling process, the input impedance is too large, and the delay between sampling is not long enough, resulting in the C_{IN} voltage being constantly pulled down.

Figure 2-6. Ideal diagram of sampling with insufficient interval



Therefore, it is necessary to add the necessary delay between every two samples. Next, we discuss the appropriate value of this delay.

According to the previous analysis, this interval includes the time T1 plus the time T2. When the external input impedance is relatively large, the time constant of T1 phase is much smaller than that of T2 phase, so T2 >> T1, here we only consider T2 time.

For the T2 time period, the time cost when the difference between the sampling capacitor voltage and the input signal VIN is within 0.5LSB is calculated by formula (1-7), and the expression of T2 can be obtained by solving the following equation:

$$V_{Cadc(t)}=V_{cin(t)}=(V_{IN}-V_{CX0})\left(1-e^{-\frac{t}{\tau 2}}\right)+V_{CX0} = V_{IN}-0.5LSB$$

$$T2=-\tau 2*\ln\left(\frac{\alpha+1}{8192}\right) \qquad (2\text{-}1)$$

Therefore, we have a conclusion: for SAR ADC, the voltage on the sampling capacitor must be fully charged or discharged within the sampling time, and the difference between the voltage on sampling capacitor and the external input voltage should not exceed 0.5LSB. Otherwise, no matter how excellent the performance of the ADC is, the best sampling accuracy cannot be obtained. For the extremely high input impedance, we add a capacitor to limit the amplitude of voltage drop or rising pulse during a single sampling. However, in this case, it is necessary to add sufficient time delay between each two sampling to charge the internal sampling capacitor, so as to ensure that the voltage difference between the sampling capacitor and the external signal is within the quantization error range when the sampling switch is closed

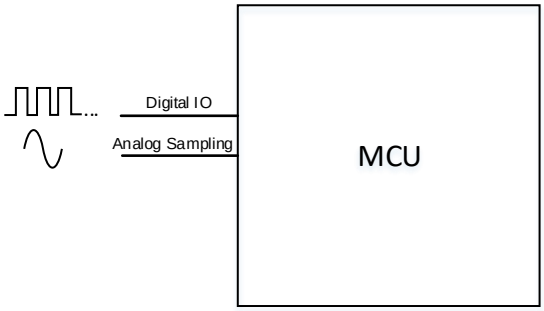
In particular, when ADC is working in continuous sampling mode or scanning sampling mode, if the input impedance is too large, the sampling result of the channel with too large input impedance will be affected by the signal of the previous sampling channel. This phenomenon will be significantly improved by increasing the sampling time to meet the impact of input

impedance.

2.6. Influence of crosstalk between I/O

Due to the capacitive coupling between pins and even bonding wires inside the chip, the crosstalk between I/O will have a significant impact on the sampling accuracy of ADC, especially when the analog sampling channel of ADC is adjacent to the digital I/O (such as PWM output). As shown in ***Figure 2-7. Diagram of crosstalk between analog and digital I/O***.

Figure 2-7. Diagram of crosstalk between analog and digital I/O



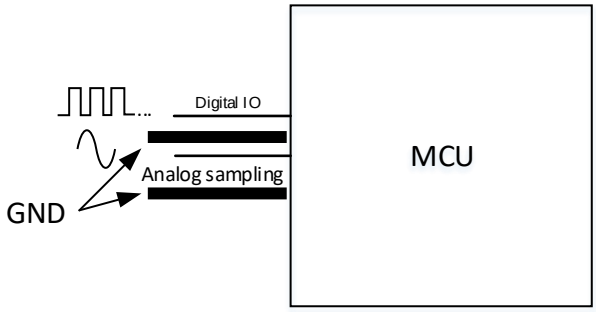
As shown in ***Figure 2-8. The waveform of crosstalk between analog I/O and digital I/O***. The diagram shows the waveform when the channel of ADC is close to the PWM output channel. When there is a level reversal on PWM output channel, the signal fluctuation will be caused on the adjacent ADC sampling channels. If the ADC takes a sampling at this time, the sampling result may have a large error.

Figure 2-8. The waveform of crosstalk between analog I/O and digital I/O

There are several methods to try to reduce the impact of crosstalk on ADC sampling. First, in terms of pin planning, it is necessary to plan in advance to keep the digital I/Os that need to be continuously flipped away from the ADC sampling channel. If the frequently flipped digital I/O cannot be far away from the analog sampling port due to resource constraints, we can take some measures in layout to reduce the impact. For example, we can isolate it by adding

a certain area of GND between the digital I/O and the analog channel, as shown in ***Figure 2-9. Add ground shield between analog and digital I/O.*** Of course, as the ground shield cannot cover the inside of the chip, the crosstalk between bonding wires will still exist. In addition, slowing down the edge of the digital signal will also reduce the impact of crosstalk. For example, adding a capacitor with an appropriate capacitance value to the digital signal to slow down the drive speed of the MCU digital IO port can also significantly slow down the edge of this digital signal. At the software level, we also have some attempts, such as performing an ADC conversion when the digital I/O port is not flipped, provided that the application allows this action.

Figure 2-9. Add ground shield between analog and digital I/O



2.7. Improve accuracy of ADC by software

Some series of GD32 MCU have the on-chip hardware oversampling function of ADC. For details, please refer to the user manual. The on-chip hardware oversampling circuit performs data preprocessing to offload the CPU. It can handle multiple conversions and average them into a single data with increased data width. It provides a result with the following formula (2-2), where N and M can be adjusted, and $D_{out}(n)$ is the n-th output digital signal of the ADC. It is at the cost of reducing the sampling rate in exchange for higher data resolution

$$Result = \frac{1}{M} * \sum_{n=0}^{N-1} D_{out}(n) \quad (2\text{-}2)$$

The on-chip hardware oversampling circuit performs the following functions: summing and bit right shifting. The oversampling ratio N is defined by the OVSR[2:0] bits in the ADC_OVSAMPCTL register. It can range from 2x to 256x. The division coefficient M means bit right shifting up to 8-bit. It is configured through the OVSS[3:0] bits in the ADC_OVSAMPCTL register.

Table 2-2. Maximum output results vs N and M Grayed values indicates truncation

Oversampling ratio	Max Raw data	No-shift OVSS=0000	1-bit shift OVSS=0001	2-bit shift OVSS=0010	3-bit shift OVSS=0011	4-bit shift OVSS=0100	5-bit shift OVSS=0101	6-bit shift OVSS=0110	7-bit shift OVSS=0111	8-bit shift OVSS=1000
2x	0x1FFE	0x1FFE	0x0FFF	0x07FF	0x03FF	0x01FF	0x00FF	0x007F	0x003F	0x001F

Oversampling ratio	Max Raw data	No-shift OVSS=0000	1-bit shift OVSS=0001	2-bit shift OVSS=0010	3-bit shift OVSS=0011	4-bit shift OVSS=0100	5-bit shift OVSS=0101	6-bit shift OVSS=0110	7-bit shift OVSS=0111	8-bit shift OVSS=1000
4x	0x3FFC	0x3FFC	0x1FFE	0x0FFF	0x07FF	0x03FF	0x01FF	0x00FF	0x007F	0x003F
8x	0x7FF8	0x7FF8	0x3FFC	0x1FFE	0x0FFF	0x07FF	0x03FF	0x01FF	0x00FF	0x007F
16x	0xFFF0	0xFFF0	0x7FF8	0x3FFC	0x1FFE	0x0FFF	0x07FF	0x03FF	0x01FF	0x00FF
32x	0x1FFE0	0xFFE0	0xFFF0	0x7FF8	0x3FFC	0x1FFE	0x0FFF	0x07FF	0x03FF	0x01FF
64x	0x3FFC0	0xFFC0	0xFFE0	0xFFF0	0x7FF8	0x3FFC	0x1FFE	0x0FFF	0x07FF	0x03FF
128x	0x7FF80	0xFF80	0xFFC0	0xFFE0	0xFFF0	0x7FF8	0x3FFC	0x1FFE	0x0FFF	0x07FF
256x	0xFFF00	0xFF00	0xFF80	0xFFC0	0xFFE0	0xFFF0	0x7FF8	0x3FFC	0x1FFE	0x0FFF

The conversion timings in oversampled mode do not change compared to standard conversion mode: the sampling time remains equal throughout the oversampling sequence. New data is supplied every N conversion.

For MCU without on-chip hardware oversampling module, some filtering algorithms can also be used in software algorithm to reduce the fluctuation of input signal sampling value. For example, the most common averaging algorithm, which requires CPU computing power and a certain amount of RAM space in the process. This averaging algorithm is suitable for the case where the input signal changes slowly and there is occasional pulse interference. If the signal change frequency is greater than the execution frequency of the average filtering algorithm, the details of the signal change will be lost, and the average sampling result cannot reproduce all the information of the signal.

3. Revision history

Table 3-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	June.10.2022
1.1	Add content of Influence of crosstalk between I/O	Dec.12.2022

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