GigaDevice Semiconductor Inc.

GD32F5HC Hardware Development Guide

Application Notes
AN321

Revision 1.0

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1. Introduction

This hardware application development guide is specially designed for developers working with the highly integrated 32-bit general-purpose MCU GD32F5HC series, which is based on the Arm® Cortex®-M33 processor and TrustZone® technology. It provides developers with an overall understanding of hardware development for the GD32F5HC series, including topics such as power supply, reset, clock configuration, boot mode settings, and program downloading and debugging.The purpose of the Application Notes is to enable developers to quickly get started with GD32F5HC series, quickly develop and use the product hardware, and save time for studying the manual, thus accelerating the product development progress.

The Application Notes is described in eight parts:

1. Power supply: It mainly introduces the design of the power management, power supply, and reset functions of GD32F5HC series.
2. Clock: It mainly introduces the design of the high and low speed clock functions of GD32F5HC series.
3. Boot configuration: It mainly introduces the BOOT configuration and design of GD32F5HC series.
4. Typical peripheral module: It mainly introduces the hardware design of the main functional modules of GD32F5HC series.
5. Download debug circuit: It mainly introduces the typical download debug circuits recommended for GD32F5HC series.
6. Reference circuit and PCB layout design: It mainly introduces the precautions for hardware circuit design and PCB layout design of GD32F5HC series.
7. Steel mesh and soldering: It mainly introduces the selection and usage method of the steel mesh and the reflow soldering temperature curves.
8. Package description: It mainly introduces the types and names of packages included in GD32F5HC series.

This document also introduces the minimum system hardware resources used in GD32F5HCxx application development.

Table 1-1. Applicable product

Type	Model
MCU	GD32F5HCxx Series

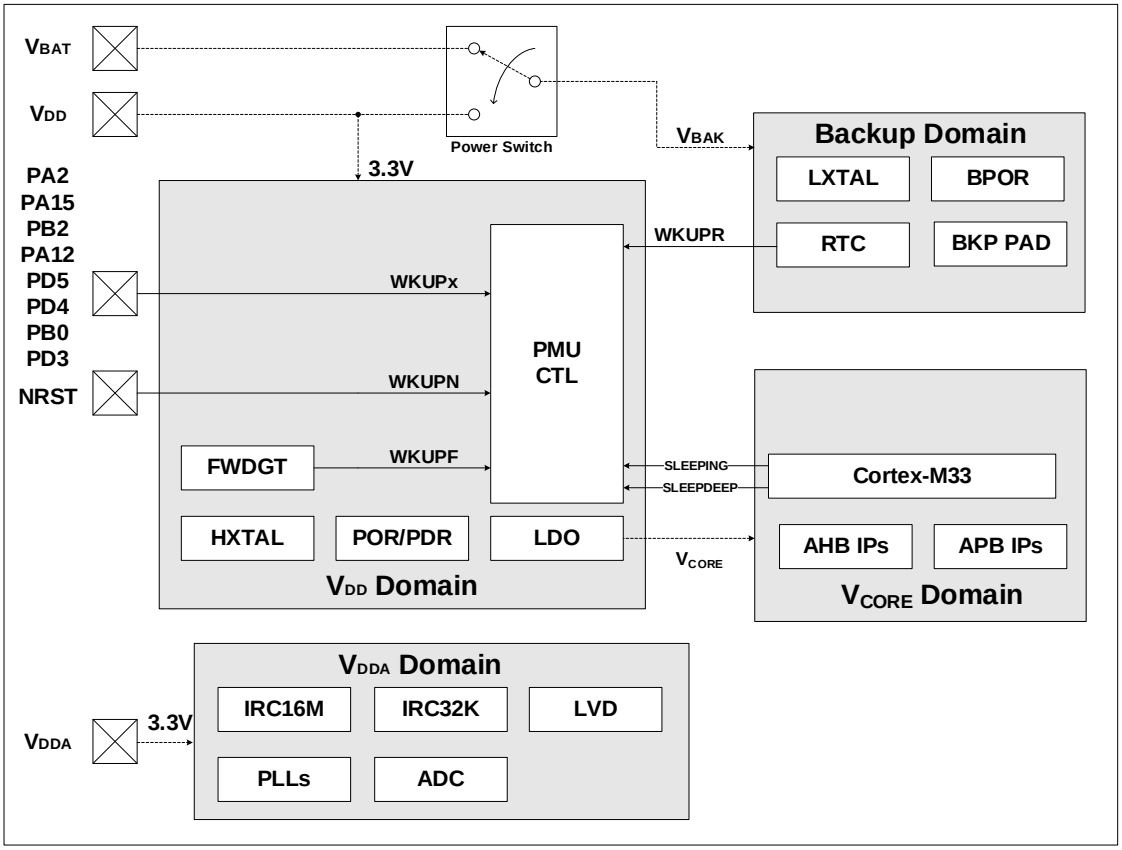
Note: This application note is for reference only. In case of any conflict with the user manual or datasheet, the user manual or datasheet shall prevail.

2. Hardware design

2.1. Power supply

The operating voltage of V_{DD} / V_{DDA} domain of GD32F5HCxx ranges from 2.7 V to 3.63 V. As shown in ***Figure 2-1. Overview of power domains of GD32F5HC***, The GD32F5HC series devices have three power domains, including the V_{DD} / V_{DDA} domain.The V_{DD} / V_{DDA} domain is powered directly by the external power supply. An LDO regulator is embedded within the V_{DD} / V_{DDA} domain to supply power to the V_{CORE} domain.In the backup domain, there is a power switch that automatically switches the backup domain's power source to the V_{BAT} pin when the V_{DD} power is turned off. At this time, the backup domain is powered by the V_{BAT} pin (battery).

Figure 2-1. Overview of power domains of GD32F5HC



LVD: Low Voltage Detector
LDO: Voltage Regulator
BPOR: V_{BAK} Power On Reset
POR: Power On Reset
PDR: Power Down Reset

2.1.1. Backup domain

The supply voltage of backup domain ranges from 1.62 V to 3.63 V. The power switch in the backup domain selects V_{DD} or V_{BAT} (battery) as the power supply, and then V_{BAK} powers the backup domain. In order to ensure the contents of the register in the backup domain and

normal operation of RTC, when V_{DD} is off, V_{BAT} pin can be powered by being connected to a battery or other backup power supply. If there are no battery-powered external applications, it is recommended to connect V_{BAT} pin to V_{DD} pin after being connected via a 100 nF capacitor to ground.

Precautions for V_{BAT} power supply:

In terms of power consumption of V_{BAT} pin, theoretically, when V_{DD} is powered on, the power switch in the backup domain is connected to V_{DD}, with no current passing through V_{BAT} pin. However, when ADC channel is used for V_{BAT} measurement in the main program, V_{BAT} will be divided by 4 due to MCU design and flow into ADC channel, thus causing extra power consumption at V_{BAT} pin.

2.1.2. V_{DD}/V_{DDA} power domain

V_{DD}/V_{DDA} power domain includes two parts: V_{DD} domain and V_{DDA} domain. If V_{DDA} is not equal to V_{DD}, the voltage difference between them must not exceed 300 mV (V_{DDA} and V_{DD} inside the chip are connected through back-to-back diodes). To avoid noise, V_{DDA} can be connected to V_{DD} through an external filter circuit, and V_{SSA} can be connected to V_{SS} through a specific circuit (single-point grounding through 0 Ω resistors or magnetic beads, etc.).

2.1.3. Power-saving modes

The GD32F5HC series provides four power-saving modes, namely sleep mode, deep-sleep mode, standby mode, and SRAM sleep mode.Their comparison is listed in ***Table 2-1. Summary of power-saving modes***.

Table 2-1. Summary of power-saving modes

Mode	Sleep mode	Deep sleep mode	Standby mode	SRAM Sleep
Description	Only the CPU clock is off	1. Turn off all clocks in the V_{CORE} domain. 2. Disable IRC16M, IRC48M, HXTAL, and PLL.	1. Power off the V_{CORE} domain. 2. Disable IRC16M, IRC48M, HXTAL, and PLL..	At least one of SRAM1 / SRAM2 / SRAM3 is powered down
LDO status	On (in normal power consumption and normal drive modes)	On (in normal/low power consumption and normal/low drive modes)	Off	Enabled (normal power mode or low-power mode, normal drive or low-drive mode)
Setting	SLEEPDEEP = 0	SLEEPDEEP = 1 STBMOD = 0	SLEEPDEEP = 1 STBMOD = 1, WURST = 1	SRAMxPSLEEP = 1 (x = 1/2/3)
Entry command	WFI or WFE	WFI or WFE	WFI or WFE	-
Wake-up	Wake up MCU from	Wake up MCU from	1. NRST pin	SRAMxPWAKE

Mode	Sleep mode	Deep sleep mode	Standby mode	SRAM Sleep
	the sleep mode which was entered through WFI by any interrupt. Wake up MCU from the sleep mode which was entered through WFE by any event or interrupt in the case that the SEVONPEND bit is set to 1.	deep sleep mode which was entered through WFI by any interrupt. Wake up MCU from the deep sleep mode which was entered through WFE by any event from EXTI or interrupt in the case that the SEVONPEND bit is set to 1.	2. WKUP pin 3. FWDGT resetting 4. RTC	= 1 (x = 1/2/3)
Delay in wake-up	None	IRC16M wake-up time The wake-up time shall be extended for LDO if it is in low power mode.	Power-on sequence	100 ns

Note: In standby mode, all I/O pins are in a high-impedance state, except for the RESET pin, the PC14 and PC15 pins used as LXTAL oscillator pins, and the enabled WKUP pins.

See ***Table 2-2. Power-saving modes of RTC*** for the power-saving modes of RTC.

Table 2-2. Power-saving modes of RTC

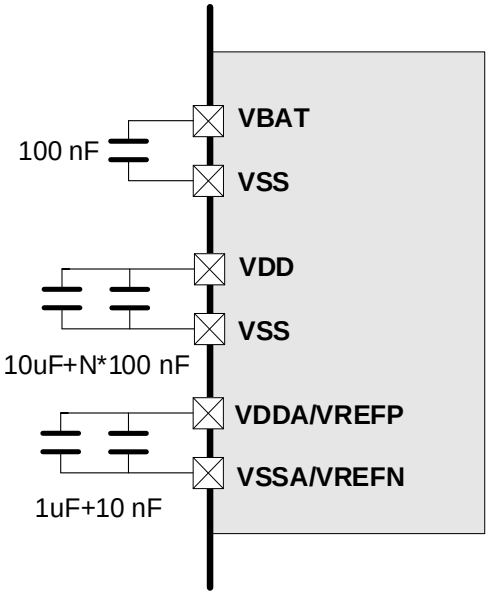
Mode	Whether to operate in such mode	Method for exiting from such mode
Sleep mode	Yes	RTC interrupt
Deep sleep mode	Operating when the clock source is LXTAL or IRC32K	RTC clock/intrusion/timestamp/wake-up event
Standby mode	Operating when the clock source is LXTAL or IRC32K	RTC clock/intrusion/timestamp/wake-up event

2.1.4. Power supply design

The system requires a stable power supply, and pay attention to the following precautions during development and use:

- The VDD pins must be connected to external to-ground capacitors (N * 100 nF ceramic capacitor + not less than 10 uF tantalum capacitor; at least a VDD pin shall be connected to a not less than 10 uF capacitor to GND, while other VDD pins shall be connected to 100 nF capacitors).
- The VDDA/VREFP pins must be connected to external to-ground capacitors (10 nF + 1 uF ceramic capacitors are recommended).
- The VBAT pin must be connected to an external battery.If no external battery is used, it is recommended to connect the VBAT pin to the VDD pin through a 100nF capacitor to ground.

Figure 2-2. Power supply design recommended for GD32F5HC



Note: All decoupling capacitors must be installed close to VDDA, VDDA/VREFP, and VBAT pins of the chip.

2.2. Power detection and reset

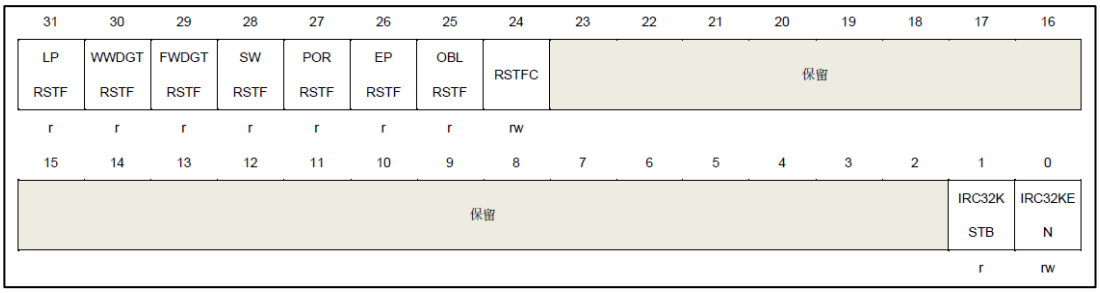
The reset control of GD32F5HC series includes three types: power reset, system reset, and backup domain reset. Power reset is also called cold reset, which works for all systems except the backup domain. System reset works for all parts other than SW-DP controller and backup domain, including processor core and peripheral IPs. Backup domain reset works for backup area. Reset can be triggered by the external signal, internal event, and reset generator.

Table 2-3. Reset contents under different reset types

Reset mode	Power reset	System reset	Backup domain reset
Reset contents	All systems except the backup domain	All parts other than SW-DP controller and backup domain, including processor core and peripheral IPs	Backup area

The MCU reset sources can be obtained by querying the RCU_RSTSCK register, which can only be cleared by a power-on reset. Therefore, during use, after obtaining the reset source, the reset flag can be cleared through the RSTFC control bit. Afterwards, in the event of a watchdog reset or other reset events, it can be more accurately reflected in the RCU_RSTSCK register.

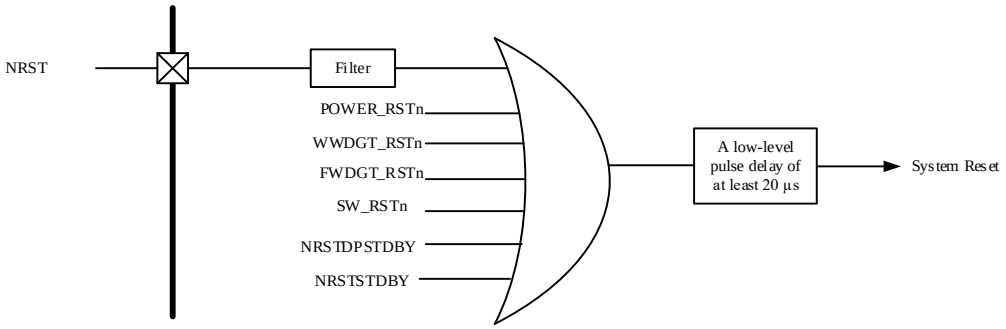
Figure 2-3. RCU_RSTSCK register



During the power supply and system reset process, NRST will maintain a low level until the reset is complete. If the MCU does not operate, an oscilloscope can be used to monitor the waveform of the NRST pin to determine if the chip is continuously experiencing reset events.

MCU integrates a power-up / power-down reset circuit, when a reset occurs, the system reset pulse generator ensures that each reset source (external or internal) can have a low level pulse delay of at least 20 μs. To prevent unintended reset triggering, it is recommended to place a capacitor (typically 100nF) on the NRST pin.The reset mothod in ***Figure 2-4. System reset circuit*** is thesystem reset.

Figure 2-4. System reset circuit



A backup domain reset is generated when one of the following events occurs:

1. The BKPRST bit in the backup domain control register is set to '1';
2. Backup domain power-on reset (when both V_{DD} and V_{BAT} are powered down, and then V_{DD} or V_{BAT} is powered up).

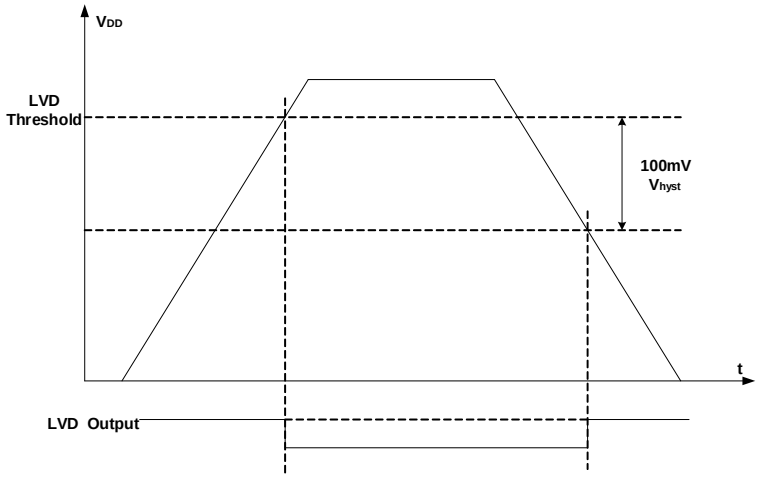
2.2.1. LVD

LVD is used to detect whether the supply voltage of V_{DD} is lower than the low voltage detection threshold, which is set by the LVDT[2:0] bit in the power control register (PMU_CTL0). LVD is enabled by setting LVDEN. The LVDF bit in the power status register (PMU_CS0) indicates whether the low voltage event connected to line 16 of EXTI occurs. An interrupt can be generated by setting line 16 of EXTI. ***Figure 2-5. LVD threshold waveform*** shows the relation between the supply voltage of V_{DD} / V_{DDA} and the output signal of LVD. (The interrupt signal of LVD depends on the rising or falling edge configuration of line 16 of EXTI). The hysteresis voltage V_{hyst} is 100 mV.

LVD application scenario: When the power supply of MCU is subject to external interference,

such as voltage drop, we can set the low voltage detection threshold (greater than the PDR value) through LVD. Once the voltage drops to the threshold, LVD interrupt is enabled, and operations such as soft reset can be set in the interrupt function to avoid other exceptions in MCU.

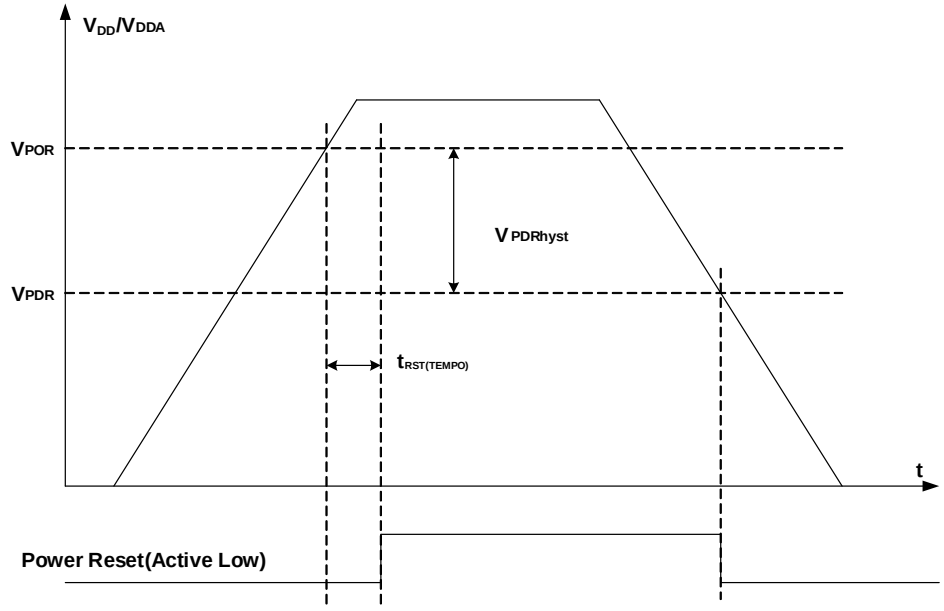
Figure 2-5. LVD threshold waveform



2.2.2. POR / PDR

The POR/PDR (Power-On/Power-Down Reset) circuit monitors V_{DD} / V_{DDA} and generates a power reset signal when the voltage falls below a specific threshold, resetting the entire chip except for the backup domain. V_{POR} represents the power-on reset threshold voltage, V_{PDR} represents the power-down reset threshold voltage, and the hysteresis voltage V_{hyst} value should be referenced from the chip datasheet. Its timing is shown in ***Figure 2-6. POR / PDR waveform***.

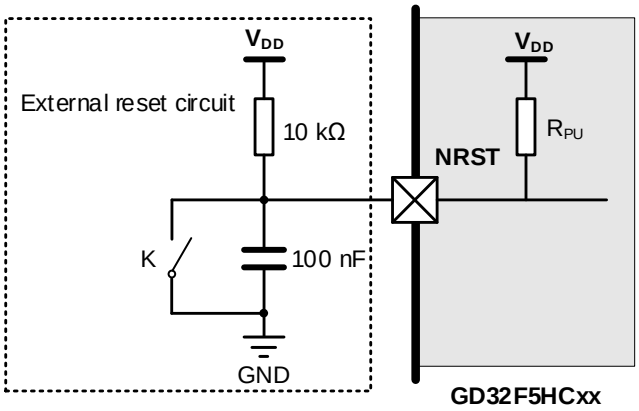
Figure 2-6. POR / PDR waveform



2.2.3. NRST pin

To prevent accidental triggering of the reset for the MCU's NRST pin, it is recommended to place a capacitor on the NRST pin (a typical value is 100 nF).

Figure 2-7. Recommended external reset circuit

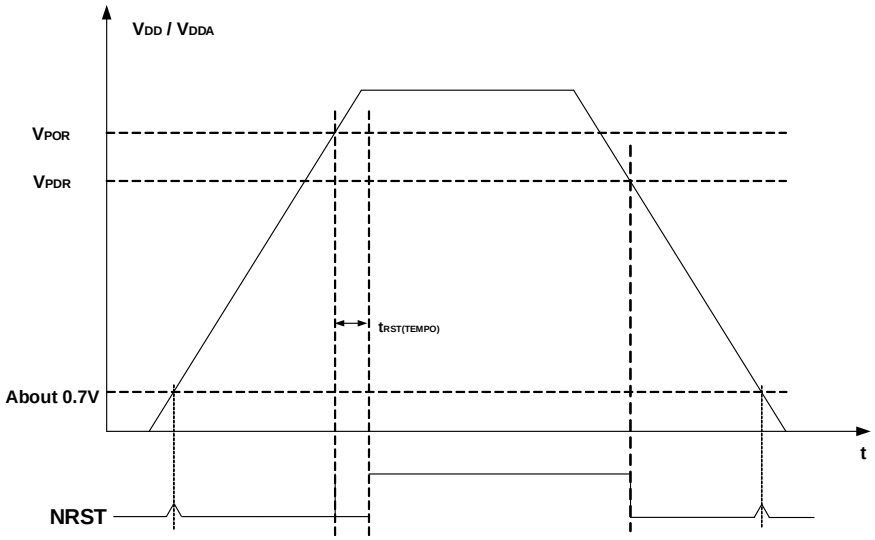


Note:

1. 10 kΩ pull-up resistor is recommended so that voltage interference would not cause abnormal operation of the chip.
2. Considering the impact of static electricity, an ESD protection diode can be installed at the NRST pins.
3. Although there is a hardware POR circuit inside MCU, it is recommended to add an external NRST reset resistance-capacitance circuit.
4. If MCU starts abnormally (due to voltage fluctuation), the capacitance of NRST to ground can be appropriately increased to extend the MCU reset completion time and avoid the abnormal power-on sequence zone.

Due to the threshold voltage characteristics of the MOS transistor, during the power-up and power-down process of the chip, when V_{DD} / V_{DDA} < 0.7 V, the internal pull-down MOS transistor of the chip will not pull down the NRST pin. Therefore, during the power-up and power-down process, when V_{DD} / V_{DDA} ≈ 0.7 V, a small pulse occurs, which does not affect the normal operation of the chip, as shown by the red pulse in ***Figure 2-8. The illustration of the pulse of the NRST pin power-up/down MOS transistor***.

Figure 2-8. The illustration of the pulse of the NRST pin power-up/down MOS transistor



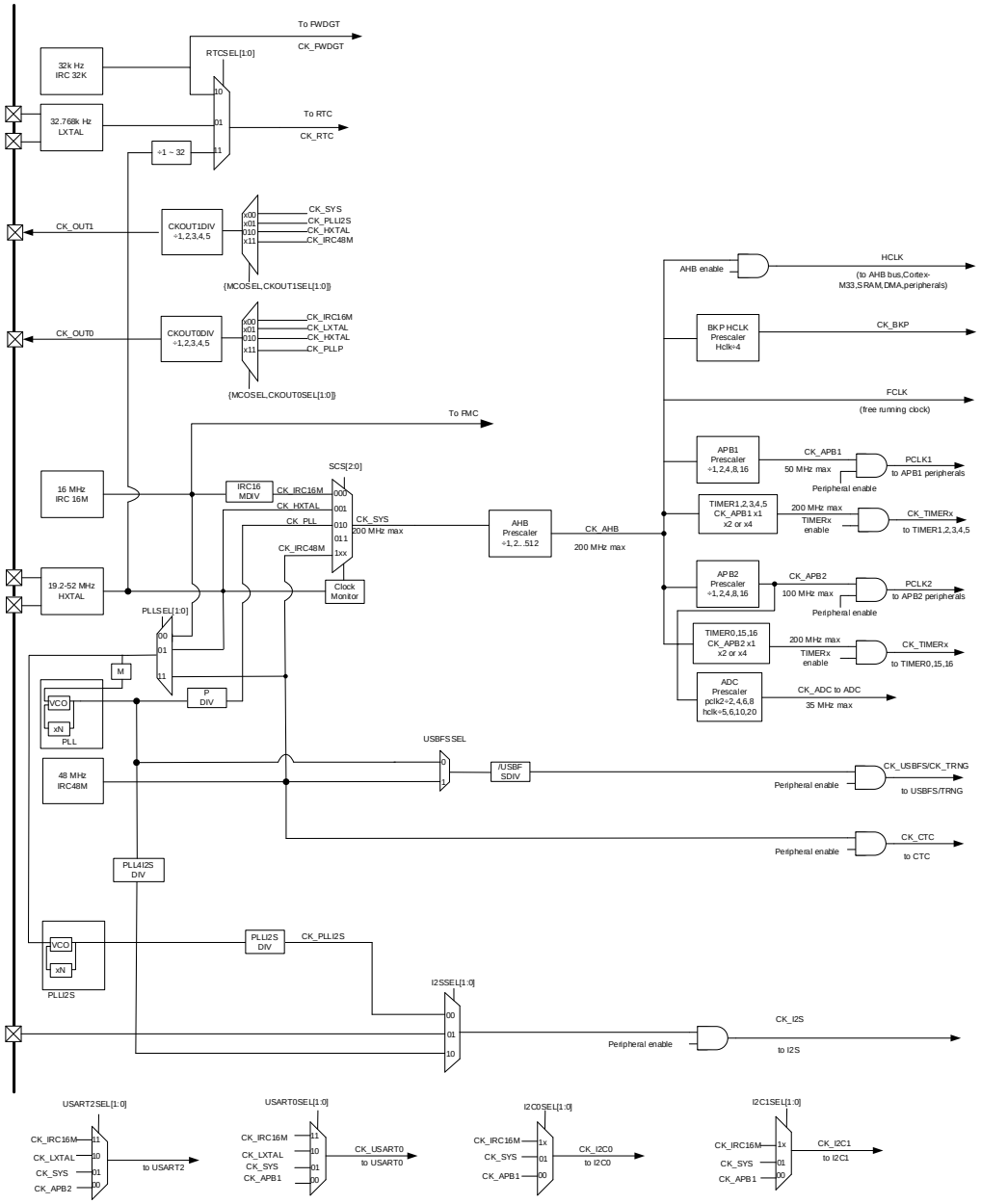
Due to the difference in charging and discharging speeds, the pulse duration of the falling edge is slightly longer than that of the rising edge, both of which are at the millisecond level.

2.3. Clock

GD32F5HC series contains a complete built-in clock system, and the appropriate clock sources can be selected according to different application scenarios. The main features of the clock are as follows:

- 19.2 - 52 MHz External High-Speed Crystal Oscillator (HXTAL)
- Internal 16 MHz RC oscillator (IRC16M)
- Internal 48 MHz RC oscillator (IRC48M)
- 32.768 kHz low speed crystal oscillator (LXTAL)
- Internal 32 kHz RC oscillator (IRC32K)
- HXTAL, IRC16M, or IRC48M selected as the clock source of PLL and PLLI2S
- HXTAL clock monitor

Figure 2-9. Clock tree



Note: The maximum operating frequency of the GD32F5HC series MCU is 200 MHz.

2.3.1. External high-speed crystal oscillator clock (HXTAL)

19.2 - 52 MHz high-speed crystal oscillator (passive crystal) can provide an accurate master clock for the system. The crystal of specific frequency must be installed close to the HXTAL pins, and the external resistors and matching capacitors connected to the crystal must be adjusted according to the selected oscillator parameters. HXTAL can also use the bypass input mode to input the clock source. In the bypass input mode, the signal is connected to the OSC_IN pin, the OSC_OUT pin remains suspended, and the Bypass function of HXTAL needs to be enabled on the software (It can be enabled by configuring the HXTALBPS and HXTALEN bits in the RCU_CTL register).

Figure 2-10. HXTAL external crystal circuit

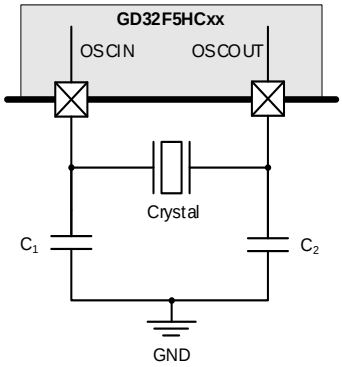
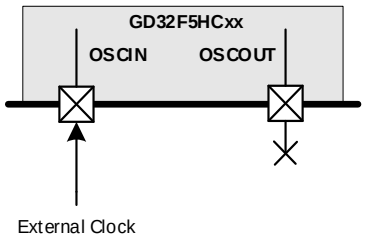


Figure 2-11. HXTAL external clock circuit in bypass mode



Note:

1. When the bypass input mode is used, the signal is input from the OSC_IN pin, and the OSC_OUT pin remains suspended.
2. For the size of the external matching capacitor, refer to the formula: $C_1 = C_2 = 2 * (C_{LOAD} - C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, typically 10 pF. When an external high-speed crystal is recommended, try to choose a crystal with a load capacitance of about 20 pF, so that the external matching capacitors C_1 and C_2 can be merely 20 pF, and the crystal shall be installed as close as possible to the crystal oscillator pins on the PCB layout.
3. C_S is the parasitic capacitance on the PCB layout and IC pins. The closer the crystal is to the MCU, the smaller the C_S, and vice versa. Therefore, in practical applications, when the crystal is far away from the MCU and works abnormally, the capacitance of the external matching capacitor can be appropriately reduced;
4. When an external high-speed crystal is used, it is recommended to connect 1 MΩ resistors in parallel at both ends of the crystal to make the crystal easier to start oscillation.
5. Accuracy: external active crystal oscillator > external passive crystal > internal IRC16M;
6. Normally, Bypass is enabled when an active crystal oscillator is used. At this time, the high level should not be lower than 0.7 V_{DD}, and the low level should not be higher than 0.3 V_{DD}. If Bypass is not enabled, the amplitude requirements for the active crystal oscillator will be greatly reduced.
7. The wires between the resonator and MCU clock pins, namely the wires to OSC_OUT and OSC_IN pins of MCU, may have different lengths due to spatial limit of PCB layout. As a result, the stray capacitance introduced by the two PCB wires will be inconsistent,

resulting in unequal load capacitance values on both sides of the resonator. This difference is required to match the actual PCB. In this case, it is recommended to contact the resonator manufacturer to measure the actual value.

2.3.2. External low-speed crystal oscillator clock (LXTAL)

LXTAL crystal is a 32.768 kHz external low-speed crystal (passive crystal), which can provide a low-power consumption and high-precision clock source for RTC. The RTC module of MCU is just like a counter whose accuracy will be affected by the crystal performance, matching capacitor, and PCB material. LXTAL can also support bypass clock input (active crystal oscillator), which can be enabled by setting LXTALBPS and LXTALEN bits in RCU_BDCTL.

Figure 2-12. LXTAL external crystal circuit

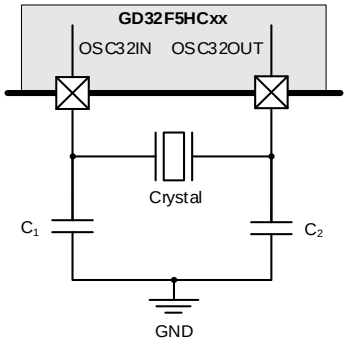
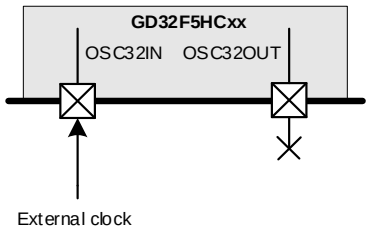


Figure 2-13. LXTAL external clock circuit in bypass mode



Note:

1. When the bypass input mode is used, the signal is input from the OSC32_IN pin, and the OSC32_OUT pin remains suspended.
2. For the size of the external matching capacitor, refer to the formula: $C_1 = C_2 = 2 * (C_{LOAD} - C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, which empirically ranges from 2 pF to 7 pF and is recommended to be 5 pF for calculation. When an external crystal is recommended, try to choose a crystal with a load capacitance of about 10 pF, so that the external matching capacitors C_1 and C_2 can be merely10 pF, and the crystal shall be installed as close as possible to the crystal oscillator pins on the PCB layout.
3. When IRC32K is selected as the clock source of RTC that is separately powered by external V_{BAT}, RTC will stop counting if MCU is powered down. After MCU is powered on again, RTC will keep counting starting from the previous count value. If external V_{BAT}

shall separately power RTC and RTC can still perform normal counting after MCU is powered down, LXTAL must be selected as the clock source of RTC.

4. The drive capability of LXTAL can be set in MCU. If it is difficult for an external low-speed crystal to start oscillation during actual debugging, the drive capability of LXTAL can be adjusted to high drive capability.
5. The wires between the resonator and MCU clock pins, namely the wires to OSC_OUT and OSC_IN pins of MCU, may have different lengths due to spatial limit of PCB layout. As a result, the stray capacitance introduced by the two PCB cables will be inconsistent, resulting in unequal load capacitance values on both sides of the resonator. A difference is required to match the actual PCB. In this case, it is recommended to contact the resonator manufacturer to measure the actual value.

2.3.3. Clock output capability (CKOUT)

GD32F5HC series MCU can output 32 kHz to 200 MHz clock signal. Different clock signals can be selected by setting the CK_OUT0 clock source selection bit field CKOUT0SEL in the clock configuration register 0(RCU_CFG0). CK_OUT1 clock output source can be selected by setting the CKOUT1SEL bit filed in the clock configuration register RCU_CFG0. GPIO pins shall be set in the alternate function I/O (AFIO) mode to output the selected clock signal.

Table 2-4. Clock source selection for clock output 0

Clock source selection bit field for clock output 0	Clock source
00	CK_IRC16M
01	CK_LXTAL
10	CK_HXTAL
11	CK_PLLP

Table 2-5. Clock source selection for clock output 1

Clock source selection bit field for clock output 1	Clock source
00	CK_SYS
01	CK_PLLI2S
10	CK_HXTAL
11	CK_IRC48M

2.3.4. HXTAL clock monitor (CKM)

The HXTAL clock monitoring function can be enabled by setting the HXTAL clock monitoring enable bit CKMEN in the control register RCU_CTL. The function must be enabled after the HXTAL boot delay is over and disabled after HXTAL stops. Once an HXTAL fault is monitored, HXTAL will be automatically disabled, and the HXTAL clock blocking interrupt flag bit CKMIF in the interrupt register RCU_INT will be set to 1, which will generate the HXTAL fault event. The fault-induced interrupt is connected to the non-maskable interrupt (NMI) of Cortex®-M33. In the case of the failure of HXTAL that is selected as the clock source of the system or PLL, IRC16M will be selected as the clock source of the system and PLL will be automatically

disabled.

Note: After the HXTAL clock monitor is enabled, the hardware will automatically enable the IRC16M clock, regardless of the status of the IRC16MEN control bit.

2.4. Boot configuration

During startup of the GD32F5HC series, the BOOT0 and BOOT1 pins are used to select the boot memory address.

When reset is released, the value of BOOTx (x = 0/1), obtained from either the pin or the EFBOOTx bit, is latched. The user can set the BOOTx value to select the desired boot mode. Upon exiting Standby mode, the BOOTx pins or EFBOOTx bits are resampled (depending on the values of the EFBOOTLK and SWBOOTx bits in the EFUSE_CTL register). Therefore, they must retain the desired boot mode configuration while in Standby mode. After a startup delay, the boot area selection is completed before the processor reset is released.

The embedded bootloader resides in the system memory and is used to reprogram the main memory of the on-chip Flash. The bootloader can be activated through specific interfaces; please refer to the Boot Mode section in the datasheet.

The embedded bootloader, located in the system memory, is used to reprogram the Flash memory. The bootloader can be activated through one of the following serial interfaces: USART0 (PA8, PB15), USART1 (PA2, PA3), USART2 (PB10, PB11), and USBFS (PB12, PB13).

Note: When the MCU boots from system memory, the USART and USB interfaces remain in detection mode. Therefore, the unused USART RX pins (PA8, PA3, PB11) must be kept at a stable logic level. The unused USB DP pin (PB12) should not be pulled down; a pull-up is recommended. This design helps prevent unintended triggering during connection.

The BOOT0 value can be sourced either from the BOOT0 pin or from the EFBOOT0 bit in the EFUSE_CTL register, allowing the GPIO pin to be freed when needed. Similarly, the BOOT1 value can be sourced from the PA14 pin or from the EFBOOT1 bit in the EFUSE_CTL register, also enabling the release of the GPIO pin when required.

In circuit design, to run the user program, the BOOT0 pin must not be left floating and is recommended to be pulled down to GND through a 10 kΩ resistor. To run the System Memory for program updates, set the BOOT0 pin high and the BOOT1 pin low. After the update is completed, pull BOOT0 low and power up again to execute the user program. Executing programs from SRAM is mainly used for debugging purposes.

Table 2-6. BOOT0 mode

EFUSE_CTL		FMC_OBR1		BOOT0 PC8	BOOT0
SWBOOT0	EFBOOT0	SWBOOT0	nBOOT0		
0	-	1	-	0	0
0	-	1	-	1	1

EFUSE_CTL		FMC_OBR1		BOOT0 PC8	BOOT0
SWBOOT0	EFBOOT0	SWBOOT0	nBOOT0		
0	-	0	1	-	0
0	-	0	0	-	1
1	0	-	-	-	0
1	1	-	-	-	1

Table 2-7. BOOT1 mode

EFUSE_CTL		FMC_OBR1		BOOT1 PA14 SWBOOT1	BOOT1
SWBOOT1	EFBOOT1	SWBOOT1	nBOOT1		
0	-	1	-	0	-
0	-	1	-	0	-
0	-	0	1	0	-
0	-	0	0	0	-
1	0	-	-	1	0
1	1	-	-	1	1

The boot addresses for TrustZone® enabled and disabled modes are defined in Table 1-11 “Boot Modes when TrustZone® is Disabled (TZEN=0)” and Table 1-12 “Boot Modes when TrustZone® is Enabled (TZEN=1)”, respectively. When the EFBOOTLK bit in the EFUSE_CTL register is set to 1, the boot memory address is selected according to the BOOT1 and BOOT0 settings.

Table 2-8. Boot mode when TrustZone® is disabled, TZEN=0

EFBOOTLK	BOOT0	BOOT1	Boot Address	Boot Region
0	0	-	0x08000000	SIP Flash
0	1	0	0x0BF40000	Bootloader / ROM
0	1	1	0x0A000000	SRAM0
1	0	-	0x08000000	SIP Flash
1	1	-	0x0BF40000	Bootloader / ROM

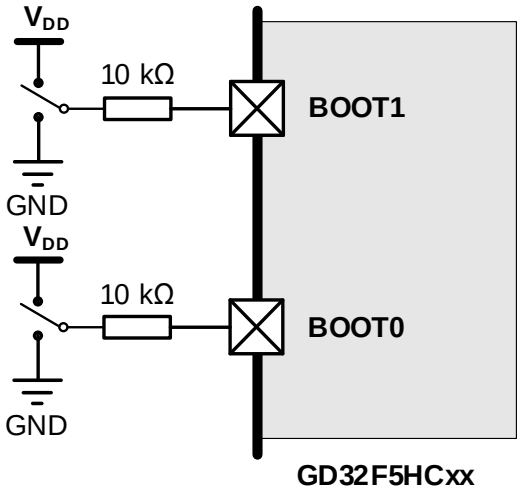
When TrustZone® is enabled through the TZEN bit, the startup space must be located in the secure region.

Table 2-9. Boot mode when TrustZone® is enabled, TZEN=1

GSSACMD == 8’hc(1)	EFBOOTLK	BOOT0	BOOT1	EFSB	Boot Address	Boot Region
0	0	0	-	0	0x0C000000	SIP Flash
0	0	0	-	1	0X0FF84000	secure boot
0	0	1	0	-	0x0FF80000	GSSA
0	0	1	1	-	0x0E000000	SRAM0
-	1	0	-	0	0x0C000000	SIP Flash
-	1	0	-	1	0X0FF84000	secure boot
-	1	1	-	-	0x0FF80000	GSSA
1	0	-	-	-	0x0FF80000	GSSA

Note: When the GSSACMD bit field is 0x0C, it represents 1; otherwise, it represents 0.

Figure 2-14. Recommended BOOT circuit design



Note:

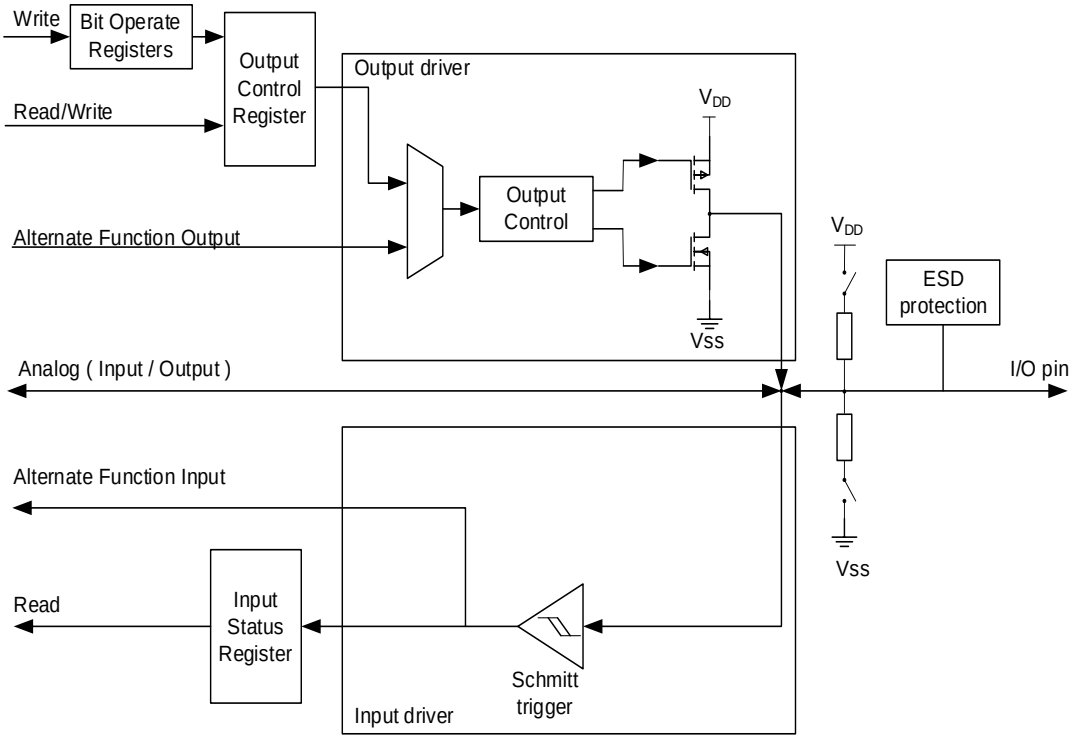
1. After MCU runs, if the BOOT state is changed, it will take effect only after the system is reset.
2. Once the BOOT1 pin states are sampled, they can be released for other purposes.

2.5. Typical peripheral modules

2.5.1. GPIO circuit

GD32F5HC series can support up to 54 general purpose I/O (GPIO) pins, including PA0 ~ PA15，PB0 ~ PB15，PC0 ~ PC15 and PD0 ~ PD5. Each pin can be set separately through the register. The basic structure of the GPIO pin is shown in ***Figure 2-15. Basic structure of standard IO***:

Figure 2-15. Basic structure of standard IO



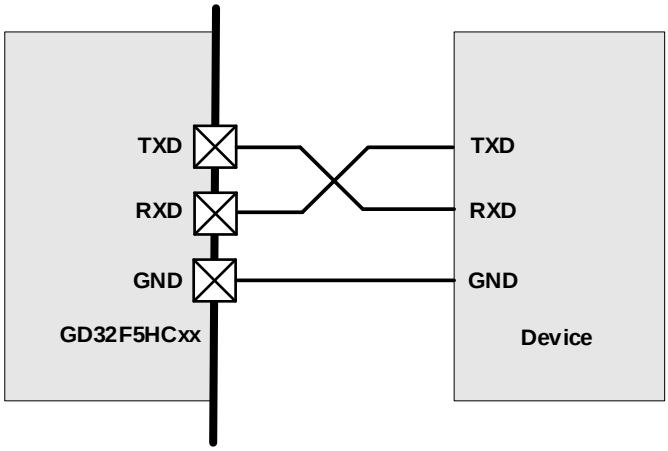
Note:

1. All I/O pins are 5 V tolerant, refer to the Datasheet for details. When a 5 V tolerant I/O pin is directly connected to 5 V, it is recommended to configure the I/O as open-drain mode, with the high-level output achieved through an external pull-up resistor.
2. Each GPIO pin can be configured by software as output (push-pull or open-drain), input, alternate function, or analog mode.
3. During or after reset, the alternate functions are not activated, and all GPIO ports are configured in analog mode. In analog mode, pull-up (PU) and pull-down (PD) resistors are disabled. To maintain consistent power consumption, it is recommended to configure all I/O pins as analog input first, and then modify them to the required mode according to application needs (including internal ports that are not externally connected).
4. To improve EMC performance, unused I/O pins are recommended to be pulled up or down by hardware (when the bootloader uses the USART interface, the USB pins must not be pulled down and are recommended to be pulled up).
5. As four IO pins (namely PC13, PC14, PC15, and PI8) have poor drive capability and limited current output capability, they can not work beyond 2 MHz after being set in output mode.
6. Peripheral interrupt/event line can be used only if the pins are set in input mode.
7. For pins connected to off-board components, switches, or buttons, it is recommended to add ESD protection circuits near the external connection. For more hardware protection design information, refer to the official document AN163 GD32 MCU EMC Hardware Protection Design Reference.

2.5.2. USART circuit

GD32F5HC series products provide three USARTs (USART0, USART1 and USART2. See *Figure 2-16. USART/UART reference circuit* for cross connection of pins when using USART/UART.

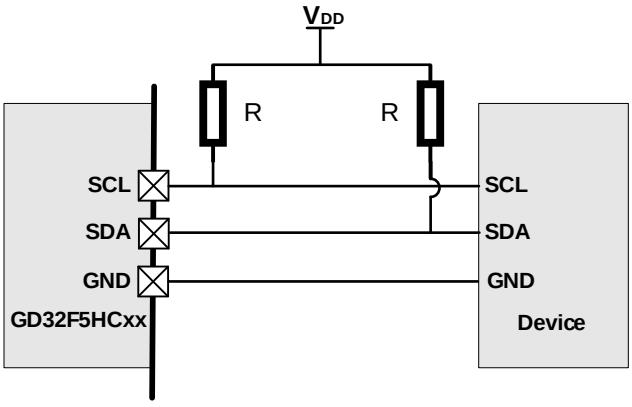
Figure 2-16. USART/UART reference circuit



2.5.3. I2C circuit

The GD32F5HC series provides two I2C peripherals, I2C0 and I2C1, which support Standard mode (up to 100 kHz), Fast mode (up to 400 kHz), and Fast+ mode (up to 1 MHz). Both SDA and SCL are bidirectional lines, and all I2C channels can operate in either master or slave mode. Multi-master mode is also supported. The I2C interface module supports DMA operation, effectively reducing the CPU workload.

Figure 2-17. I2C reference circuit



For connection to the output pole of the I2C bus device, considering wired-AND, it is required to set a high level when idle.

For the OC/OD circuits, the response speed and power consumption are determined by the pull-up resistor. A smaller pull-up resistor results in faster response, sharper signal edges, and better signal quality, but higher power consumption. Conversely, a larger pull-up resistor leads to slower response, smoother signal edges, poorer signal quality, but

lower power consumption.

Table 2-10. Reference relation between transmission mode and pull-up resistor

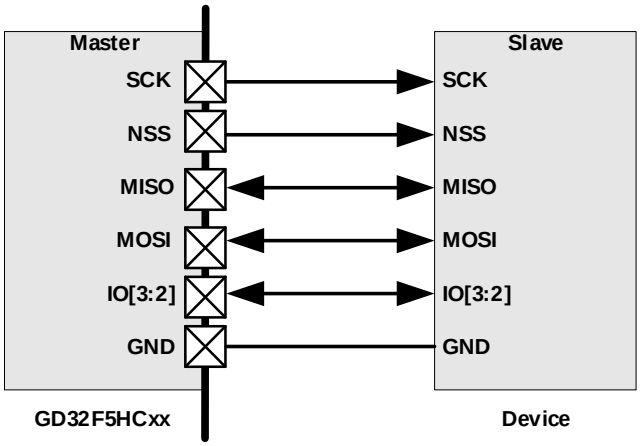
Transmission mode	Pull-up resistor (kΩ)
Standard mode	4.7
Fast mode	2.2
Fast mode plus	1.5

Considering actual wiring of I2C and complex conditions of the circuit board, the resistances of the pull-up resistor listed in ***Table 2-10. Reference relation between transmission mode and pull-up resistor*** are for reference only. In actual use, a string set can be installed between SDA and SCL to adjust the signal quality.

2.5.4. SPI circuit

The GD32F5HC series provides two SPI interfaces, among which only SPI0 supports the quad-wire SPI master mode. Except for the 4-wire SPI mode, all SPI interfaces can operate in either master or slave mode.

Figure 2-18. SPI reference circuit in four-wire mode



The above figure is only for reference when SPI0 works in four-wire mode. At that time, GD32F5HC series chip can only work as hosts. The following four connection methods in typical work modes are available for general SPI after being properly set through registers. GD32F5HC series chips can work as masters or slaves in the following work modes.

Figure 2-19. Connection of SPI in typical full duplex mode

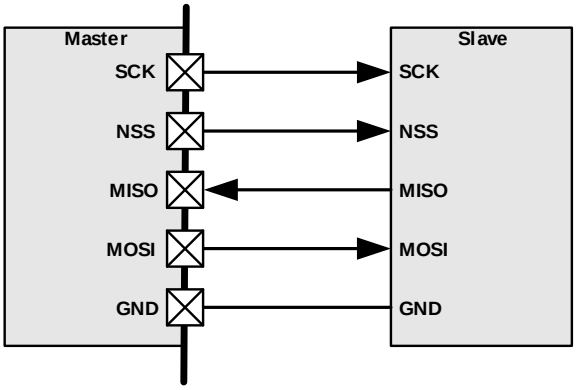


Figure 2-20. Connection of SPI in typical simplex mode (master: receiving; slave: transmitting)

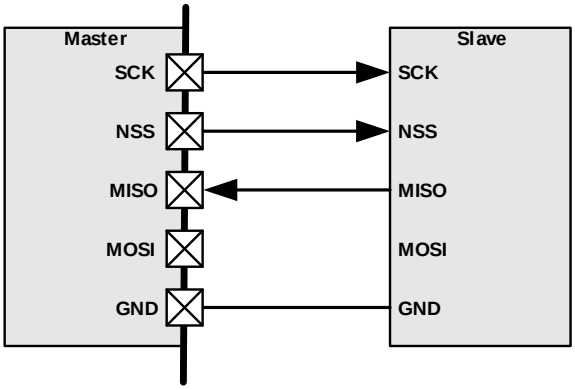


Figure 2-21. Connection of SPI in typical simplex mode (master: transmitting; slave: receiving)

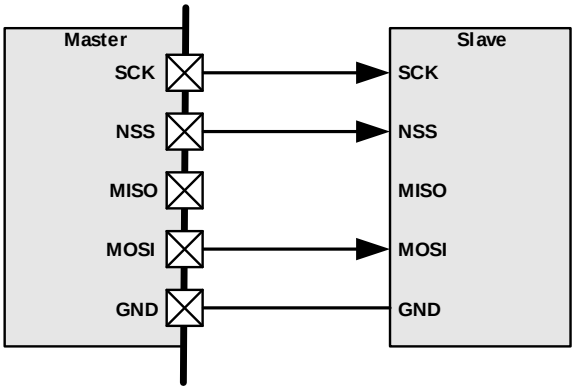
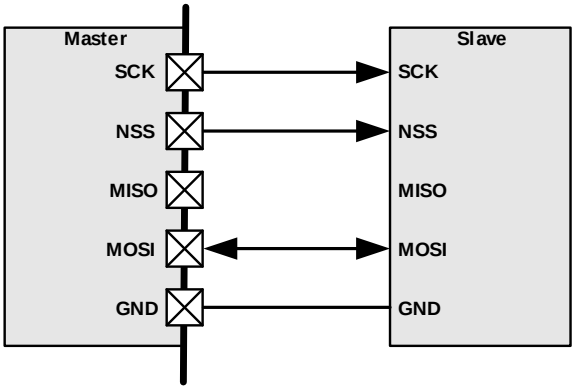


Figure 2-22. Connection of SPI in typical bidirectional line mode



2.5.5. Battery circuit

When V_{DD} is powered down, normal operation of the backup domain of GD32F5HC series chips can be kept by powering the V_{BAT} pin. The following circuits are for reference when an external battery is used to power the V_{BAT} pin.

Figure 2-23. Non-rechargeable battery reference circuit

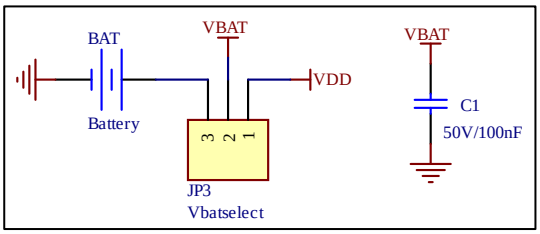


Figure 2-24. Non-rechargeable battery reference circuit

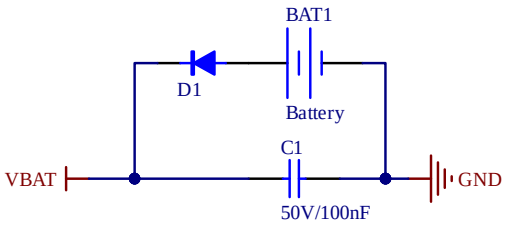
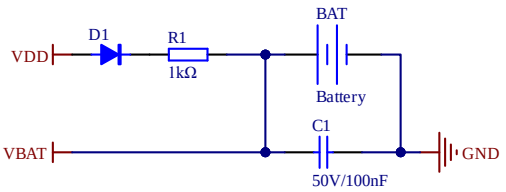


Figure 2-25. Rechargeable battery reference circuit



When referring to the above circuits, pay attention to the battery voltage, voltage drop of the diode, and supply voltage range of the V_{BAT} pin against overvoltage or undervoltage. For the resistor in the rechargeable battery reference circuit, its resistance is selected according to the battery characteristics.

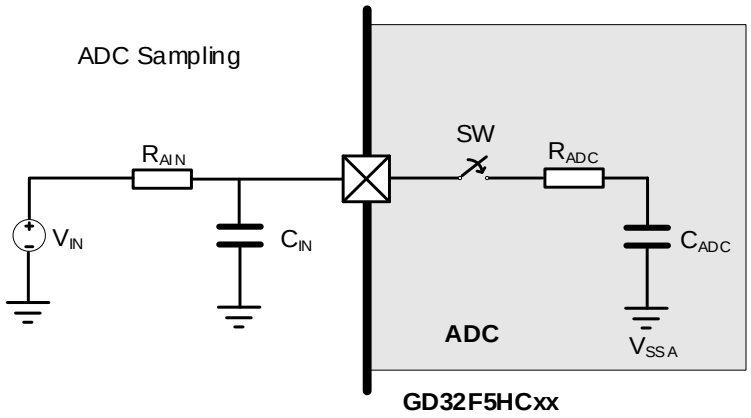
2.5.6. ADC circuit

The GD32F5HC series integrates a 12-bit successive approximation analog-to-digital converter (ADC) module, which provides up to 12 channels capable of measuring 9 external signal sources, 2 internal signal sources, and 1 external battery voltage (V_{BAT}) monitoring signal source.Internal signal is measured through the temperature sensor channel (ADC_CH9) and internal reference voltage input channel (ADC_CH10), while external signal is measured through the supply pin input channel (ADC_ CH11) for monitoring the external battery voltage (V_{BAT}). The temperature sensor reflects temperature changes and is not suitable for measuring absolute temperature. To measure the accurate temperature, an external temperature sensor must be used. The internal reference voltage V_{REFINT} provides a stable output voltage for ADC and is internally connected to ADC0_CH10. A pin is provided for monitoring the external battery voltage (V_{BAT}), which is converted to $V_{BAT}/4$.

If ADC collects the external input voltage during use and the sampled data fluctuates greatly, it may be caused by interferences due to power supply fluctuation. In this case, calibration can be done by sampling the internal V_{REFINT} to derive the external sampled voltage.

When designing the ADC circuit, it is recommended to install a small capacitor of 500 pF at the ADC input pins.

Figure 2-26. Design of ADC acquisition circuit



To obtain better conversion results, it is recommended to reduce f_{ADC} as much as possible during use, try to select a large value of sampling period, and minimize the input impedance when designing external circuits. If necessary, use the op-amp following to reduce the input impedance. When f_{ADC} is 35 MHz, the relation between the input impedance and the sampling period is as follows.

Table 2-11. Relation between sampling period and external input impedance when f_{ADC} is 35 MHz

T_s (cycles)	t_s (us)	$R_{AIN\ max}$ (kΩ)
1.5	0.04	0.88
14.5	0.41	12.84
27.5	0.79	24.80

T_s (cycles)	t_s (us)	$R_{AIN\ max}$ (kΩ)
55.5	1.59	50.57
83.5	2.39	76.33
111.5	3.19	102.1
143.5	4.10	131.5
479.5	13.7	440.7

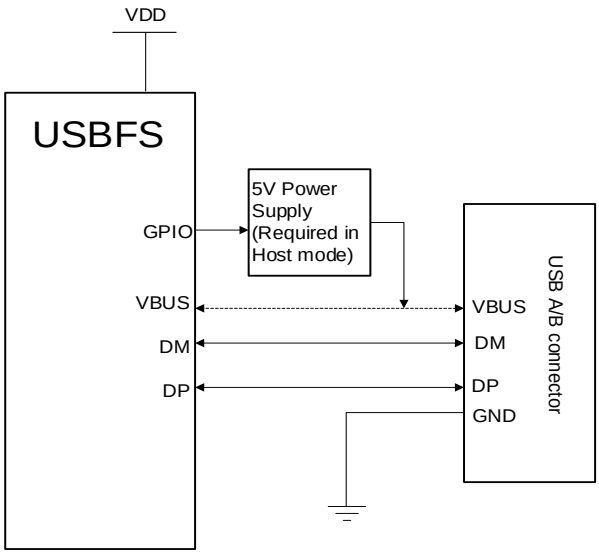
2.5.7. USB circuit

The GD32F5HC series MCUs support a USBFS interface. The USBFS integrates an internal full-speed USB PHY, eliminating the need for an external PHY chip. It supports all four transfer types defined by the USB 2.0 specification (control transfer, bulk transfer, interrupt transfer, and isochronous transfer). The USBFS can operate as a host, a device, or a dual-role device (DRD), and includes an internal full-speed PHY. The maximum supported data rate for USBFS is full speed.

The internal clock may be unable to reach the accuracy of not less than 500 ppm, which is specified in the USB protocol, so it is recommended to use an external crystal or active crystal oscillator as the clock source of the USB module when using the USB function.

The pull-up and pull-down resistors are already integrated within the internal Full-Speed PHY, and the USBFS can automatically control them according to the current mode (Host, Device, or OTG mode) and connection status. A typical connection diagram using the internal Full-Speed PHY is shown in *Figure2-27. Connection diagram in Host or Device mode*.

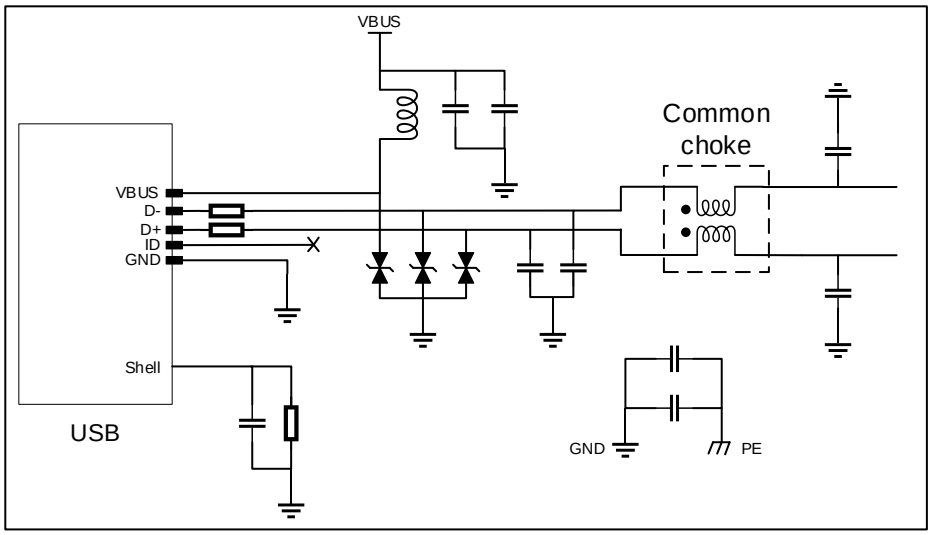
Figure2-27. Connection diagram in Host or Device mode



For better ESD performance of USB during circuit design, it is recommended to design a resistance-capacitance discharge isolation circuit for the USB shell. When high EMC performance is required, common mode chokes and TVS diodes can be used to suppress common mode interference and prevent electrostatic discharge from affecting USB

communication quality. The reference circuit design is shown in ***Figure 2-28. Recommended USB Reference Circuit***.

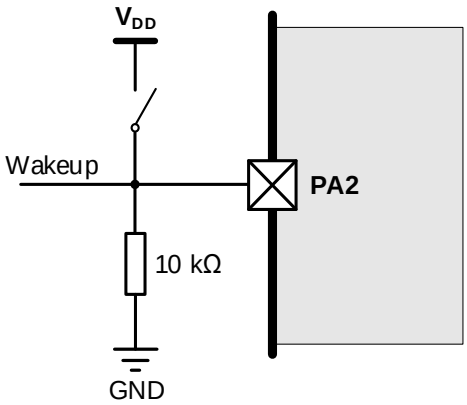
Figure 2-28. Recommended USB Reference Circuit



2.5.8. Wake-up circuit in standby mode

GD32F5HC series supports three low power modes, namely sleep mode, deep sleep mode, and standby mode. MCU in standby mode consumes the least power, but wake-up of MCU in such mode costs the longest time. MCU in standby mode can be woken up through the rising edge of the WKUP pin by setting the WUPEN bit in the PMU_CS register rather than the corresponding GPIO. The reference circuit design of the WKUP wake-up pin is as follows:

Figure 2-29. Recommended circuit design for external wake-up pin in standby mode



Note: During circuit design in this mode, if there are series resistors between the WKUP pin and V_{DD}, additional power consumption may be generated.

2.6. Download debug circuit

The core of GD32F5HC series supports JTAG debug interface and SWD interface. The standard JTAG interface is a 20-pin interface, including 5-wire signal interface. The standard SWD interface is a 5-pin interface, including 2-wire signal interface.

Note: After resetting, the debug related ports are in input PU/PD mode, where:
PA15: JTDI is in pull-up mode.
PA14: JTCK/SWCLK is in pull-down mode.
PA13: JTMS/SWDIO is in pull-up mode.
PB4: NJTRST is in pull-up mode.
PB3: JTDO is in floating mode.

Table 2-12. Allocation of JTAG download debug interfaces

Alternate function	GPIO port
JTMS	PA13
JTCK	PA14
JTDI	PA15
JTDO	PB3
NJTRST	PB4

Figure 2-30. Recommended JTAG wiring reference design

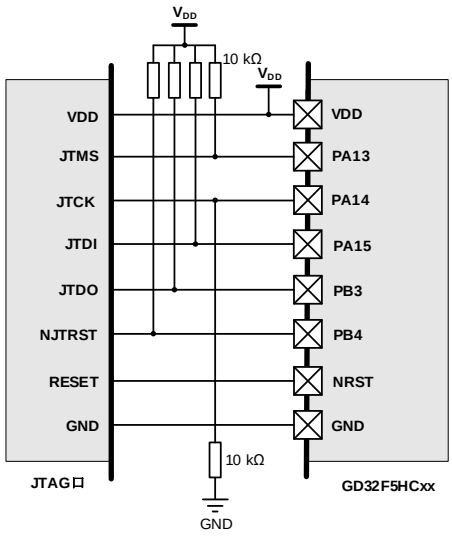
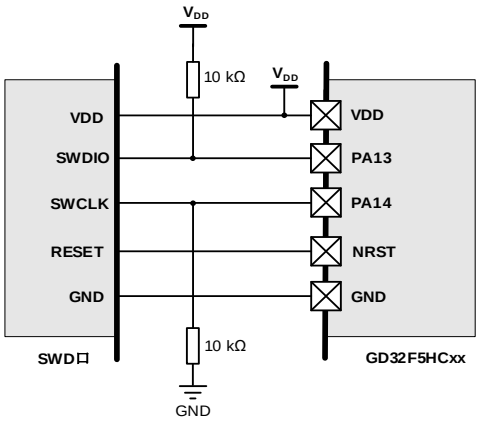


Table 2-13. Allocation of SWD download debug interfaces

Alternate function	GPIO port
SWDIO	PA13
SWCLK	PA14

Figure 2-31. Recommended SWD wiring reference design

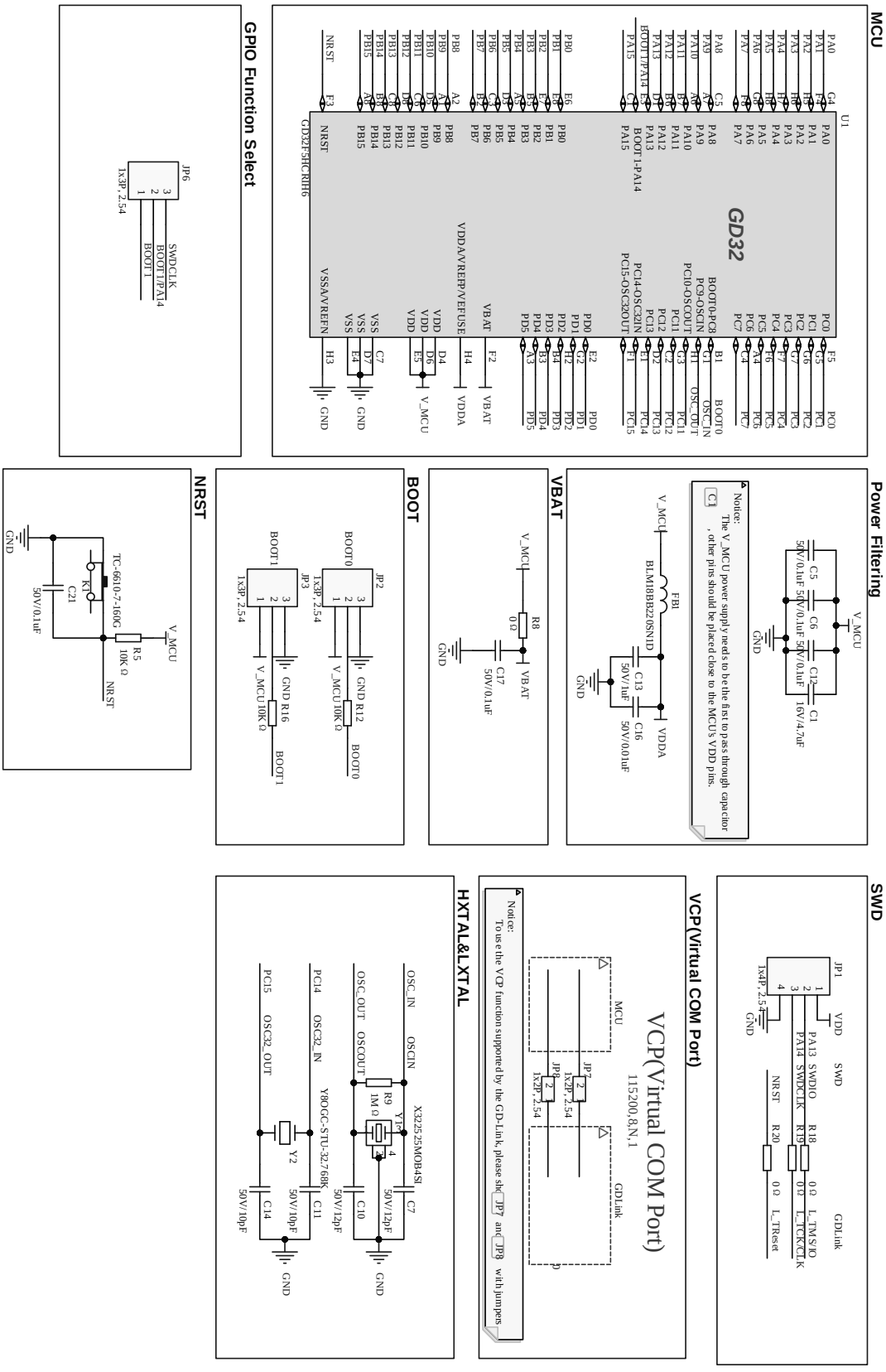


The following methods can be used to improve the reliability of SWD download debug communication and enhance the anti-interference capacity of download debug.

1. Shorten the length of the two signal wires of SWD to not more than 15 cm.
2. Twist the two SWD wires and the GND wire together.
3. Connect a small capacitor of tens of pF in parallel at two signal wires of SWD to GND.
4. Connect 100 Ω to 1 kΩ resistor to any IO of the two signal lines of SWD.

2.7. Reference schematic diagram design

Figure 2-32. Reference schematic diagram design recommended for GD32F5HC series



3. PCB Layout design

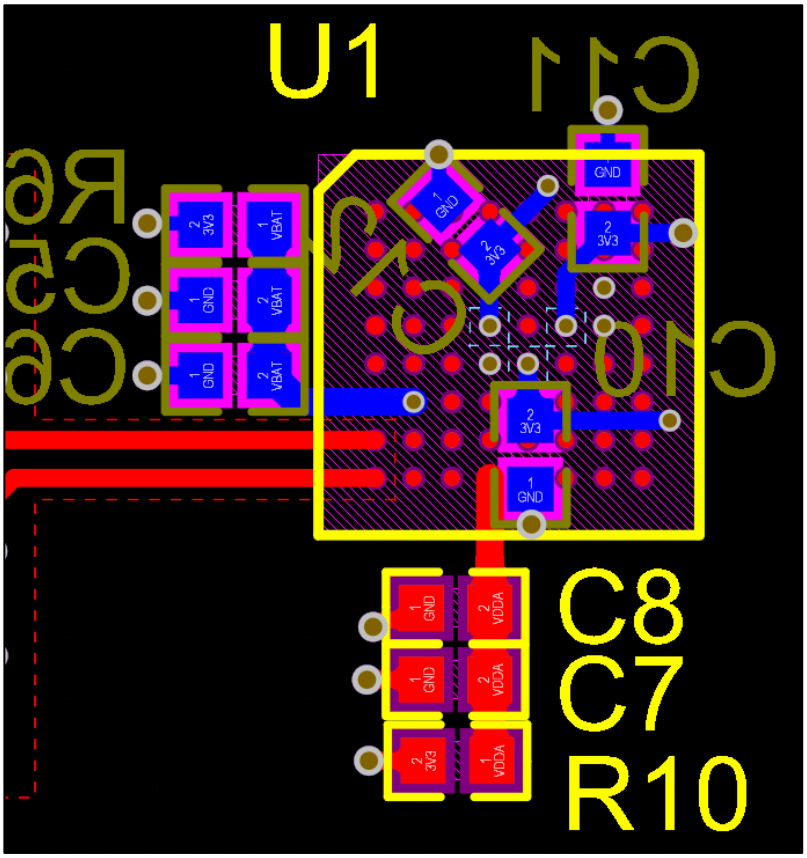
Both the performance of supporting peripheral components and the PCB layout are crucial for more stable functions and better EMC performance of MCU. In addition, if conditions permit, try to choose a PCB design scheme with an independent GND layer and an independent power layer, thus providing better EMC performance. Otherwise, it is also necessary to ensure a good power supply and grounding design, for example, by keeping the integrity of the GND plane under MCU whenever possible.

In applications with high power or strong interference, it is necessary to consider keeping MCU away from these strong interference sources.

3.1. Power supply decoupling capacitor

The power supply of GD32F5HC series has V_{DD}, V_{DDA}, V_{REFP}, and other power supply pins. The 100 nF decoupling capacitor can be ceramic MLCC and must be installed as close as possible to the power supply pins. The power supply shall be wired to the power supply pins of MCU through the capacitor. It is recommended to punch vias close to the capacitor pad for the layout.

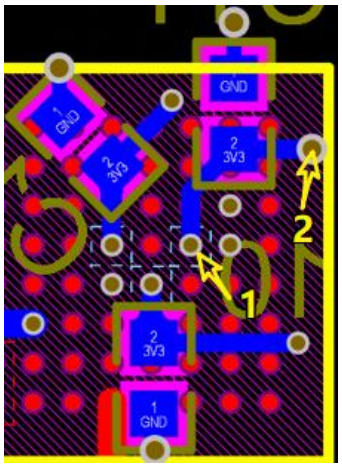
Figure 3-1. Recommended layout design of decoupling capacitor at power supply pins



From the perspective of power integrity and signal integrity, it is recommended that the

customer adopt a four-layer PCB design. The second layer should be designed as a complete GND plane, and the third layer should be designed as a complete Power plane. For the decoupling capacitor design, it is advised to use the region method (the blue square area is used to prevent Via1 from drawing power directly from the Power layer). During power supply, the current should flow through Via2 to obtain power from the Power layer, then pass through the decoupling capacitor to reach the MCU's V_{DD} pin. This configuration ensures the optimal decoupling capacitor performance.

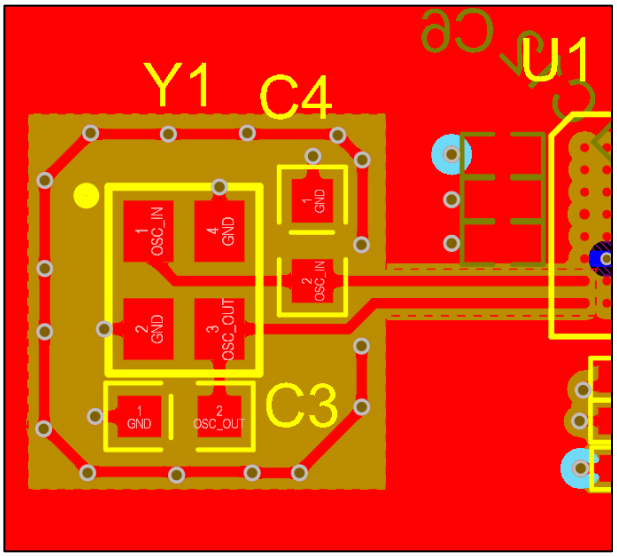
Figure 3-2. Region design reference



3.2. Clock circuit

The clock of GD32F5HC series includes HXTAL and LXTAL. The clock circuit (including the crystal or crystal oscillator and capacitors) shall be installed close to the clock pins of MCU, and the clock wiring shall be wrapped by GND as much as possible.

Figure 3-3. Recommended clock pin layout design (passive crystal)



Note:

1. The crystal shall be installed as close as possible to the clock pins of MCU, and the

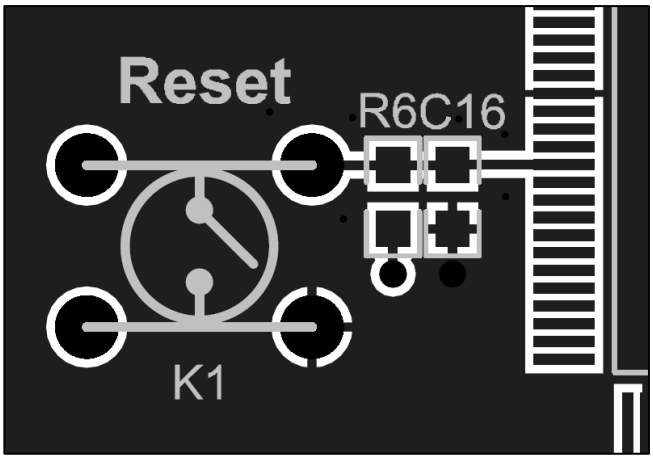
matching capacitors shall be installed as close as possible to the crystal.

2. The whole circuit should be arranged on the same layer as MCU as much as possible, and the wiring should not pass through the layer as much as possible.
3. Clock devices and adjacent layers below the wiring area shall be kept empty whenever possible and free of any clock-irrelevant wiring and copper laying.
4. Components with high power and strong interference risks and high-speed wiring should be kept away from the clock crystal circuit as much as possible;
5. The clock wire shall be wrapped by GND to achieve a shielding effect.

3.3. Reset circuit

The reference PCB layout for NRST pin wiring is as follows:

Figure 3-4. Recommended Layout design for NRST pin wiring



Note: The resistors and capacitors of the reset circuit should be installed as close as possible to the NRST pins of MCU, and the NRST wiring should be kept away from components with strong interference risks and high-speed wiring as much as possible. If conditions permit, it is better to wrap the NRST wiring by GND to achieve a better shielding effect.

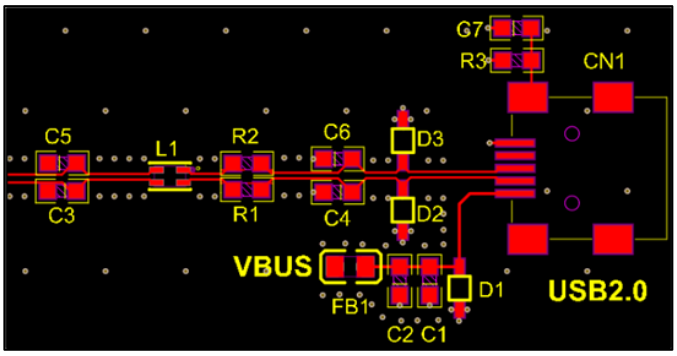
3.4. USB circuit

For GD32F5HC series MCU, the USBFS module has two differential signal lines (namely DM and DP). After the USBHS module is connected to the external high-speed PHY, two differential signal lines (namely DM and DP) will also be led out in the PHY chip. It is recommended to apply 90 Ω characteristic impedance to the PCB layout and wire the differential signal lines to a minimum length whenever possible in strict accordance with the equal length and distance rule. If the two lines are unequal in length, the shorter line can be compensated for with a snake-shaped line at the end.

The reference wiring of the differential signal lines (DM and DP) is as follows:

Figure 3-5. Recommended layout design for wiring of differential signal lines (DM and

DP)



Recommendation: R2 = R1 = 0 Ω, R3= 1 MΩ, C7 = 4700 pF.

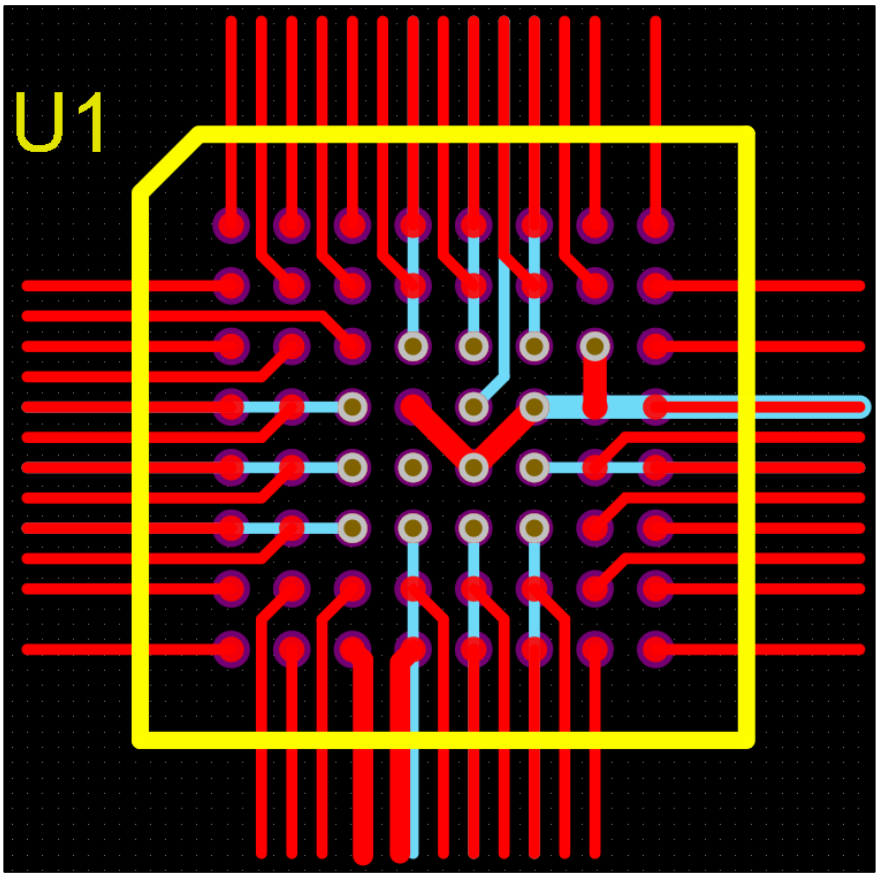
Note:

1. Provide a proper layout to shorten the wiring distance of the differential signal lines.
2. Draw two differential signal lines first, on which there shall be up to two pairs of vias in symmetrical layout. It is generally not recommended to change layers for differential signals; however, if layer transition is necessary, it is advised to place two GND vias close to the USB via transition location.
3. Wire two lines in symmetrical and parallel manner for close coupling. Avoid arced, 45° or 90° wiring.
4. Symmetrically arrange the resistance-capacitance and EMC devices connected to the differential signal lines or test points thereon.
5. When high EMC performance is required, common mode chokes and TVS diodes can be used to suppress common mode interference and prevent electrostatic discharge from affecting USB communication quality.

3.5. Fan-out of BGA package

Some models of GD32F5HC series MCU have BGA64 (0.4 mm Pitch) package, for which the following wiring rules and fan-out modes are recommended.

Figure 3-6. Fan-out mode of BGA176 package



For BGA packages with a 0.4 mm pitch, it is recommended to set the design rules to 4 mil for trace width and spacing. The recommended trace width is 5-8 mil for power pins and 4 mil for I/O pins. Fan-out should be performed using the via-in-pad method. The fan-out routing is shown in ***Figure 3-6. Fan-out mode of BGA176 package***.

4. Steel mesh and soldering

4.1. Steel mesh

When SMT is applied, the thickness and opening size of the leak of the steel mesh depend on the type of solder paste and the distribution, density, and spacing of pad openings. Overlarge opening of the leak of the steel mesh often leads to distribution of too much solder paste, which is prone to "bridging" during soldering. Too small opening of the leak will lead to application of little solder paste and thus cause insufficient strength of the solder joint or "cold solder".

4.1.1. Recommended thickness of steel mesh

The thickness and opening size of the steel mesh generally follow these rules: The width-to-thickness ratio shall be higher than 1.5 (that is, the opening width of the steel mesh shall be 1.5 times the thickness of the steel mesh or above), and the area ratio shall be higher than 0.66 (that is, the opening area of the steel mesh shall be 0.66 times the lateral area of the opening column or above), which can ensure to the greatest extent that there is proper amount of solder paste on the pad when brushing.

The recommended thickness of the steel mesh of GD32F5HC series new products are listed in ***Table 4-1. Recommended thickness of steel mesh of GD32F5HC series chip***.

Table 4-1. Recommended thickness of steel mesh of GD32F5HC series chip

Chip package	Thickness (mm)
BGA64 (4x4, 0.4pitch)	0.12
QFN56(7x7, 0.4pitch)	0.12
QFN56(7x7, 0.4pitch)	0.12

In practice, the above table can only be for reference for the thickness of the steel mesh of GD32F5HC series products. The thickness of the steel mesh of PCB shall be evaluated in combination with the density of PCB devices, pitch value of other chip pins, pad dimensions, and process requirements.

4.1.2. Cleaning and use of steel mesh

Cleaning

- The steel mesh shall be cleaned before use to remove contaminants contacted during transportation or long-term storage.
- The steel mesh shall be cleaned in time after use and packed in a special storage position.
- The steel mesh to be cleaned shall not be placed randomly to prevent it from being damaged or bringing other contaminants.
- The steel mesh shall be placed vertically in a special storage position and isolated from

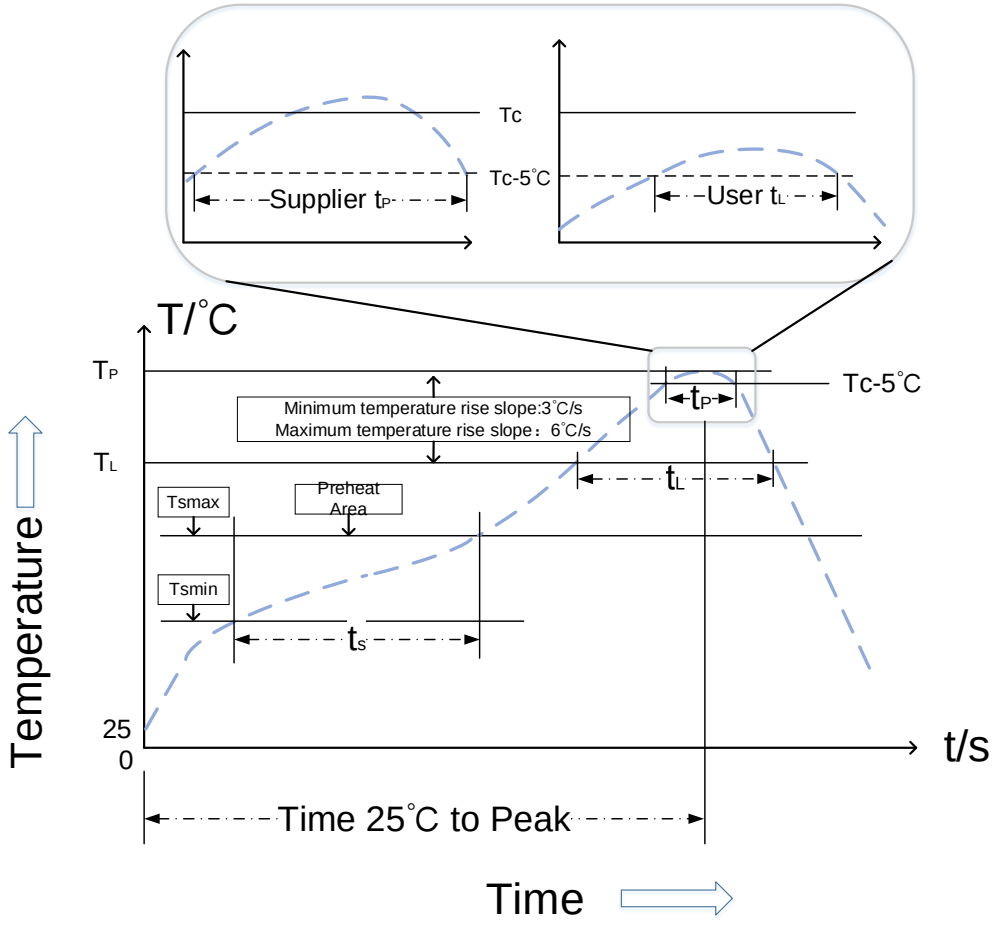
each other.

Use

- Solder paste for soldering shall be applied after being heated and stirred evenly to prevent the steel mesh from being blocked.
- The steel mesh shall be gently moved to prevent bumping against hard objects or sharp devices.
- When brushing, the steel mesh shall be kept close to PCB, and attention shall be paid to the adjustment of the pressure on the scraper until there is no residual solder paste on the intact steel mesh.
- The steel mesh shall be lifted for demolding at a proper speed about 3 s after brushing.
- When reaching the service life limit, generally 100,000 times, the steel mesh shall be scrapped.

4.2. Soldering

Figure 4-1. Recommended reflow soldering temperature curve



During actual processing and production, the reflow soldering temperature curve shall be set with reference to many factors, including component characteristics, PCB material, component distribution density, and solder paste composition. The above soldering

temperature curve for GD32F5HC series chips is introduced below for reference.

Table 4-2. Reflow soldering parameters

Characteristic parameter	Lead-free assembly
Average temperature rise slope from 217 °C to peak temperature	Maximum 3 °C / s
Preheating duration (150 °C to 200 °C)	60 s to 120 s
Duration for keeping the temperature above 217 °C	60 s to 150 s
Peak temperature	260 + 5 / - 0 °C
Duration for true peak temperature of below 5 °C	30 s
Temperature drop slope	Maximum 6 °C / s
Duration for temperature rising from 25 °C to peak temperature	Maximum 8 min

5. Package description

GD32F5HC series has a total of two package types, namely BGA64 and QFN56.

Table 5-1. Package Description

Ordering code	Package
GD32F5HCRIL6	BGA64 (4x4, 0.4pitch)
GD32F5HCPIQ6	QFN56(7x7, 0.4pitch)
GD32F5HCPIQ7	QFN56(7x7, 0.4pitch)

(Original dimensions are in millimeters)

6. Revision history

Table 6-1. Revision history

Revision No.	Description	Date
1.0	Initial release	Apr. 09, 2026

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