

**GigaDevice Semiconductor Inc.**

**GD32 MCU Device Assembly Guide**

**Application Notes**

**AN283**

Revision 1.0

(Nov. 2025)

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## 1. Introduction

This document is specifically designed for engineers developing GD32 MCUs. It introduces the packaging types of GD32 MCUs and the concept of Moisture Sensitivity Level (MSL), while providing guidance on PCB pad design and device soldering.

The parameters provided in this document are suggested values and should be evaluated in conjunction with the device datasheet and the PCB assembly manufacturer's assessment.

## 2. Introduction to the Packaging Types of GD32 MCU

The existing packaging types of GD32 MCU products are shown in [Table 2-1. GD32 MCU Packaging Types](#).

**Table 2-1. GD32 MCU Packaging Types**

Package Type	Number of Pins
TSSOP	20, 24
LGA	20
QFP	32, 48, 64, 80, 100, 128, 144, 176
QFN	24, 28, 32, 36, 40, 48, 56, 64
BGA	64, 100, 176, 240, 257
CSP	25, 49, 81

From the table above, it can be seen that the current GD32 MCU products all use SMD (Surface Mounted Devices) packaging. Compared to THD (Through-hole Devices) packaging, SMD packaging has the following advantages:

- Small size, lightweight, and more pins, which facilitate high-density integration and product miniaturization
- Suitable for automated production, offering high efficiency and stable quality
- Low parasitic parameters and excellent high-frequency characteristics
- Can be installed without drilling holes on the PCB

Of course, SMD packaging also has some disadvantages, such as:

- Lower mechanical strength of soldering compared to THT packaging
- Higher requirements for soldering processes

### 3. PCB Footprint Design

#### 3.1. Introduction to Land Pad Types

For surface-mount devices, there are two types of land pads:

- SMD (Solder mask-defined): The solder mask opening is smaller than the metal pad
- NSMD (Non-solder mask-defined): The solder mask opening is larger than the metal pad

Due to the stability and precision of the copper etching process, NSMD pads are manufactured with greater dimensional accuracy. NSMD pads have a larger solder adhesion area, which can improve the reliability of solder joints. Compared to SMD pads, NSMD pads have larger spacing between them, making routing easier and allowing for wider trace widths. However, NSMD pads are more prone to pad detachment or lead neck breakage due to mechanical stress compared to SMD pads. It is recommended to use NSMD-type pads, but under certain conditions, SMD pads may be required to achieve better mechanical stress resistance. The schematic diagrams of SMD and NSMD pads are shown in [Figure 3-1. Schematic Diagrams of SMD and NSMD Pads](#).

Figure 3-1. Schematic Diagrams of SMD and NSMD Pads



#### 3.2. Land Pad Design Recommendations for Different Package Types

##### 3.2.1. Land Pad Design Recommendations for TSSOP/QFP Packages

The pad design recommendations for TSSOP and QFP packages are shown in [Figure 3-2. Land Pad Design Recommendations for TSSOP/QFP Packages](#)

. The pads should extend 0.25-0.45 mm towards the center of the device and 0.15-0.55 mm outward. The recommended pad width is detailed in [Table 3-1. Recommended Pad Width for TSSOP/QFP Packages Based on Pin Pitch](#).

Figure 3-2. Land Pad Design Recommendations for TSSOP/QFP Packages

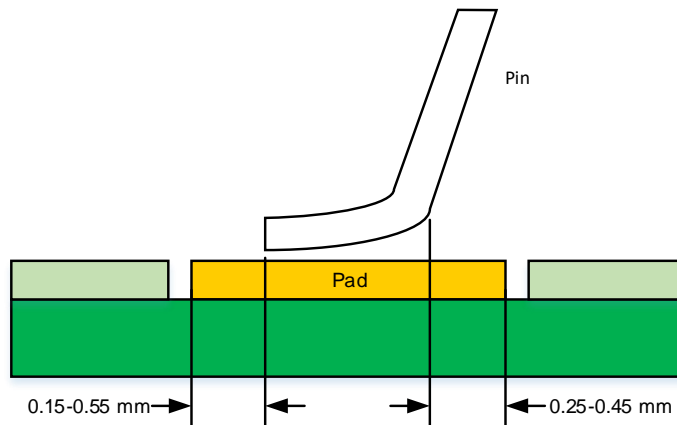


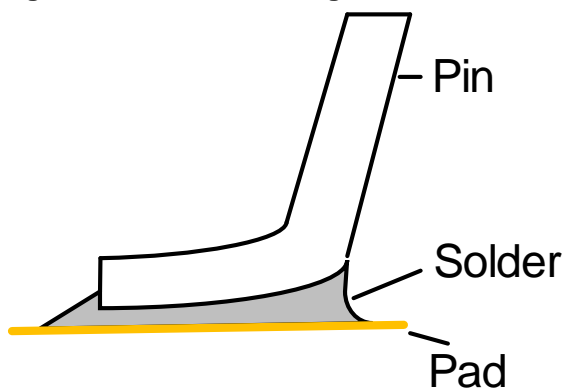
Table 3-1. Recommended Pad Width for TSSOP/QFP Packages Based on Pin Pitch

Pin Pitch (mm)	Recommended Pad Width (mm)
0.40	0.26
0.50	0.30
0.65	0.38
0.80	0.50

- If the PCB space is sufficient, it is recommended that the pads extend 0.45mm inward and 0.55mm outward on the TSSOP/QFP pins
- Ensure that the PCB pad does not extend beneath the package body

The illustration of well-soldered TSSOP/QFP pin solder joints is shown in [Figure 3-3. Schematic Diagrams of Well-Soldered TSSOP/QFP Pin Solder Joints](#).

Figure 3-3. Schematic Diagrams of Well-Soldered TSSOP/QFP Pin Solder Joints



### 3.2.2. Land Pad Design Recommendations for QFN Packages

The pad design recommendations for QFN packages are shown in [Figure 3-4. Land Pad Design Recommendations for QFN Packages](#). As illustrated, the pad should extend 0.00-0.05 mm towards the center of the device and 0.20-0.40 mm outward. The recommended pad width is provided in [Table 3-2. Recommended Pad Width for QFN Packages Based on Pin Pitch](#).

Figure 3-4. Land Pad Design Recommendations for QFN Packages

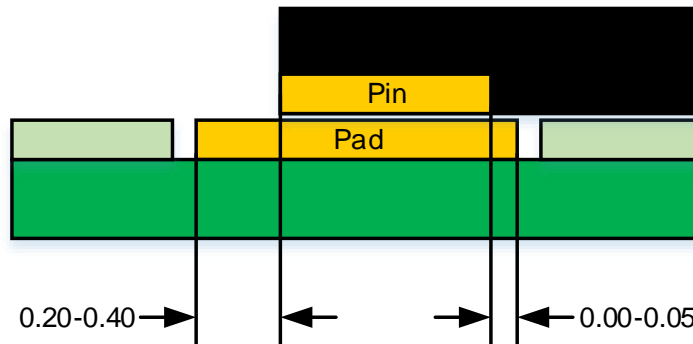


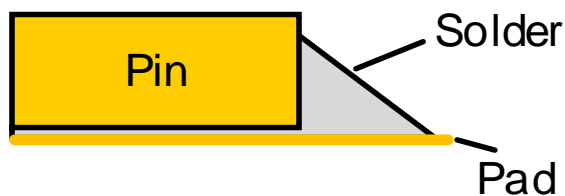
Table 3-2. Recommended Pad Width for QFN Packages Based on Pin Pitch

Pin Pitch (mm)	Recommended pad width (mm)
0.35	0.18
0.40	0.20
0.50	0.25
0.65	0.37
0.80	0.40

To prevent the risk of short circuits, ensure that the inward extension of the pad maintains a certain gap between the pad and the chip's EPAD as well as the pad beneath the EPAD. It is generally recommended that this gap be greater than or equal to 0.25 mm

A schematic diagram of well-soldered QFN pin solder joints is shown in [Figure 3-5. Schematic Diagrams of Well-Soldered QFN Pin Solder Joints](#).

Figure 3-5. Schematic Diagrams of Well-Soldered QFN Pin Solder Joints



### 3.2.3. Land Pad Design Recommendations for LGA Packages

Currently, the GD32 MCU only offers the LGA20 package for LGA packaging. The LGA20 package is similar to the QFN package, and the pad design can refer to the recommendations in section [3.2.2 Land Pad Design Recommendations for QFN Packages](#).

### 3.2.4. Land Pad Design Recommendations for LGA Packages

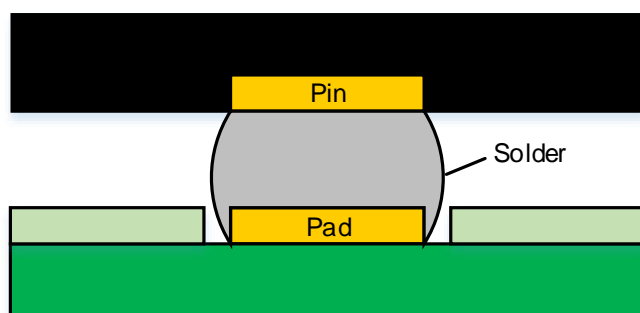
The pad design recommendations for BGA packages are shown in [Table 3-3. Recommended Pad Width for BGA Packages Based on Pin Pitch](#).

**Table 3-3. Recommended Pad Width for BGA Packages Based on Pin Pitch**

Pin Pitch (mm)	Recommended pad diameter (mm)
0.35	0.20
0.40	0.22
0.50	0.25
0.65	0.30
0.80	0.37

The diameter of the solder mask is related to the pin pitch. For GD32 MCU BGA packages with smaller pin pitch, it is recommended that the solder mask opening diameter be 0.1 mm larger than the pad diameter.

A schematic diagram of well-soldered BGA pin solder joints is shown in [Figure 3-6. Schematic Diagrams of Well-Soldered BGA Pin Solder Joints.](#)

**Figure 3-6. Schematic Diagrams of Well-Soldered BGA Pin Solder Joints**

### 3.2.5. Land Pads and Thermal Vias Design Recommendations for QFN/QFP

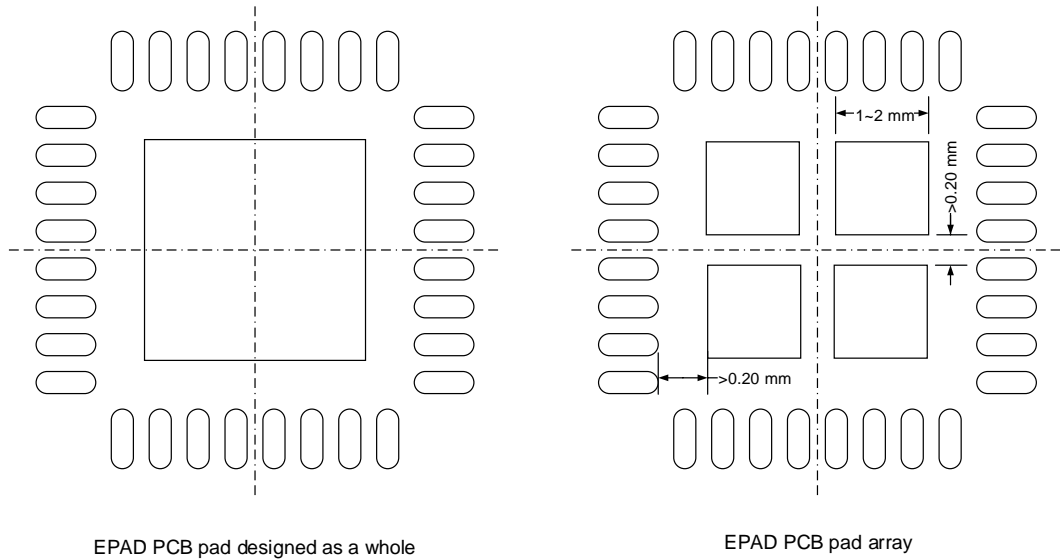
#### EPAD

Most QFN packages feature an EPAD at the bottom to enhance the thermal and electrical performance of the package. Some QFP packages also include an EPAD, primarily to improve thermal performance. To further optimize the heat dissipation performance of the package, it is recommended to add thermal vias to the EPAD and incorporate a complete thermal plane in the PCB.

The size of the PCB pad can be larger or smaller compared to the EPAD, but to maximize the thermal and electrical performance of the product, it is recommended that the PCB pad size closely matches the EPAD size. To prevent bridging and short circuits during soldering, the distance between the EPAD PCB pad and other pads or pins should be greater than 0.2mm. The PCB pad for the EPAD can be designed as a single block similar in size and shape to the EPAD, or it can be divided into a symmetrical array of square or rectangular pads, as shown in [Figure 3-7. EPAD PCB Land Pad Design.](#)

For the pad array, the recommended length/width of the rectangles is 1 to 2mm, and the distance between rectangles should be greater than 0.2mm. If space permits, a gap of 0.4mm can be chosen.

Figure 3-7. EPAD PCB Land Pad Design

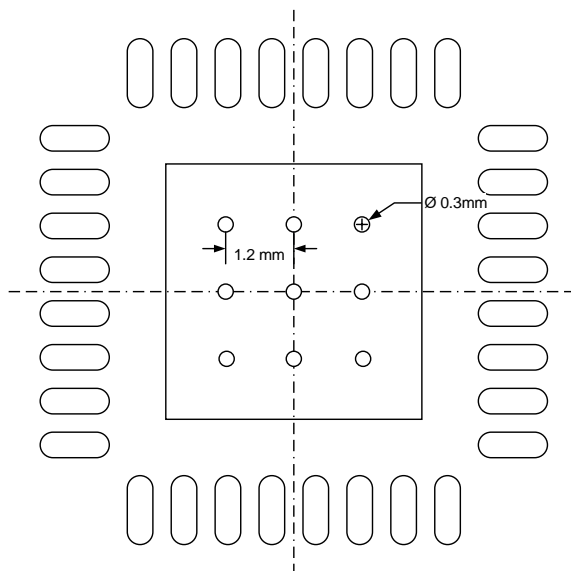


To achieve better thermal and electrical performance for the chip, it is recommended to evenly distribute thermal vias on the EPAD PCB pad as follows:

- It is recommended to set the thermal via spacing to 1.2mm
- It is recommended to select a thermal via diameter of 0.3mm with 1oz copper plating inside. To prevent solder from flowing into the vias, it is suggested to use via plugging

The recommended thermal via design is shown in [Figure 3-8. Thermal Via Design in EPAD PCB Land Pad](#).

Figure 3-8. Thermal Via Design in EPAD PCB Land Pad



## 4. Introduction to Moisture Sensitivity Level (MSL)

Moisture Sensitivity Level (MSL) indicates the floor life, storage environment, and storage precautions after the device packaging is opened. MSL is a classification standard used to evaluate the sensitivity of components to moisture. The higher the level number, the more sensitive the component is to moisture. The floor life for different MSL levels is shown in [Table 4-1. Floor Life for Different Moisture Sensitivity Levels \(MSL\)](#).

**Table 4-1. Floor Life for Different Moisture Sensitivity Levels (MSL)**

MSL	Floor life	Condition
1	Unlimited	30 °C / 85% RH
2	1 year	30 °C / 60% RH
2a	4 weeks	
3	168 hours	
4	72 hours	
5	48 hours	
5a	24 hours	
6	Must be baked before use and reflow soldered within the time specified on the label	

The component packaging includes a desiccant and a humidity indicator card. After opening the packaging bag, the storage condition of the components should be checked immediately.

During high-temperature reflow soldering, the moisture inside the components expands due to the increased temperature, which may lead to interface separation between the encapsulation plastic and the chip or substrate, bond wire damage, chip damage, and internal cracks. In severe cases, the components may even explode due to expansion, a phenomenon known as the "popcorn effect." Therefore, components that exceed their floor life must be baked before use. The baking procedure can refer to IPC/JEDEC J-STD-033C. During baking, attention should be paid to the temperature tolerance of plastic housings (trays, reels, or tubes). Note that plastic reels cannot withstand high-temperature baking.

The packaging surface of GD32 MCU components is marked with the moisture sensitivity level and the peak reflow soldering temperature, as shown in [Figure 4-1. Moisture Sensitivity Level \(MSL\) and Reflow Peak Temperature Marking on Device Packaging](#).

**Figure 4-1. Moisture Sensitivity Level (MSL) and Reflow Peak Temperature Marking**

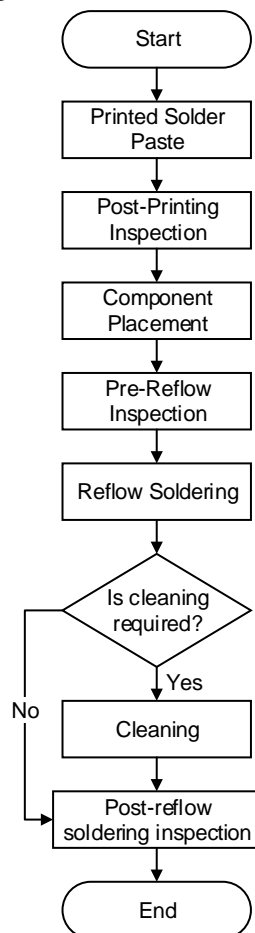
on Device Packaging

	<b>Caution</b> This bag contains <b>MOISTURE-SENSITIVE DEVICES</b>	LEVEL <div style="border: 1px solid black; padding: 5px; display: inline-block;"> <b>3</b> </div> <small>If blank, see adjacent bar code label</small>
<ol style="list-style-type: none"> <li>1. Calculated shelf life in sealed bag: 12 months at &lt;40°C and &lt;90% relative humidity (RH)</li> <li>2. Peak package body temperature: <u>260</u> °C <small>If blank, see adjacent bar code label</small></li> <li>3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be             <ol style="list-style-type: none"> <li>a) Mounted within: <u>168</u> hours of factory conditions <small>If blank, see adjacent bar code label</small> ≤30°C/60% RH. or</li> <li>b) Stored per J-STD-033</li> </ol> </li> <li>4. Devices require bake. before mounting, if:             <ol style="list-style-type: none"> <li>a) Humidity Indicator Card reads &gt;10% for level 2a - 5a devices or &gt;60% for level 2 devices when read at 23 ± 5°C</li> <li>b) 3a or 3b are not met</li> </ol> </li> <li>5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure</li> </ol>		
Bag Seal Date: _____ <small>If blank, see adjacent bar code label</small>		
<small>Note: Level and body temperature defined by IPC/JEDEC J-STD-020</small>		

## 5. Assembly Process and Inspection

Common assembly processes include wave soldering and reflow soldering. Wave soldering is mainly used for soldering through-hole components or packages with larger pin pitches. GD32 MCU products are recommended to be soldered using reflow soldering and are not recommended for wave soldering. Below is an introduction to the reflow soldering process. The reflow soldering process is shown in [Figure 5-1. Reflow Soldering Process](#).

**Figure 5-1. Reflow Soldering Process**



### 5.1. Solder Paste Printing

#### 5.1.1. Introduction and Selection of Solder Paste

Solder paste is one of the most important materials in the SMT process. It mainly consists of alloy solder and flux, with alloy solder accounting for 80% to 95% of the total solder paste. The content of alloy solder determines the thickness of the solder after welding, as well as the viscosity and printability of the solder paste. The composition of flux is relatively complex, including binders, thixotropic agents, activators, etc., which are used to remove oxides from

the surface of pins and pads, prevent oxidation during the welding process, and improve wettability.

Solder paste can be divided into leaded and lead-free types based on lead content. In early soldering processes, leaded solder paste was primarily used, with tin and lead as its main components. In recent years, due to environmental considerations, lead-free solder paste has been increasingly adopted, with lead content less than 1000 ppm (<0.1%).

Alloy solder can be classified into several grades based on the particle diameter, as shown in [Table 5-1. The Relationship Between Alloy Solder Powder Particle Size Grades and Particle Diameter](#). For packages with smaller pin pads, the stencil openings are also smaller, requiring solder paste with higher alloy solder particle size grades. Based on experience, for square stencil openings, the minimum stencil opening size must be greater than or equal to 5 times the particle diameter; for circular stencil openings, the minimum stencil opening size must be greater than or equal to 8 times the particle diameter.

**Table 5-1. The Relationship Between Alloy Solder Powder Particle Size Grades and Particle Diameter**

Alloy Solder Powder Particle Size Grade	Particle Diameter (μm)
1	75~150
2	45~75
3	25~45
4	20~38
5	15~25
6	5~15
7	2~11

Flux can be classified into four types based on its main composition: Rosin-based (RO), Resin-based (RE), Organic Acid-based (OR), and Inorganic-based (IN). Rosin-based flux can be further divided into three types based on activity level: R type, RMA type, and RA type. R type is non-active flux with no corrosiveness; RMA type is moderately active flux with low corrosiveness and better soldering performance compared to R type; RA type is highly active flux with better soldering performance than R type and RMA type but has stronger corrosiveness.

Solder paste can be divided into two types based on flux composition: cleaning type and no-clean type. Cleaning type solder paste requires cleaning with solvents or other solutions after soldering; otherwise, it may cause short circuits or corrosion of the circuit board. No-clean type solder paste does not require cleaning after soldering, and it is recommended to use no-clean type solder paste.

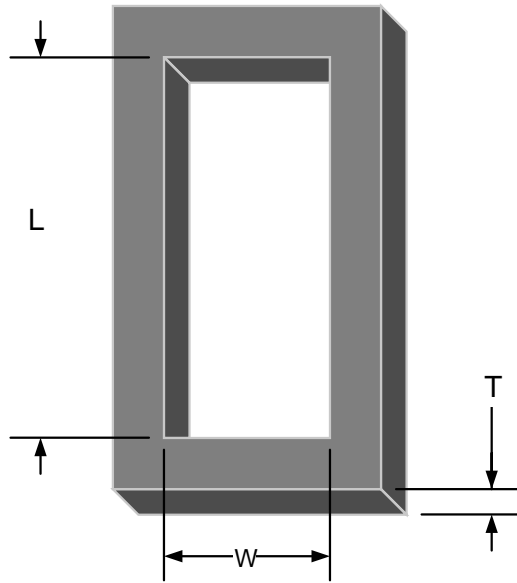
### 5.1.2. Introduction and Selection of Stencil

In the SMT process, stencils are typically used to print solder paste onto the pads. The stencil's pad opening size is usually close to or slightly smaller than the pad size. The

thickness of the stencil and the size of the openings determine the amount of solder paste applied to the pads. The amount of solder paste is crucial for the reliability of solder joints; therefore, it is necessary to select the appropriate stencil thickness and opening size based on different package types.

The schematic diagram of stencil pad openings is shown in [Figure 5-2. Stencil Opening Diagram](#).

**Figure 5-2. Stencil Opening Diagram**



To ensure better release of solder paste from the pads, attention must be paid to the aspect ratio and area ratio of the stencil pad openings. The calculation formulas for aspect ratio and area ratio are shown in equations [\(5-1\)](#) and [\(5-2\)](#).

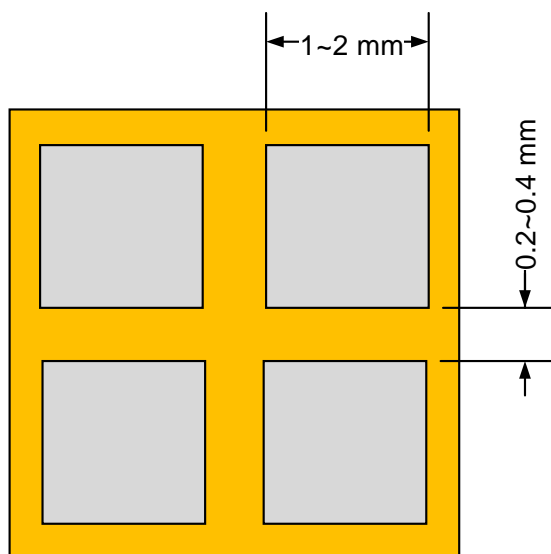
$$\text{Aspect Ratio} = \frac{W}{T} \quad (5-1)$$

$$\text{Area Ratio} = \frac{L \times W}{2 \times (L + W) \times T} \quad (5-2)$$

When the length of the connection pad is significantly greater than its width, the aspect ratio ( $W/T$ ) serves as a one-dimensional simplified form of the area ratio ( $W/2T$ ). The general design principle is that the aspect ratio should be greater than 1.5, and the area ratio should be greater than 0.66. Adding rounded corners to the stencil openings can improve stencil cleanliness.

Typically, the stencil opening size is either identical to or slightly smaller than the pin pad size. To reduce the gap between the chip EPAD and the pad, as well as to facilitate gas discharge during the soldering process, the stencil opening for EPAD pads is usually set to 60% of the pad size. For EPAD pads larger than 2×2 mm, it is recommended to use a rectangular array-style stencil opening, as illustrated in [Figure 5-3. EPAD Stencil opening Example](#).

Figure 5-3. EPAD Stencil opening Example



## 5.2. Component Placement

The accuracy of component placement determines the reliability of soldering. The smaller the pin pitch of the component, the higher the requirement for placement accuracy. Therefore, it is recommended to use equipment equipped with a vision recognition system. The component placement accuracy should reach  $\pm 0.1\text{mm}$ , and for component with a pin pitch of less than  $0.4\text{mm}$ , the placement accuracy should reach  $\pm 0.05\text{mm}$ . Slight misalignment of the component is acceptable, as mildly misaligned component will self-align during reflow soldering.

## 5.3. Introduction to Reflow Soldering and Precautions

During the reflow soldering production process, the soldering temperature profile is a critical variable that significantly impacts the product yield rate. The selection of the temperature profile should follow the recommendations of the solder paste manufacturer. It is recommended to use nitrogen during the reflow soldering process, as nitrogen can reduce the oxidation of PCB pads and pins while improving the wettability of the solder.

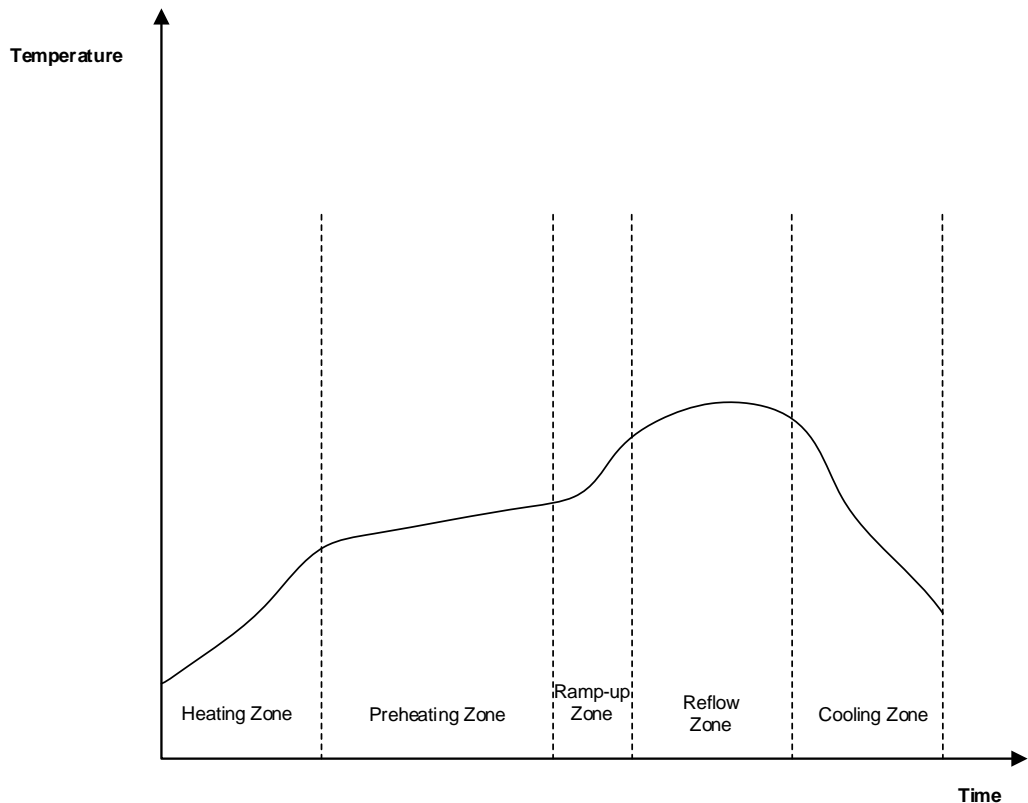
A typical reflow soldering temperature profile is shown in [Figure 5-4. Typical Reflow Soldering Temperature Profile](#) is divided into five zones:

- Preheat Zone: At this stage, the PCB and components should be evenly heated, and the volatile solvents in the solder paste begin to evaporate during the heating process. The maximum heating rate is generally no more than  $3^{\circ}\text{C}/\text{second}$  to avoid excessive stress on the package
- Soak Zone: Typically, the temperature in this zone ranges from  $150^{\circ}\text{C}$  to  $200^{\circ}\text{C}$ , and the PCB assembly remains in this zone for 60 to 120 seconds. During this interval, volatile

substances in the solder paste are further removed, and the flux begins to assist in removing oxides from the pads and pins. Additionally, sufficient time is provided to ensure the PCB assembly reaches a uniform temperature

- **Ramp-Up Zone:** In this zone, the temperature of the PCB assembly gradually rises to the melting point of the solder paste alloy. The heating rate should not exceed 3°C/second to avoid excessive stress on the package
- **Reflow Zone:** In this zone, the temperature of the PCB assembly exceeds the melting point of the solder paste alloy. The assembly should remain in this zone long enough to allow the liquid solder to uniformly wet the pads and pins. However, the duration should not be too long, as it may lead to brittle solder joints and damage to the PCB assembly
- **Cooling Zone:** The faster the cooling rate of the PCB assembly, the smaller the grain size of the solder paste crystals, resulting in stronger structural reliability. However, the cooling rate should generally not exceed 6°C/second to avoid excessive stress on the package

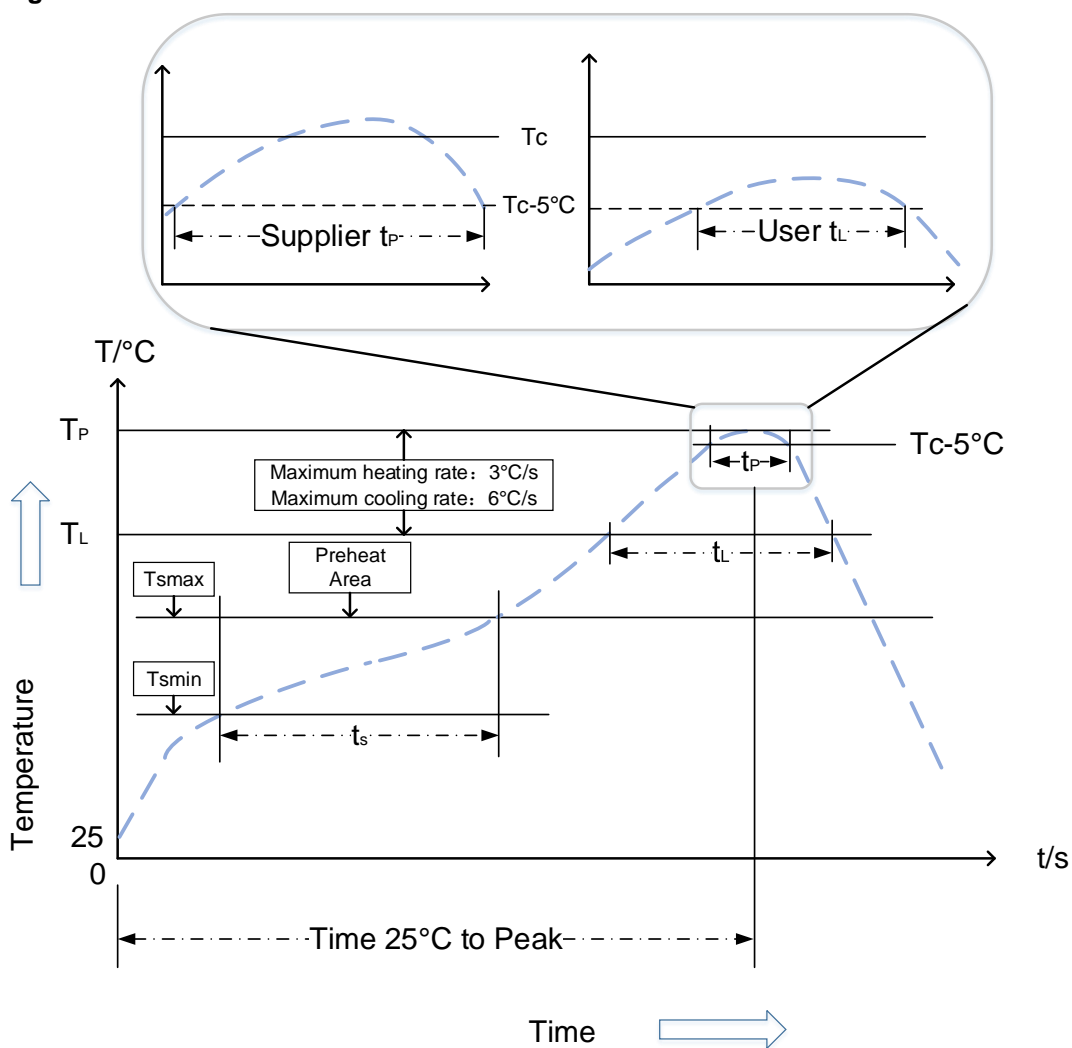
**Figure 5-4. Typical Reflow Soldering Temperature Profile**



According to the IPC/JEDEC J-STD-020 standard, the peak reflow temperature of surface-mount devices depends on the package thickness and volume. The relationship between the peak reflow temperature of lead-free process devices and package thickness and volume is shown in [Table 5-2. The relationship between the peak reflow temperature of lead-free process devices and the package thickness and volume](#). For GD32 MCU products, the peak reflow temperature can be found on the reflow peak temperature label attached to the package surface.

Package Thickness (mm)	Package Volume (mm3) <350	Package Volume (mm3) 350-2000	Package Volume (mm3) >2000
< 1.6mm	260°C	260°C	260°C
1.6mm ~ 2.5mm	260°C	250°C	245°C
> 2.5mm	250°C	245°C	245°C

**Figure 5-5. J-STD-020 Classification Reflow Profile**



**Table 5-3. Description of Classification Reflow Profile Parameters**

Characteristic Parameters	Lead-Free Assembly
Preheat stage	
Minimum Temperature ( $T_{smin}$ )	150 °C
Maximum Temperature ( $T_{smax}$ )	200 °C
Time ( $t_s$ ) from $T_{smin}$ to $T_{smax}$	60 ~ 120 s
Ramp-Up Rate ( $T_L$ to $T_P$ )	Up to 3 °C / s
Liquidus Temperature ( $T_L$ )	217 °C
Time above $T_L$ ( $t_L$ )	60 ~ 150 s
Peak temperature	Must not exceed the peak temperature specified on the chip package
Duration within 5 °C of Peak Temperature	Up to 30 s
Ramp-Down Rate ( $T_P$ to $T_L$ )	Up to 6 °C / s
Time from 25 °C to Peak Temperature	Up to 8 min

During the actual soldering process, the heating and cooling rates may vary due to the different thermal capacities of various parts of the PCB assembly. Therefore, it is recommended to use thermocouples to monitor the temperature at different locations of the PCB assembly during reflow soldering. Additionally, it is advised to install a thermocouple at the center of the bottom of the chip package to ensure that the peak temperature does not exceed the peak temperature specified on the chip package.

## 5.4. PCB Cleaning

After reflow soldering is completed, it is usually necessary to decide whether cleaning is required based on the type of flux used and the requirements of PCB components. For packages such as BGA and QFN, which have relatively small gaps between components and the PCB, cleaning is often more challenging. Therefore, it is recommended to use no-clean flux for soldering. However, the activity of no-clean flux is generally lower than that of other types of flux, so it may be necessary to use nitrogen purging or other methods to achieve optimal soldering results.

## 5.5. Inspection

The post-soldering inspection process is also a very important step, as it can identify risks in advance and prevent issues during later debugging. The main soldering inspection methods include visual inspection, optical inspection, and X-ray inspection. As components on circuit boards become increasingly miniaturized and densely packed, visual inspection is becoming progressively more challenging.

For chips with pins located on the exterior of the package, common soldering defects include solder balls, cold solder joints, and short circuits. These defects can usually be detected through visual and optical inspection. However, for packages with pins located underneath the chip, such as QFN and BGA, common soldering defects include cold solder joints and short circuits, which cannot be detected through visual or optical inspection. For these types of packages, X-ray inspection is recommended.

## 5.6. Common Causes of Soldering Short Circuits and Open Circuits

Common causes of soldering short circuits include:

- Excessive misalignment or excessive application of solder paste during printing
- Deformation of component pins
- Misalignment during package placement
- Mismatch in PCB pad design
- Incompatibility of the reflow soldering temperature profile

Common causes of soldering open circuits include:

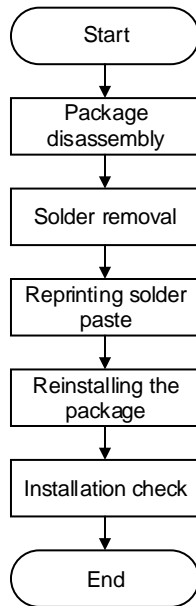
- Insufficient or missing solder paste printed on the pads
- Insufficient wettability and activity of the solder paste
- Incompatibility of the reflow soldering temperature profile
- PCB warping during the soldering process
- Oxidation of component pins or PCB pads

## 6. Rework

For components with soldering issues or other defects, you can refer to the content of this section for rework processing. For chips removed during rework, it is not recommended to reuse them. Our company does not guarantee their quality; therefore, unless it is necessary to locate and reproduce the issue, please avoid reusing the chips.

The common rework process is illustrated in [Figure 6-1. Rework process flow diagram](#).

**Figure 6-1. Rework process flow diagram**



During the rework process, the following points should be noted:

- It is recommended to bake the PCB assembly before rework to reduce the risk of damage to the components and PCB
- Minimize the thermal impact on nearby electronic components during the removal and soldering process
- Ensure that the maximum temperature limits of the PCB and components are not exceeded during the rework process

## 7. Revision history

Table 7-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Nov. 7, 2025

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