GigaDevice Semiconductor Inc.

Device limitations of GD32F5HC

Errata Sheet

Revision 1.0

(Apr. 2026)

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1. Introduction

This document applies to GD32F5HC product series, as shown in ***Table 1-1. Applicable products***. It offers technical guidance for using GD32 MCU and provides workaround to current device limitations.

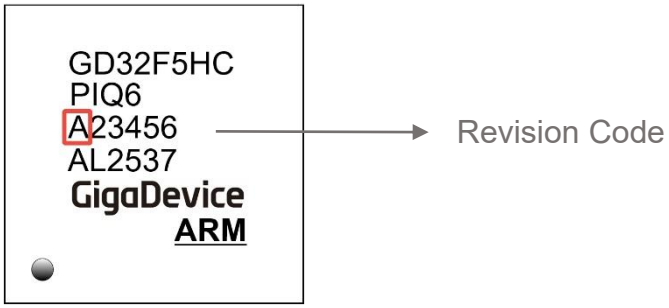
Table 1-1. Applicable products

Type	Part Numbers
MCU	GD32F5HCxx series

1.1. Revision identification

The device revision can be identified according to the mark on the top of the package. The 1st code on Line 3 of the mark is the product revision code, as shown in ***Figure 1-1. Device revision code of GD32F5HC***.

Figure 1-1. Device revision code of GD32F5HC



1.2. Summary of device limitations

The device limitations of GD32F5HC are shown in ***Table 1-2. Device limitations***, please refer to Section 2 for more details.

Table 1-2. Device limitations

Module	Limitations	Workaround
		Rev. Code A
USART	*The high baud rate of USART will cause data loss when using hardware flow control mode*	Y
	In Smartcard mode, RTF is set prematurely when the receive timeout threshold (RT) is configured as 0	Y
	In Smartcard mode during data reception, a parity error detected during TX transmission is considered a retransmission, and FERR and RBNE cannot be set	N
	In Smartcard mode during data reception, EBF flag may fail to be set	N

Module	Limitations	Workaround
		Rev. Code A
	during retransmission	
	When automatic baud rate detection mode 1 and the data bit inversion function are enabled simultaneously, the reception of the data for auto baud rate detection fails	Y
	When an auto baud rate detection error occurs, the USART_BAUD register is updated with an incorrect baud rate value	Y
	When the TX FIFO function is disabled, the TFE flag is cleared when writing data to TDATA	Y
	When the TX FIFO function is enabled, the TFNF flag is not cleared as expected	Y
	In deep sleep mode, the parity error caused by wakeup frames will set PERR bit	Y
	In deep sleep mode, the parity error caused by wakeup frames will set PERR bit but not EPERR	Y
	In Smartcard mode, the PERR flag is set abnormally	N
	In synchronous mode, the PERR flag is set abnormally	N
	When DENR = 1, DDRE = 0, and HCM = 1, RTS remains asserted high	N
I2C	*When I2C is operating as a master transmitter, if the slave responds with NACK to the last byte, a START condition cannot be correctly issued in the transfer complete interrupt*	Y
TIMER	*Probabilistic break false trigger occurs when BRKP and BRKEN are both set*	Y
Core	*Access permission faults are prioritized over unaligned Device memory faults*	N

Note:

Y = Limitation present, workaround available

N = Limitation present, no workaround available

'--' = Limitation fixed

2. Descriptions of device limitations

2.1. USART

2.1.1. The high baud rate of USART will cause data loss when using hardware flow control mode

Description & impact

When using hardware flow control, during high baud rate communication of the USART, data loss may occur due to CTS not being pulled low in time (flow control delay).

Workarounds

Avoid using high baud rates, or use 2 stop bits at high baud rates. When hardware flow control is enabled and 1-bit stop bits are used, the baud rate should be limited to within 1.47 MHz (APB2 = 100 MHz) and 0.74 MHz (APB1 = 50 MHz).

2.1.2. In Smartcard mode, RTF is set prematurely when the receive timeout threshold (RT) is configured as 0

Description & impact

In Smartcard mode, when the receive timeout threshold (RT) is set to 0, the receive timeout flag (RTF) is set at the START bit of the first data frame.

Workarounds

Configure the RT register with the desired receive timeout threshold value plus 11.

2.1.3. In Smartcard mode during data reception, a parity error detected during TX transmission is considered a retransmission, and FERR and RBNE cannot be set

Description & impact

In Smartcard mode during data reception, a parity error detected during TX transmission is considered a retransmission, but the TX pin does not detect a NACK signal. The read data buffer not empty flag (RBNE) and the framing error flag (FERR) cannot be set.

Workarounds

Not available.

2.1.4. In Smartcard mode during data reception, EBF flag may fail to be set during retransmission

Description & impact

In Smartcard mode reception, if the retransmitted data frame satisfies the block count value = BL + 4, and the current retransmitted data frame remains with a parity error and is not moved into the data register, the block end flag (EBF) cannot be set. Additionally, the subsequent BL counter continues counting, causing counter overflow, and EBF remains reset.

Workarounds

Not available.

2.1.5. When automatic baud rate detection mode 1 and the data bit inversion function are enabled simultaneously, the reception of the data for auto baud rate detection fails

Description & impact

When automatic baud rate detection mode 1 (ABDM = 01) and the data bit inversion function (DINV = 1) are enabled, after sending an automatic baud rate detection request (ABDCMD = 1), the data received in the next frame differs from the data on the RX line as retrieved from USART_RDATA, resulting in a reception error.

Note: The issue only affects the data of the auto baud rate detection frame.

Workarounds

If the user is concerned about the data of the automatic baud rate detection frame, one of the following solutions can be used:

1. If both the automatic baud rate detection function and data bit inversion function are required, automatic baud rate detection mode 0 (ABDM = 00) can be used instead.
2. Manually invert the most significant bit of the data in software. If parity check is enabled, the parity bit must be recalculated in software.

2.1.6. When an auto baud rate detection error occurs, the USART_BAUD register is updated with an incorrect baud rate value

Description & impact

When an auto baud rate detection error occurs, the USART_BAUD register is updated with an incorrect baud rate value.

Workarounds

When this issue occurs (ABDE = 1), reconfigure the baud rate to the default value.

2.1.7. When the TX FIFO function is disabled, the TFE flag is cleared when writing data to TDATA

Description & impact

When the TX FIFO function is disabled, the TFE (TX FIFO Empty) flag is cleared when writing data to TDATA.

Workarounds

When the TX FIFO function is disabled, ignore all TX FIFO-related status flags.

2.1.8. When the TX FIFO function is enabled, the TFNF flag is not cleared as expected

Description & impact

When the TX FIFO function is enabled, continuously writing data until the FIFO is full results in TFNF = 0. If one data word is then transmitted, TFNF becomes 1. Subsequently, writing one data word into the FIFO fills it again, but TFNF remains 1 instead of being cleared to 0 as expected.

Workarounds

When using the TX FIFO function, use the TFF or TFT flag instead of the TFNF flag as the criterion when writing data.

2.1.9. In deep sleep mode, the parity error caused by wakeup frames will set PERR bit

Description & impact

In deep sleep mode, parity errors caused by wake-up frames will set the PERR bit. For example, when using USART address-match to wake up from deep sleep mode, if a frame with a parity error and a non-matching address is received first, followed by a frame with no parity error and a matching address, the PERR and EPERR bit will be set after wakeup.

Workarounds

The software ignores the parity error flag generated in this case.

2.1.10. In deep sleep mode, the parity error caused by wakeup frames will set PERR bit but not EPERR

Description & impact

In deep sleep mode, parity errors caused by wake-up frames will set the PERR bit but not EPERR bit. For example, when using USART address-match to wake up from deep sleep mode, if a frame with a parity error and a non-matching address is received first, followed by a frame with parity error and a matching address, the PERR bit will be set after wakeup while the EPERR bit remains reset.

Workarounds

The software ignores the parity error flag generated in this case.

2.1.11. In Smartcard mode, the PERR flag is set abnormally

Description & impact

In Smartcard mode, when NACK is disabled (NKEN = 0) and SCRTNUM is configured to a non-zero value, the PERR bit fails to be set after the USART receives a frame with a parity error.

Workarounds

Not available.

2.1.12. In synchronous mode, the PERR flag is set abnormally

Description & impact

In synchronous mode, when the data bit inversion function is enabled (DINV = 1), the PERR bit will still be set even if the USART receives a frame with no parity error.

Workarounds

Not available. Do not enable the data bit inversion function in synchronous mode.

2.1.13. When DENR = 1, DDRE = 0, and HCM = 1, RTS remains asserted high

Description & impact

When DENR = 1, DDRE = 0, and HCM = 1, the RTS signal remains asserted high, causing hardware flow control to fail.

Workarounds

Ensure that the above three conditions are not all true at the same time during operation.

2.2. I2C

2.2.1. When I2C is operating as a master transmitter, if the slave responds with NACK to the last byte, a START condition cannot be correctly issued in the transfer complete interrupt

Description & impact

When I2C is operating as a master and has finished transmitting the last byte of data, if the slave responds with a NACK signal, the master cannot correctly issue a START condition within the transfer complete (TC) interrupt, meaning the next transfer cannot be initiated.

Workarounds

Send a STOP condition in the NACK interrupt handler first, then initiate the next transfer.

2.3. TIMER

2.3.1. Probabilistic break false trigger occurs when BRKP and BRKEN are both set

Description & impact

When BRKP (break input signal polarity) and BRKEN (break input signal enable) are both set, a probabilistic false triggering of the break function may occur.

Workarounds

When using the break function, configure BRKP as input active low.

2.4. Core

About Cortex-M33 limitations, please refer to “Cortex-M33 AT623 and Cortex-M33 with FPU AT624 Software Developer Errata Notice”. This document can be downloaded on ARM official website.

2.4.1. Access permission faults are prioritized over unaligned Device memory faults

This limitation refers to Arm ID number 1080541 in “Cortex-M33 AT623 and Cortex-M33 with FPU AT624 Software Developer Errata Notice”.

Description & impact

A load or store which causes an unaligned access to Device memory will result in an UNALIGNED UsageFault exception. However, if the region is not accessible because of the MPU access permissions (as specified in MPU_RBAR.AP), then the resulting MemManage fault will be prioritized over the UsageFault.

This erratum affects all configurations of the Cortex-M33 processor with the MPU enabled.

The failure occurring conditions are as follows:

The MPU is enabled and:

- A load/store access occurs to an address which is not aligned to the data type specified in the instruction.
- The memory access hits one region only.
- The region attributes (specified in the MAIR register) mark the location as Device memory.
- The region access permissions prevent the access (that is, unprivileged or write not allowed).

The implications of this limitation is that the MemManage fault caused by the access permission violation will be prioritized over the UNALIGNED UsageFault exception because of the memory attributes.

Workarounds

Not available. However, it is expected that no existing software is relying on this behavior since it was permitted in Armv7-M. (The CM33 is Armv8-M).

3. Revision history

Table 3-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Apr.10 2026

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