GigaDevice Semiconductor Inc.

Differences between GD32F5HC and GD32W515 products

Application Note
AN299

Revision 1.2

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1. Introduction

This application note introduces the characteristic differences between GD32F5HC and GD32W515 product series, mainly for electric characteristics and peripheral function characteristics, the differences are described in the following paragraphs.

Note: This application note is for reference only. In case of any conflict with the user manual or datasheet, the user manual or datasheet shall prevail.

2. Electrical characteristics differences

For details about the electrical characteristics, refer to the GD32W515xx Datasheet and GD32F5HCxx Datasheet.

3. Peripheral function differences

3.1. Flash memory controller (FMC)

The FMC difference is reflected in the configuration of option byte register 1, which refers to ***Table 3-1. Differences of FMC function***.

Table 3-1. Differences of FMC function

Part numbers	Option byte register 1 (FMC_OBR1)
GD32W515xx	Not supported
GD32F5HCxx	Supported. nBOOT1, SWBOOT1, nBOOT0, SWBOOT0, FWDGSPD_STDBY, FWDGSPD_DPSLP, and nWDG_HW are configurable

3.2. Electronic fuse (EFUSE)

The EFUSE difference is reflected in the FWDGT option configuration (HWDG bit in EFUSE_USER_CTL register), which refers to ***Table 3-2. Differences of EFUSE function***.

Table 3-2. Differences of EFUSE function

Part numbers	FWDGT option configuration (HWDG bit)
GD32W515xx	Supported
GD32F5HCxx	Not supported

3.3. Power management unit (PMU)

The PMU differences are reflected in the core voltage selection in Deep-sleep mode and the WKUP pins configuration, which refers to ***Table 3-2. Differences of EFUSE function***.

Table 3-3. Differences of PMU function

Part numbers	Core voltage selection in Deep-sleep mode	WKUP pins
GD32W515xx	Not support configuration	PA2/PA12/PA15/PB2, wakeup only on the rising edge
GD32F5HCxx	Support configuration (0.9/1.0/1.1/1.2V)	PA2 / PA12 / PA15 / PB2 / PB0 PD3 / PD4, PD5, wake up can be configured to rising or falling edge

3.4. Reset and clock unit (RCU)

The RCU differences are reflected in the system reset circuitry and clock selection, which refers to ***Table 3-4. Differences of RCU function***. Additionally, only GD32F5HCxx supports the internal 48M RC oscillators (IRC48M).

Table 3-4. Differences of RCU function

Part numbers	IRC48M	PLL	PLLI2S	PLLDIG	System clock
GD32W515xx	Not supported	HXTAL or IRC16M selectable	HXTAL	Supported	IRC16M, HXTAL, CK_PLLP or CK_PLLDIG
GD32F5HCxx	Supported	HXTAL, IRC16M, or IRC48M selectable	HXTAL, IRC16M, or IRC48M selectable	Not supported	IRC16M, IRC48M, HXTAL or CK_PLL

3.5. True random number generator (TRNG)

The DMA difference is reflected in power mode selection of TRNG, which refers to ***Table 3-5. Differences of TRNG function***.

Table 3-5. Differences of TRNG function

Part numbers	Power mode selection
GD32W515xx	Not supported
GD32F5HCxx	Supports four power modes: ultra low, low, medium, and high

3.6. Direct memory access controller (DMA)

The DMA difference is reflected in round-robin group arbitration for "ultra high" priority level (definition in RREN bit of DMA_CHxCTL register), which refers to ***Table 3-6. Differences of DMA function***.

Table 3-6. Differences of DMA function

Part numbers	Round-robin group arbitration for "ultra high" priority level channels
GD32W515xx	Not supported
GD32F5HCxx	Supported

3.7. Analog to digital converter (ADC)

The ADC differences are reflected in DMA requests and external channel numbers, which refers to ***Table 3-7. Differences of ADC function***.

Table 3-7. Differences of ADC function

Part numbers	DMA requests	external channel numbers
GD32W515xx	Support regular sequence DMA requests	Up to 9 channels
GD32F5HCxx	Support regular sequence and injection sequence DMA requests	Up to 12 channels

3.8. Free watchdog timer (FWDGT)

The FWDGT differences are reflected in the behavior after entering Deep-sleep mode and Standby mode, as well as whether the window function, which refers to ***Table 3-8. Differences of FWDGT function***.

Table 3-8. Differences of FWDGT function

Part numbers	Behavior after entering Deep-sleep mode and Standby mode	Window function
GD32W515xx	continue working	Not supported
GD32F5HCxx	can be configured to continue or stop working by the option byte FWDGSPD_STDBY or FWDGSPD_DPSLP	Supported

Additionally, FWDGT timeout differences can be referenced in ***Table 3-9. Min/max FWDGT timeout period at 32KHz (IRC32K) (Only for GD32F5HCxx)*** and ***Table 3-10. Min/max FWDGT timeout period at 32KHz (IRC32K) (Only for GD32W515xx)***.

Table 3-9. Min/max FWDGT timeout period at 32KHz (IRC32K) (Only for GD32F5HCxx)

Prescaler divider	PSC[2:0] bits	Min timeout (ms) RLD[11:0]= 0x000	Max timeout (ms) RLD[11:0]= 0xFFF
1/4	000	0.125	512
1/8	001	0.25	1024
1/16	010	0.5	2048
1/32	011	1.0	4096
1/64	100	2.0	8192
1/128	101	4.0	16384
1/256	110 or 111	8.0	32768

Table 3-10. Min/max FWDGT timeout period at 32KHz (IRC32K) (Only for GD32W515xx)

Prescaler divider	PSC[2:0] bits	Min timeout (ms) RLD[11:0]=0x000	Max timeout (ms) RLD[11:0]=0xFFF
1/4	000	0.03125	511.90625
1/8	001	0.03125	1023.78125
1/16	010	0.03125	2047.53125
1/32	011	0.03125	4095.03125
1/64	100	0.03125	8190.03125

Prescaler divider	PSC[2:0] bits	Min timeout (ms) RLD[11:0]=0x000	Max timeout (ms) RLD[11:0]=0xFFF
1/128	101	0.03125	16380.03125
1/256	110 or 111	0.03125	32760.03125

3.9. Timer（TIMER）

The TIMER differences are reflected in clock source configuration, quadrature decoder, master-slave management and timers interconnection, which refers to the < GD32W51x_B513_F5HC_User_Manual> for details.

3.10. Universal synchronous/asynchronous receiver /transmitter (USART)

The USART difference is reflected in auto baudrate detection function, which refers to ***Table 3-11. Differences of USART function***.

Table 3-11. Differences of USART function

Part numbers	Auto baudrate detection
GD32W515xx	Not supported
GD32F5HCxx	Supported

3.11. Quad-SPI interface (QSPI)

The QSPI difference is reflected in secure transfer function, which refers to ***Table 3-12. Differences of QSPI function***.

Table 3-12. Differences of QSPI function

Part numbers	secure transfer
GD32W515xx	Supported
GD32F5HCxx	Not supported

3.12. Inter-integrated circuit interface (I2C)

The I2C difference is reflected in Wakeup from Deep-sleep mode, which refers to ***Table 3-13. Differences of I2C function***.

Table 3-13. Differences of I2C function

Part numbers	Wakeup from Deep-sleep mode
GD32W515xx	Support I2C0 wakeup
GD32F5HCxx	Support I2C0/I2C1 wakeup

3.13. Cryptographic acceleration unit (CAU)

The CAU difference is reflected in data appending, which refers to ***Table 3-14. Differences of CAU function***.

Table 3-14. Differences of CAU function

Part numbers	Data appending
GD32W515xx	Not supported
GD32F5HCxx	Supported

4. Other differences

4.1. Clock

Maximum operating clock frequency difference of processor core refer to ***Table 4-1. Difference of system maximum operating clock frequency***.

Table 4-1. Difference of system maximum operating clock frequency

Part Numbers	Maximum operating frequency
GD32W515xx	Up to 180MHz
GD32F5HCxx	Up to 200MHz

4.2. Memory

Memory size difference refers to ***Table 4-2. Differences of memory size***.

Table 4-2. Differences of memory size

Part numbers	SRAM
GD32W515xx	Up to 448KB
GD32F5HCxx	Up to 320KB

4.3. Boot configuration

Boot configuration differences refer to ***Table 4-3. BOOT0 modes (Only for GD32F5HCxx)***, ***Table 4-4. BOOT0 modes (Only for GD32W515xx)***, ***Table 4-5. BOOT1 modes (Only for GD32F5HCxx)*** and ***Table 4-6. BOOT1 modes (Only for GD32W515xx)***.

Table 4-3. BOOT0 modes (Only for GD32F5HCxx)

EFUSE_CTL		FMC_OBR1		BOOT0 PC8 pin	BOOT0
SWBOOT0	EFBOOT0	SWBOOT0	nBOOT0		
0	-	1	-	0	0
0	-	1	-	1	1
0	-	0	1	-	0
0	-	0	0	-	1
1	0	-	-	-	0
1	1	-	-	-	1

Table 4-4. BOOT0 modes (Only for GD32W515xx)

SWBOOT0	EFBOOT0	BOOT0 PC8 pin	BOOT0
0	-	0	0
0	-	1	1
1	0	-	0

SWBOOT0	EFBOOT0	BOOT0 PC8 pin	BOOT0
1	1	-	1

Table 4-5. BOOT1 modes (Only for GD32F5HCxx)

EFUSE_CTL		FMC_OBR1		BOOT1 PA14 pin	BOOT1
SWBOOT1	EFBOOT1	SWBOOT1	nBOOT1		
0	-	1	-	0	0
0	-	1	-	1	1
0	-	0	1	-	0
0	-	0	0	-	1
1	0	-	-	-	0
1	1	-	-	-	1

Table 4-6. BOOT1 modes (Only for GD32W515xx)

SWBOOT1	EFBOOT1	BOOT1 PA14 pin	BOOT1
0	-	0	0
0	-	1	1
1	0	-	0
1	1	-	1

4.4. Number of peripherals

Number of peripherals difference refers to ***Table 4-7. Differences of number of peripherals*** .

Table 4-7. Differences of number of peripherals

Part numbers	CTC	SDIO	DCI	TSI	HPDF	Wi-Fi
GD32W515xx	Not supported	Supported				
GD32F5HCxx	Supported	Not supported				

4.5. Package

Package difference refers to ***Table 4-8. Differences of package***.

Table 4-8. Differences of package

Part numbers	BGA64	QFN56	QFN36
GD32W515xx	Not supported	Supported	Supported
GD32F5HCxx	Supported	Supported	Not supported

5. Revision history

Table 5-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Oct.5, 2025
1.1	Update ***Table 3-1. Differences of FMC function*** and ***Table 3-4. Differences of RCU function***	Dec.26, 2025
1.2	1. Update ***Reset and clock unit (RCU)*** 2. Add other differences, refer to ***Clock*** section	Mar.31, 2026

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