GigaDevice Semiconductor Inc.

GD32E53Pxx
Arm® Cortex®-M33 32-bit MCU

Datasheet

Revision 0.9RC1

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1. General description

The GD32E53Pxx device belongs to the high-performance line of GD32 MCU family. It is a new 32-bit general-purpose microcontroller based on the Arm® Cortex®-M33 core. The Cortex®-M33 processor is a 32-bit processor that possesses low interrupt latency and low-cost debug. The characteristics of integrated and advanced make the Cortex®-M33 processor suitable for market products that require microcontrollers with high performance and low power consumption. The Cortex®-M33 processor is based on the Armv8 architecture and supports a powerful and scalable instruction set including general data processing I/O control tasks, advanced data processing bit field manipulations and DSP.

The GD32E53Pxx device incorporates the Arm® Cortex®-M33 32-bit processor core operating at 252 MHz frequency. It provides up to 512 KB main Flash memory, 192+4KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer three 12-bit ADCs, two 12-bit DAC, as well as standard and advanced communication interfaces: up to four SPIs, an OSPI, two I2Ss, three I2Cs, four USARTs and two UARTs, three CAN-FDs, a USBFS and a SDIO. Additional peripherals as an EXMC interface, two comparators (CMP), a cryptographic acceleration unit (CAU), a Hash Acceleration Unit (HAU), CRC calculation unit (CRC), a true random number generator (TRNG), and a trigger selection controller (TRIGSEL) are included.

The device operates from a 1.71V to 3.6V power supply and available in -40 to +85 °C temperature range. Four power saving modes provide the flexibility for maximum optimization of power consumption, an especially important consideration in low power applications.

The above features make GD32E53Pxx devices suitable for a wide range of interconnection and advanced applications, especially in areas such as industrial control, consumer and handheld equipment, embedded modules, human machine interface, security and alarm systems, graphic display, audio player, automotive navigation, drone, IoT and so on



2. Device overview

2.1. Device information

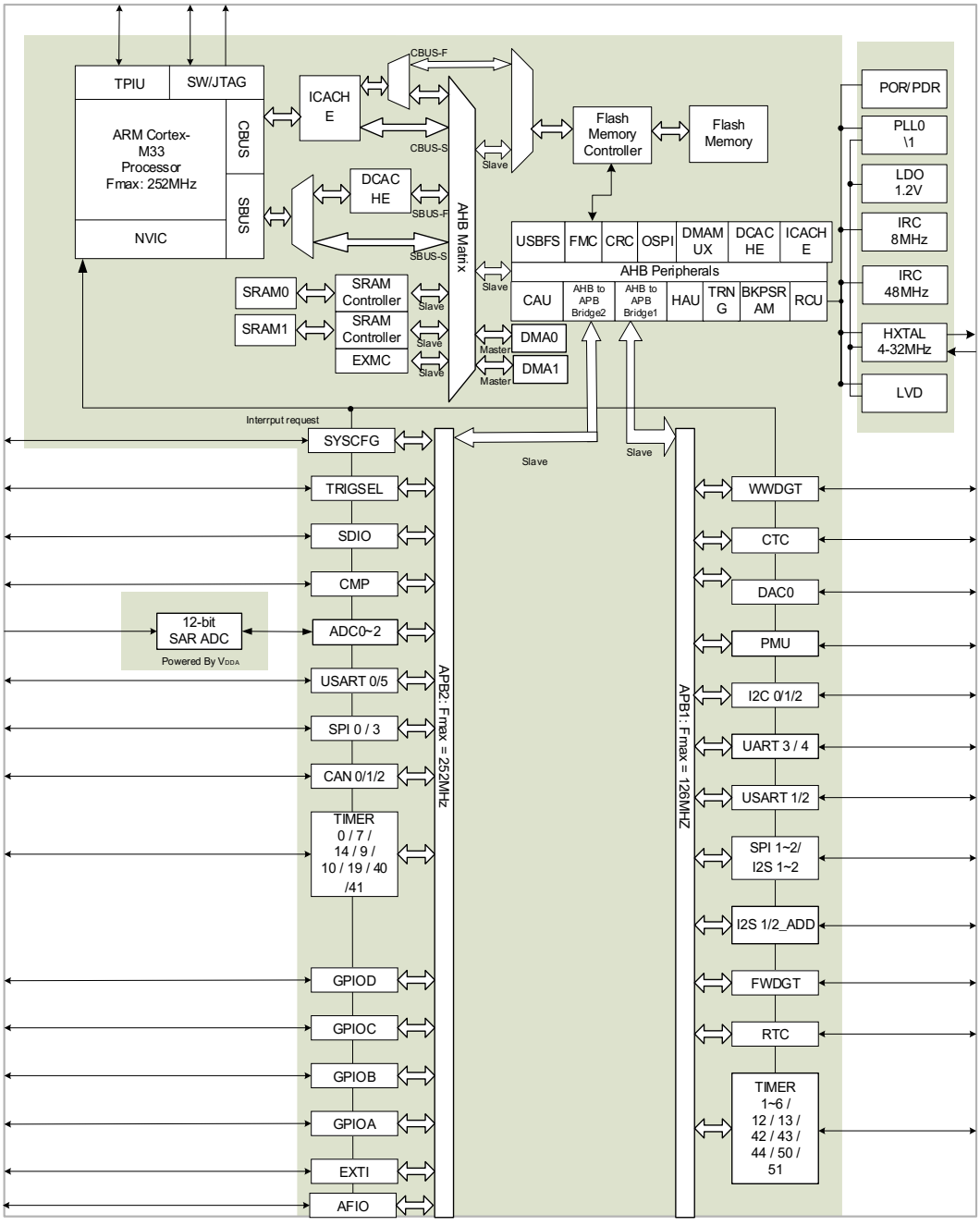
Table 2-1. GD32E53Pxx devices features and peripheral list

Part Number		GD32E53Pxx
		RET6
FLASH(KB)		512
SRAM (KB)		192+4+8M PSRAM
Timers	General timer (16-bit)	13 (2-4,9-10,12-14,40-44)
	General timer (32-bit)	1 (1)
	Advanced timer(16-bit)	3 (0,7,19)
	Basic timer (16-bit)	4 (5,6,50,51)
	SysTick	1
	Watchdog	2
	RTC	1
Connectivity	USART	4 (0-2,5)
	UART	2
	I2C	3 (0-2)
	SPI/I2S	4/2 (0-3)/(1-2)
	CAN	3xFD
	SDIO	1
	OSPI	1
	USBFS	1
GPIO		51
EXMC		1
CAU		1
HAU		1
TRIGSEL		1
CRC		1
TRNG		1
12bit ADC	Units	3
	Channels	20
DAC	Units	1

Part Number		GD32E53Pxx
		RET6
	Channels	2
CMP		2
Package		LQFP64

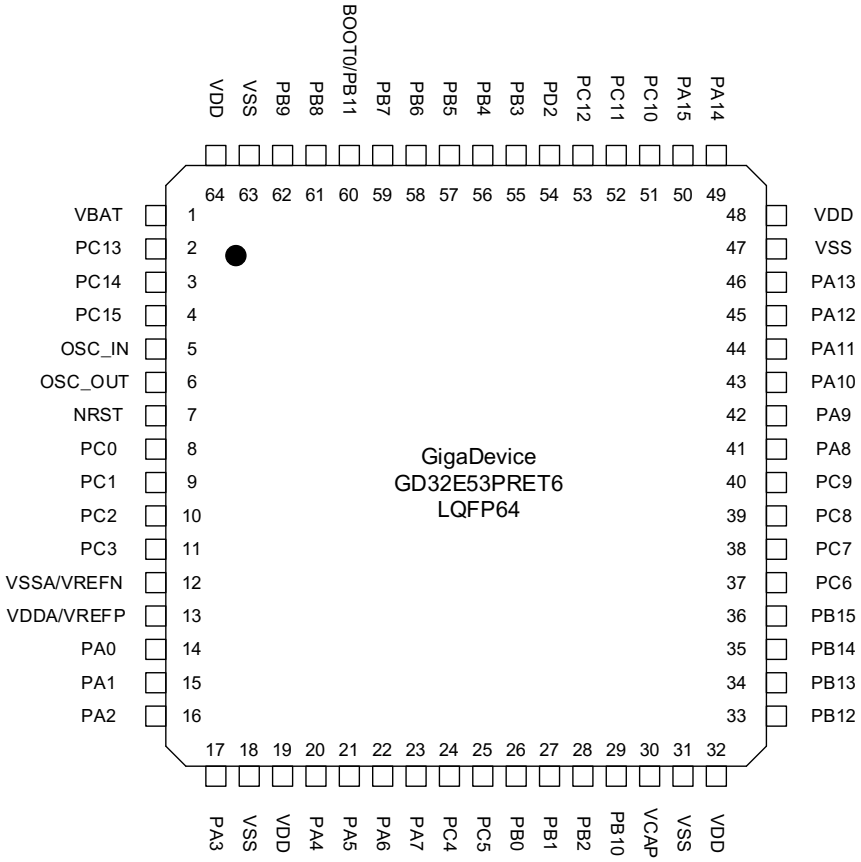
2.2. Block diagram

Figure 2-1. GD32E53Pxx block diagram



2.3. Pinouts and pin assignment

Figure 2-2. GD32E53PRx LQFP64 pin pinouts


VDD 64
VSS 63
PB9 62
PB8 61
BOOT0/PB11 60
PB7 59
PB6 58
PB5 57
PB4 56
PB3 55
PD2 54
PC12 53
PC11 52
PC10 51
PA15 50
PA14 49
VBAT 1
PC13 2
PC14 3
PC15 4
OSC_IN 5
OSC_OUT 6
NRST 7
PC0 8
PC1 9
PC2 10
PC3 11
VSSA/VREFN 12
VDDA/VREFP 13
PA0 14
PA1 15
PA2 16
48 VDD
47 VSS
46 PA13
45 PA12
44 PA11
43 PA10
42 PA9
41 PA8
40 PC9
39 PC8
38 PC7
37 PC6
36 PB15
35 PB14
34 PB13
33 PB12
GigaDevice
GD32E53PRET6
LQFP64
17 PA3
18 VSS
19 VDD
20 PA4
21 PA5
22 PA6
23 PA7
24 PC4
25 PC5
26 PB0
27 PB1
28 PB2
29 PB10
30 VCAP
31 VSS
32 VDD

2.4. Memory map

Table 2-2. GD32E53Pxx memory map

Pre-defined Regions	Bus	Address	Peripherals
External device	AHB3	0xC000 0000 - 0xDFFF FFFF	Reserved
		0xB000 0000 - 0xBFFF FFFF	OSPI(MEM)
		0xA000 1400 - 0xAFFF FFFF	Reserved
		0xA000 1000 - 0xA000 13FF	Reserved
		0xA000 0000 - 0xA000 0FFF	EXMC - SWREG
External RAM		0x9000 0000 - 0x9FFF FFFF	Reserved
		0x7000 0000 - 0x8FFF FFFF	EXMC - NAND
		0x6000 0000 - 0x6FFF FFFF	EXMC - NOR/PSRAM/SRAM
Peripheral	AHB1	0x5000 0000 - 0x5003 FFFF	USBFS
		0x4008 0400 - 0x4FFF FFFF	Reserved
		0x4008 0000 - 0x4008 03FF	Reserved
		0x4004 0000 - 0x4007 FFFF	Reserved
		0x4002 BC00 - 0x4003 FFFF	Reserved
		0x4002 B000 - 0x4002 BBFF	Reserved
		0x4002 A000 - 0x4002 AFFF	Reserved
		0x4002 8000 - 0x4002 9FFF	Reserved
		0x4002 6800 - 0x4002 7FFF	Reserved
		0x4002 6400 - 0x4002 67FF	DCACHE
		0x4002 6000 - 0x4002 63FF	ICACHE
		0x4002 5000 - 0x4002 5FFF	OSPI(REG)
		0x4002 4000 - 0x4002 4FFF	BKPSRAM
		0x4002 3C00 - 0x4002 3FFF	TRNG
		0x4002 3800 - 0x4002 3BFF	HAU
		0x4002 3400 - 0x4002 37FF	CAU
		0x4002 3000 - 0x4002 33FF	CRC
		0x4002 2C00 - 0x4002 2FFF	Reserved
		0x4002 2800 - 0x4002 2BFF	Reserved
		0x4002 2400 - 0x4002 27FF	Reserved
		0x4002 2000 - 0x4002 23FF	FMC
		0x4002 1C00 - 0x4002 1FFF	Reserved
		0x4002 1800 - 0x4002 1BFF	Reserved
		0x4002 1400 - 0x4002 17FF	Reserved
		0x4002 1000 - 0x4002 13FF	RCU
		0x4002 0C00 - 0x4002 0FFF	Reserved
		0x4002 0800 - 0x4002 0BFF	DMAMUX
		0x4002 0400 - 0x4002 07FF	DMA1

Pre-defined Regions	Bus	Address	Peripherals
		0x4002 0000 - 0x4002 03FF	DMA0
		0x4001 9C00 - 0x4001 FFFF	Reserved
	APB2	0x4001 9800 - 0x4001 9BFF	SYSCFG
		0x4001 9400 - 0x4001 97FF	Shared APB/CAN2 SRAM
		0x4001 9000 - 0x4001 93FF	TRIGSEL
		0x4001 8D00 - 0x4001 8FFF	Reserved
		0x4001 8C00 - 0x4001 8CFF	Shared APB/CAN SRAM (256 bytes)
		0x4001 8800 - 0x4001 8BFF	Shared APB/CAN SRAM
		0x4001 8400 - 0x4001 87FF	SPI3
		0x4001 8000 - 0x4001 83FF	SDIO
		0x4001 7C00 - 0x4001 7FFF	CMP
		0x4001 7800 - 0x4001 7BFF	Reserved
		0x4001 7400 - 0x4001 77FF	CAN2
		0x4001 7000 - 0x4001 73FF	USART5
		0x4001 6C00 - 0x4001 6FFF	Reserved
		0x4001 6800 - 0x4001 6BFF	Reserved
		0x4001 5C00 - 0x4001 67FF	Reserved
		0x4001 5800 - 0x4001 5BFF	Reserved
		0x4001 5400 - 0x4001 57FF	TIMER10
		0x4001 5000 - 0x4001 53FF	TIMER9
		0x4001 4C00 - 0x4001 4FFF	TIMER40
		0x4001 4800 - 0x4001 4BFF	TIMER19
		0x4001 4400 - 0x4001 47FF	TIMER41
		0x4001 4000 - 0x4001 43FF	TIMER14
		0x4001 3C00 - 0x4001 3FFF	ADC2
		0x4001 3800 - 0x4001 3BFF	USART0
		0x4001 3400 - 0x4001 37FF	TIMER7
		0x4001 3000 - 0x4001 33FF	SPI0
		0x4001 2C00 - 0x4001 2FFF	TIMER0
		0x4001 2800 - 0x4001 2BFF	ADC1
		0x4001 2400 - 0x4001 27FF	ADC0
		0x4001 2000 - 0x4001 23FF	CAN1
		0x4001 1C00 - 0x4001 1FFF	CAN0
		0x4001 1800 - 0x4001 1BFF	Reserved
		0x4001 1400 - 0x4001 17FF	GPIOD
		0x4001 1000 - 0x4001 13FF	GPIOC
		0x4001 0C00 - 0x4001 0FFF	GPIOB

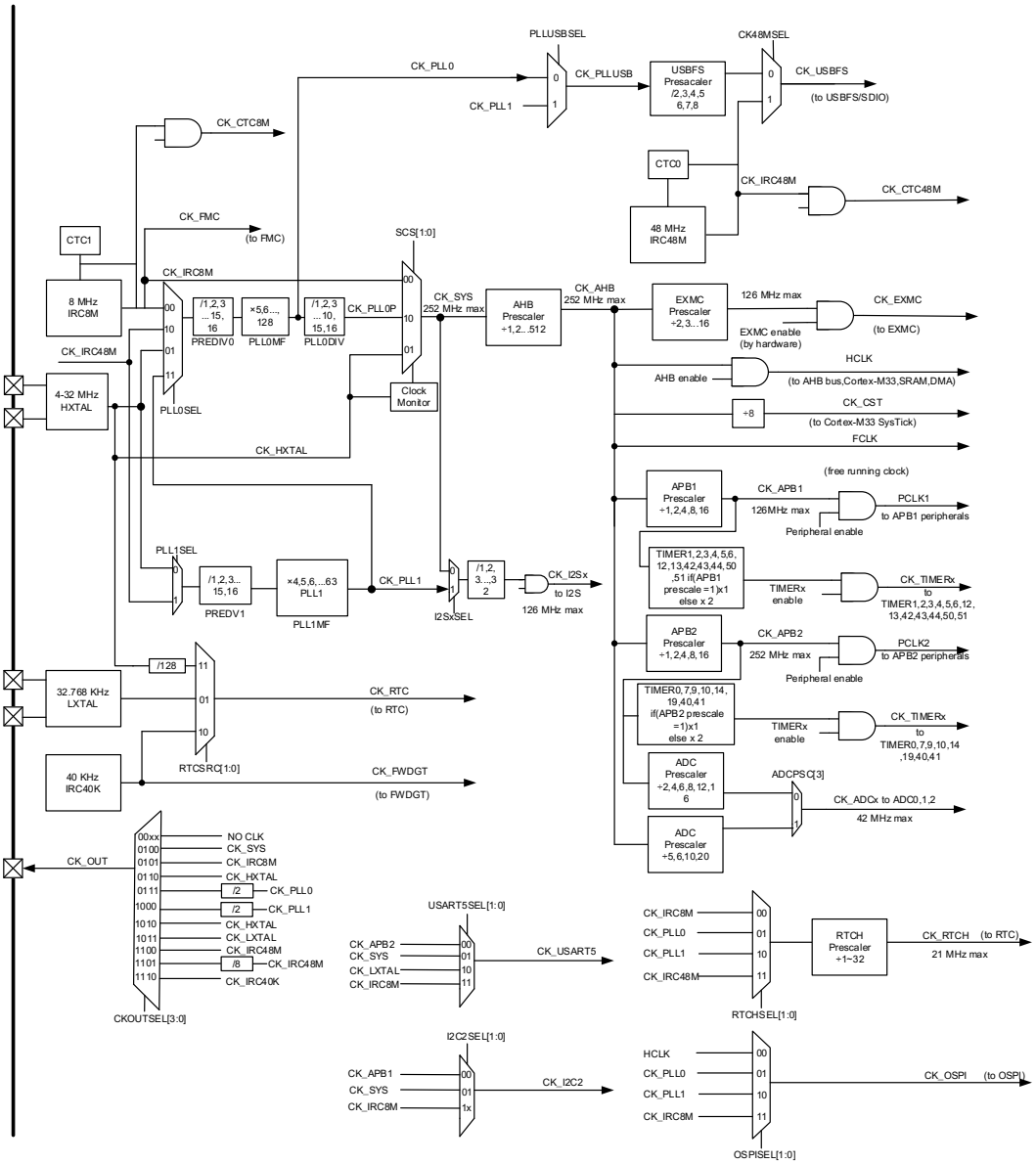
Pre-defined Regions	Bus	Address	Peripherals
		0x4001 0800 - 0x4001 0BFF	GPIOA
		0x4001 0400 - 0x4001 07FF	EXTI
		0x4001 0000 - 0x4001 03FF	AFIO
	APB1	0x4000 F400 - 0x4000 FFFF	Reserved
		0x4000 F000 - 0x4000 F3FF	TIMER51
		0x4000 EC00 - 0x4000 EFFF	TIMER50
		0x4000 E800 - 0x4000 EBFF	TIMER44
		0x4000 E400 - 0x4000 E7FF	TIMER43
		0x4000 E000 - 0x4000 E3FF	TIMER42
		0x4000 D000 - 0x4000 DFFF	Reserved
		0x4000 CC00 - 0x4000 CFFF	CTC1
		0x4000 C800 - 0x4000 CBFF	CTC0
		0x4000 C400 - 0x4000 C7FF	Reserved
		0x4000 C000 - 0x4000 C3FF	I2C2
		0x4000 8C00 - 0x4000 BFFF	Reserved
		0x4000 8800 - 0x4000 8BFF	Reserved
		0x4000 8400 - 0x4000 87FF	Reserved
		0x4000 8000 - 0x4000 BFFF	Reserved
		0x4000 7C00 - 0x4000 7FFF	Reserved
		0x4000 7800 - 0x4000 7BFF	Reserved
		0x4000 7400 - 0x4000 77FF	DAC0
		0x4000 7000 - 0x4000 73FF	PMU
		0x4000 6C00 - 0x4000 6FFF	Reserved
		0x4000 6800 - 0x4000 6BFF	Reserved
		0x4000 6400 - 0x4000 67FF	Reserved
		0x4000 6000 - 0x4000 63FF	Reserved
		0x4000 5C00 - 0x4000 5FFF	Reserved
		0x4000 5800 - 0x4000 5BFF	I2C1
		0x4000 5400 - 0x4000 57FF	I2C0
		0x4000 5000 - 0x4000 53FF	UART4
		0x4000 4C00 - 0x4000 4FFF	UART3
		0x4000 4800 - 0x4000 4BFF	USART2
		0x4000 4400 - 0x4000 47FF	USART1
		0x4000 4000 - 0x4000 43FF	I2S2_ADD
		0x4000 3C00 - 0x4000 3FFF	SPI2/I2S2
		0x4000 3800 - 0x4000 3BFF	SPI1/I2S1
		0x4000 3400 - 0x4000 37FF	I2S1_ADD
		0x4000 3000 - 0x4000 33FF	FWDGT
		0x4000 2C00 - 0x4000 2FFF	WWDGT
		0x4000 2800 - 0x4000 2BFF	RTC

Pre-defined Regions	Bus	Address	Peripherals
		0x4000 2400 - 0x4000 27FF	Reserved
		0x4000 2000 - 0x4000 23FF	TIMER13
		0x4000 1C00 - 0x4000 1FFF	TIMER12
		0x4000 1800 - 0x4000 1BFF	Reserved
		0x4000 1400 - 0x4000 17FF	TIMER6
		0x4000 1000 - 0x4000 13FF	TIMER5
		0x4000 0C00 - 0x4000 0FFF	TIMER4
		0x4000 0800 - 0x4000 0BFF	TIMER3
		0x4000 0400 - 0x4000 07FF	TIMER2
		0x4000 0000 - 0x4000 03FF	TIMER1
SRAM	AHB	0x2007 0000 - 0x3FFF FFFF	Reserved
		0x2006 0000 - 0x2006 FFFF	Reserved
		0x2003 0000 - 0x2005 FFFF	Reserved
		0x2002 0000 - 0x2002 FFFF	SRAM1
		0x2000 0000 - 0x2001FFFF	SRAM0
Code	AHB	0x1FFF F810 - 0x1FFF FFFF	Reserved
		0x1FFF F800 - 0x1FFF F84F	Option Bytes
		0x1FFF F000 - 0x1FFF F7FF	Boot loader
		0x1FFF C010 - 0x1FFF EFFF	
		0x1FFF C000 - 0x1FFF C00F	
		0x1FFF B000 - 0x1FFF BFFF	
		0x1FFF 7800 - 0x1FFF AFFF	Reserved
		0x1FFF 6800 - 0x1FFF 77FF	OTP
		0x1FFF 0000 - 0x1FFF 6FFF	Reserved
		0x1FFE C010 - 0x1FFE FFFF	External memories
		0x1FFE C000 - 0x1FFE C00F	
		0x1001 0000 - 0x1FFE BFFF	
		0x1000 0000 - 0x1000 FFFF	
		0x0F00 0000 - 0x0FFF FFFF	Reserved
		0x0E03 0000 - 0x0EFF FFFF	Reserved
		0x0E02 0000 - 0x0E02 FFFF	SRAM1
		0x0E00 0000 - 0x0E01 FFFF	SRAM0
		0x083C 0000 - 0x0DFF FFFF	Reserved
		0x0830 0000 - 0x083B FFFF	Reserved
		0x0808 0000 - 0x082F FFFF	Reserved
		0x0800 0000 - 0x0807 FFFF	Main Flash
		0x0030 0000 - 0x07FF FFFF	Reserved
		0x0010 0000 - 0x002F FFFF	Reserved
		0x0008 0000 - 0x000F FFFF	Reserved
		0x0002 0000 - 0x0007 FFFF	External memories

Pre-defined Regions	Bus	Address	Peripherals
		0x0000 0000 - 0x0001 FFFF	

2.5. Clock tree

Figure 2-3. GD32E53Pxx clock tree



Legend:

HXTAL: High speed crystal oscillator

LXTAL: Low speed crystal oscillator

IRC8M: Internal 8M RC oscillators

IRC40K: Internal 40K RC oscillator

IRC48M: Internal 48M RC oscillators

2.6. Pin definitions

2.6.1. GD32E53PRx LQFP64 pin definitions

Table 2-3. GD32E53PRx LQFP64 pin definitions

GD32E53PRx LQFP64				
Pin Name	**Pins**	**Pin Type**	**I/O Level**	**Functions description**
VBAT	1	P	-	Default: VBAT
PC13	2	I/O	-	Default: PC13 Alternate: EVENTOUT Additional: RTC_TAMP0, RTC_TS0, RTC_OUT, WKUP1
PC14	3	I/O	-	Default: PC14 Alternate: EVENTOUT Additional: OSC32IN
PC15	4	I/O	-	Default: PC15 Alternate: EVENTOUT Additional: OSC32OUT
OSCIN-PD0	5	I/O	-	Default: OSCIN, PD0
OSCOUT-PD1	6	I/O	-	Default: OSCOUT, PD1
NRST	7	-	-	Default: NRST
PC0	8	I/O	-	Default: PC0 Alternate: TIMER7_CH0_ON, TIMER0_CH0, OSPI_IO7, EXMC_NADV, EVENTOUT Additional: ADC01_IN10
PC1	9	I/O	-	Default: PC1 Alternate: TIMER7_CH1_ON, TIMER0_CH1, OSPI_IO4, EVENTOUT Additional: ADC01_IN11
PC2	10	I/O	-	Default: PC2 Alternate: TIMER7_CH2_ON, TIMER0_CH2, I2S1_ADD_SD, OSPI_IO2, OSPI_IO5, EXMC_NWE, EVENTOUT Additional: ADC01_IN12
PC3	11	I/O	-	Default: PC3 Alternate: TIMER7_CH3_ON, EXMC_A0, OSPI_IO0, OSPI_IO6, EVENTOUT Additional: ADC01_IN13
VSSA-	12	P	-	Default: VSSA, VREFN

GD32E53PRx LQFP64				
Pin Name	**Pins**	**Pin Type**	**I/O Level**	**Functions description**
VREFN				
VDDA-VREFP	13	P	-	Default: VDDA, VREFP
PA0	14	I/O	-	Default: PA0 Alternate: USART1_CTS, TIMER1_CH0_ETI, CAN0_RX, TIMER4_CH0, TIMER7_ETI, USART2_RX, TRIGSEL_IN5, EVENTOUT, SPI3_IO2 Additional: WKUP0, ADC012_IN0
PA1	15	I/O	-	Default: PA1 Alternate: USART1_RTS, TIMER1_CH1, TIMER14_MCH0, TIMER4_CH1, OSPI_IO3, TRIGSEL_IN6, OSPI_DQS, EVENTOUT, SPI3_IO3 Additional: ADC012_IN1
PA2	16	I/O	-	Default: PA2 Alternate: USART1_TX, TIMER1_CH2, TIMER43_CH0, TIMER4_CH2, USART2_RX, SPI0_IO2, CMP0_OUT, EXMC_D4, EVENTOUT Additional: WKUP3, ADC012_IN2, CMP0_IM2
PA3	17	I/O	-	Default: PA3 Alternate: USART1_RX, TIMER1_CH3, TIMER43_CH1, TIMER4_CH3, TIMER14_CH1, SPI0_IO3, TRIGSEL_OUT1, OSPI_SCK, EXMC_D5, EVENTOUT Additional: ADC012_IN3
VSS	18	P	-	Default: VSS
VDD	19	P	-	Default: VDD
PA4	20	I/O	-	Default: PA4 Alternate: SPI0_NSS, USART1_CK, SPI2_NSS, I2S2_WS, TRIGSEL_OUT0, EXMC_D6, EVENTOUT Additional: DAC0_OUT0, ADC01_IN4, CMP0_IM0, CMP1_IM0
PA5	21	I/O	-	Default: PA5 Alternate: SPI0_SCK, TIMER4_ETI, TIMER41_BRKIN, UART3_TX, EXMC_D7, EVENTOUT Additional: DAC0_OUT1, CMP0_IM1, CMP1_IM1, ADC01_IN5
PA6	22	I/O	-	Default: PA6

GD32E53PRx LQFP64				
Pin Name	**Pins**	**Pin Type**	**I/O Level**	**Functions description**
				Alternate: SPI0_MISO, TIMER2_CH0, TIMER0_BRKIN, TIMER12_CH0, TIMER7_BRKIN, UART3_RX, TRIGSEL_OUT2, OSPI_IO3, EVENTOUT, TIMER41_CH1 Additional: ADC01_IN6
PA7	23	I/O	-	Default: PA7 Alternate: SPI0_MOSI, TIMER2_CH1, TIMER0_CH0_ON, TIMER13_CH0, TIMER7_CH0_ON, TRIGSEL_OUT3, OSPI_IO2, EVENTOUT, TIMER44_CH1 Additional: ADC01_IN7, CMP0_IP
PC4	24	I/O	-	Default: PC4 Alternate: TIMER7_CH3, USART0_TX, EXMC_NE1, EVENTOUT Additional: ADC01_IN14
PC5	25	I/O	-	Default: PC5 Alternate: USART0_RX, CAN2_RX, TIMER14_BRKIN, USART2_RX, OSPI_DQS, EXMC_NOE, EVENTOUT Additional: ADC01_IN15, WKUP4
PB0	26	I/O	-	Default: PB0 Alternate: TIMER0_CH1_ON, TIMER2_CH2, TIMER7_CH1_ON, OSPI_IO1, EVENTOUT, SPI3_SCK Additional: ADC01_IN8, CMP1_IP
PB1	27	I/O	-	Default: PB1 Alternate: TIMER0_CH2_ON, TIMER2_CH3, TIMER7_CH2_ON, CMP1_OUT, OSPI_IO0, EVENTOUT, SPI3_MISO Additional: ADC01_IN9
PB2	28	I/O	5VT	Default: PB2 Alternate: TIMER1_CH3, USART2_RX, I2C1_SDA, CAN2_TX, TIMER0_CH3_ON, RTC_OUT, OSPI_DQS, OSPI_SCK, EVENTOUT, SPI3_MOSI Additional: CMP1_IM3, ADC2_IN13, ADC1_IN16
PB10	29	I/O	5VT	Default: PB10 Alternate: TIMER1_CH2, USART2_TX, I2C1_SCL, CAN2_RX, TIMER7_CH3_ON, I2C1_SDA, OSPI_CSN1, OSPI_CSN0, EVENTOUT,

GD32E53PRx LQFP64				
Pin Name	**Pins**	**Pin Type**	**I/O Level**	**Functions description**
				SPI3_NSS, TIMER4_CH2 Additional: ADC2_IN14, ADC1_IN17
VCAP	30	P	-	Default: VCAP
VSS	31	P	-	Default: VSS
VDD	32	P	-	Default: VDD
PB12	33	I/O	5VT	Default: PB12 Alternate: USART2_CK, SPI1_NSS, I2S1_WS, I2C1_SMBA, CAN1_RX, TIMER0_BRKIN, OSPI_nSCK, EXMC_D13, EVENTOUT, TIMER4_CH3 Additional: ADC2_IN15
PB13	34	I/O	5VT	Default: PB13 Alternate: USART2_CTS, SPI1_SCK, I2S1_CK, TIMER0_CH0_ON, CAN1_TX, OSPI_IO4, OSPI_IO2, RTC_REFIN, EVENTOUT Additional: ADC2_IN16
PB14	35	I/O	5VT	Default: PB14 Alternate: USART2_RTS, SPI1_MISO, TIMER0_CH1_ON, I2S1_ADD_SD, TIMER14_CH0, OSPI_IO5, OSPI_IO0, EXMC_D0, EVENTOUT, TIMER40_CH0
PB15	36	I/O	5VT	Default: PB15 Alternate: SPI1_MOSI, I2S1_SD, TIMER0_CH2_ON, USART2_RX, CAN1_RX, TIMER14_CH1, TIMER14_MCH0, RTC_REFIN, EVENTOUT, TIMER40_CH1 Additional: WKUP6, ADC2_IN18
PC6	37	I/O	5VT	Default: PC6 Alternate: TIMER2_CH0, I2S1_MCK, TIMER7_CH0, USART5_TX, SDIO_D6, OSPI_IO5, EXMC_D1, EVENTOUT, SPI3_NSS
PC7	38	I/O	5VT	Default: PC7 Alternate: TIMER2_CH1, I2S2_MCK, TIMER7_CH1, USART5_RX, SDIO_D7, OSPI_IO6, EVENTOUT, SPI3_SCK
PC8	39	I/O	5VT	Default: PC8 Alternate: TIMER2_CH2, TIMER7_CH2, USART5_CK, SDIO_D0, EXMC_NE1, EVENTOUT, SPI3_MISO
PC9	40	I/O	5VT	Default: PC9

GD32E53PRx LQFP64				
Pin Name	**Pins**	**Pin Type**	**I/O Level**	**Functions description**
				Alternate: TIMER2_CH3, TIMER7_CH3, USART5_RTS, USART5_DE, UART4_TX, SDIO_D1, OSPI_IO0, EXMC_NADV, EVENTOUT, SPI3_MOSI, I2C2_SDA
PA8	41	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, USBFS_SOF, CK_OUT, UART4_RX, CTC_SYNC, TRIGSEL_OUT4, USART5_CTS, EVENTOUT, SPI3_IO2, I2C2_SCL
PA9	42	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN, CAN2_RX, USART5_RTS, USART5_DE, TRIGSEL_OUT5, EVENTOUT, SPI3_IO3, I2C2_SMBA
PA10	43	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, USART0_TX, CAN2_TX, USART5_CK, TIMER42_BRKIN, CMP1_OUT, EVENTOUT
PA11	44	I/O	5VT	Default: PA11 Alternate: USART0_CTS, CAN0_RX, TIMER0_CH3, TIMER40_CH0, USART5_TX, SPI1_MOSI, TRIGSEL_IN0, EVENTOUT Additional: USBFS_DM
PA12	45	I/O	5VT	Default: PA12 Alternate: USART0_RTS, CAN0_TX, TIMER0_ETI, TIMER40_CH1, USART5_RX, TIMER41_CH0, CMP0_OUT, EVENTOUT, TIMER4_CH0 Additional: USBFS_DP
PA13	46	I/O	5VT	Default: JTMS, SWDIO, PA13 Alternate: USART5_CTS, TIMER41_MCH0, EVENTOUT, TIMER4_CH1
VDD	48	P	-	Default: VDD
VSS	47	P	-	Default: VSS
PA14	49	I/O	5VT	Default: JTCK, SWCLK, PA14 Alternate: EVENTOUT
PA15	50	I/O	5VT	Default: JTDI, PA15 Alternate: TIMER1_CH0_ETI, SPI0_NSS, SPI2_NSS, I2S2_WS, TIMER19_CH1BRKIN, USART1_RX, OSPI_IO3, OSPI_CSN0, EVENTOUT, OSPI_CSN1, TIMER4_CH3

GD32E53PRx LQFP64				
Pin Name	**Pins**	**Pin Type**	**I/O Level**	**Functions description**
PC10	51	I/O	5VT	Default: PC10 Alternate: USART2_TX, UART3_TX, SPI2_SCK, I2S2_CK, TIMER7_CH0BRKIN, SDIO_D2, OSPI_IO1, EVENTOUT, I2C2_SCL
PC11	52	I/O	5VT	Default: PC11 Alternate: USART2_RX, UART3_RX, SPI2_MISO, TIMER7_CH1BRKIN, I2S2_ADD_SD, SDIO_D3, OSPI_CSN0, EXMC_D2, EVENTOUT, OSPI_CSN1
PC12	53	I/O	5VT	Default: PC12 Alternate: USART2_CK, UART4_TX, SPI2_MOSI, I2S2_SD, TIMER7_CH2BRKIN, SDIO_CK, TRIGSEL_IN2, EXMC_D3, EVENTOUT, TIMER40_MCH0
PD2	54	I/O	5VT	Default: PD2 Alternate: TIMER2_ETI, UART4_RX, TIMER19_CH2BRKIN, SDIO_CMD, EXMC_NWE, EVENTOUT, TIMER4_CH0, TIMER42_CH0
PB3	55	I/O	5VT	Default: PB3，JTDO Alternate: TRACESWO, TIMER1_CH1, SPI0_SCK, SPI2_SCK, I2S2_CK, TIMER19_ETI, CK_OUT, TRIGSEL_IN1, OSPI_IO1, EVENTOUT, UART3_TX, OSPI_IO6
PB4	56	I/O	5VT	Default: PB4, NJTRST Alternate: TIMER2_CH0, SPI0_MISO, SPI2_MISO, TIMER19_CH0_ON, I2S2_ADD_SD, TRIGSEL_OUT6, OSPI_SCK, EVENTOUT, TIMER44_BRKIN, TIMER0_CH0BRKIN, TIMER42_CH0, I2C2_SDA, UART3_RX
PB5	57	I/O	-	Default: PB5 Alternate: TIMER2_CH1, SPI0_MOSI, I2C0_SMBA, CAN1_RX, TIMER19_CH1_ON, SPI2_MOSI, I2S2_SD, OSPI_nSCK, EVENTOUT, TIMER44_CH0, TIMER0_CH1BRKIN, TIMER41_BRKIN, I2C2_SCL Additional: WKUP5
PB6	58	I/O	5VT	Default: PB6 Alternate: USART0_TX, I2C0_SCL, TIMER3_CH0, CAN1_TX, TIMER19_CH2_ON, SPI0_IO2, I2C1_SCL, OSPI_CSN0, EVENTOUT,

GD32E53PRx LQFP64				
Pin Name	**Pins**	**Pin Type**	**I/O Level**	**Functions description**
				OSPI_CSN1, TIMER0_CH2BRKIN, TIMER42_MCH0, OSPI_IO7
PB7	59	I/O	5VT	Default: PB7 Alternate: USART0_RX, I2C0_SDA, TIMER3_CH1, TIMER19_CH3_ON, EXMC_NADV, SPI0_IO3, TRIGSEL_OUT7, OSPI_DQS, EVENTOUT, TIMER44_MCH0, USART1_TX, I2C1_SDA
BOOT0-PB11	60	I/O	-	Default: BOOT0, PB11 Alternate: EVENTOUT, UART3_RX
PB8	61	I/O	5VT	Default: PB8 Alternate: I2C0_SCL, CAN0_RX, TIMER3_CH2, TIMER9_CH0, TIMER19_BRKIN, SDIO_D4, EVENTOUT, UART4_TX, TIMER42_CH1, I2C2_SDA
PB9	62	I/O	5VT	Default: PB9 Alternate: I2C0_SDA, CAN0_TX, TIMER3_CH3, TIMER10_CH0, TIMER19_CH0BRKIN, SDIO_D5, CMP0_OUT, EVENTOUT, TIMER44_CH1, UART4_RX, TIMER41_MCH0 Additional: WKUP7
VSS	63	P	-	Default: VSS
VDD	64	P	-	Default: VDD

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

2.6.2. GD32E53Pxx pin alternate functions

Table 2-4. Port A alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13
PA0	USART1_CTS	TIMER1_CH0_ETI	CAN0_RX	TIMER4_CH0	TIMER7_ETI	USART2_RX	TRIGSEL_IN5		EVENTOUT	SPI3_IO2				
PA1	USART1_RTS	TIMER1_CH1	TIMER14_MCH0	TIMER4_CH1		OSPI_IO3	TRIGSEL_IN6	OSPI_DQS	EVENTOUT	SPI3_IO3				
PA2	USART1_TX	TIMER1_CH2	TIMER43_CH0	TIMER4_CH2	USART2_RX	SPI0_IO2	CMP0_OUT	EXMC_D4	EVENTOUT					
PA3	USART1_RX	TIMER1_CH3	TIMER43_CH1	TIMER4_CH3	TIMER14_CH1	SPI0_IO3	TRIGSEL_OUT1	EXMC_D5	EVENTOUT	OSPI_SCK				
PA4	SPI0_NSS	USART1_CK	SPI2_NSS/I2S2_WS				TRIGSEL_OUT0	EXMC_D6	EVENTOUT					
PA5	SPI0_SCK			TIMER4_ETI	TIMER41_BRKIN	UART3_TX		EXMC_D7	EVENTOUT					
PA6	SPI0_MISO	TIMER2_CH0	TIMER0_BRKIN	TIMER12_CH0	TIMER7_BRKIN	UART3_RX	TRIGSEL_OUT2	OSPI_IO3	EVENTOUT			TIMER41_CH1		
PA7	SPI0_MOSI	TIMER2_CH1	TIMER0_CH0_ON	TIMER13_CH0	TIMER7_CH0_ON		TRIGSEL_OUT3	OSPI_IO2	EVENTOUT	TIMER44_CH1				
PA8	USART0_CK	TIMER0_CH0	USBFS_SOF	CK_OUT	UART4_RX	CTC_SYNC	TRIGSEL_OUT4	USART5_CTS	EVENTOUT	SPI3_IO2			I2C2_SCL	
PA9	USART0_TX	TIMER0_CH1	TIMER14_BRKIN	CAN2_RX	USART5_RTS/USAR		TRIGSEL_OUT5		EVENTOUT	SPI3_IO3			I2C2_SM	

					T5_DE								BA	
PA10	USART0_RX	TIMER0_CH2	USART0_TX	CAN2_TX	USART5_CK	TIMER42_BRKIN	CMP1_OUT		EVENTOUT					
PA11	USART0_CTS	CAN0_RX	TIMER0_CH3	TIMER40_CH0	USART5_TX	SPI1_MOSI	TRIGSEL_IN0		EVENTOUT					
PA12	USART0_RTS	CAN0_TX	TIMER0_ETI	TIMER40_CH1	USART5_RX	TIMER41_CH0	CMP0_OUT		EVENTOUT		TIMER4_CH0			
PA13	JTMS/SWDIO				USART5_CTS	TIMER41_MCH0			EVENTOUT		TIMER4_CH1			
PA14	JTCK/SWCLK								EVENTOUT					
PA15	JTDI	TIMER1_CH0_ETI	SPI0_NSS	SPI2_NSS/I2S2_WS	TIMER19_CH1BRKIN	USART1_RX	OSPI_IO3	OSPI_CSN0	EVENTOUT	OSPI_CSN1	TIMER4_CH3			

Table 2-5. Port B alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13
PB0	TIMER0_CH1_ON	TIMER2_CH2		TIMER7_CH1_ON				OSPI_IO1	EVENTOUT	SPI3_SCK				
PB1	TIMER0_CH2_ON	TIMER2_CH3		TIMER7_CH2_ON			CMP1_OUT	OSPI_IO0	EVENTOUT	SPI3_MISO				
PB2	TIMER1_CH3	USART2_RX	I2C1_SDA	CAN2_TX	TIMER0_CH3_ON	RTC_OUT	OSPI_DQS	OSPI_SCK	EVENTOUT	SPI3_MOSI				
PB3	JTDO/TRACESWO	TIMER1_CH1	SPI0_SCK	SPI2_SCK/I2S2_CK	TIMER19_ETI	CK_OUT	TRIGSEL_IN1	OSPI_IO1	EVENTOUT	UART3_TX			OSPI_IO6	
PB4	NJTRST	TIMER2_CH0	SPI0_MISO	SPI2_MISO	TIMER19_CH0_ON	I2S2_ADD_SD	TRIGSEL_OUT6	OSPI_SCK	EVENTOUT	TIMER44_BRKIN	TIMER0_CH0BRKIN	TIMER42_CH0	I2C2_SDA	UART3_RX
PB5	TIMER2_CH	SPI0_MOSI	I2C0_SMB	CAN1_RX	TIMER19_C	SPI2_MOSI/I		OSPI_	EVENT	TIMER44_	TIMER0_CH	TIMER41_	I2C2_	

	1		A		H1_ON	2S2_SD		nSCK	OUT	CH0	1BRKIN	BRKIN	SCL	
PB6	USART0_TX	I2C0_SCL	TIMER3_CH0	CAN1_TX	TIMER19_CH2_ON	SPI0_IO2	I2C1_SCL	OSPI_CSN0	EVENTOUT	OSPI_CSN1	TIMER0_CH2BRKIN	TIMER42_MCH0	OSPI_IO7	
PB7	USART0_RX	I2C0_SDA	TIMER3_CH1	EXMC_NADV	TIMER19_CH3_ON	SPI0_IO3	TRIGSEL_OUT7	OSPI_DQS	EVENTOUT	TIMER44_MCH0		USART1_TX	I2C1_SDA	
PB8	I2C0_SCL	CAN0_RX	TIMER3_CH2	TIMER9_CH0	TIMER19_BRKIN	SDIO_D4			EVENTOUT		UART4_TX	TIMER42_CH1	I2C2_SDA	
PB9	I2C0_SDA	CAN0_TX	TIMER3_CH3	TIMER10_CH0	TIMER19_CH0BRKIN	SDIO_D5	CMP0_OUT		EVENTOUT	TIMER44_CH1	UART4_RX	TIMER41_MCH0		
PB10	TIMER1_CH2	USART2_TX	I2C1_SCL	CAN2_RX	TIMER7_CH3_ON	I2C1_SDA	OSPI_CSN1	OSPI_CSN0	EVENTOUT	SPI3_NSS	TIMER4_CH2			
BOOT0/ PB11									EVENTOUT	UART3_RX				
PB12	USART2_CK	SPI1_NSS/I2S1_WS	I2C1_SMBA	CAN1_RX	TIMER0_BRKIN		OSPI_nSCK	EXMC_D13	EVENTOUT		TIMER4_CH3			
PB13	USART2_CTS	SPI1_SCK/I2S1_CK	TIMER0_CH0_ON	CAN1_TX		OSPI_IO4	OSPI_IO2	RTC_REFIN	EVENTOUT					
PB14	USART2_RTS	SPI1_MISO	TIMER0_CH1_ON	I2S1_ADD_SD	TIMER14_CH0	OSPI_IO5	OSPI_IO0	EXMC_D0	EVENTOUT			TIMER40_CH0		
PB15	SPI1_MOSI/I2S1_SD	TIMER0_CH2_ON	USART2_RX	CAN1_RX	TIMER14_CH1	TIMER14_MCH0		RTC_REFIN	EVENTOUT			TIMER40_CH1		

Table 2-6. Port C alternate functions summary

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13
PC0	TIMER7_CH0_ON	TIMER0_CH0					OSPI_IO7	EXMC_NADV	EVENTOUT					

PC1	TIMER7_CH1_ON	TIMER0_CH1					OSPI_IO4		EVENTOUT					
PC2	TIMER7_CH2_ON	TIMER0_CH2		I2S1_ADD_SD		OSPI_IO2	OSPI_IO5	EXMC_NWE	EVENTOUT					
PC3	TIMER7_CH3_ON					OSPI_IO0	OSPI_IO6	EXMC_A0	EVENTOUT					
PC4	TIMER7_CH3		USART0_TX					EXMC_NE1	EVENTOUT					
PC5			USART0_RX	CAN2_RX	TIMER14_BRKIN	USART2_RX	OSPI_DQS	EXMC_NOE	EVENTOUT					
PC6	TIMER2_CH0	I2S1_MCK		TIMER7_CH0	USART5_TX	SDIO_D6	OSPI_IO5	EXMC_D1	EVENTOUT	SPI3_NSS				
PC7	TIMER2_CH1	I2S2_MCK		TIMER7_CH1	USART5_RX	SDIO_D7	OSPI_IO6		EVENTOUT	SPI3_SCK				
PC8	TIMER2_CH2		TIMER7_CH2		USART5_CK	SDIO_D0		EXMC_NE1	EVENTOUT	SPI3_MISO				
PC9	TIMER2_CH3		TIMER7_CH3	USART5_RTS/USART5_DE	UART4_TX	SDIO_D1	OSPI_IO0	EXMC_NADV	EVENTOUT	SPI3_MOSI			I2C2_SDA	
PC10	USART2_TX	UART3_TX	SPI2_SCK/I2S2_CK	TIMER7_CH0BRKIN		SDIO_D2	OSPI_IO1		EVENTOUT				I2C2_SCL	
PC11	USART2_RX	UART3_RX	SPI2_MISO	TIMER7_CH1BRKIN	I2S2_ADD_SD	SDIO_D3	OSPI_CSN0	EXMC_D2	EVENTOUT	OSPI_CSN1				
PC12	USART2_CK	UART4_TX	SPI2_MOSI/I2S2_SD	TIMER7_CH2BRKIN		SDIO_CK	TRIGSEL_IN2	EXMC_D3	EVENTOUT			TIMER40_MCH0		

PC13									EVENTOUT					
PC14									EVENTOUT					
PC15									EVENTOUT					

Table 2-7. Port D alternate functions summary

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13
PD0														
PD1														
PD2	TIMER2_ETI	UART4_RX			TIMER19_CH2BRKIN	SDIO_CMD			EVENTOUT		TIMER4_CH0	TIMER42_CH0		

3. Functional description

3.1. Arm® Cortex®-M33 core

The Cortex®-M33 processor is a 32-bit processor that possesses low interrupt latency and low-cost debug. The characteristics of integrated and advanced make the Cortex®-M33 processor suitable for market products that require microcontrollers with high performance and low power consumption. The Cortex®-M33 processor is based on the Armv8 architecture and supports a powerful and scalable instruction set including general data processing I/O control tasks, advanced data processing bit field manipulations and DSP. Some system peripherals listed below are also provided by Cortex®-M33:

- Internal Bus Matrix connected with Code bus, System bus, and Private Peripheral Bus (PPB) and debug accesses.
- Nested Vectored Interrupt Controller (NVIC).
- Breakpoint Unit (BPU).
- Data Watchpoint and Trace (DWT).
- Instrumentation Trace Macrocell (ITM).
- Serial Wire JTAG Debug Port (SWJ-DP).
- Trace Port Interface Unit (TPIU).
- Memory Protection Unit (MPU).
- Floating Point Unit (FPU).
- DSP Extension (DSP).
- Software Built-In Self Test (SBIST) controller

3.2. On-chip memory

- Up to 512KB of main flash memory for instruction and data.
- 0~5 waiting time within 512KB when CPU executes instructions.
- 80B option bytes block for user application requirements.
- Up to 192KB+4KB of SRAM.
- Supports 7-bit ECC function when reading and writing first 64KB SRAM0.

The Flash memory consists of up to 512 KB main Flash organized into 256 pages with 2 KB capacity per page and an 18 KB Information Block for the Boot Loader. The main Flash memory contains a total of up to 256 pages which can be erased individually. ***Table 2-2. GD32E53Pxx memory map*** shows the memory map of the GD32E53Pxx series of devices, including Flash, SRAM, peripheral, and other pre-defined regions.

3.3. Clock, reset and supply management

- External 4 to 32 MHz crystal oscillator.
- Internal 8 MHz RC oscillator.
- Internal 48 MHz RC oscillator.
- Internal 40 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator.
- Integrated system clock PLL.
- 1.71V to 3.6V application supply and I/Os.
- Power supply supervision: POR / PDR monitor / LVD monitor / OVD monitor / VOVD monitor / VAUVD monitor / VAOVD monitor / VUVD monitor.

The clock control unit provides a range of frequencies and clock functions. These include a Internal 8M RC oscillator (IRC8M), a Internal 48M RC oscillator (IRC48M), a High Speed crystal oscillator (HXTAL), a Low Speed Internal 40K RC oscillator (IRC40K), a Low Speed crystal oscillator (LXTAL), two Phase Lock Loop (PLLs), a HXTAL clock monitor, clock prescalers, clock multiplexers and clock gating circuitry.

The clocks of the AHB, APB and Cortex®-M33 are derived from the system clock (CK_SYS) which can source from the IRC8M, HXTAL or PLL0P. The maximum operating frequency of the system clock (CK_SYS) can be up to 252 MHz. See ***Figure 2-3. GD32E53Pxx clock tree*** for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components except for the SW-DP controller and the Backup domain. Power-on reset (POR) and power-down reset (PDR) are always active. The device remains in reset mode when VDD is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold.

Power supply schemes:

- V_{DD} range: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} range: external analog power supplies for ADC, DAC, CMP. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} range: power supply for RTC unit, LXTAL oscillator, BPOR and BREG, and three BKP PADs, BLDO, including PC13 to PC15.

Note: When the system clock frequency reaches or exceeds 252 MHz, the V_{DD} must be 3.0V or higher.

3.4. Boot modes

GD32E53Pxx supports three BOOT modes, including:

- Boot from main Flash memory (default).
- Boot from system memory.

■ Boot from on-chip SRAM.

The GD32E53x series provide three kinds of boot sources which can be selected by the BOOT0 pin and boot configuration bits BOOTLK, nBOOT1, SWBT0 and nBOOT0 in the User option byte. The details are shown in the following table ***Table 2-8. Boot modes***. When SWBT0=1, the value on the BOOT0 pin is latched on the 4th rising edge of CK_SYS after a reset. It is up to the user to set the boot mode configuration after a power-on reset or a system reset to select the required boot source. When SWBT0=1, once the boot mode configuration has been sampled, they are free and can be used for other purposes.

Table 2-8. Boot modes

Selected boot area	Boot mode configuration				
	BOOTLK	nBOOT1 bit	BOOT0 pin	SWBT0 bit	nBOOT0 bit
Main Flash memory	1	x	x	0	1
System memory	1	1	x	0	0
Embedded SRAM	1	0	x	0	0
Main Flash memory	1	x	0	1	x
System memory	1	1	1	1	x
Embedded SRAM	1	0	1	1	x
Main Flash memory	0	x	x	x	x

The boot loader is located in non-user system memory. It is used to reprogram the Flash memory by using USART0(PA9/PA10), USART1(PA2/PA3), USART2(PB10/PB15) and USBFS(PA11/PA12) in device mode. It also can be used to transfer and update the Flash memory code, the data and the vector table sections.

To ensure system reliability and stability, it is recommended not to connect peripherals that may generate interference signals (such as sensor outputs, watchdog chips, buttons, etc.) to the above-mentioned pins during the hardware design stage, in order to avoid affecting the normal function of the Bootloader and causing abnormal outputs to the connected peripherals.

Note: When booting from system memory, the USART RX pins (PA10/PA3/PB15) are in input level detection mode. Therefore, unused USART RX pins (PA10/PA3/PB15) need to be kept at a stable logic level to prevent false triggering.

Ability to use the BOOTLK bit to force boot from a unique entry point in the Main Flash memory regardless of others mode configuration.

3.5. Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are sleep mode, deep-sleep mode, deep-sleep 1 mode and standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep mode**

  In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt / event can wake up the system.

- **Deep-sleep mode**

  In deep-sleep mode, all clocks in the V_{CORE} domain are off, and all of the high speed crystal oscillator (IRC8M, IRC48M, HXTAL) and PLL are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the 16 external lines. When exiting the deep-sleep mode, the IRC8M is selected as the system clock.

- **Deep-sleep 1 mode**

  In Deep-sleep 1 mode, all clocks in the V_{CORE} domain are off, and all of IRC8M, IRC48M, HXTAL and PLLs are disabled. The power of COREOFF domain is cut off. The contents of registers in COREOFF domain are lost. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep 1 mode including the 16 external lines, waking up from Deep-sleep 1 mode needs an additional delay to power on COREOFF domain. When exiting the deep-sleep 1 mode, the IRC8M is selected as the system clock.

- **Standby mode**

  In standby mode, the whole V_{CORE} domain is power off, the LDO is shut down, and all of IRC8M, IRC48M, HXTAL and PLL are disabled. The contents of SRAM and registers (except backup registers) are lost. There are five wakeup sources for the standby mode, including the external reset from NRST pin, the rising edge on WKUP pins, the FWDGT reset, the RTC event and LXTAL clock monitor.

3.6. Instruction cache (ICACHE)

- Support 8KB cache with 2 ways, 256 cache lines per way and 16B per cache line
- Support fetch address without any wait state if cache hit
- ICACHE interface support two 32-bit slave ports and one 32-bit master port and one 128-bit master port. One slave port is execution port, the other one is for registers access. Master 0 port outputs to fast bus, while master 1 port outputs to slow bus.
- Cache access support hit-under-miss and paired master access feature
- Support memory address remap
- Support pLRU replacement policy and critical-word-first refill policy.
- Support remaps region AHB transaction burst type configuration.
- Support two performance counters: 32-bit hit monitor counter and16-bit miss monitor counter.
- Operation management: Cache invalidate and optional interrupt handle.

The instruction cache (ICACHE) is based on CBUS code bus of Cortex®-M33 processor. It is necessary to improve the performance in fetching instruction and data from both internal

and external memories.

3.7. Data cache (DCACHE)

- Support 4KB cache with 2 ways, 128 cache lines per way and 16B per cache line
- Support fetch address without any wait state if cache hit
- DCACHE interface support one 32-bit slave ports and one 32-bit master port and one 32-bit slave port. One slave port is execution port, the other one is for registers access. Master port outputs to bus.
- Cache access support hit-under-miss and paired master access feature
- Supprot forceable Write-Through policy
- Supports byte, half-word and word writes
- Support Pseudo-random replacement policy and critical-word-first refill policy.
- Error management and optional interrupt handle.
- Maintenance operations: Cache invalidate, Cache invalidate range, Cache clean range, Cache clean and invalidate range
- Support four performance counters: two hit monitor counters(32-bit), Count read hit and write hit events and two miss monitor counters(16-bit), Count read miss and write miss events.

Data Cache (DCACHE), as an essential component of the Cortex®-M33 processor's S-AHB system bus, aims to enhance the overall performance of external memory data transfers. DCACHE employs multiple advanced technologies, including hit/miss parallel processing mechanisms and a critical-word-first fill strategy, effectively improving the data access efficiency of external memory.

3.8. Clock trim controller (CTC)

- Two external reference signal sources: GPIO(CTC_SYNC), LXTAL clock.
- Provide software reference sync pulse.
- Automatically trimmed by hardware without any software action.
- 16 bits trim counter with reference signal source capture and reload.
- 8 bits clock trim base value to frequency evaluation and automatically trim.
- Enough flag or interrupt to indicate the clock is OK (CKOKIF), warning (CKWARNIF) or error (ERRIF).

The Clock Trim Controller (CTC) is used to trim internal 48MHz/8MHz RC oscillator (IRC48M/ IRC8M) automatically by hardware. The CTC unit trim the frequency of the IRC48M/ IRC8M based on an external accurate reference signal source. It can automatically adjust the trim value to provide a precise IRC48M/ IRC8M clock.

3.9. Trigger selection controller (TRIGSEL)

- Support up to 125 trigger input signals.
- Each peripheral has its corresponding register to select trigger input signal.
- TRIGSEL register can be configured up to 4 outputs to peripheral.
- Trigger input source could be external input signal or output of peripheral.
- Trigger selection output could be for external output or peripheral input.

The trigger selection controller (TRIGSEL) allows software to select the trigger input signal for various peripherals. TRIGSEL provides a flexible mechanism for a peripheral to select different trigger inputs. With TRIGSEL, there are up to 4 trigger selection outputs could be selected for each peripheral. And every output could be selected from different trigger input signal.

3.10. General-purpose and alternate-function I/Os (GPIO and AFIO)

- Up to 51 general purpose I/O pins (GPIO), all mappable on 16 external interrupt lines.
- Each pin weak pull-up / pull-down function.
- Output push-pull / open drain enable control.
- Analog input / output configuration.
- Alternate function input / output configuration.

GD32E53Pxx is up to 51 general purpose I/O pins (GPIO) for the device to implement logic input/output functions. Each GPIO port has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt / Event Controller Unit (EXTI).

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), input, peripheral alternate function or analog mode. Each GPIO pin can be configured as pull-up, pull-down or floating. All GPIOs are high-current capable except for analog mode.

3.11. Direct memory access controller (DMA)

- 12 channels (7 for DMA0 and 5 for DMA1) and each channel are configurable.
- Support independent 8, 16, 32-bit memory and peripheral transfer.
- Support independent fixed, increasing, decreasing and offset (only channel 0) address generation algorithm of memory and peripheral.
- Support channel preemption, when current channel is preempted, it is set as pending and will run the next time its priority is the highest.
- Support four transfer mode:
  - Single data element per request
  - One block transfer per request

  - Per link-list descriptor transfer per request
  - All link-list transfer per request
- Support repeat area access
- Peripherals supported: Timers, ADC, DAC, SPI, I2S, I2C, USART, UART, CAU, HAU.

The direct memory access (DMA) controller provides a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory.

There are 12 channels in the DMA controller (7 for DMA0 and 5 for DMA1). Each channel is dedicated to manage memory access requests from one or more peripherals. An arbiter is implemented inside to handle the priority among DMA requests.

3.12. DMA request multiplexer (DMAMUX)

- 12 channels for DMAMUX request multiplexer.
- 4 channels for DMAMUX request generator.
- Support 20 trigger inputs and 20 synchronization inputs.

DMAMUX is a transmission scheduler for DMA requests. The DMAMUX request multiplexer is used for routing a DMA request line between the peripherals / generated DMA request (from the DMAMUX request generator) and the DMA controller. Each DMAMUX request multiplexer channel selects a unique DMA request line, unconditionally or synchronously with events from its DMAMUX synchronization inputs. The DMA request is pending until it is served by the DMA controller which generates a DMA acknowledge signal (the DMA request signal is de-asserted).

3.13. CRC calculation unit (CRC)

- Supports 8 / 16 / 32bits data input.
- For 8 / 16 / 32 bit input data length, the calculation cycles are 1 / 2 / 4 AHB clock cycles.
- User configurable polynomial value and size (7 / 8 / 16 / 32 bits).
- Free 8-bit register is unrelated to calculation and can be used for any other goals by any other peripheral devices.

A cyclic redundancy checks (CRC) is an error-detecting code commonly used in digital networks and storage devices to detect accidental changes to raw data. The CRC calculation unit can be used to calculate 7 / 8 / 16 / 32 bit CRC code within user configurable polynomial.

3.14. True random number generator (TRNG)

- About 40 periods of TRNG_CLK are needed between two consecutive random numbers.
- 32-bit random value seed is generated from analog noise, so the random number is a

true random number.

The true random number generator (TRNG) module can generate a 32-bit random value by using continuous analog noise.

3.15. Hash Acceleration Unit (HAU)

- 32-bit AHB slave peripheral.
- High performance of computation of hash algorithms.
- Little-endian data representation.
- Multiple data types are supported, including no swapping, half-word swapping, byte swapping, and bit swapping with 32-bit data words.
- Automatic data padding to fill the 512-bit message block for digest computation.
- DMA transfer is supported.

The hash acceleration unit is used for information security. The secure hash algorithm (SHA-256) is supported for various applications. The digest will be computed and the length is 256 bits for a message up to (2^{64} - 1) bits computed by SHA-256 algorithm respectively.

3.16. Cryptographic Acceleration Unit (CAU)

- AES encryption/decryption algorithm is supported.
- DMA transfer for incoming and outgoing data is supported.
- Supports the ECB algorithm.
- Supports 128-bit, 192-bit and 256-bit keys.
- 8*32-bit input and output FIFO.
- Multiple data types are supported, including No swapping, Half-word swapping Byte swapping and Bit swapping.
- Data can be transferred by DMA, CPU during interrupts, or without both of them.

The cryptographic acceleration unit (CAU) is used to encipher and decipher data with AES (128, 192, or 256) algorithm. AES algorithms with different key sizes are supported to perform data encryption and decryption in the CAU in multiple modes. The CAU is a 32-bit peripheral, DMA transfer is supported and data can be accessed in the input and output FIFO.

3.17. Analog to digital converter (ADC)

- 12-bit, 10-bit, 8-bit or 6-bit configurable resolution for ADC.
- Programmable sampling time.
- DMA support.
- Up to 3 analog watchdogs.
- Oversampling ratio arbitrarily adjustable from 2x to 256x.
- Temperature sensor.

- Start-of-conversion can be initiated by software or TRIGSEL.

A 12-bit successive approximation analog-to-digital converter module (ADC) is integrated on the MCU chip. ADC0 has 16 external channels, 5 internal channel (temperature sensor VSENSE, internal reference voltage VREFINT, external battery power supply VBAT, positive reference voltage VREFP, negative reference voltage VREFN), ADC1 has 18 external channels, 3 internal channel (internal reference voltage VREFINT, positive reference voltage VREFP, negative reference voltage VREFN), ADC2 has 17 external channels, 4 internal channel (internal reference voltage VREFINT, negative reference voltage VREFN, positive reference voltage VREFP, negative reference voltage VREFN).

Analog watchdog allows the application to detect if the input voltages exceed the user-set high and low thresholds.

All ADC sampling channels support a variety of operation modes. After sampling and conversion, the conversion results can be stored in the corresponding data registers according to the least significant bit (LSB) alignment or the most significant bit (MSB) alignment.

An on-chip hardware oversample scheme improves performances and reduces the computational burden of MCU.

3.18. Digital to analog converter (DAC)

- 8-bit or 12-bit resolution.
- Left or right data alignment.
- DMA capability for each channel.
- Conversion update synchronously.
- Conversion triggered by external triggers.
- Configurable internal buffer.
- Extern voltage reference, VREFP.
- Noise wave generation (LFSR noise mode and triangle noise mode).
- Two DAC channels in concurrent mode.

The Digital-to-analog converter converts 12-bit digital data to a voltage on the external pins. The digital data can be configured to 8-bit or 12-bit mode, left-aligned or right-aligned mode. DMA can be used to update the digital data on external triggers. The output voltage can be optionally buffered for higher drive capability.

3.19. Comparator (CMP)

- Rail-to-rail comparators.
- Configurable hysteresis.
- Each comparator has configurable analog input source.
- Outputs with blanking source.

- Outputs to I/O.
- Outputs to timers for triggering.
- Outputs to EXTI.
- Outputs to NVIC.
- Outputs to TRIGSEL.

The general purpose CMP can work either standalone (all terminal are available on I/Os) or together with the timers.

It can be used to wake up the MCU from low-power mode by an analog signal, provide a trigger source when an analog signal is in a certain condition, achieve some current control by working together with a PWM output of a timer and the DAC. It blanking function can be used for false overcurrent detection in motor control applications.

3.20. Real time clock (RTC)

- Support calendar function, which can support year, month, date (day of month), day (day of week), hours, minutes, seconds and subseconds.
- Daylight saving compensation supported, which is realized through software.
- External high-accuracy low frequency (50Hz or 60Hz) clock can be used to achieve higher calendar accuracy through the reference clock detection option function.
- Atomic clock adjustment for calendar calibration performed by digital calibration function. Maximum adjustment accuracy is 0.95PPM for smooth digital calibration, 0.0625PPM for high-resolution calibration.
- Sub-second adjustment by shift function.
- Two separate Time-stamp function for saving event time.
- Two tamper sources can be chosen and tamper type is configurable (RTC_TAMP0 and RTC_TAMP1).
- Programmable calendar and two field maskable alarms.
- Maskable interrupt source.
- Thirty-two 32-bit (128 bytes total) universal backup registers which can keep data under power saving mode. Backup register will be reset if tamper event detected.

The RTC provides time that includes hours / minutes / seconds / sub-seconds and a calendar that includes year / month / day / weekday. The time and calendar are expressed in BCD code except for sub-seconds. Sub-seconds are expressed in binary code. Hour adjustment for daylight saving time. Working in power saving mode and smart wakeup are software configurable. Support improving calendar accuracy using external accurate low frequency clock.

3.21. Timers and PWM generation

- Three 16-bit Advanced timer (TIMER0, TIMER7, TIMER19), three 16-bit General-L0 timers (TIMER2, TIMER3, TIMER4), one 32-bit General-L0 timer (TIMER1), four 16-bit

General-L2 timer (TIMER9, TIMER10, TIMER12, TIMER13). six 16-bit General-L3 timer (TIMER14, TIMER40, TIMER41, TIMER42, TIMER43, TIMER44), four 16-bit Basic timer (TIMER5, TIMER6, TIMER50, TIMER51).

- Up to 4 independent channels of PWM, output compare or input capture for each general timer and external trigger input.
- 16-bit, motor control PWM advanced timer with programmable dead-time generation for output match.
- Decoder interface controller with two inputs using quadrature decoder and decoder modes.
- 24-bit SysTick timer down counter.
- 2 watchdog timers (free watchdog timer and window watchdog timer).

The advanced timer module (TIMER0/7/19) is a four-channel timer that supports both input capture and output compare. They can generate PWM signals to control motor or be used for power management applications. The advanced timer has a 16-bit counter that can be used as an unsigned counter. In addition, the advanced timers can be programmed and be used for counting, their external events can be used to drive other timers. Timer also includes a dead-time insertion module which is suitable for motor control applications. Timers are completely independent with each other, but they may be synchronized to provide a larger timer with their counter value increasing in unison.

The general level0 timer module (TIMER1/2/3/4) is a four-channel timer that supports input capture and output compare. They can generate PWM signals to control motor or be used for power management applications. The general level0 timer has a 16-bit or 32-bit counter that can be used as an unsigned counter. In addition, the general level0 timers can be programmed and be used for counting, their external events can be used to drive other timers. Timers are completely independent with each other, but they may be synchronized to provide a larger timer with their counter value increasing in unison.

The general level2 timer module (Timer9, 10, 12, 13) is a one-channel timer that supports input capture, output compare. They can generate PWM signals to be used for power management applications. The general level2 time reference is a 16-bit counter that can be used as an unsigned counter. In addition, the general level2 timers can be programmed and be used to count or time external events that drive other Timers.

The general level3 timer module (TIMER14/40/41/42/43/44) is a three-channel timer that supports both input capture and output compare. They can generate PWM signals to control motor or be used for power management applications. The general level3 timer has a 16-bit counter that can be used as an unsigned counter.

The basic timer module (TIMER5/6/50/51) has a 16-bit counter that can be used as an unsigned counter. The basic timer can be configured to generate a DMA request and a TRGO to connect to DAC.

The GD32E53Pxx has two watchdog peripherals, free watchdog timer and window watchdog timer. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-stage prescaler. It is clocked from an independent 40 KHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep, deep-sleep1 and standby modes.

The window watchdog timer is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. The window watchdog timer generates an early wakeup status flag when the counter reaches 0x40. Interrup occurs if it is enabled.

3.22. Universal synchronous/asynchronous receiver transmitter (USART/UART)

- Maximum speed up to 31.5 MBits/s for USART5 when the clock frequency is 252 MHz and oversampling is by 8.
- Maximum speed up to 31.5 MBits/s for USART0, USART1, USART2, UART3 and UART4 when the clock frequency CK_APB2 is 252MHz and oversampling is by 8.
- Supports both asynchronous and clocked synchronous serial communication modes.
- IrDA support.
- LIN break genUSATeration and detection.
- ISO 7816-3 compliant smartcard interface.
- Serial port TX can be configured as infrared modulation output, with adjustable modulation signal duty cycle and selectable modulation polarity (only supported by USART2).

The USART (USART0, USART1, USART2, USART5) and UART (UART3, UART4) are used to transfer data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART/UART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART/UART transmitter and receiver.

3.23. Inter-integrated circuit (I2C)

- Up to four I2C bus interfaces can support both master and slave mode with a frequency up to 1 MHz (Fast mode plus).
- Provide arbitration function, optional PEC (packet error checking) generation and checking.
- Supports 7-bit and 10-bit addressing mode and general call addressing mode.
- SMBus 3.0 and PMBus 1.3 compatible.

The I2C (inter-integrated circuit) module provides an I2C interface which is an industry standard two-line serial interface for MCU to communicate with external I2C interface. I2C bus uses two serial lines: a serial data line, SDA, and a serial clock line, SCL. The I2C

interface implements standard I2C protocol with standard mode (up to 100KHz), fast mode (up to 400KHz) and fast mode plus (up to 1MHz) as well as CRC calculation and checking, SMBus (system management bus), and PMBus (power management bus).

3.24. Controller area network (CAN)

- Supports CAN protocols version 2.0A, B.
- Supports CAN FD Frame with up to 64 data bytes (ISO11898-1 and Bosch CAN FD specification V1.0).
- Baud rates up to 1 Mbit/s when classical frames and 8 Mbit/s when FD frames.
- Supports transmitter delay compensation.
- Supports the time-triggered communication.
- Interrupt enable and clear.

CAN bus (Controller Area Network) is a bus standard designed to allow microcontrollers and devices to communicate with each other without a host computer.

The CAN network interfaces of this series supports the CAN protocol 2.0A and B, ISO11898-1:2015 and BOSCH CAN-FD specifications. The CAN interface automatically handles the transmission and the reception of CAN frames. The CAN0 and CAN1 provides 28 scalable/configurable identifier filter banks. The CAN2 independently provides 14 scalable/configurable identifier filter banks. Three transmit mailboxes are provided to the software for transfer messages. The transmission scheduler decides which mailbox will be transmitted firstly. Three complete messages can be stored in every FIFO. The FIFOs are managed completely by hardware. Two receiving FIFOs are used by hardware to store the incoming messages. In addition, the CAN controller provides all hardware functions, which supports the time-triggered communication option, in safety-critical applications.

3.25. Serial peripheral interface (SPI)

- Master or slave operation with full-duplex or simplex mode.
- Separate transmit and receive buffer, 16 bits wide.
- Data frame size can be 8 or 16 bits.
- Hardware CRC calculation, transmission and checking.
- SPI TI mode supported.
- SPI NSS pulse mode supported.
- Quad-SPI configuration available in master mode (only in SPI0 and SPI3).

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). All SPIs can be served by the DMA controller. The serial peripheral interface (SPI) provides a SPI protocol of data transmission and reception function in master or slave mode. Both full-duplex and simplex communication modes are supported, with hardware CRC calculation and checking. Quad-SPI master mode is also supported in SPI0 and SPI3.

3.26. Inter-IC sound (I2S)

- Master or slave operation with transmission or reception mode
- Master or slave operation with full-duplex mode (only in SPI1 and SPI2)
- Four I2S standards supported: Philips, MSB justified, LSB justified and PCM standard
- Data length can be 16 bits, 24 bits or 32 bits
- Channel length can be 16 bits or 32 bits
- Transmission and reception using a 16 bits wide buffer
- Audio sample frequency can be 8 kHz to 192 kHz using I2S clock divider
- Programmable idle state clock polarity
- Master clock (MCK) can be output
- Transmission and reception using DMA

The inter-IC sound (I2S) supports four audio standards: I2S Philips standard, MSB justified standard, LSB justified standard, and PCM standard. I2S works at either master or slave mode for transmission and reception. The audio sampling frequencies from 8 KHz to 192 KHz is supported.

3.27. Octal-SPI interface(OSPI)

- Three functional modes: indirect mode, status polling mode, memory-mapped mode
- Support read and write in memory-mapped mode.
- Support single, dual, quad, dual CSN and octal communication.
- Support data strobe support (DQS).
- Fully programmable command format for both indirect and memory-mapped mode.
- Support SDR (single data rate) and DTR (double transfer rate).
- Support two frame format:
  - the standard frame format.
  - HyperBus™ frame format.
- Support wrap for both standard frame format and HyperBus™ frame format.
- Integrated FIFO for transmission/reception.
- 8, 16 and 32-bits data access.
- DMA channel for indirect mode.
- Interrupt generation on FIFO threshold, status match, timeout, transfer complete and access error.

The OSPI is a specialized interface that communicate with external memories such as serial PSRAMS, serial NAND, serial NOR Flash, HyperRAMTM and HypterFlashTM memories. The interface supports single, dual, quad, dual CSN and octal SPI mode.

3.28. Secure digital input/output interface (SDIO)

- MMC: Full support for Multimedia Card System Specification Version 4.2(and previous versions) Card and three different data bus modes: 1-bit (default), 4-bit and 8-bit.
- SD Card: Full support for SD Memory Card Specifications Version 2.0.
- SD I/O: Full support for SD I/O Card Specification Version 2.0 card and two different data bus modes: 1-bit (default) and 4-bit.
- CE-ATA: Full compliance with CE-ATA digital protocol Version 1.1.
- 48MHz data transfer frequency and 8-bit data transfer mode.
- Interrupt and DMA request to processor.
- Completion Signal enables and disable feature (CE-ATA).

The secure digital input/output interface (SDIO) defines the SD, SD I/O, MMC and CE-ATA card host interface, which provides command/data transfer between the APB2 system bus and SD memory cards, SD I/O cards, Multimedia Card (MMC) and CE-ATA devices.

3.29. External memory controller (EXMC)

- Supported external memory: PSRAM, NOR Flash and 8-bit or 16-bit NAND Flash.
- Each bank has its own chip-select signal which can be configured independently.
- 8 or 16 bits bus width.
- Embedded ECC hardware for NAND Flash access.

The external memory controller EXMC, is used as a translator for MCU to access a variety of external memory. By configuring the related registers, it can automatically convert AMBA memory access protocol into a specific memory access protocol, such as PSRAM, NOR Flash, NAND Flash. Users can also adjust the timing parameters in the configuration registers to improve memory access efficiency. EXMC access space is divided into multiple banks; each bank is assigned to access a specific memory type with flexible parameter configuration as defined in the control registers.

3.30. Universal serial bus full-speed interface (USBFS)

- Supports USB 2.0 host mode at Full-Speed(12Mb/s) or Low-Speed(1.5Mb/s)
- Supports USB 2.0 device mode at Full-Speed(12Mb/s)

USB Full-Speed (USBFS) controller provides a USB-connection solution for portable devices. USBFS supports host and device modes. USBFS contains a full-speed internal USB PHY and external PHY chip is not contained. USBFS supports all the four types of transfer (control, bulk, Interrupt and isochronous) which defined in USB 2.0 protocol.

3.31. Debug mode

- Serial wire JTAG debug port (SWJ-DP).

The GD32E53Pxx series provide a large variety of debug, trace and test features. They are implemented with a standard configuration of the Arm® CoreSight™ module together with a daisy chained standard TAP controller. Debug and trace functions are integrated into the Arm® Cortex®-M33. The debug system supports serial wire debug (SWD) and trace functions in addition to standard JTAG debug.

3.32. Package and operation temperature

- LQFP64 (GD32E53PRx).
- Operation temperature range: -40°C to +85°C (industrial level).

4. Electrical characteristics

4.1. Parameter introduction

- Parameter conditions: Unless otherwise specified, all values given for V_{DD} = V_{DDA} = 3.3 V, T_A = 25°C, and all voltages are referenced to Vss.
- Value guaranteed by design, not 100% tested in production indicates that the value is derived from design or simulation and/or process characteristics.
- Value guaranteed by characterization, not 100% tested in production indicates that the value is derived from comprehensive evaluation after random test.
- Value guaranteed by sample, not 100% tested in production indicates that the value is derived from testing parameters with a small sample size.
- Guaranteed by characterization, the minimum and maximum values refer to random tests and represent the mean value plus or minus three times the standard deviation (mean +/-3σ).
- If the value is not specially indicated, it means the value guaranteed by 100% tested in production.

See the following table for some abbreviation terms and their descriptions in this chapter.

Table 4-1. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
CAN	Controller Area Network
DAC	Digital-to-Analog Converter
DMA	Direct Memory Access
GPIO	General Purpose Input / Output
JTAG	Joint Test Action Group
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
USB	Universal Serial Bus
SPI	Serial Peripheral Interface

4.2. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly over the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-2. Absolute maximum ratings(1)(4)

Symbol	Parameter	Min	Max	Unit
V_{DD}	External voltage range(2)	V_{SS} - 0.3	V_{SS} + 4.0	V
V_{DDA}	External analog supply voltage	V_{SSA} - 0.3	V_{SSA} + 4.0	V
V_{BAT}	External battery supply voltage	V_{SS} - 0.3	V_{SS} + 4.0	V
V_{IN}	Input voltage on 5V tolerant pin(3)	V_{SS} - 0.3	V_{DD} + 4.0	V
	Input voltage on other I/O	V_{SS} - 0.3	4.0	V
$\|\Delta V_{DDx}\|$	Variations between different VDD power pins	-	50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between different ground pins	-	50	mV
I_{IO}	Maximum current for each GPIO pin	-	±25	mA
$\sum I_{IO}$	Maximum current sunk/sourced by all GPIO pins	-	±100	mA
I_{DD}	Maximum current into each VDD pin	-	100	mA
$\sum I_{DD}$	Total current into all VDD pins	-	200	mA
I_{SS}	Maximum current into each V_{SS} pin	-	100	mA
$\sum I_{SS}$	Total current into all VSS pins	-	200	mA
I_{INJ}	Injected current on each GPIO pin(5)	—	-5/0	I_{INJ}
$\sum I_{INJ}$	Total injected current on all GPIO pins(6)	—	±25	$\sum I_{INJ}$
T_{STG}	Storage temperature range	-65	150	°C
T_J	Maximum junction temperature	-	125	°C

(1) Guaranteed by design, not tested in production.

(2) All main power and ground pins should be connected to an external power source within the allowable range.

(3) V_{IN} maximum value cannot exceed 5.5 V.

(4) It is recommended that V_{DD} and V_{DDA} are powered by the same source. The maximum difference between V_{DD} and V_{DDA} does not exceed 300 mV during power-up and operation.

4.3. General operating conditions

Table 4-3. DC operating conditions(1)(2)

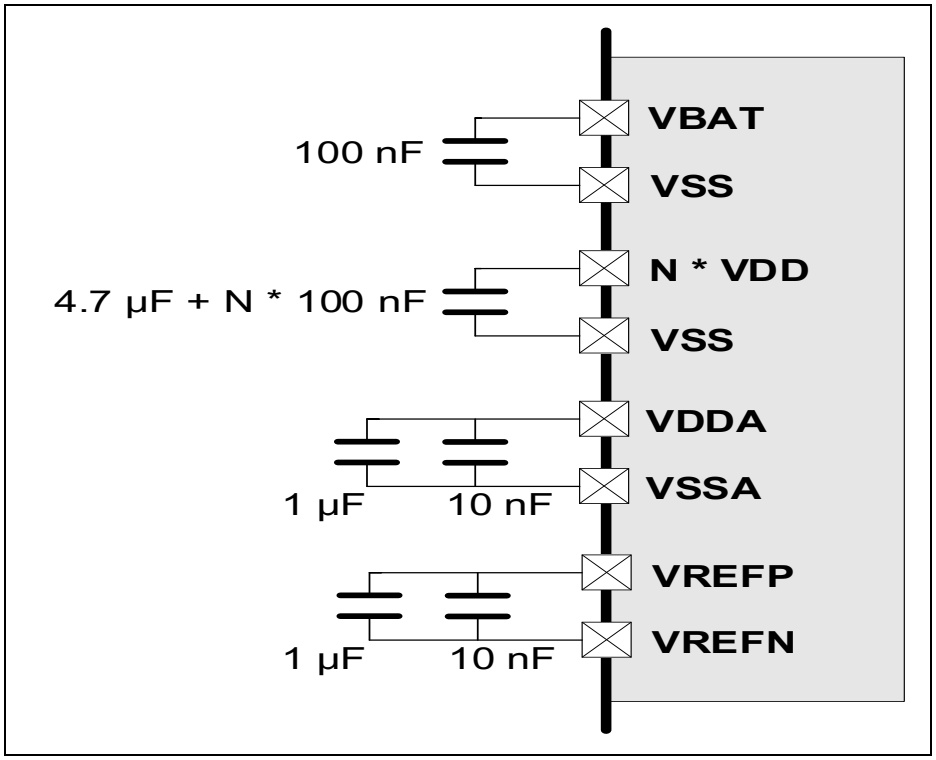
Symbol	Parameter	Conditions	Min(1)	Typ	Max	Unit
V_{DD}	Supply voltage	-	1.71	3.3	3.6	V
V_{DDA}	Analog supply voltage, f_{ADCMAX} = 42 MHz	-	2.4	3.3	3.6	V
	Analog supply voltage, f_{ADCMAX} = 14 MHz		1.71	-	3.6	
V_{BAT}	Battery supply voltage	-	1.62	-	3.6	V
V_{CORE}	Core logic supply voltage powered by internal voltage regulator	-	-	1.2	-	V
f_{HCLK}	AHB2 clock frequency	V_{CORE} = 1.2V	-	-	252	MHz
		V_{CORE} = 1.1V	-	-	TBD	
f_{APB1}	APB1 clock frequency	V_{CORE} = 1.2V	-	-	126	MHz
		V_{CORE} = 1.1V	-	-	TBD	
f_{APB2}	APB2 clock frequency	V_{CORE} = 1.2V	-	-	252	MHz
		V_{CORE} = 1.1V	-	-	TBD	
P_D	Power dissipation at T_A = 85°C of LQFP64	-	-	-	826	mW
T_A	Ambient temperature	-	-40	-	85	°C
T_J(3)	Junction temperature	-	-40	-	125	°C

(1) Guaranteed by design, not tested in production.

(2) It is recommended that V_{DD} and V_{DDA} are powered by the same source. The maximum difference between V_{DD} and V_{DDA} does not exceed 300 mV during power-up and operation.

(3) The device junction temperature must be kept below maximum T_J, otherwise it may cause permanent damage to the device.

Figure 4-1. Recommended power supply decoupling capacitors(1)(2)



(1) The VREFP and VREFN pins are only available on no less than 100-pin packages, or else the VREFP and VREFN pins are not available and internally connected to VDDA and VSSA pins.

(2) All decoupling capacitors need to be as close as possible to the pins on the PCB board.

4.4. Power supply requirement characteristics

Table 4-4. Power supply requirement characteristics (1)

Symbol	Description	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	-	µs/V
	V_{DD} fall time rate		20	-	
t_{VDDA}	V_{DDA} rise time rate	-	0	-	µs/V
	V_{DDA} fall time rate		20	-	

(1) Value guaranteed by design, not 100% tested in production.

4.5. Power supply supervisor characteristics

Table 4-5. Power supply supervisor characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{LVD}	V_{DD} under voltage detector level selection	LVDT<3:0> = 0000(rising edge)	1.75	1.8	1.85	V
		LVDT<3:0> = 0000(falling edge)	1.65	1.7	1.75	
		LVDT<3:0> = 0001(rising edge)	1.85	1.9	1.95	

Symbol	Description	Conditions	Min	Typ	Max	Unit
		LVDT<3:0> = 0001(falling edge)	1.75	1.8	1.85	
		LVDT<3:0> = 0010(rising edge)	1.95	2.0	2.05	
		LVDT<3:0> = 0010(falling edge)	1.85	1.9	1.95	
		LVDT<3:0> = 0011(rising edge)	2.05	2.1	2.15	
		LVDT<3:0> = 0011(falling edge)	1.95	2.0	2.05	
		LVDT<3:0> = 0100(rising edge)	2.15	2.2	2.25	
		LVDT<3:0> = 0100(falling edge)	2.05	2.1	2.15	
		LVDT<3:0> = 0101(rising edge)	2.25	2.3	2.35	
		LVDT<3:0> = 0101(falling edge)	2.15	2.2	2.25	
		LVDT<3:0> = 0110(rising edge)	2.35	2.4	2.45	
		LVDT<3:0> = 0110(falling edge)	2.25	2.3	2.35	
		LVDT<3:0> = 0111(rising edge)	2.42	2.5	2.58	
		LVDT<3:0> = 0111(falling edge)	2.32	2.4	2.48	
		LVDT<3:0> = 1000(rising edge)	2.52	2.6	2.68	
		LVDT<3:0> = 1000(falling edge)	2.42	2.5	2.58	
		LVDT<3:0> = 1001(rising edge)	2.62	2.7	2.78	
		LVDT<3:0> = 1001(falling edge)	2.52	2.6	2.68	
		LVDT<3:0> = 1010(rising edge)	2.72	2.8	2.88	
		LVDT<3:0> = 1010(falling edge)	2.62	2.7	2.78	
		LVDT<3:0> = 1011(rising edge)	2.82	2.9	2.98	
		LVDT<3:0> = 1011(falling edge)	2.72	2.8	2.88	
		LVDT<3:0> = 1100(rising edge)	2.92	3.0	3.08	
		LVDT<3:0> = 1100(falling edge)	2.82	2.9	2.98	
		LVDT<3:0> = 1101(rising edge)	3.02	3.1	3.18	
		LVDT<3:0> = 1101(falling edge)	2.92	3.0	3.08	
		LVDT<3:0> = 1110(rising edge)	3.12	3.2	3.28	
		LVDT<3:0> = 1110(falling edge)	3.02	3.1	3.18	
		LVDT<3:0> = 1111(rising edge)	3.22	3.3	3.38	

Symbol	Description	Conditions	Min	Typ	Max	Unit
		LVDT<3:0> = 1111(falling edge)	3.12	3.2	3.28	
$V_{HYST(LVD)}$	LVD hysteresis	-	-	100	-	mV
V_{OVD}	V_{DD} overvoltage detector level selection	OVDT<1:0> = 00(rising edge)	3.57	3.65	3.73	V
		OVDT<1:0> = 00(falling edge)	3.47	3.55	3.63	
		OVDT<1:0> = 01(rising edge)	3.67	3.75	3.83	
		OVDT<1:0> = 01(falling edge)	3.57	3.65	3.73	
		OVDT<1:0> = 10(rising edge)	3.77	3.85	3.93	
		OVDT<1:0> = 10(falling edge)	3.67	3.75	3.83	
		OVDT<1:0> = 11(rising edge)	3.87	3.95	4.03	
		OVDT<1:0> = 11(falling edge)	3.77	3.85	3.93	
$V_{HYST(OVD)}$	OVD hysteresis	-	-	100	-	mV
V_{POR}(2)	Power on reset threshold	-	TBD	TBD	TBD	V
V_{PDR}(2)	Power down reset threshold	-	TBD	TBD	TBD	V
$V_{HYST(POR_PDR)}$	Hysteresis of POR and PDR	-	-	100	-	mV
$t_{RST(TEMPO)}$	Power on reset temporization	-	-	2.5	-	ms
V_{BOR8}(2)	Brownout level 8 threshold	Falling edge	TBD	TBD	TBD	V
		Rising edge	TBD	TBD	TBD	
V_{BOR7}(2)	Brownout level 7 threshold	Falling edge	TBD	TBD	TBD	V
		Rising edge	TBD	TBD	TBD	
V_{BOR6}(2)	Brownout level 6 threshold	Falling edge	TBD	TBD	TBD	V
		Rising edge	TBD	TBD	TBD	
V_{BOR5}(2)	Brownout level 5 threshold	Falling edge	TBD	TBD	TBD	V
		Rising edge	TBD	TBD	TBD	
V_{BOR4}(2)	Brownout level 4 threshold	Falling edge	TBD	TBD	TBD	V
		Rising edge	TBD	TBD	TBD	
V_{BOR3}(2)	Brownout level 3 threshold	Falling edge	TBD	TBD	TBD	V
		Rising edge	TBD	TBD	TBD	
V_{BOR2}(2)	Brownout level 2 threshold	Falling edge	TBD	TBD	TBD	V
		Rising edge	TBD	TBD	TBD	
V_{BOR1}(2)	Brownout level 1 threshold	Falling edge	TBD	TBD	TBD	V
		Rising edge	TBD	TBD	TBD	
$V_{HYST(BOR)}$	BOR hysteresis	-	-	TBD	-	mV

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{AUVD}	V_{DDA} under voltage detector level selection	VAUVDVC[3:0] = 0000 (rising edge)	1.75	1.8	1.85	
		VAUVDVC[3:0] = 0000 (falling edge)	1.65	1.7	1.75	
		VAUVDVC[3:0] = 0001 (rising edge)	1.85	1.9	1.95	
		VAUVDVC[3:0] = 0001 (falling edge)	1.75	1.8	1.85	
		VAUVDVC[3:0] = 0010 (rising edge)	1.95	2.0	2.05	
		VAUVDVC[3:0] = 0010 (falling edge)	1.85	1.9	1.95	
		VAUVDVC[3:0] = 0011 (rising edge)	2.05	2.1	2.15	
		VAUVDVC[3:0] = 0011 (falling edge)	1.95	2.0	2.05	
		VAUVDVC[3:0] = 0100 (rising edge)	2.15	2.2	2.25	
		VAUVDVC[3:0] = 0100 (falling edge)	2.05	2.1	2.15	
		VAUVDVC[3:0] = 0101 (rising edge)	2.25	2.3	2.35	
		VAUVDVC[3:0] = 0101 (falling edge)	2.15	2.2	2.25	
		VAUVDVC[3:0] = 0110 (rising edge)	2.35	2.4	2.45	
		VAUVDVC[3:0] = 0110 (falling edge)	2.25	2.3	2.35	
		VAUVDVC[3:0] = 0111 (rising edge)	2.42	2.5	2.58	
		VAUVDVC[3:0] = 0111 (falling edge)	2.32	2.4	2.48	
		VAUVDVC[3:0] = 1000 (rising edge)	2.52	2.6	2.68	
		VAUVDVC[3:0] = 1000 (falling edge)	2.42	2.5	2.58	
		VAUVDVC[3:0] = 1001 (rising edge)	2.62	2.7	2.78	
		VAUVDVC[3:0] = 1001 (falling edge)	2.52	2.6	2.68	
		VAUVDVC[3:0] = 1010 (rising edge)	2.72	2.8	2.88	

Symbol	Description	Conditions	Min	Typ	Max	Unit
		VAUVDVC[3:0] = 1010 (falling edge)	2.62	2.7	2.78	
		VAUVDVC[3:0] = 1011 (rising edge)	2.82	2.9	2.98	
		VAUVDVC[3:0] = 1011 (falling edge)	2.72	2.8	2.88	
		VAUVDVC[3:0] = 1100 (rising edge)	2.92	3.0	3.08	
		VAUVDVC[3:0] = 1100 (falling edge)	2.82	2.9	2.98	
		VAUVDVC[3:0] = 1101 (rising edge)	3.02	3.1	3.18	
		VAUVDVC[3:0] = 1101 (falling edge)	2.92	3.0	3.08	
		VAUVDVC[3:0] = 1110 (rising edge)	3.12	3.2	3.28	
		VAUVDVC[3:0] = 1110 (falling edge)	3.02	3.1	3.18	
		VAUVDVC[3:0] = 1111 (rising edge)	3.22	3.3	3.38	
		VAUVDVC[3:0] = 1111 (falling edge)	3.12	3.2	3.28	
$V_{HYST(AUVD)}$	Hysteresis of V_{DDA} under voltage detector	-	-	100	-	mV
V_{AOVD}	V_{DDA} overvoltage detector level selection	VAOVDVC<1:0> = 00 (rising edge)	3.57	3.65	3.73	V
		VAOVDVC <1:0> = 00 (falling edge)	3.47	3.55	3.63	
		VAOVDVC <1:0> = 01 (rising edge)	3.67	3.75	3.83	
		VAOVDVC <1:0> = 01 (falling edge)	3.57	3.65	3.73	
		VAOVDVC <1:0> = 10 (rising edge)	3.77	3.85	3.93	
		VAOVDVC <1:0> = 10 (falling edge)	3.67	3.75	3.83	
		VAOVDVC <1:0> = 11 (rising edge)	3.87	3.95	4.03	
		VAOVDVC <1:0> = 11 (falling edge)	3.77	3.85	3.93	
$V_{HYST(AOVD)}$	Hysteresis of V_{DDA} overvoltage detector	-	-	100	-	mV

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{VOVD}	V_{CORE} overvoltage level selection	VOVDVC[1:0] = 00(rising edge)	1.22	1.25	1.28	V
		VOVDVC[1:0] = 00(falling edge)	1.195	1.225	1.255	
		VOVDVC[1:0] = 01(rising edge)	1.27	1.3	1.33	
		VOVDVC[1:0] = 01(falling edge)	1.245	1.275	1.305	
		VOVDVC[1:0] = 10(rising edge)	1.32	1.35	1.38	
		VOVDVC[1:0] = 10(falling edge)	1.295	1.325	1.355	
		VOVDVC[1:0] = 11(rising edge)	1.37	1.4	1.43	
		VOVDVC[1:0] = 11(falling edge)	1.345	1.375	1.405	
$V_{HYST(VOVD)}$	Hysteresis of V_{CORE} overvoltage detector	-	-	25	-	mV
V_{VUVD}	V_{CORE} under voltage level selection	VUVDVC[1:0] = 00(rising edge)	1.045	1.075	1.105	V
		VUVDVC[1:0] = 00(falling edge)	1.02	1.05	1.08	
		VUVDVC[1:0] = 01(rising edge)	0.945	0.975	1.005	
		VUVDVC[1:0] = 01(falling edge)	0.92	0.95	0.98	
		VUVDVC[1:0] = 1x(rising edge)	0.845	0.875	0.905	
		VUVDVC[1:0] = 1x(falling edge)	0.82	0.85	0.88	
$V_{HYST(VUVD)}$	Hysteresis of V_{CORE} under voltage detector	-	-	25	-	mV
V_{DD_EF}	V_{DD_EF} under voltage detector level selection	BOREF_TH<2:0> = 000 (rising edge)	-	1.61	-	V
		BOREF_TH<2:0> = 000 (falling edge)	-	1.57	-	
		BOREF_TH<2:0> = 001 (rising edge)	-	1.66	-	
		BOREF_TH<2:0> = 001 (falling edge)	-	1.62	-	
		BOREF_TH<2:0> = 010 (rising edge)	-	1.71	-	
		BOREF_TH<2:0> = 010 (falling edge)	-	1.67	-	
		BOREF_TH<2:0> = 011 (rising edge)	-	1.76	-	
		BOREF_TH<2:0> = 011 (falling edge)	-	1.72	-	
		BOREF_TH<2:0> = 100	-	1.81	-	

Symbol	Description	Conditions	Min	Typ	Max	Unit
		(rising edge)				
		BOREF_TH<2:0> = 100 (falling edge)	-	1.77	-	
		BOREF_TH<2:0> = 101 / 110 / 111(rising edge)	-	1.86	-	
		BOREF_TH<2:0> = 101 / 110 / 111(falling edge)	-	1.82	-	
$V_{HYST(BOREF)}$	Hysteresis of V_{DD_EF} under voltage detector	-	-	40	-	mV
I_{BOR}	BOR power consumption	$V_{DD} = V_{DDA} = 3.3$ V	-	1.5	-	μA
I_{LVD}	LVD power consumption	$V_{DD} = V_{DDA} = 3.3$ V	-	13	-	μA
I_{OVD}	OVD power consumption	$V_{DD} = V_{DDA} = 3.3$ V	-	13	-	μA
I_{AOVD}	AOVD power consumption	$V_{DD} = V_{DDA} = 3.3$ V	-	13	-	μA
I_{AUVD}	AUVD power consumption	$V_{DD} = V_{DDA} = 3.3$ V	-	13	-	μA
I_{VOVD}	VOVD power consumption	$V_{DD} = V_{DDA} = 3.3$ V	-	4	-	μA
I_{VUVD}	VUVD power consumption	$V_{DD} = V_{DDA} = 3.3$ V	-	4	-	μA
I_{BOREF}	BOREF power consumption	$V_{DD} = V_{DDA} = 3.3$ V	-	5	-	μA

(1) Value guaranteed by design, not 100% tested in production.

(2) Value guaranteed characterization, not 100% tested in production.

Figure 4-2. POR / PDR waveform

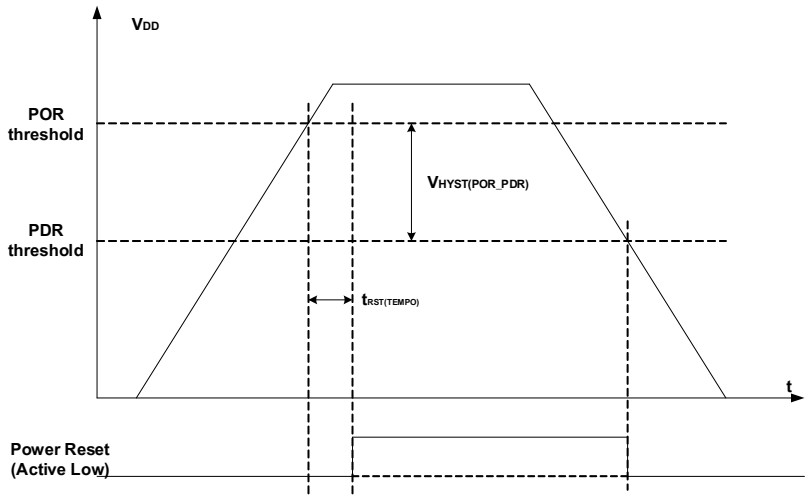


Figure 4-3. BOR waveform (Ignore POR / PDR)

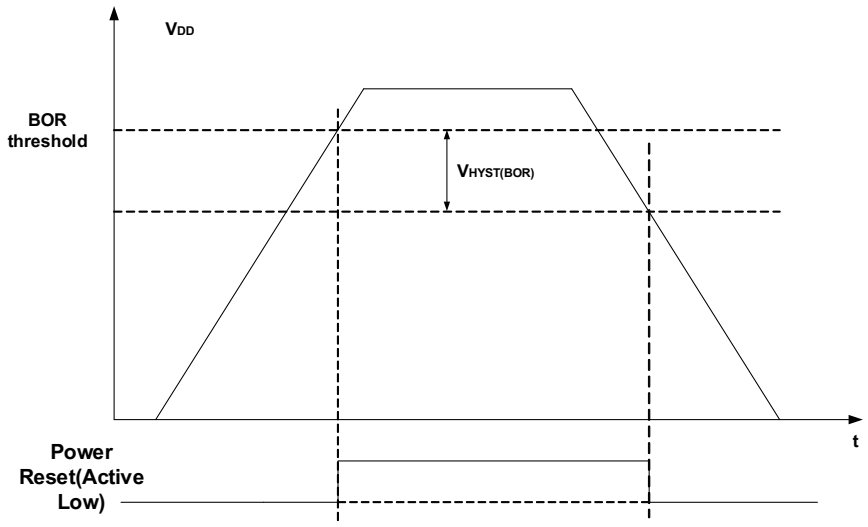


Figure 4-4. LVD threshold waveform

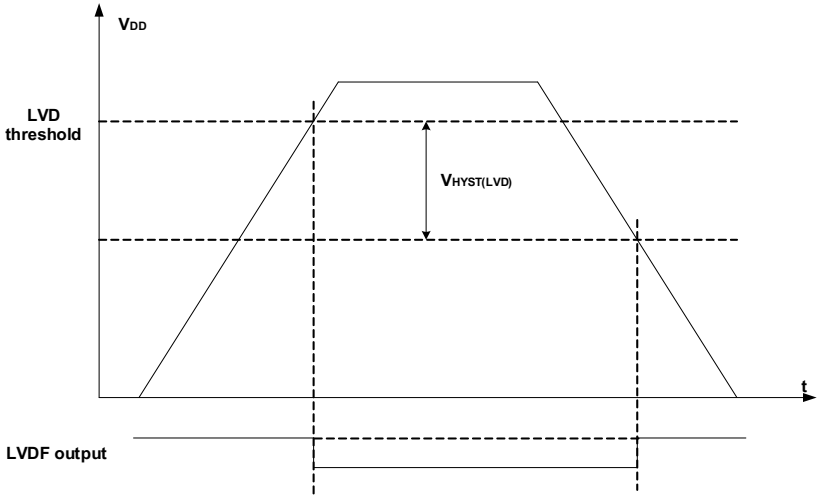


Figure 4-5. OVD threshold waveform

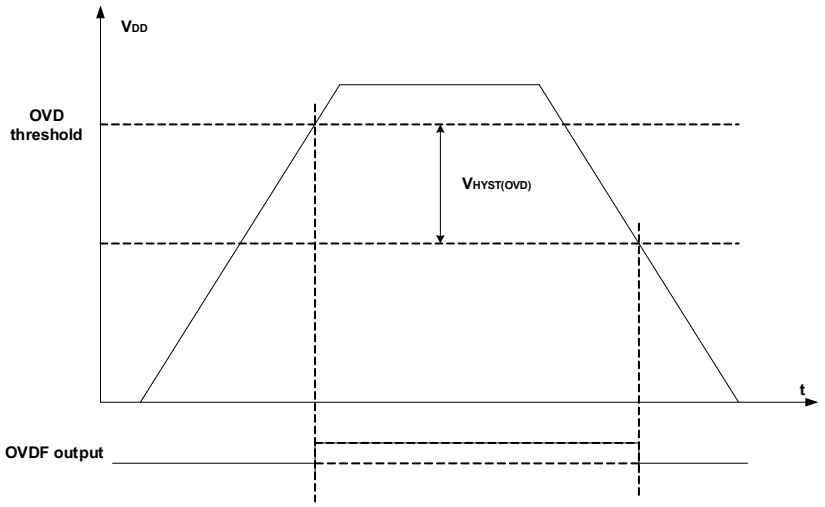


Figure 4-6. AOVD threshold waveform

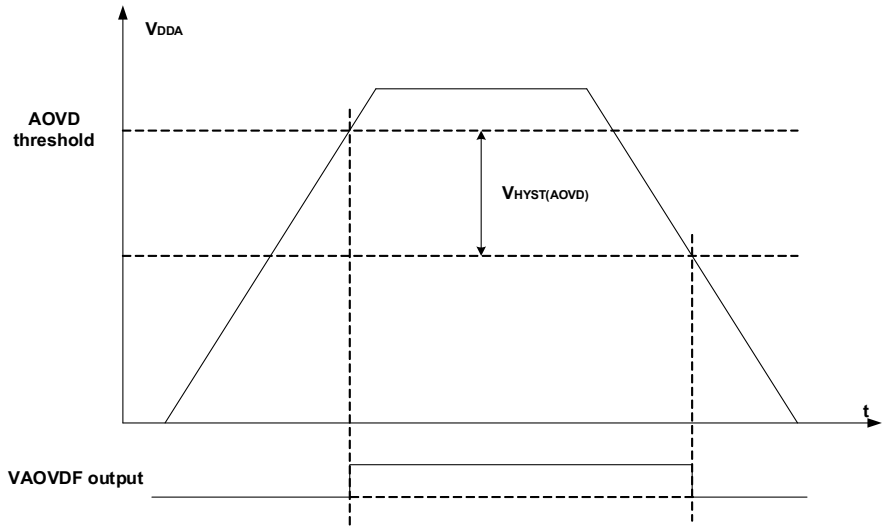


Figure 4-7. AUVD threshold waveform

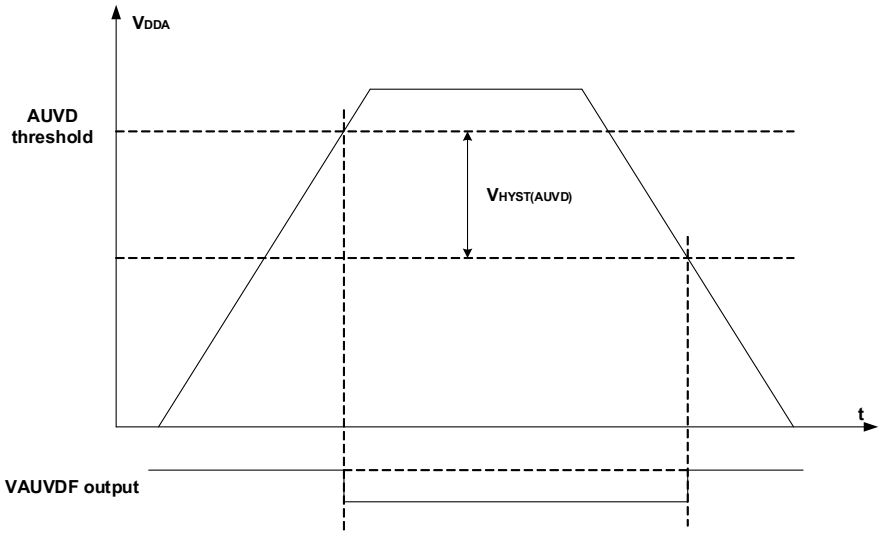


Figure 4-8. VUVD threshold waveform

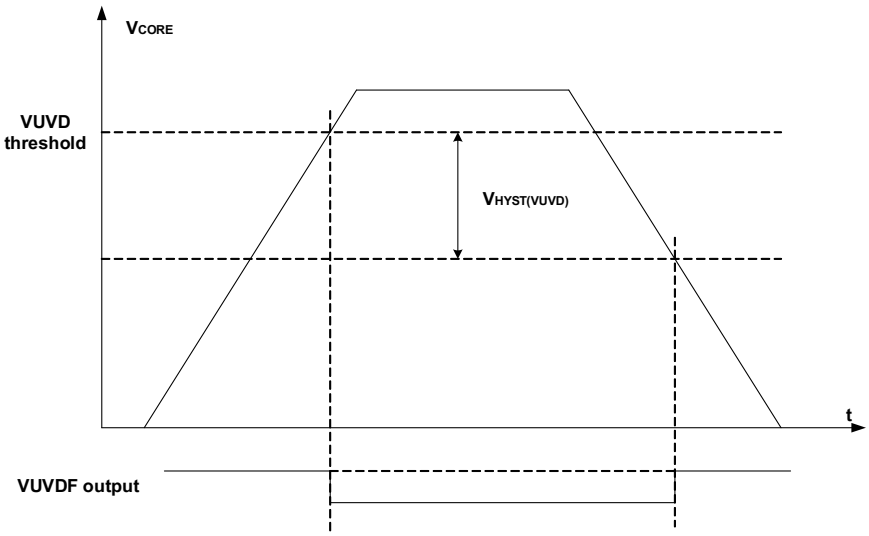


Figure 4-9. VOVD threshold waveform

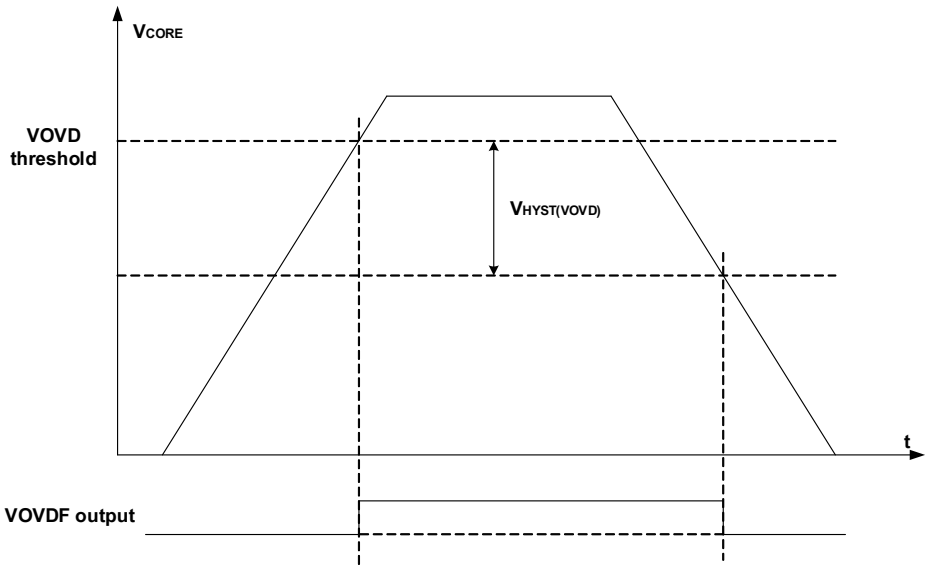
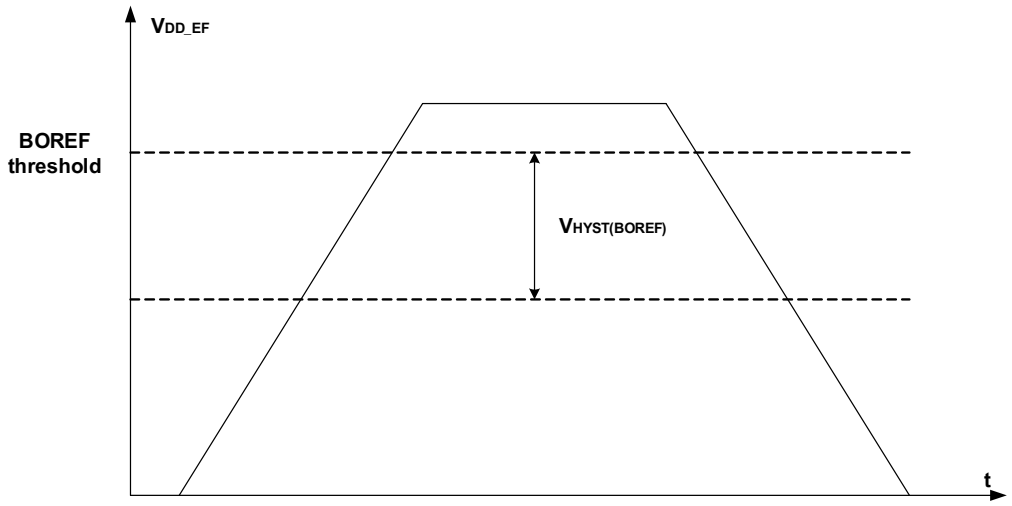


Figure 4-10. BOREF threshold waveform(1)



(1) The BOREF has no flag bit. When the V_{DD_EF} voltage is insufficient to support normal eflash operation, internal erase / write protection is directly activated without outputting any external indication signal. Erase / write operations automatically resume once the V_{DD_EF} voltage recovers to levels supporting proper eflash functionality.

4.6. Start-up timing

Table 4-6. Start-up timings of Operating conditions(1)(2)(3)(4)

Symbol	Description	Conditions	Typ	Max	Unit
t_{ST}	Start-up time	Clock source from IRCxxM	TBD	TBD	μs

(1) Value guaranteed by characterization, not 100% tested in production.

(2) After power-up, the start-up time is the time between the rising edge of NRST high and the first I/O instruction conversion in SystemInit function.

(3) PLL is off.
(4) V_{DD} = V_{DDA} = 3.3 V

4.7. Wake-up timing

Table 4-7. Power saving mode wakeup timings characteristics(1)(2)

Symbol	Description	Conditions	Typ	Max	Unit
t_{Sleep}	Wakeup from Sleep mode	V_{CORE} = 1.1 V	TBD	TBD	μs
		V_{CORE} = 1.2 V	TBD	TBD	
$t_{Deep-sleep}$	Wakeup from Deep-sleep mode (LDO in normal power)	V_{CORE} = 0.85 V	TBD	TBD	
		V_{CORE} = 1.0 V	TBD	TBD	
		V_{CORE} = 1.1 V	TBD	TBD	
		V_{CORE} = 1.2 V	TBD	TBD	
	Wakeup from Deep-sleep mode (LDO in low power mode)	V_{CORE} = 0.85 V	TBD	TBD	
		V_{CORE} = 1.0 V	TBD	TBD	
		V_{CORE} = 1.1 V	TBD	TBD	
		V_{CORE} = 1.2 V	TBD	TBD	
$t_{Deep-sleep\ 1}$	Wakeup from Deep-sleep 1 mode (LDO in normal power)	V_{CORE} = 0.85 V	TBD	TBD	
		V_{CORE} = 1.0 V	TBD	TBD	
		V_{CORE} = 1.1 V	TBD	TBD	
		V_{CORE} = 1.2 V	TBD	TBD	
	Wakeup from Deep-sleep 1 mode (LDO in low power mode)	V_{CORE} = 0.85 V	TBD	TBD	
		V_{CORE} = 1.0 V	TBD	TBD	
		V_{CORE} = 1.1 V	TBD	TBD	
		V_{CORE} = 1.2 V	TBD	TBD	
$t_{Standby}$	Wakeup from Standby mode	-	TBD	TBD	

(1) Value guaranteed by characterization, not 100% tested in production.
(2) The wakeup time is measured from the wakeup event to the point at which the application code reads the first instruction under the below conditions: V_{DD} = V_{DDA} = 3.3 V, IRC8M = System clock = 8 MHz.

4.8. Power consumption

The The power consumption is measured as described in ***Figure 4-11. Power consumption measurement diagram*** The current consumption values are derived from the tests powered by V_{DD} = V_{DDA} except BKP_ONLY mode, while the current is I_{SUM}. In BKP_ONLY mode, the RTC unit and LXTAL oscillator are powered by the V_{BAT}, while the current is I_{BAT}. Unless otherwise stated, V_{DD} = V_{DDA} = 3.3 V is applied to supply pins in typical current consumption columns, and V_{DD} = V_{DDA} = $V_{DD(MAX)}$ is applied in maximum current consumption columns.

The MCU is configured under the following conditions:

- All I/O pins are in analog input mode

- All peripherals are disabled except when explicitly mentioned
- When the peripherals are enabled $f_{APB1} = f_{APB2} / 2 = f_{HCLK} / 2$.

Figure 4-11. Power consumption measurement diagram

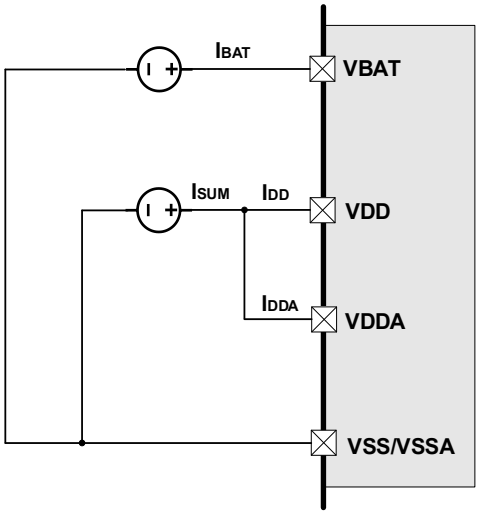


Table 4-8. Power consumption in Run mode(1)(2)(3)

Symbol	Description	Conditions					Typ		Max		Unit
		Execute from	Peripherals	General	Vcore	f_{HCLK}	25 °C	85 °C	25 °C	85 °C	
I_{SUM}	Sum of supply current from VDD and VDDA (Run mode)	FLASH	All disabled	HXTAL(bypass) = 8 MHz, PLL on, System clock = f_{HCLK}	1.2 V	252 MHz	TBD	TBD	TBD	TBD	mA
						220 MHz	TBD	TBD	TBD	TBD	
						168 MHz	TBD	TBD	TBD	TBD	
						108 MHz	TBD	TBD	TBD	TBD	
						72 MHz	TBD	TBD	TBD	TBD	
						36 MHz	TBD	TBD	TBD	TBD	
						8 MHz(4)	TBD	TBD	TBD	TBD	
				IRC 8 M = 8 MHz, PLL on, System clock = f_{HCLK}	1.2 V	252 MHz	TBD	TBD	TBD	TBD	
						220 MHz	TBD	TBD	TBD	TBD	
						168 MHz	TBD	TBD	TBD	TBD	
						108 MHz	TBD	TBD	TBD	TBD	
						72 MHz	TBD	TBD	TBD	TBD	
						36 MHz	TBD	TBD	TBD	TBD	
						8 MHz(4)	TBD	TBD	TBD	TBD	
		SRAM	All disabled	HXTAL(bypass) = 8 MHz, PLL on, System clock = f_{HCLK}	1.2 V	252 MHz	TBD	TBD	TBD	TBD	
						220 MHz	TBD	TBD	TBD	TBD	
						168 MHz	TBD	TBD	TBD	TBD	
						108 MHz	TBD	TBD	TBD	TBD	
						72 MHz	TBD	TBD	TBD	TBD	
						36 MHz	TBD	TBD	TBD	TBD	
						8 MHz(4)	TBD	TBD	TBD	TBD	
				IRC 8 M = 8 MHz,	1.2 V	252 MHz	TBD	TBD	TBD	TBD	

Symbol	Description	Conditions					Typ		Max		Unit
		Execute from	Peripherals	General	Vcore	f_{HCLK}	25 °C	85 °C	25 °C	85 °C	
				PLL on, System clock = f_{HCLK}		220 MHz	TBD	TBD	TBD	TBD	
						168 MHz	TBD	TBD	TBD	TBD	
						108 MHz	TBD	TBD	TBD	TBD	
						72 MHz	TBD	TBD	TBD	TBD	
						36 MHz	TBD	TBD	TBD	TBD	
						8 MHz(4)	TBD	TBD	TBD	TBD	
		FLASH	All disabled	HXTAL(bypass) = 8 MHz, PLL on, System clock = f_{HCLK}	1.1 V	200 MHz	TBD	TBD	TBD	TBD	
						168 MHz	TBD	TBD	TBD	TBD	
						108 MHz	TBD	TBD	TBD	TBD	
						72 MHz	TBD	TBD	TBD	TBD	
						36 MHz	TBD	TBD	TBD	TBD	
						8 MHz(4)	TBD	TBD	TBD	TBD	
				IRC 8 M = 8 MHz, PLL on, System clock = f_{HCLK}	1.1 V	200 MHz	TBD	TBD	TBD	TBD	
						168 MHz	TBD	TBD	TBD	TBD	
						108 MHz	TBD	TBD	TBD	TBD	
						72 MHz	TBD	TBD	TBD	TBD	
						36 MHz	TBD	TBD	TBD	TBD	
						8 MHz(4)	TBD	TBD	TBD	TBD	
		SRAM	All disabled	HXTAL(bypass) = 8 MHz, PLL on, System clock = f_{HCLK}	1.1 V	200 MHz	TBD	TBD	TBD	TBD	
						168 MHz	TBD	TBD	TBD	TBD	
						108 MHz	TBD	TBD	TBD	TBD	
						72 MHz	TBD	TBD	TBD	TBD	
						36 MHz	TBD	TBD	TBD	TBD	
						8 MHz(4)	TBD	TBD	TBD	TBD	

Symbol	Description	Conditions					Typ		Max		Unit
		Execute from	Peripherals	General	Vcore	f_{HCLK}	25 °C	85 °C	25 °C	85 °C	
				IRC 8 M = 8 MHz, PLL on, System clock = f_{HCLK}	1.1 V	200 MHz	TBD	TBD	TBD	TBD	
						168 MHz	TBD	TBD	TBD	TBD	
						108 MHz	TBD	TBD	TBD	TBD	
						72 MHz	TBD	TBD	TBD	TBD	
						36 MHz	TBD	TBD	TBD	TBD	
						8 MHz(4)	TBD	TBD	TBD	TBD	
		FLASH	All enabled	HXTAL(bypass) = 8 MHz, PLL on, System clock = f_{HCLK}	1.2 V	252 MHz	TBD	TBD	TBD	TBD	
		SRAM					TBD	TBD	TBD	TBD	
		FLASH		IRC 8 M = 8 MHz, PLL on, System clock = f_{HCLK}			TBD	TBD	TBD	TBD	
		SRAM					TBD	TBD	TBD	TBD	
		FLASH	All enabled	HXTAL(bypass) = 8 MHz, PLL on, System clock = f_{HCLK}	1.1 V	200 MHz	TBD	TBD	TBD	TBD	
		SRAM					TBD	TBD	TBD	TBD	
		FLASH		IRC 8 M = 8 MHz, PLL on, System clock = f_{HCLK}			TBD	TBD	TBD	TBD	
		SRAM					TBD	TBD	TBD	TBD	

(1) Value guaranteed by characterization, not 100% tested in production.

(2) During power consumption test, GPIO needs to be configure as Analog Input mode.

(3) ICache off, PRENFETCH on.

(4) PLL off.

Table 4-9. Power consumption in Run mode with different codes(1)(2)

Symbol	Description	Conditions				Typ	Unit	Typ	Unit
		Execute from	General	Vcore	Code				
I_{SUM}	Sum of supply current from VDD and VDDA (Run mode)	FLASH	HXTAL(bypass) = 8 MHz, PLL on, System clock = 252 MHz, f_{HCLK} = 252 MHz, All peripherals disabled	1.2 V	Coremark	TBD	mA	TBD	µA /MHz
					Coremark	TBD		TBD	
			HXTAL(bypass) = 8 MHz, PLL on, System clock = 200 MHz, f_{HCLK} = 200 MHz, All peripherals disabled						
		SRAM	HXTAL(bypass) = 8 MHz, PLL on, System clock = 252 MHz, f_{HCLK} = 252 MHz, All peripherals disabled	1.2 V	Coremark	TBD		TBD	
					Coremark	TBD		TBD	
			HXTAL(bypass) = 8 MHz, PLL on, System clock = 200 MHz, f_{HCLK} = 200 MHz, All peripherals disabled						

(1) Value guaranteed by sample, not 100% tested in production.

(2) During power consumption test, GPIO needs to be configure as Analog Input mode.

Table 4-10. Power consumption in Sleep mode(1)(2)

Symbol	Description	Conditions				Typ		Max		Unit
		Peripherals	General	Vcore	f_{HCLK}	25 °C	85 °C	25 °C	85 °C	
I_{SUM}	Sum of supply current from VDD and VDDA (Sleep mode)	All disabled	HXTAL(bypass) = 8 MHz, PLL on, System clock = f_{HCLK}, CPU clock off	1.2 V	252 MHz	TBD	TBD	TBD	TBD	mA
					220 MHz	TBD	TBD	TBD	TBD	
					200 MHz	TBD	TBD	TBD	TBD	
					168 MHz	TBD	TBD	TBD	TBD	
					108 MHz	TBD	TBD	TBD	TBD	
					72 MHz	TBD	TBD	TBD	TBD	
					36 MHz	TBD	TBD	TBD	TBD	
					8 MHz	TBD	TBD	TBD	TBD	
				1.1 V	200 MHz	TBD	TBD	TBD	TBD	
					168 MHz	TBD	TBD	TBD	TBD	
					108 MHz	TBD	TBD	TBD	TBD	

Symbol	Description	Conditions				Typ		Max		Unit
		Peripherals	General	Vcore	f_{HCLK}	25 °C	85 °C	25 °C	85 °C	
					72 MHz	TBD	TBD	TBD	TBD	
					36 MHz	TBD	TBD	TBD	TBD	
					8 MHz	TBD	TBD	TBD	TBD	
			IRC8M = 8 MHz, PLL on, System clock = f_{HCLK}, CPU clock off	1.2 V	252 MHz	TBD	TBD	TBD	TBD	
					220 MHz	TBD	TBD	TBD	TBD	
					200 MHz	TBD	TBD	TBD	TBD	
					168 MHz	TBD	TBD	TBD	TBD	
					108 MHz	TBD	TBD	TBD	TBD	
					72 MHz	TBD	TBD	TBD	TBD	
					36 MHz	TBD	TBD	TBD	TBD	
					8 MHz	TBD	TBD	TBD	TBD	
				1.1 V	200 MHz	TBD	TBD	TBD	TBD	
					168 MHz	TBD	TBD	TBD	TBD	
					108 MHz	TBD	TBD	TBD	TBD	
					72 MHz	TBD	TBD	TBD	TBD	
					36 MHz	TBD	TBD	TBD	TBD	
					8 MHz	TBD	TBD	TBD	TBD	
		All enabled	HXTAL(bypass) = 8 MHz, PLL on, System clock = f_{HCLK}, CPU clock off	1.2 V	252 MHz	TBD	TBD	TBD	TBD	
					220 MHz	TBD	TBD	TBD	TBD	
					200 MHz	TBD	TBD	TBD	TBD	
				1.1 V	200 MHz	TBD	TBD	TBD	TBD	
			IRC8M = 8 MHz, PLL on, System clock = f_{HCLK}, CPU	1.2 V	252 MHz	TBD	TBD	TBD	TBD	
					220 MHz	TBD	TBD	TBD	TBD	

Symbol	Description	Conditions				Typ		Max		Unit
		Peripherals	General	Vcore	f_{HCLK}	25 °C	85 °C	25 °C	85 °C	
			clock off		200 MHz	TBD	TBD	TBD	TBD	
				1.1 V	200 MHz	TBD	TBD	TBD	TBD	

(1) During power consumption test, GPIO needs to be configure as Analog Input mode.

(2) Value guaranteed by characterization, not 100% tested in production.

Table 4-11. Power consumption in Deep-sleep mode(1)(2)

Symbol	Description	Conditions			Typ		Max		Unit
		General	V_{CORE}	V_{DD}	25 °C	85 °C	25 °C	85 °C	
I_{SUM}	Sum of supply current from VDD and VDDA (Deep-sleep mode)	LDO in normal power mode, IRC40K off, RTC off	0.9 V	1.71V	TBD	TBD	TBD	TBD	µA
				3.3V	TBD	TBD	TBD	TBD	
				3.6V	TBD	TBD	TBD	TBD	
		LDO in low power mode, IRC40K off, RTC off		1.71V	TBD	TBD	TBD	TBD	
				3.3V	TBD	TBD	TBD	TBD	
				3.6V	TBD	TBD	TBD	TBD	
		LDO in normal power mode, IRC40K off, RTC off	1.1 V	1.71V	TBD	TBD	TBD	TBD	
				3.3V	TBD	TBD	TBD	TBD	
				3.6V	TBD	TBD	TBD	TBD	
		LDO in low power mode, IRC40K off, RTC off		1.71V	TBD	TBD	TBD	TBD	
				3.3V	TBD	TBD	TBD	TBD	
				3.6V	TBD	TBD	TBD	TBD	
		LDO in normal power mode, IRC40K off, RTC off	1.2 V	1.71V	TBD	TBD	TBD	TBD	
				3.3V	TBD	TBD	TBD	TBD	
				3.6V	TBD	TBD	TBD	TBD	
		LDO in low power mode, IRC40K off, RTC off		1.71V	TBD	TBD	TBD	TBD	
				3.3V	TBD	TBD	TBD	TBD	
				3.6V	TBD	TBD	TBD	TBD	

(1) During power consumption test, GPIO needs to be configure as Analog Input mode.

(2) Value guaranteed by characterization, not 100% tested in production.

Table 4-12. Power consumption in Deep-sleep 1 mode(1)(2)

Symbol	Description	Conditions			Typ		Max		Unit
		General		V_{DD}	25 °C	85 °C	25 °C	85 °C	
I_{SUM}	Sum of supply current from VDD and VDDA (Deep-sleep 1 mode)	LDO in normal power, IRC40K off, RTC off	0.9 V	1.71V	TBD	TBD	TBD	TBD	μA
				3.3V	TBD	TBD	TBD	TBD	
				3.6V	TBD	TBD	TBD	TBD	
		LDO in low power, IRC40K off, RTC off		1.71V	TBD	TBD	TBD	TBD	
				3.3V	TBD	TBD	TBD	TBD	
				3.6V	TBD	TBD	TBD	TBD	
		LDO in normal power, IRC40K off, RTC off	1.1 V	1.71V	TBD	TBD	TBD	TBD	
				3.3V	TBD	TBD	TBD	TBD	
				3.6V	TBD	TBD	TBD	TBD	
		LDO in low power, IRC40K off, RTC off		1.71V	TBD	TBD	TBD	TBD	
				3.3V	TBD	TBD	TBD	TBD	
				3.6V	TBD	TBD	TBD	TBD	
		LDO in normal power, IRC40K off, RTC off	1.2 V	1.71V	TBD	TBD	TBD	TBD	
				3.3V	TBD	TBD	TBD	TBD	
				3.6V	TBD	TBD	TBD	TBD	
		LDO in low power, IRC40K off, RTC off		1.71V	TBD	TBD	TBD	TBD	
				3.3V	TBD	TBD	TBD	TBD	
				3.6V	TBD	TBD	TBD	TBD	

(1) During power consumption test, GPIO needs to be configure as Analog Input mode.

(2) Value guaranteed by characterization, not 100% tested in production.

Table 4-13. Power consumption in Standby mode(1)(2)

Symbol	Description	Conditions			Typ		Max		Unit
		General	RAM retention	V_{DD}	25 °C	85 °C	25 °C	85 °C	
I_{SUM}	Sum of supply current from VDD and VDDA (Standby mode)	LXTAL off, IRC40K on, RTC on	Enable	1.71V	TBD	TBD	TBD	TBD	µA
				3.3V	TBD	TBD	TBD	TBD	
				3.6V	TBD	TBD	TBD	TBD	
		LXTAL off, IRC40K on, RTC off		1.71V	TBD	TBD	TBD	TBD	
				3.3V	TBD	TBD	TBD	TBD	
				3.6V	TBD	TBD	TBD	TBD	
		LXTAL off, IRC40K off, RTC off		1.71V	TBD	TBD	TBD	TBD	
				3.3V	TBD	TBD	TBD	TBD	
				3.6V	TBD	TBD	TBD	TBD	
		LXTAL off, IRC40K on, RTC on	Disable	1.71V	TBD	TBD	TBD	TBD	
				3.3V	TBD	TBD	TBD	TBD	
				3.6V	TBD	TBD	TBD	TBD	
		LXTAL off, IRC40K on, RTC off		1.71V	TBD	TBD	TBD	TBD	
				3.3V	TBD	TBD	TBD	TBD	
				3.6V	TBD	TBD	TBD	TBD	
		LXTAL off, IRC40K off, RTC off		1.71V	TBD	TBD	TBD	TBD	
				3.3V	TBD	TBD	TBD	TBD	
				3.6V	TBD	TBD	TBD	TBD	

(1) Value guaranteed by characterization, not 100% tested in production.

(2) During power consumption test, GPIO needs to be configure as Analog Input mode.

Table 4-14. Power consumption in BKP_ONLY mode(1)(2)

Symbol	Description	Conditions		Typ		Unit
		General	V_{BAT}	25 °C	85 °C	
I_{BAT}	LXTAL+RTC current from VBAT (BKP_ONLY mode)	VDD off, VDDA off, LXTAL on with external crystal, RTC on, LXTAL High driving	1.71V	2.0	2.4	μA
			3.0V	4.1	4.2	
			3.3V	4.7	4.7	
			3.6V	5.3	5.4	
		VDD off, VDDA off, LXTAL on with external crystal, RTC on, LXTAL Medium High driving	1.71V	1.7	2.0	
			3.0V	3.7	3.7	
			3.3V	4.3	4.3	
			3.6V	5.0	5.0	
		VDD off, VDDA off, LXTAL on with external crystal, RTC on, LXTAL Medium Low driving	1.71V	1.4	1.6	
			3.0V	3.4	3.3	
			3.3V	4.0	3.9	
			3.6V	4.7	4.6	
		VDD off, VDDA off, LXTAL on with external crystal, RTC on, LXTAL Low driving	1.71V	1.3	1.5	
			3.0V	3.3	3.2	
			3.3V	3.9	3.8	
			3.6V	4.6	4.5	
		VDD off, VDDA off, LXTAL clocked bypass, RTC on	1.71V	0.2	0.4	
			3.0V	0.5	0.7	
			3.3V	0.6	0.9	
			3.6V	0.7	1.1	
		VDD off, VDDA off,	1.71V	0.0	0.2	

Symbol	Description	Conditions		Typ		Unit
		General	V_{BAT}	25 °C	85 °C	
		LXTAL off	3.0V	0.0	0.2	
			3.3V	0.0	0.3	
			3.6V	0.1	0.5	

(1) Value guaranteed by sample, not 100% tested in production.

(2) During power consumption test, GPIO needs to be configure as Analog Input mode.

The current consumption of the on-chip peripherals is given in the following table. To avoid adding the CPU dynamic power consumption to the peripheral power consumption, the MCU needs to enter sleep mode to stop the CPU operation during current measurement. The MCU is configured under the following conditions:

· All I/O pins are in analog input mode

· The given value is in the table calculated by measuring the difference of the current consumptions:

-- The target peripheral is clocked on and enters sleep mode

-- All peripherals are clocked off and enter sleep mode

The power consumption of the digital part of the on-chip peripherals is given in the following table. The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

The values in the table are equal to the peripheral current divided by the clock frequency of the corresponding BUS.

Table 4-15. Peripheral current consumption characteristics(1)

Peripherals		Typical consumption	Unit
APB1	DAC	2.89	μA/MHz
	I2C0	8.06	
	I2C1	8.46	
	I2C2	14.66	
	PMU	7.42	
	SPI1	18.27	
	SPI2	10.10	
	TIMER1	33.71	
	TIMER12	7.79	
	TIMER13	8.22	
	TIMER2	27.13	
	TIMER3	27.92	
	TIMER4	27.35	
	TIMER42	36.61	
	TIMER43	36.34	
	TIMER44	36.91	
	TIMER5	4.11	
	TIMER50	4.28	
	TIMER51	4.30	
	TIMER6	3.89	
	UART3	5.58	
	UART4	5.68	
	USART1	8.88	
	USART2	9.36	

Peripherials		Typical consumption	Unit
	WWDGT	0.76	
	CTC1	1.28	
	CTC0	1.56	
APB2	ADC0	6.88	
	ADC1	6.37	
	ADC2	6.98	
	AF	0.33	
	CAN0	13.50	
	CAN1	12.82	
	CAN2	14.07	
	CMP	1.39	
	PA	10.74	
	PB	10.82	
	PC	10.82	
	PD	10.44	
	PE	10.74	
	SDIO	11.89	
	SPI0	3.31	
	SPI3	3.17	
	SYSCFG	8.65	
	TIMER0	38.63	
	TIMER10	4.37	
	TIMER14	20.15	
	TIMER19	39.03	
	TIMER40	19.58	
	TIMER41	20.11	
	TIMER7	38.40	
	TIMER9	4.26	
	TRIGSEL	2.13	
	USART0	9.16	
	USART5	23.06	
AHB	BKSRAM	2.73	
	CAU	72.57	
	CRC	0.91	
	DMA0	13.72	
	DMA1	10.67	
	DMAMUX	9.70	
	EXMC	12.14	
	HAU	2.70	
	OSPI	36.57	
	SRAM	10.32	

Peripherials		Typical consumption	Unit
	TRNG	1.26	
	USBFS	26.42	

(1) Value guaranteed by sample, not 100% tested in production.

4.9. EMC characteristics

System level ESD (Electrostatic discharge, according to IEC 61000-4-2) and EFT (Electrical Fast Transient/burst, according to IEC 61000-4-4) testing result is given in the ***Table 4-16. System level ESD and EFT characteristics*** (1). System level ESD is for end-customer operation, it includes ESD field events on system level occur in an unprotected area (outside EPA). System level ESD protection necessary to satisfy higher ESD levels.

Table 4-16. System level ESD and EFT characteristics (1)(2)

Symbol	Description	Conditions	Package	Class	Level
V_{ESD}	Contact / Air mode high voltage stressed on few special I/O pins	V_{DD} = 3.3 V, T_A = 25 °C, f_{HCLK} = 252 MHz IEC 61000-4-2	LQFP100	CD 8KV AD 15KV	4A
V_{EFT}	Fast transient high voltage burst stressed on Power and GND	V_{DD} = 3.3 V, T_A = 25 °C, f_{HCLK} = 252 MHz IEC 61000-4-4	LQFP100	4KV	4A

(1) Value guaranteed by sample, not 100% tested in production.

(2) The explanation of the evaluation methods for system-level ESD and system-level EFT test methods and test levels can be referred to in AN127 and AN128.

EMI (Electromagnetic Interference) emission test result is given in the ***Table 4-17. EMI characteristics***, The electromagnetic field emitted by the device are monitored while an application, executing EEMBC code, is running. The test is compliant with SAE J1752-3 standard which specifies the test board and the pin loading.

Table 4-17. EMI characteristics(1)(2)

Symbol	Description	Conditions	Package	Max vs. [f_{HXTAL}/f_{HCLK}] 8 / 252 MHz			Unit
				0.1-30MHz	30-130MHz	130MHz-1GHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, f_{HCLK} = 252 MHz, conforms to SAE J1752-3	LQFP100	11.4	9.4	8.73	dBµV

(1) Value guaranteed by sample, not 100% tested in production.

(2) The explanation of the chip-level EMI test methods can be referred to in AN125.

4.10. Electrical sensitivity

Component level ESD include HBM (Human body model, according to ANSI / ESDA /

JEDEC JS-001) and CDM (ANSI / ESDA / JEDEC JS-002), that ESD field events during manufacturing in an ESD protected area, such as PCB assembly/repair, IC assembly/test and Fab environment. The ESD protected area (EPA) has many measures, for instance ESD protective packaging, grounding person wrist strap to ground (or flooring/footwear), grounded work surface and ionizer.

Static latch-up (LU, according to JEDEC78) test is based on the two measurement methods, I/O current injection value (I-test) and power supply over-voltage value.

Table 4-18. Component level ESD and latch-up characteristics(1)(2)

Symbol	Description	Conditions	Package	Max	Unit	Level
V_{HBM}	Human body model electrostatic discharge voltage (Any pin combination)	T_A = 25 °C; JS-001	LQFP64	4000	V	3A
V_{CDM}	Charge device model electrostatic discharge voltage (All pins)	T_A = 25 °C; JS-002	LQFP64	1000	V	C3
LU	I-test	T_A = 125°C; JESD78	LQFP64	+/- 200	mA	Class II.A
	V_{supply} over voltage			5.4	V	

(1) Value guaranteed by sample, not 100% tested in production.

(2) The levels of system-level ESD and chip-level ESD are not related. The differences between the two can be referred to in AN159.

4.11. External clock characteristics

Table 4-19. High speed external clock (HXTAL) generated from a crystal/ceramic characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL}	Crystal or ceramic frequency	1.71 V <= V_{DD} <= 3.6 V	4	8	32	MHz
R_F	Feedback resistor	V_{DD} = 3.3 V	-	400	-	kΩ
C_{HXTAL}(2)	Recommended load capacitance on OSCIN and OSCOUT	-	-	20	-	pF
$Ducy_{(HXTAL)}$	Crystal or ceramic duty cycle	-	35	50	65	%
g_m	Oscillator transconductance	Startup	-	23	-	mA/V
$I_{DDHXTAL}$	Crystal or ceramic operating current	V_{DD} = 3.3 V, f_{HCLK} = f_{IRC8M} = 8 MHz T_A = 25 °C	-	0.5	-	mA
$t_{ST(HXTAL)}$(3)	Crystal or ceramic startup time	V_{DD} = 3.3 V, f_{HCLK} = f_{IRC8M} = 8 MHz T_A = 25 °C	-	2	-	ms

(1) Value guaranteed by design, not 100% tested in production.

(2) $C_{HXTAL1} = C_{HXTAL2} = 2*(C_{LOAD} - C_S)$, For C_{HXTAL1} and C_{HXTAL2}, it is recommended matching capacitance on OSCIN and OSCOUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

(3) $t_{ST(HXTAL)}$ is the startup time measured from the moment it is enabled (by software) to the 8 MHz oscillator stabilization flag is SET. This value varies significantly with the crystal manufacturer.

Table 4-20. High speed external clock characteristics (HXTAL in bypass mode)(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL_ext}	External clock source or oscillator frequency	1.71 V <= V_{DD} <= 3.6 V	1	-	50	MHz
V_{HXTALH}	OSCIN input pin high level voltage	V_{DD} = 3.3 V	0.7V_{DD}	-	V_{DD}	V
V_{HXTALL}	OSCIN input pin low level voltage		V_{SS}	-	0.3V_{DD}	V
$t_{H/L(HXTAL)}$	OSCIN high or low time	-	5	-	-	ns
$t_{R/F(HXTAL)}$	OSCIN rise or fall time	-	-	-	10	ns
C_{IN}	OSCIN input capacitance	-	-	5	-	pF
$Ducy_{(HXTAL)}$	Duty cycle	-	30	-	70	%

(1) Value guaranteed by design, not 100% tested in production.

Table 4-21. Low speed external clock (LXTAL) generated from a crystal/ceramic characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LXTAL}	Crystal or ceramic frequency	V_{DD} = 3.3 V	-	32.768	-	kHz
R_F	Internal feedback resistor	-	-	10	-	MΩ
C_{LXTAL}(2)	Recommended matching capacitance on OSC32IN and OSC32OUT	-	-	10	-	pF
$Ducy_{(LXTAL)}$	Crystal or ceramic duty cycle	-	30	-	70	%
g_m	Oscillator transconductance	Lower driving capability	-	-	4	µA/V
		Medium low driving capability	-	-	6	
		Medium high driving capability	-	-	12	
		Higher driving capability	-	-	18	
$I_{DD(LXTAL)}$	Crystal or ceramic operating current	LXTALDRI[1:0] = 00	-	0.7	-	µA
		LXTALDRI[1:0] = 01	-	0.8	-	
		LXTALDRI[1:0] = 10	-	1.2	-	
		LXTALDRI[1:0] = 11	-	1.6	-	
$t_{ST(LXTAL)}$(3)	Crystal or ceramic startup time	V_{DD} = 3.3 V	-	2	-	s

(1) Value guaranteed by design, not tested in production.

(2) $C_{LXTAL1} = C_{LXTAL2} = 2*(C_{LOAD} - C_S)$, For C_{LXTAL1} and C_{LXTAL2}, it is recommended matching capacitance on OSC32IN and OSC32OUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

(3) $t_{ST(LXTA)}$ is the startup time measured from the moment it is enabled (by software) to the 32.768 kHz oscillator stabilization flag is SET. This value varies significantly with the crystal manufacturer.

Table 4-22. Low speed external user clock characteristics (LXTAL in bypass mode)(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LXTAL_ext}	External clock source or oscillator frequency	V_{DD} = 3.3 V	-	32.768	1000	kHz
V_{LXTALH}	OSC32IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{LXTALL}	OSC32IN input pin low level voltage	-	V_{SS}	-	$0.3V_{DD}$	
$t_{H/L(LXTAL)}$	OSC32IN high or low time	-	450	-	-	ns
$t_{R/F(LXTAL)}$	OSC32IN rise or fall time	-	-	-	50	
C_{IN}	OSC32IN input capacitance	-	-	5	-	pF
$Ducy_{(LXTAL)}$	Duty cycle	-	30	50	70	%

(1) Value guaranteed by design, not 100%tested in production.

4.12. Internal clock characteristics

Table 4-23. High speed internal clock (IRC8M) characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC8M}	High Speed Internal Oscillator (IRC8M) frequency	-	-	8	-	MHz
ACC_{IRC8M}	IRC8M oscillator Frequency accuracy, Factory-trimmed(2)	$V_{DD} = V_{DDA}$ = 3.3 V, T_A = -40 °C ~ +105 °C	TBD	-	TBD	%
		$V_{DD} = V_{DDA}$ = 3.3 V, T_A = 0 °C ~ +105 °C	TBD	-	TBD	%
	IRC8M oscillator Frequency accuracy, User trimming step	-	-	0.5	-	%
$Ducy_{IRC8M}$	IRC8M oscillator duty cycle	f_{IRC8M} = 8 MHz	45	50	55	%
$I_{DDAIRC8M}$	IRC8M oscillator operating current	f_{IRC8M} = 8 MHz	-	74.7	-	μA
$t_{ST(IRC8M)}$	IRC8M oscillator startup time	f_{IRC8M} = 8 MHz	-	1.54	-	μs

(1) Value guaranteed by design, not tested in production.

(2) Value guaranteed by characterization, not 100% tested in production.

Table 4-24. Low speed internal clock (IRC40K) characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC40K}	Low Speed Internal oscillator (IRC40K) frequency	-	-	40	-	kHz
ACC_{IRC40K}	IRC40K oscillator Frequency accuracy, Factory-trimmed(2)	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +105 °C	TBD	-	TBD	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = 0 °C ~ +105 °C	TBD	-	TBD	%
	IRC40K oscillator Frequency accuracy, User trimming step	-	-	3.06	-	%
$I_{DDA(IRC40K)}$	IRC40K oscillator operating current	f_{IRC40K} = 40 kHz	-	429	-	μA
$t_{ST(IRC40K)}$	IRC40K oscillator startup time	f_{IRC40K} = 40 kHz	-	20	-	μs

(1) Value guaranteed by design, not tested in production.
(2) Value guaranteed by characterization, not 100% tested in production.

Table 4-25. High speed internal clock (IRC48M) characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC48M}	High Speed Internal Oscillator (IRC48M) frequency	-	-	48	-	MHz
ACC_{IRC48M}	IRC48M oscillator Frequency accuracy, Factory-trimmed(2)	V_{DD} = V_{DDA} = 3.3 V, T_A = -40 °C ~ +105 °C	TBD	-	TBD	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = 0 °C ~ +105 °C	TBD	-	TBD	%
	IRC48M oscillator Frequency accuracy, User trimming step	-	-	0.67	-	%
D_{IRC48M}	IRC48M oscillator duty cycle	f_{IRC48M} = 48 MHz	45	50	55	%
$I_{DDAIRC48M}$	IRC48M oscillator operating current	f_{IRC48M} = 48 MHz	-	339	-	μA
$t_{ST(IRC48M)}$	IRC48M oscillator startup time	f_{IRC48M} = 48 MHz	-	1.66	-	μs

(1) Value guaranteed by design, not 100% tested in production.
(2) Value guaranteed by characterization, not 100% tested in production.

4.13. PLL characteristics

Table 4-26. PLL1 characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}	PLL input clock frequency	-	4	-	16	MHz
f_{PLLOUT}	PLL output clock frequency	-	32	-	504	MHz
f_{VCO}	PLL VCO output clock frequency	-	32	-	504	MHz
t_{LOCK}	PLL lock time	-	100	-	300	μs
I_{DD}	Current consumption on V_{DD}	VCO freq = 504 MHz		1300		μA
$Jitter_{PLL}$(3)	Cycle to cycle Jitter (rms)	System clock	-	40	-	ps
	Cycle to cycle Jitter (peak to peak)		-	400	-	

(1) Value guaranteed by design, not tested in production.

(2) System clock = IRC8M = 8 MHz, PLL clock source = IRC8M/2 = 4 MHz, f_{PLLOUT} = 504 MHz.

(3) Value given with main PLL running.

Table 4-27. PLL2 characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}	PLL input clock frequency	-	4	-	16	MHz
f_{PLLOUT}	PLL output clock frequency	-	32	-	240	MHz
f_{VCO}	PLL VCO output clock frequency	-	32	-	240	MHz
t_{LOCK}	PLL lock time	-	100	-	300	μs
I_{DD}	Current consumption on V_{DD}	VCO freq = 240 MHz	-	850	-	μA
$Jitter_{PLL}$	Cycle to cycle Jitter	-	-	40	-	ps

(1) Value guaranteed by design, not tested in production.

Table 4-28. PLL1 spread spectrum clock generation (SSCG) characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{mod}	Modulation frequency	-	-	-	10	kHz
mdamp	Peak modulation amplitude	-	-	-	2	%
MODCNT* MODSTEP	-	-	-	-	2^{15}-1	-

(1) Value guaranteed by design, not tested in production.

Equation 1: SSCG configuration equation:

$MODCNT=round(f_{PLLIN}/4/f_{mod})$

$MODSTEP = round(mdamp*PLLN*2^{15}/(MODCNT*100))$

The formula above (***Equation 1***) is SSCG configuration equation.

4.14. Memory characteristics

Table 4-29. Flash memory characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
$I_{DD(FLASH)}$	Max supply current from V_{DD} during FLASH operation	Erasing	-	4	-	mA
		Programming	-	5	-	
PE_{CYC}(2)	Number of guaranteed program /erase cycles before failure (Endurance)	T_A = -40 °C ~ +85 °C	100	-	-	kcycles
t_{RET}(2)	Data retention time	T_A = 85 °C after up to 0 kcycle	25	-	-	years
		T_A = 85 °C after up to 10 kcycles	15	-	-	years
t_{PROG}	Double word programming time	-	-	90	-	μs
t_{PROG_PAGE}	One page (2 Kbytes) programming time	Normal programming	-	11.520	-	ms
t_{PROG_BANK}	One bank (512 Kbyte) programming time	Normal programming	-	2949	-	
t_{ERASE}	Page erase time	T_A = -40°C ~ +85 °C	16	-	20	
t_{MERASE}	Mass erase time	T_A = -40°C ~ +85 °C	-	18	-	

(1) Value guaranteed by design, not 100% tested in production.
(2) Value guaranteed by characterization, not 100% tested in production.

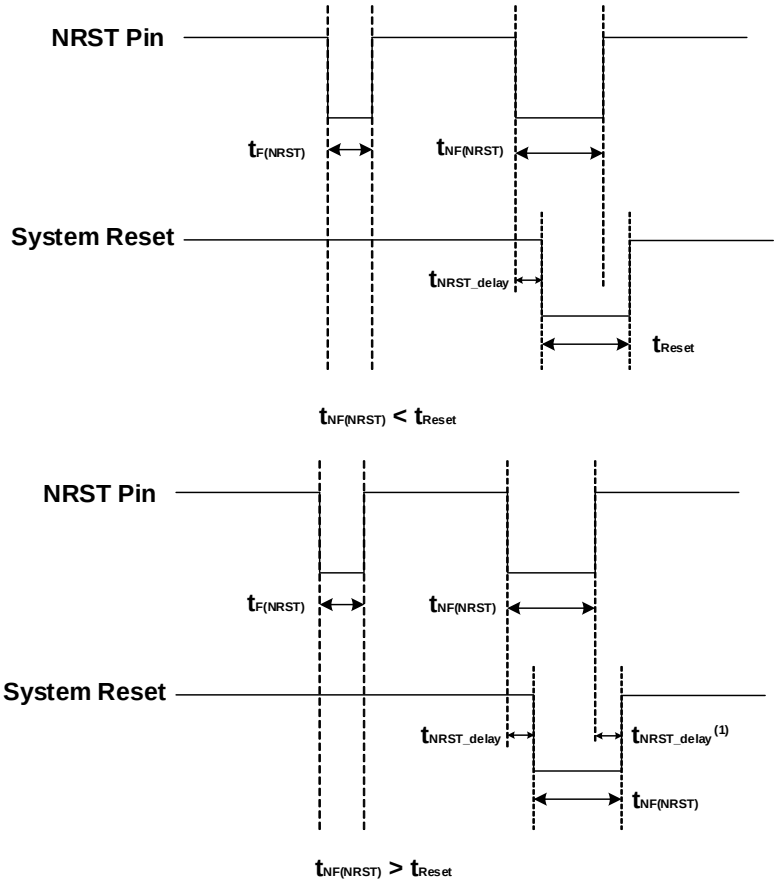
4.15. NRST pin characteristics

Table 4-30. NRST pin characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST Input low level voltage	-	-	-	0.35V_{DD}	V
$V_{IH(NRST)}$	NRST Input high level voltage	-	0.65V_{DD}	-	-	
$V_{HYST(NRST)}$	Schmitt trigger Voltage hysteresis	V_{DD} = V_{DDA} = 1.71 V	-	328	-	mV
		V_{DD} = V_{DDA} = 3.3 V	-	376	-	
		V_{DD} = V_{DDA} = 3.6 V	-	396	-	
$R_{PU(NRST)}$	Pull-up equivalent resistor	V_{IN} = V_{SS}	-	40	-	kΩ
$t_{F(NRST)}$	NRST input filtered pulse	-	-	-	0.87	μs
$t_{NF(NRST)}$	NRST input not filtered pulse	-	1.4	-	-	μs
t_{Reset}(2)	Reset stretch time	-	2.62	3.16	4.46	ms
t_{NRST_delay}(3)	System reset delay time	-	TBD	-	TBD	μs

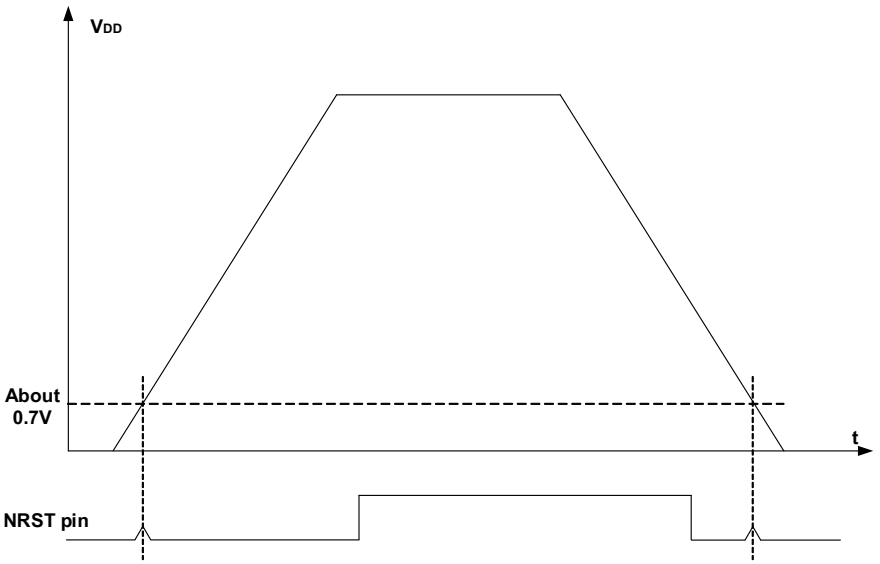
(1) Value guaranteed by design, not 100% tested in production.
(2) When the NRST pin is held low longer than t_{Reset}, system reset duration equals NRST pin's pull-down time and t_{Reset} is overridden.
(3) The NRST pin is left floating.

Figure 4-12. NRST pin level and system reset timing diagram



(1) Besides t_{NRST_delay}, the time required to charge the NRST pin decoupling capacitor must also be considered.

Figure 4-13. NRST pin power-on / power-off MOS transistor pulse diagram



4.16. GPIO current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below VSS or above VDD (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures. The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the -5 μA/+0 μA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Table 4-31. GPIO current injection susceptibility(1)

Symbol	Description		Functional susceptibility		Unit
			Negative injection	Positive injection	
I_{INJ}	Injected current on pin	BOOT0	-5	0	mA
		NRST	0	0	
		Input current on 5V tolerant I/O pins	-5	NA(2)	
		Input current on other I/O pins	-5	0	

(1) Value guaranteed by sample, not 100% tested in production.

(2) NA: Not applicable.

4.17. GPIO characteristics

Table 4-32. I/O port static characteristics(1)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
$V_{IL(GPIO)}$	IO Low level input voltage		1.71 V <= V_{DD} = V_{DDA} <= 3.6 V	-	-	0.3V_{DD}	V
$V_{IH(GPIO)}$	IO High level input voltage		1.71 V <= V_{DD} = V_{DDA} <= 3.6 V	0.7V_{DD}	-	-	V
$V_{HYS(GPIO)}$	Input hysteresis		1.71 V <= V_{DD} = V_{DDA} <= 3.6 V	-	330	-	mV
I_{LEAK}	IO input leakage current		1.71 V <= V_{DD} = V_{DDA} <= 3.6 V	-	-	TBD	μA
$R_{PU(GPIO)}$	Internal pull-up resistor	All pins	-	40	-	-	kΩ
		PA10	-	10	-	-	
$R_{PD(GPIO)}$	Internal pull-down resistor	All pins	-	40	-	-	kΩ
		PA10	-	10	-	-	

(1) Value guaranteed by design, not tested in production.

Table 4-33. Output voltage characteristics for all I/Os except PC13, PC14, PC15(1)(2)

Symbol	Description	Conditions		Min	Typ	Max	Unit
V_{OL0}	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	Max IO_speed = 100 MHz, OSPDx<1:0> = 11	V_{DD} = 1.71 V	-	-	TBD	V
			V_{DD} = 3.3 V	-	-	TBD	
			V_{DD} = 3.6 V	-	-	TBD	
	Low level output voltage for an IO Pin (I_{IO} = +20 mA)		V_{DD} = 1.71 V	-	-	TBD	
			V_{DD} = 3.3 V	-	-	TBD	
			V_{DD} = 3.6 V	-	-	TBD	
V_{OH0}	High level output voltage for an IO Pin (I_{IO} = +8 mA)		V_{DD} = 1.71 V	TBD	-	-	V
			V_{DD} = 3.3 V	TBD	-	-	
			V_{DD} = 3.6 V	TBD	-	-	
	High level output voltage for an IO Pin (I_{IO} = +20 mA)		V_{DD} = 1.71 V	TBD	-	-	
			V_{DD} = 3.3 V	TBD	-	-	
			V_{DD} = 3.6 V	TBD	-	-	
V_{OL1}	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	Max IO_speed = 50 MHz, OSPDx<1:0> = 10	V_{DD} = 1.71 V	-	-	TBD	V
			V_{DD} = 3.3 V	-	-	TBD	
			V_{DD} = 3.6 V	-	-	TBD	
	Low level output voltage for an IO Pin (I_{IO} = +20 mA)		V_{DD} = 1.71 V	-	-	TBD	
			V_{DD} = 3.3 V	-	-	TBD	
			V_{DD} = 3.6 V	-	-	TBD	
V_{OH1}	High level output voltage for an IO Pin (I_{IO} = +8 mA)		V_{DD} = 1.71 V	TBD	-	-	V
			V_{DD} = 3.3 V	TBD	-	-	
			V_{DD} = 3.6 V	TBD	-	-	
	High level output		V_{DD} = 1.71 V	TBD	-	-	

Symbol	Description	Conditions		Min	Typ	Max	Unit
	voltage for an IO Pin (I_{IO} = +20 mA)		V_{DD} = 3.3 V	TBD	-	-	
			V_{DD} = 3.6 V	TBD	-	-	
V_{OL2}	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	Max IO_speed = 10 MHz, OSPDx<1:0> = 01	V_{DD} = 1.71 V	-	-	TBD	V
			V_{DD} = 3.3 V	-	-	TBD	
			V_{DD} = 3.6 V	-	-	TBD	
	Low level output voltage for an IO Pin (I_{IO} = +15 mA)		V_{DD} = 1.71 V	-	-	TBD	
			V_{DD} = 3.3 V	-	-	TBD	
			V_{DD} = 3.6 V	-	-	TBD	
V_{OH2}	High level output voltage for an IO Pin (I_{IO} = +8 mA)		V_{DD} = 1.71 V	TBD	-	-	V
			V_{DD} = 3.3 V	TBD	-	-	
			V_{DD} = 3.6 V	TBD	-	-	
	High level output voltage for an IO Pin (I_{IO} = +15 mA)		V_{DD} = 1.71 V	TBD	-	-	
			V_{DD} = 3.3 V	TBD	-	-	
			V_{DD} = 3.6 V	TBD	-	-	
V_{OL3}	Low level output voltage for an IO Pin (I_{IO} = +1 mA)	Max IO_speed = 2 MHz, OSPDx<1:0> = 00	V_{DD} = 1.71 V	-	-	TBD	V
			V_{DD} = 3.3 V	-	-	TBD	
			V_{DD} = 3.6 V	-	-	TBD	
	Low level output voltage for an IO Pin (I_{IO} = +4 mA)		V_{DD} = 1.71 V	-	-	TBD	
			V_{DD} = 3.3 V	-	-	TBD	
			V_{DD} = 3.6 V	-	-	TBD	
V_{OH3}	High level output voltage for an IO Pin (I_{IO} = +1 mA)		V_{DD} = 1.71 V	TBD	-	-	
			V_{DD} = 3.3 V	TBD	-	-	
			V_{DD} = 3.6 V	TBD	-	-	
	High level output voltage for an IO Pin (I_{IO} = +4 mA)		V_{DD} = 1.71 V	TBD	-	-	
			V_{DD} = 3.3 V	TBD	-	-	
			V_{DD} = 3.6 V	TBD	-	-	

(1) Value guaranteed by characterization, not 100% tested in production.

(2) All pins except PC13 / PC14 / PC15. Since PC13 to PC15 are supplied through the Power Switch, which can only be obtained by a small current (typical source capability 3 mA shared between these IOs, but sink capability is same as other IO), the speed of GPIOs PC13 to PC15 should not exceed 2 MHz when they are in output mode (maximum load: 30 pF.

Table 4-34. I/O port AC characteristics(1)(2)(3)(4)

Symbol	Description	Conditions		Min	Typ	Max	Unit
t_R/t_{F0}	Output high to low level fall time and output low to high level rise time	Max IO_speed = 2 MHz, OSPDx<1:0> = 00	1.71 <= V_{DD} <= 3.6 V, C_L = 10 pF	-	-	TBD	ns
			1.71 <= V_{DD} <= 3.6 V, C_L = 30 pF	-	-	TBD	
			1.71 <= V_{DD} <= 3.6 V,C_L = 50 pF	-	-	TBD	
t_R/t_{F1}	Output high to low level fall time and output low to high	Max IO_speed = 10 MHz,	1.71 <= V_{DD} <= 3.6 V, C_L = 10 pF	-	-	TBD	ns
			1.71 <= V_{DD} <= 3.6 V, C_L = 30	-	-	TBD	

Symbol	Description	Conditions		Min	Typ	Max	Unit
	level rise time	OSPDx<1:0> = 01	pF				
			1.71 <= V_{DD} <= 3.6 V,C_L = 50 pF	-	-	TBD	
t_R/t_{F2}	Output high to low level fall time and output low to high level rise time	Max IO_speed = 50 MHz, OSPDx<1:0> = 10	1.71 <= V_{DD} <= 3.6 V, C_L = 10 pF	-	-	TBD	ns
			1.71 <= V_{DD} <= 3.6 V, C_L = 30 pF	-	-	TBD	
			1.71 <= V_{DD} <= 3.6 V,C_L = 50 pF	-	-	TBD	
t_R/t_{F3}	Output high to low level fall time and output low to high level rise time	Max IO_speed = 100 MHz, OSPDx<1:0> = 11	1.71 <= V_{DD} <= 3.6 V, C_L = 10 pF	-	-	TBD	ns
			1.71 <= V_{DD} <= 3.6 V, C_L = 30 pF	-	-	TBD	
			1.71 <= V_{DD} <= 3.6 V,C_L = 50 pF	-	-	TBD	

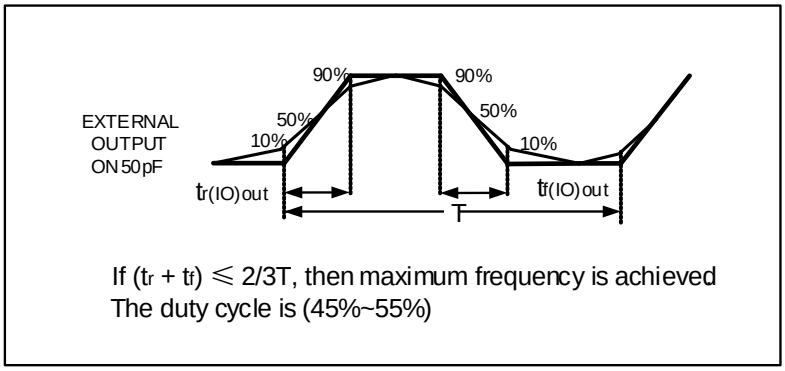
(1) The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.

(2) Value guaranteed by design, not 100% tested in production.

(3) The data is for reference only, and the specific values are related to PCB Layout.

(4) When the I/O port output speed is more than 50 MHz, it is recommended to use the compensation cell for slew rate control to reduce the I/O noise on power supply.

Figure 4-14. I/O port AC characteristics definition



4.18. Temperature sensor characteristics

Table 4-35. Temperature sensor characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
T_L	VSENSE linearity with temperature	-	+/-1.5	-	°C
Avg_Slope	Average slope	-	3.42	-	mV/°C
V_{25}	Voltage at 25 °C	-	1.24	-	V
t_{S_temp}	ADC sampling time when reading the temperature	-	17.1	-	µs

(1) Value guaranteed by design, not 100% tested in production.

Table 4-36. Temperature sensor calibration values(1)

Symbol	Test conditions	Memory address
T_{S_CAL}	Temperature sensor raw data acquired value at 25 °C, V_{DDA} = 3.3 V	0x1FFF F7F8 - 0x1FFF F7F9

(1) V_{SENSE} is internally connected to the ADC0_IN16 input channel.

Table 4-37. Temperature sensor slope at different temperatures

Symbol	Description	Memory address
T_{S_SLP1}	Temperature sensor slope at -40 °C ~ 0 °C, V_{DDA} = 3.3 V	0x1FFF F7D0 - 0x1FFF F7D1
T_{S_SLP2}	Temperature sensor slope at 0 °C ~ 25 °C, V_{DDA} = 3.3 V	0x1FFF F7D2 - 0x1FFF F7D3
T_{S_SLP3}	Temperature sensor slope at 25 °C ~ 65 °C, V_{DDA} = 3.3 V	0x1FFF F7D4 - 0x1FFF F7D5
T_{S_SLP4}	Temperature sensor slope at 65 °C ~ 85 °C, V_{DDA} = 3.3 V	0x1FFF F7D6 - 0x1FFF F7D7

4.19. Internal reference voltage characteristics

Table 4-38. Internal reference voltage characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	T_A = -40°C ~ +85 °C	TBD	1.2	TBD	V
$t_{S_VREFINT}$(1)(2)	ADC sampling time when reading the internal reference voltage	-	5	-	-	µs
$t_{STA_VREFINT}$(1)	Start time of V_{REFINT} circuit when ADC is enable	-	-	4	8	µs
$I_{DD(VREFINT_CIRCUIT)}$(1)	V_{REFINT} circuit consumption from V_{DD} when converted by ADC	V_{DD} = V_{DDA} =3.3V	-	3.5	4.2	µA
ΔV_{REFINT}(1)	Internal reference voltage spread over the temperature range	-	-	5	10	mV
T_{Coeff}(1)	Average temperature coefficient	T_A = -40°C ~ +85 °C	-	40	80	ppm/°C
$V_{DDcoeff}$(1)	Average Voltage coefficient	1.71 V <= VDD <= 3.6V	-	30	100	ppm/V

(1) Value guaranteed by design, not 100% tested in production.

(2) The shortest sampling time can be determined in the application by multiple iterations.

Table 4-39. Internal reference voltage calibration values

Symbol	Test conditions	Memory address
V_{REFINT}	V_{DD} = V_{DDA} = V_{REFP} = TBD V (+/-	0x1FFF F7FC - 0x1FFF F7FD(1)

Symbol	Test conditions	Memory address
	TBD mV), Temperature = TBD °C (+/- TBD °C)	0x1FFF F7DE - 0x1FFF F7DF(2)
		0x1FFF F7DC - 0x1FFF F7DD(3)

(1) V_{REFINT} is sampled via ADC0_IN17.
(2) V_{REFINT} is sampled via ADC1_IN18.
(3) V_{REFINT} is sampled via ADC2_IN17.

4.20. ADC characteristics

Table 4-40. ADC characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage	-	1.71	-	3.6	V
V_{IN}	ADC input voltage range	-	0	-	V_{REFP}	V
V_{REFP}(2)	Positive Reference Voltage	-	1.71	-	3.6	V
V_{REFN}	Negative Reference Voltage	-	-	V_{SSA}	-	V
f_{ADC}	ADC clock	V_{DDA} = 1.71 V to 2.4 V	0.1	-	14	MHz
		V_{DDA} = 2.4 V to 3.6 V	0.1	-	42	MHz
f_S	Sampling rate	12-bit V_{DDA} = 2.4 V to 3.6 V	-	-	3	MSPS
		10-bit V_{DDA} = 2.4 V to 3.6 V	-	-	3.5	
		8-bit V_{DDA} = 2.4 V to 3.6 V	-	-	4.2	
		6-bit V_{DDA} = 2.4 V to 3.6 V	-	-	5.25	
R_{AIN}	External input impedance	See *Equation 2*	-	-	74.16	kΩ
R_{ADC}	Input sampling switch resistance	-	-	-	0.5	kΩ
C_{ADC}	Input sampling capacitance	No pin/pad capacitance included	-	-	2.87	pF
t_s	Sampling time	f_{ADC} = 42 MHz	0.0357	-	5.7	1 / f_{ADC}
t_{CONV}	Total conversion time(including sampling time)	12-bit	-	14	-	1 / f_{ADC}
		10-bit	-	12	-	
		8-bit	-	10	-	
		6-bit	-	8	-	
t_{SU}	Startup time	-	-	-	1	µs

(1) Value guaranteed by design, not 100% tested in production.
(2) V_{REFP} should always be equal to or less than V_{DDA}, especially during power up.

Equation 2: R_{AIN} max formula $$R_{AIN} < \frac{T_s}{f_{ADC} * C_{ADC} * \ln(2^{N+2})} - R_{ADC}$$

The formula above (Equation 2) is used to determine the maximum external impedance allowed for an

error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 4-41. ADC R_{AIN} max for f_{ADC} = 42 MHz(1)

T_s (cycles)	t_s (μs)	$R_{AIN\ max}$ (kΩ)(2)
1.5	0.0357	-
7.5	0.1786	1.83
13.5	0.3214	3.70
28.5	0.6786	8.38
41.5	0.9881	12.43
55.5	1.3214	16.80
71.5	1.7024	21.79
239.5	5.7024	74.16

(1) Value guaranteed by design, not 100% tested in production.

(2) Extra internal capacitors (such as pin capacitors, etc.) need to be considered when calculating the actual R_{AIN}. Here we take 5 pF for the extra internal capacitance, C_{ADC} = 2.87 pF + 5pF = 7.87 pF.

Table 4-42. ADC dynamic accuracy at f_{ADC} = 14 MHz V_{DDA} = 1.71 V(1)(2)(3)(4)(5)

Symbol	Parameter	Test conditions		Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 14 MHz V_{DDA} = V_{REFP} = 1.71 V Input Frequency = 20 kHz	Single ended	TBD	TBD	-	bits
SNDR	Signal-to-noise and distortion ratio		Single ended	TBD	TBD	-	dB
SNR	Signal-to-noise ratio		Single ended	TBD	TBD	-	
THD	Total harmonic distortion		Single ended	-	TBD	TBD	

(1) Value guaranteed by characterization, not 100% tested in production.

(2) Results for TBD packages. The values for other packages might differ.

(3) V_{DD} = V_{DDA} = V_{REFP}= TBD, external V_{REF} were adopted.

(4) System clock = TBD, PCLKx = TBD, ADC_CLK from PCLKx.

(5) The test was carried out under the TBD power supply mode.

Table 4-43. ADC dynamic accuracy at f_{ADC} = 42 MHz V_{DDA} = 3.3 V(1)(2)(3)(4)(5)

Symbol	Parameter	Test conditions		Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 42 MHz V_{DDA} = V_{REFP} =3.3 V Input Frequency = 20 kHz	Single ended	TBD	TBD	-	bits
SNDR	Signal-to-noise and distortion ratio		Single ended	TBD	TBD	-	dB
SNR	Signal-to-noise ratio		Single ended	TBD	TBD	-	
THD	Total harmonic distortion		Single ended	-	TBD	TBD	

(1) Value guaranteed by characterization, not 100% tested in production.

(2) Results for TBD packages. The values for other packages might differ.

(3) V_{DD} = V_{DDA} = V_{REFP}= TBD, external V_{REF} were adopted.

(4) System clock = TBD, PCLKx = TBD, ADC_CLK from PCLKx.

(5) The test was carried out under the TBD power supply mode.

Table 4-44. ADC dynamic accuracy at f_{ADC} = 42 MHz V_{DDA} = 2.4 V(1)(2)(3)(4)(5)

Symbol	Parameter	Test conditions		Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 42 MHz	Single ended	TBD	TBD	-	bits
SNDR	Signal-to-noise and	V_{DDA} = V_{REFP} =2.4 V	Single ended	TBD	TBD	-	dB

Symbol	Parameter	Test conditions		Min	Typ	Max	Unit
	distortion ratio	Input Frequency = 20 kHz					
SNR	Signal-to-noise ratio		Single ended	TBD	TBD	-	
THD	Total harmonic distortion		Single ended	-	TBD	TBD	

(1) Value guaranteed by characterization, not 100% tested in production.
(2) Results for TBD packages. The values for other packages might differ.
(3) V_{DD} = V_{DDA} = V_{REFP}= TBD, external V_{REF} were adopted.
(4) System clock = TBD, PCLKx = TBD, ADC_CLK from PCLKx.
(5) The test was carried out under the TBD power supply mode.

Table 4-45. ADC static accuracy at f_{ADC} = 14 MHz V_{DDA} = 1.71 V(1)(2)(3)(4)(5)

Symbol	Parameter	Test conditions		Typ	Max	Unit
Offset	Offset error	f_{ADC} = 14 MHz V_{DDA} = V_{REFP} = 1.71 V	Single ended	TBD	TBD	LSB
DNL	Differential linearity error		Single ended	TBD	TBD	
INL	Integral linearity error		Single ended	TBD	TBD	

(1) Value guaranteed by characterization, not 100% tested in production.
(2) Results for TBD packages. The values for other packages might differ.
(3) V_{DD} = V_{DDA} = V_{REFP}= TBD, external V_{REF} were adopted.
(4) System clock = TBD, PCLKx = TBD, ADC_CLK from PCLKx.
(5) The test was carried out under the TBD power supply mode.

Table 4-46. ADC static accuracy at f_{ADC} = 42 MHz V_{DDA} = 3.3 V(1)(2)(3)(4)(5)

Symbol	Parameter	Test conditions		Typ	Max	Unit
Offset	Offset error	f_{ADC} = 42 MHz V_{DDA} = V_{REFP} = 3.3 V	Single ended	TBD	TBD	LSB
DNL	Differential linearity error		Single ended	TBD	TBD	
INL	Integral linearity error		Single ended	TBD	TBD	

(1) Value guaranteed by characterization, not 100% tested in production.
(2) Results for TBD packages. The values for other packages might differ.
(3) V_{DD} = V_{DDA} = V_{REFP}= TBD, external V_{REF} were adopted.
(4) System clock = TBD, PCLKx = TBD, ADC_CLK from PCLKx.
(5) The test was carried out under the TBD power supply mode.

Table 4-47. ADC static accuracy at f_{ADC} = 42 MHz V_{DDA} = 2.4 V(1)(2)(3)(4)(5)

Symbol	Parameter	Test conditions		Typ	Max	Unit
Offset	Offset error	f_{ADC} = 42 MHz V_{DDA} = V_{REFP} = 2.4 V	Single ended	TBD	TBD	LSB
DNL	Differential linearity error		Single ended	TBD	TBD	
INL	Integral linearity error		Single ended	TBD	TBD	

(1) Value guaranteed by characterization, not 100% tested in production.
(2) Results for TBD packages. The values for other packages might differ.
(3) V_{DD} = V_{DDA} = V_{REFP}= TBD, external V_{REF} were adopted.
(4) System clock = TBD, PCLKx = TBD, ADC_CLK from PCLKx.
(5) The test was carried out under the TBD power supply mode.

4.21. DAC characteristics

Table 4-48. DAC characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Operating voltage	-		1.71	3.3	3.6	V
V_{REFP}	Positive Reference Voltage	-		1.71	-	V_{DDA}	V
V_{REFN}	Negative Reference Voltage	-		-	V_{SSA}	-	V
R_{LOAD}	Load resistance	Resistive load with buffer ON	connected to V_{SSA}	5	-	-	kΩ
			connected to V_{DDA}	5	-	-	
Ro	Impedance output	Impedance output with buffer OFF		-	-	15	kΩ
C_{LOAD}	Load capacitance	No pin/pad capacitance included		-	-	50	pF
DAC_OUT min	Voltage on DAC_OUT output	buffer OFF		1LSB	-	V_{DDA}-1LSB	V
		buffer ON		0.2	-	V_{DDA}-0.2	V
I_{DDA}	DAC current consumption in quiescent mode	DAC output buffer ON	No load, middle code (0x800) , V_{REFP} = 3.6 V	-	430	-	uA
			No load, worst code (0xF1C) , V_{REFP} = 3.6 V	-	450	-	
		DAC output buffer OFF	No load, middle (0x800) , V_{REFP} = 3.6 V	-	0.1	-	
$I_{DDVREFP}$	DAC current consumption in quiescent mode	DAC output buffer ON	No load, middle code (0x800) , V_{REFP} = 3.6 V	-	87	-	uA
			No load, worst code (0xF1C) , V_{REFP} = 3.6 V	-	45	-	
		DAC output buffer OFF	No load, middle code (0x800) , V_{REFP} = 3.6 V	-	85	-	
DNL(2)	Differential non-linearity Error	DAC output buffer ON		-	TBD	-	LSB
		DAC output buffer OFF		-	TBD	-	
INL(2)	Integral non-linearity	DAC output buffer ON		-	TBD	-	LSB
		DAC output buffer OFF		-	TBD	-	

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Offset(2)	Offset error	DAC output buffer ON		-	TBD	-	LSB
		DAC output buffer OFF		-	TBD	-	
GE(2)	Gain error	DAC output buffer ON		-	TBD	-	%
		DAC output buffer OFF		-	TBD	-	
$T_{setting}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches the final value of +/-1LSB, +/-2LSB, +/-4LSB, +/-8LSB)	Normal mode, DAC output buffer ON, C_L <= 50 pF, R_L >= 5 kΩ	+/-1 LSB	-	1..26	-	µs
			+/-2 LSB	-	1.24	-	
			+/-4 LSB	-	1.22	-	
			+/-8 LSB	-	1.2	-	
		Normal mode, DAC output buffer OFF, +/-1LSB C_L = 10 pF		-	2	-	-
T_{wakeup}	Wakeup time from off state (setting the ENx bit in the DAC Control register) until the final value of +/-1LSB is reached	Normal mode, DAC output buffer ON, CL <= 50 pF, RL = 5 kΩ		-	5	10	µs
		Normal mode, DAC output buffer OFF, CL <= 10 pF		-	3	6	
Update rate	Max frequency for a correct DAC_OUT change from code i to i+/-1LSBs	C_{LOAD} <= 50 pF, R_{LOAD} >= 5 kΩ		-	-	4	MS/s
$PSRR_{DAC}$	Power supply rejection ratio (to V_{DDA})	-		70	90	-	dB
T_cal	Middle code offset trim time	Minimum time to verify the each code		200	-	-	µs

(1) Value guaranteed by design, not 100% tested in production.

(2) Value guaranteed by characterization, not 100% tested in production.

4.22. Comparators characteristics

Table 4-49. CMP characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
t_D	Propagation delay	V_{STEP} = 200 mV	-	11.5	-	ns
		Full Range	-	16.8	-	
$t_{SU(CMP)}$	Setup time	-	-	0.4	-	µs
$I_{DDA(CMP)}$	Current consumption from V_{DDA}	-	-	289	-	µA
I_{LEAK}	Leakage Current	-	-	2.5	-	nA
V_{OFFSET}	Offset voltage	-	-	1.5	-	mV

Symbol	Description	Conditions	Min	Typ	Max	Unit
$V_{HYST(CMP)}$	Hysteresis Voltage	Low Hysteresis	-	15.1	-	mV
		Medium Hysteresis	-	30.5	-	
		High Hysteresis	-	46.2	-	

(1) Value guaranteed by design, not 100% tested in production.

4.23. I2C characteristics

Table 4-50. I2C characteristics(1)(2)

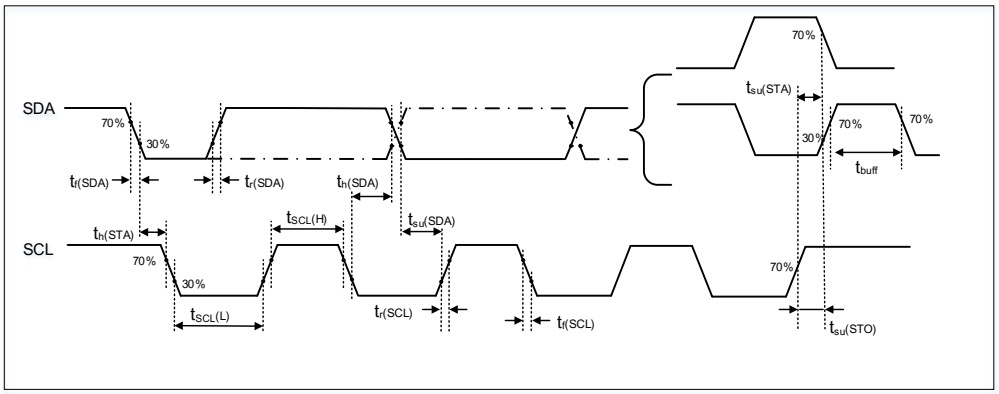
Symbol	Description	Conditions	Standard mode		Fast mode		Fast mode plus		Unit
			Min	Max	Min	Max	Min	Max	
$t_{SCL(H)}$	SCL clock high time	-	4.0	-	0.6	-	0.2	-	μs
$t_{SCL(L)}$	SCL clock low time	-	4.7	-	1.3	-	0.5	-	μs
$t_{SU(SDA)}$	SDA setup time	-	250	-	100	-	50	-	ns
$t_{H(SDA)}$	SDA data hold time	-	0(3)	3450	0(3)	900	0	450	ns
$t_{R(SDA/SCL)}$	SDA and SCL rise time	-	-	1000	-	300	-	120	ns
$t_{F(SDA/SCL)}$	SDA and SCL fall time	-	-	300	-	300	-	120	ns
$t_{H(STA)}$	Start condition hold time	-	4.0	-	0.6	-	0.26	-	μs
$t_{SU(STA)}$	Repeated Start condition setup time	-	4.7	-	0.6	-	0.26	-	μs
$t_{SU(STO)}$	Stop condition setup time	-	4.0	-	0.6	-	0.26	-	μs
t_{BUFF}	Stop to Start condition time (bus free)	-	4.7	-	1.3	-	0.5	-	μs

(1) Value guaranteed by design, not 100% tested in production.

(2) To ensure the standard mode I2C frequency, f_{PCLK1} must be at least 2 MHz. To ensure the fast mode I2C frequency, f_{PCLK1} must be at least 4 MHz. To ensure the fast mode plus I2C frequency, f_{PCLK1} must be at least a multiple of 10 MHz.

(3) The device should provide a data hold time of 300 ns at least in order to bridge the undefined region of the falling edge of SCL.

Figure 4-15. I2C bus timing diagram



4.24. SPI characteristics

Table 4-51. Standard SPI characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	-	-	-	40	MHz
$t_{SCK(H)}$	SCK clock high time	Master mode, f_{PCLKx} = 80 MHz, presc = 2	-	12.5	-	ns
$t_{SCK(L)}$	SCK clock low time	Master mode, f_{PCLKx} = 80 MHz, presc = 2	-	12.5	-	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time	-	-	-	9.7	ns
$t_{SU(MI)}$	Data input setup time	-	6	-	-	ns
$t_{H(MI)}$	Data input hold time	-	3	-	-	ns
SPI slave mode						
$t_{SU(NSS)}$	NSS enable setup time	-	12.5	-	-	ns
$t_{H(NSS)}$	NSS enable hold time	-	12.5	-	-	ns
$t_{A(SO)}$	Data output access time	-	-	12.5	-	ns
$t_{DIS(SO)}$	Data output disable time	-	-	1	-	ns
$t_{V(SO)}$	Data output valid time	-	-	8	-	ns
$t_{SU(SI)}$	Data input setup time	-	0	-	-	ns
$t_{H(SI)}$	Data input hold time	-	0	-	-	ns

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-16. SPI timing diagram - master mode

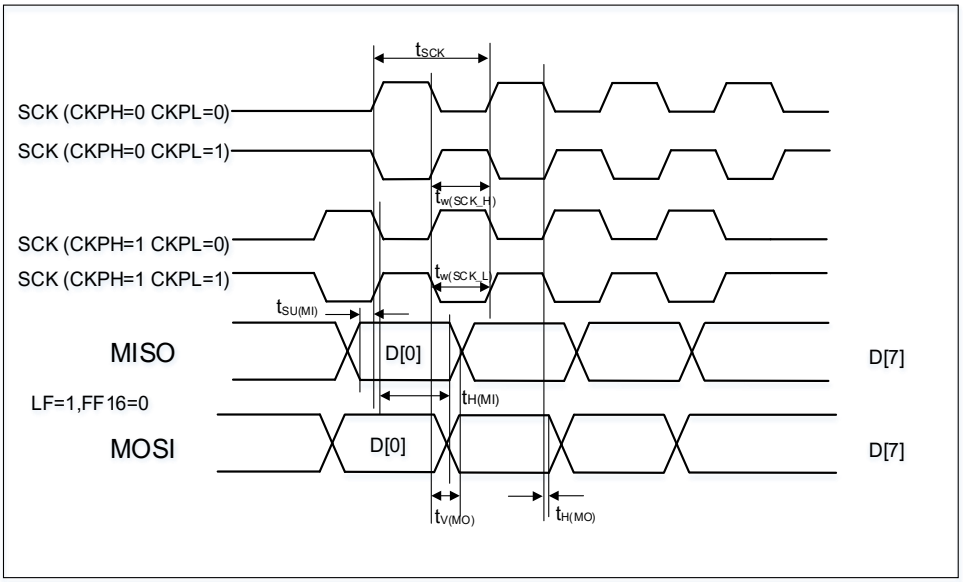


Figure 4-17. SPI timing diagram - slave mode(CKPH=0)

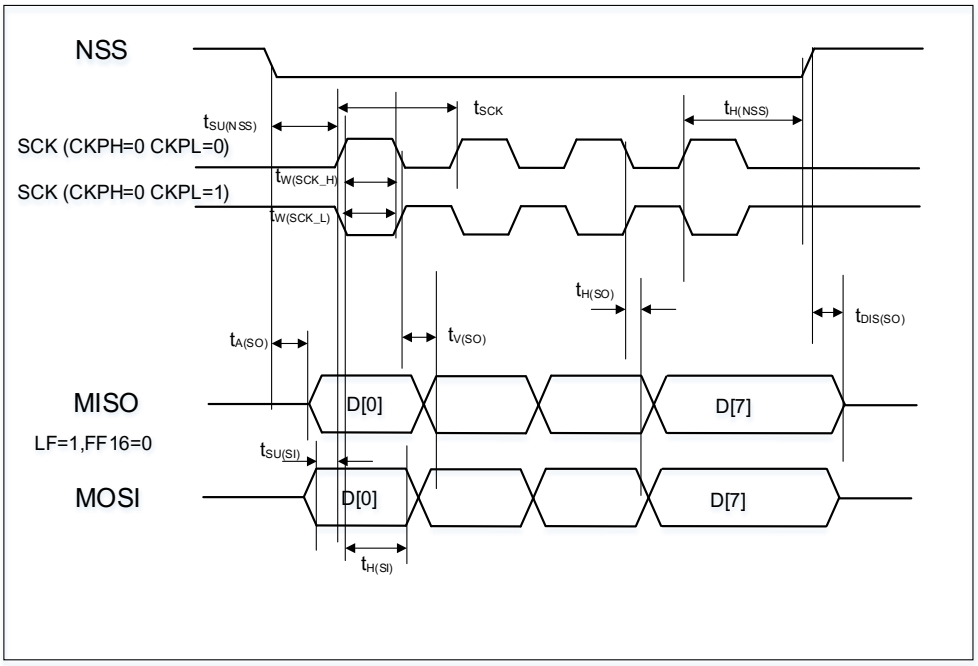
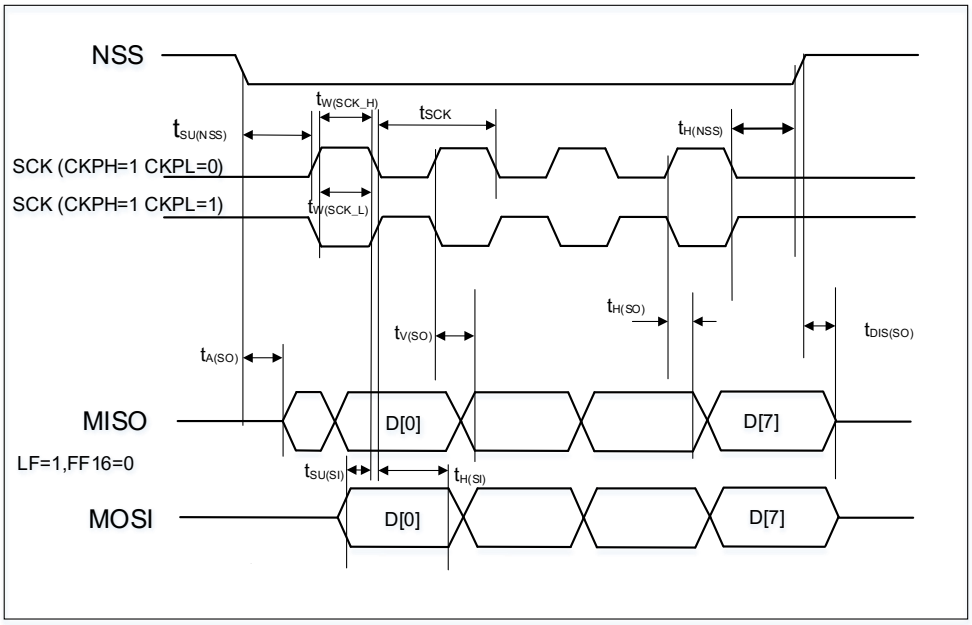


Figure 4-18. SPI timing diagram - slave mode(CKPH=1)



4.25. OSPI characteristics

Table 4-52. Standard OSPI characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SDR mode						
f_{SCK}	SCK clock frequency	-	-	-	100	MHz
$t_{SCK(H)}$	SCK clock high time, even division	-	$t_{(CK)}/2$	-	$t_{(CK)}/2+1$	ns
	SCK clock high time, odd division	-	$(n/2)*t_{(CK)}/(n+1)$	-	$(n/2)*t_{(CK)}/(n+1)+1$	ns
$t_{SCK(L)}$	SCK clock high time, even division	-	$t_{(CK)}/2-1$	-	$t_{(CK)}/2$	ns
	SCK clock high time, odd division	-	$(n/2+1)*t_{(CK)}/(n+1)-1$	-	$(n/2+1)*t_{(CK)}/(n+1)$	ns
$t_{V(MO)}$	Data output valid time	-	-	-	2	ns
$t_{H(MO)}$	Data output hold time	-	0	-	-	ns
$t_{SU(MI)}$	Data input setup time	-	0	-	-	ns
$t_{H(MI)}$	Data input hold time	-	-	-	10	ns
DTR mode (no DQS)						
f_{SCK}	SCK clock frequency	-	-	-	100	MHz
$t_{SCK(H)}$	SCK clock high time, even division	-	$t_{(CK)}/2$	-	$t_{(CK)}/2+1$	ns
	SCK clock high time, odd division	-	$(n/2)*t_{(CK)}/(n+1)$	-	$(n/2)*t_{(CK)}/(n+1)+1$	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SCK(L)}$	SCK clock high time, even division	-	$t_{(CK)}/2-1$	-	$t_{(CK)}/2$	ns
	SCK clock high time, odd division	-	$(n/2+1)*t_{(CK)}/(n+1)-1$	-	$(n/2+1)*t_{(CK)}/(n+1)$	ns
$t_{VR(SO)}$ $t_{VF(SO)}$	Data output valid time	DHQC = 1, Prescaler = 1,2 ...	-	$t_{pclk}/4+1$	$t_{pclk}/4+1.25$	ns
$t_{HR(SO)}$ $t_{HF(SO)}$	Data output hold time	DHQC = 1, Prescaler = 1,2 ...	$t_{pclk}/4$	-	-	ns
$t_{SUR(SI)}$ $t_{SUF(SI)}$	Data input setup time	-	0	-	-	ns
$t_{HR(SI)}$ $t_{HF(SI)}$	Data input hold time	-	-	-	5	ns
DTR mode (with DQS)						
f_{SCK}	SCK clock frequency	-	-	-	100	MHz
$t_{SCK(H)}$	SCK clock high time, even division	-	$t_{(CK)}/2$	-	$t_{(CK)}/2+1$	ns
	SCK clock high time, odd division	-	$(n/2)*t_{(CK)}/(n+1)$	-	$(n/2)*t_{(CK)}/(n+1)+1$	ns
$t_{SCK(L)}$	SCK clock high time, even division	-	$t_{(CK)}/2-1$	-	$t_{(CK)}/2$	ns
	SCK clock high time, odd division	-	$(n/2+1)*t_{(CK)}/(n+1)-1$	-	$(n/2+1)*t_{(CK)}/(n+1)$	ns
$t_{v(CK)}$	Clock valid time	-	-	-	$t_{(CK)}+t_{(CK)}/2$	ns
$t_{h(CK)}$	Clock hold time	-	$t_{(CK)}/2$	-	-	ns
$t_{w(CS)}$	Chip select high time	-	$3*t_{(CK)}$	-	-	ns
$t_{VR(SO)}$ $t_{VF(SO)}$	Data output valid time	DHQC = 1, Prescaler = 1,2 ...	-	$t_{pclk}/4+1$	$t_{pclk}/4+1.25$	ns
$t_{HR(SO)}$ $t_{HF(SO)}$	Data output hold time	DHQC = 1, Prescaler = 1,2 ...	$t_{pclk}/4$	-	-	ns
$t_{SUR(SI)}$ $t_{SUF(SI)}$	Data input setup time	-	0	-	-	ns
$t_{HR(SI)}$ $t_{HF(SI)}$	Data input hold time	-	-	-	5	ns

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-19. OSPI timing diagram - SDR mode

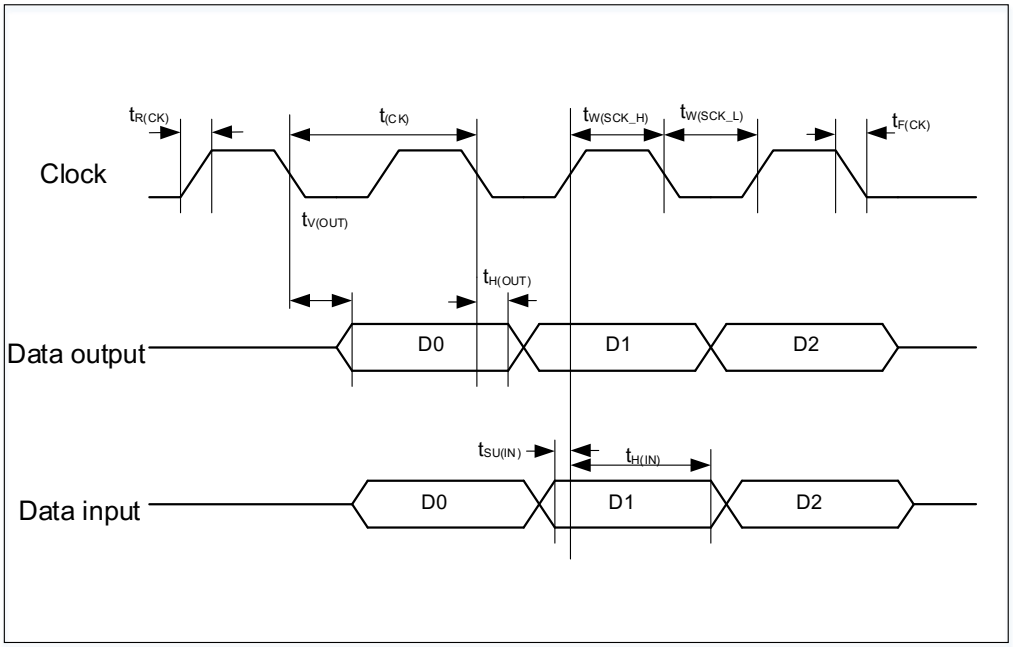
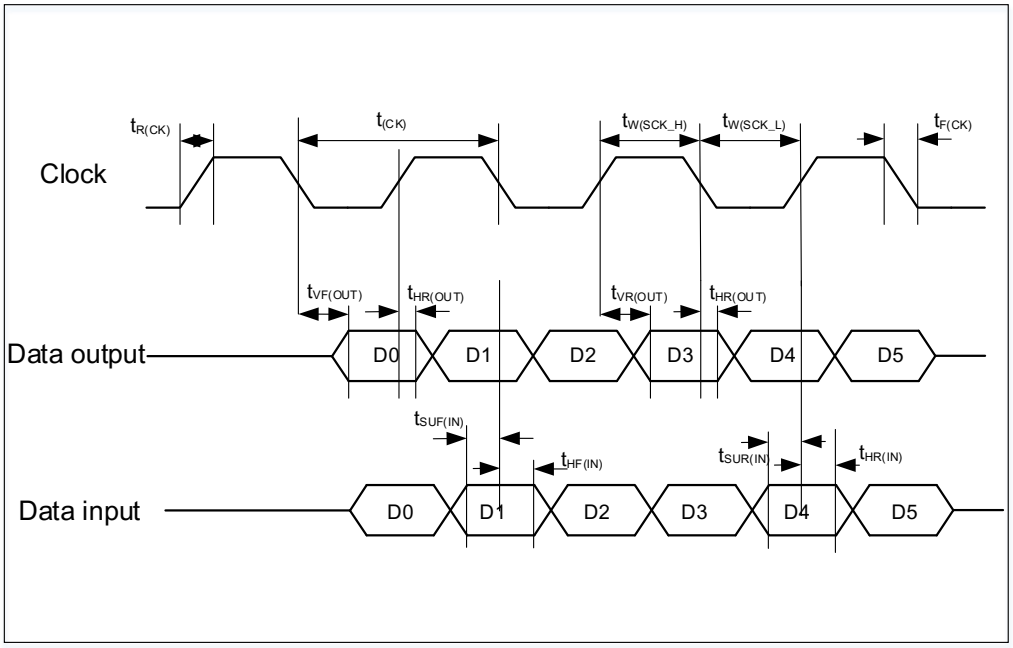


Figure 4-20. OSPI timing diagram - DTR mode



4.26. I2S characteristics

Table 4-53. I2S characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{SCK}	Clock frequency	Master mode (data: 16 bits,	-	3	-	MHz

Symbol	Description	Conditions	Min	Typ	Max	Unit
		Audio frequency = 96 kHz)				
		Slave mode	-	-	10	
t_H	Clock high time	-	-	166	-	ns
t_L	Clock low time	-	-	166	-	ns
$t_{V(WS)}$	WS valid time	Master mode	0	-	-	ns
$t_{H(WS)}$	WS hold time	Master mode	0	-	-	ns
$t_{SU(WS)}$	WS setup time	Slave mode	0	-	-	ns
$t_{H(WS)}$	WS hold time	Slave mode	2	-	-	ns
$Ducy_{(SCK)}$	I2S slave input clock duty cycle	Slave mode	-	50	-	%
$t_{SU(SD_MR)}$	Data input setup time	Master mode	2	-	-	ns
$t_{SU(SD_SR)}$	Data input setup time	Slave mode	0	-	-	ns
$t_{H(SD_MR)}$	Data input hold time	Master receiver	0	-	-	ns
$t_{H(SD_SR)}$		Slave receiver	1	-	-	ns
$t_{V(SD_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	-	12	ns
$t_{H(SD_ST)}$	Data output hold time	Slave transmitter (after enable edge)	7	-	-	ns
$t_{V(SD_MT)}$	Data output valid time	Master transmitter (after enable edge)	-	-	7	ns
$t_{H(SD_MT)}$	Data output hold time	Master transmitter (after enable edge)	4	-	-	ns

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-21. I2S timing diagram - master mode

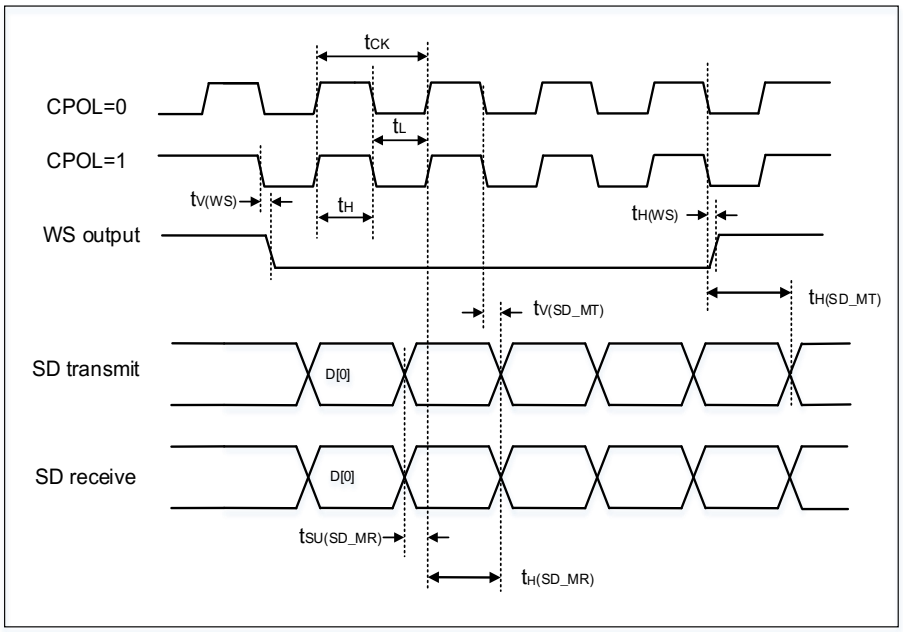
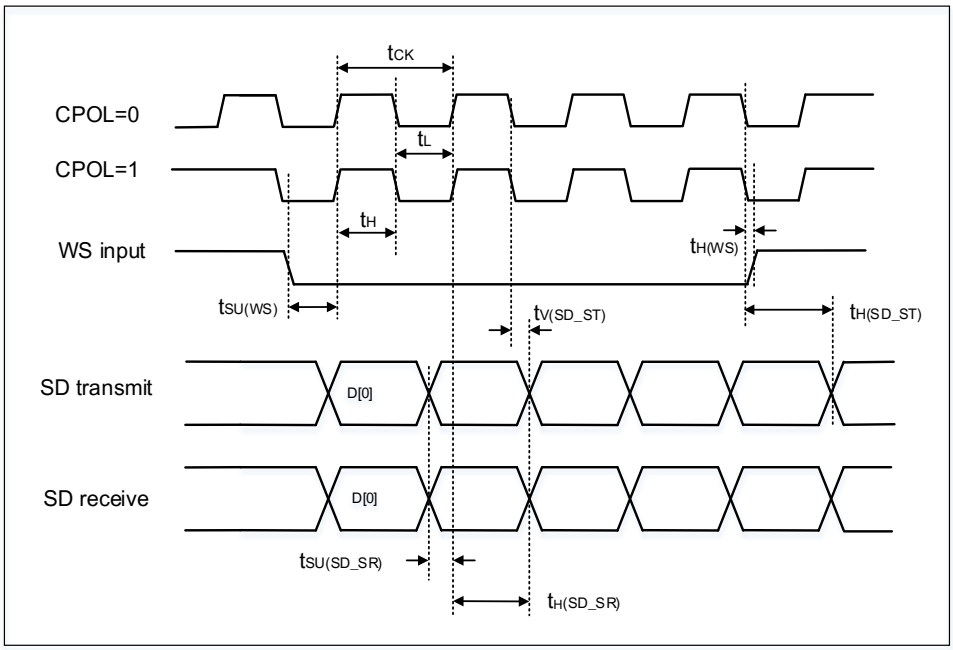


Figure 4-22. I2S timing diagram - slave mode



4.27. USART characteristics

Table 4-54. USART / UART characteristics in Synchronous mode(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	f_{PCLK2} =252 MHz	-	-	f_{PCLK2} / 8	MHz
$t_{SCK(H)}$	SCK clock high time		16	-	-	ns
$t_{SCK(L)}$	SCK clock low time		16	-	-	ns

(1) Value guaranteed by design, not 100% tested in production.

Table 4-55. USART0 characteristics in Smartcard mode(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	f_{PCLK2} =252 MHz	-	-	f_{PCLK2} / 2	MHz
$t_{SCK(H)}$	SCK clock high time		4	-	-	ns
$t_{SCK(L)}$	SCK clock low time		4	-	-	ns

(1) Value guaranteed by design, not 100% tested in production.

4.28. EXMC characteristics

Table 4-56. Asynchronous multiplexed PSRAM/NOR read timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	$7*t_{fclk}$-1	$7*t_{fclk}$+1	ns
$t_{V(NOE_NE)}$	EXMC_NEx low to EXMC_NOE low	$3*t_{fclk}$-1	-	ns
$t_{w(NOE)}$	EXMC_NOE low time	$4*t_{fclk}$-1	$4*t_{fclk}$+1	ns

$t_{h(NE_NOE)}$	EXMC_NOE high to EXMC_NE high hold time	0	-	ns
$t_{v(A_NE)}$	EXMC_NEx low to EXMC_A valid	0	-	ns
$t_{v(A_NOE)}$	Address hold time after EXMC_NOE high	0	-	ns
$t_{v(BL_NE)}$	EXMC_NEx low to EXMC_BL valid	0	-	ns
$t_{h(BL_NOE)}$	EXMC_BL hold time after EXMC_NOE high	0	-	ns
$t_{su(DATA_NE)}$	Data to EXMC_NEx high setup time	$4*t_{fclk}-1$	-	ns
$t_{su(DATA_NOE)}$	Data to EXMC_NOEx high setup time	$4*t_{fclk}-1$	-	ns
$t_{h(DATA_NOE)}$	Data hold time after EXMC_NOE high	0	-	ns
$t_{h(DATA_NE)}$	Data hold time after EXMC_NEx high	0	-	ns
$t_{v(NADV_NE)}$	EXMC_NEx low to EXMC_NADV low	0	-	ns
$t_{w(NADV)}$	EXMC_NADV low time	$t_{fclk}-1$	$t_{fclk}+1$	ns
$T_{h(AD_NADV)}$	EXMC_AD(adress) valid hold time after EXMC_NADV high	$t_{fclk}-1$	$t_{fclk}+1$	ns

(1) C_L = 30 pF.

(2) Value guaranteed by design, not 100% tested in production.

(3) Based on configure: t_{fclk} = 1 / f_{HCLK}, AddressSetupTime = 0, AddressHoldTime = 1, DataSetupTime = 1.

Table 4-57. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	$5*t_{fclk}-1$	$5*t_{fclk}+1$	ns
$t_{V(NWE_NE)}$	EXMC_NEx low to EXMC_NWE low	$t_{fclk}-1$	-	ns
$t_{w(NWE)}$	EXMC_NWE low time	$3*t_{fclk}-1$	$3*t_{fclk}+1$	ns
$t_{h(NE_NWE)}$	EXMC_NWE high to EXMC_NE high hold time	$t_{fclk}-1$	-	ns
$t_{v(A_NE)}$	EXMC_NEx low to EXMC_A valid	0	-	ns
$t_{V(NADV_NE)}$	EXMC_NEx low to EXMC_NADV low	0	-	ns
$t_{w(NADV)}$	EXMC_NADV low time	$t_{fclk}-1$	$t_{fclk}+1$	ns
$t_{h(AD_NADV)}$	EXMC_AD(address) valid hold time after EXMC_NADV high	$t_{fclk}-1$	-	ns
$t_{h(A_NWE)}$	Address hold time after EXMC_NWE high	$t_{fclk}-1$	-	ns
$t_{h(BL_NWE)}$	EXMC_BL hold time after EXMC_NWE high	$t_{fclk}-1$	-	ns
$t_{v(BL_NE)}$	EXMC_NEx low to EXMC_BL valid	0	-	ns
$t_{v(DATA_NADV)}$	EXMC_NADV high to DATA valid	$t_{fclk}-1$	-	ns
$t_{h(DATA_NWE)}$	Data hold time after EXMC_NWE high	$t_{fclk}-1$	-	ns

(1) C_L = 30 pF.

(2) Value guaranteed by design, not 100% tested in production.

(3) Based on configure: f_{HCLK} = 252 MHz, AddressSetupTime = 0, AddressHoldTime = 1, DataSetupTime = 1.

Table 4-58. Synchronous multiplexed PSRAM/NOR read timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	EXMC_CLK period	t_{exmc_clk}	-	ns
$t_{d(CLKL-NExL)}$	EXMC_CLK low to EXMC_NEx low	0	-	ns
$t_{d(CLKH-NExH)}$	EXMC_CLK high to EXMC_NEx high	$2*t_{fclk}-1$	-	ns
$t_{d(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	-	ns
$t_{d(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	-	ns
$t_{d(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	0	-	ns

$t_{d(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	$2*t_{fclk}-1$	-	ns
$t_{d(CLKL-NOEL)}$	EXMC_CLK low to EXMC_NOE low	0	-	ns
$t_{d(CLKH-NOEH)}$	EXMC_CLK high to EXMC_NOE high	$2*t_{fclk}-1$	-	ns
$t_{d(CLKL-ADV)}$	EXMC_CLK low to EXMC_AD valid	0	-	ns
$t_{d(CLKL-ADIV)}$	EXMC_CLK low to EXMC_AD invalid	0	-	ns

(1) C_L = 30 pF.

(2) Value guaranteed by design, not 100% tested in production.

(3) Based on configure: f_{HCLK} = 252 MHz, BurstAccessMode = Enable; Memory Type = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); Data Latency = 1.

Table 4-59. Synchronous multiplexed PSRAM write timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	EXMC_CLK period	t_{exmc_clk}	-	ns
$t_{d(CLKL-NExL)}$	EXMC_CLK low to EXMC_NEx low	0	-	ns
$t_{d(CLKH-NExH)}$	EXMC_CLK high to EXMC_NEx high	$2*t_{fclk}-1$	-	ns
$t_{d(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	-	ns
$t_{d(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	-	ns
$t_{d(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	0	-	ns
$t_{d(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	$2*t_{fclk}-1$	-	ns
$t_{d(CLKL-NWEL)}$	EXMC_CLK low to EXMC_NWE low	0	-	ns
$t_{d(CLKH-NWEH)}$	EXMC_CLK high to EXMC_NWE high	$2*t_{fclk}-1$	-	ns
$t_{d(CLKL-ADIV)}$	EXMC_CLK low to EXMC_AD invalid	0	-	ns
$t_{d(CLKL-DATA)}$	EXMC_A/D valid data after EXMC_CLK low	0	-	ns
$t_{h(CLKL-NBLH)}$	EXMC_CLK low to EXMC_NBL high	0	-	ns

(1) C_L = 30 pF.

(2) Value guaranteed by design, not 100% tested in production.

(3) Based on configure: f_{HCLK} = 252 MHz, BurstAccessMode = Enable; MemoryType = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); DataLatency = 1.

4.29. USBFS characteristics

Table 4-60. USBFS DC electrical characteristics(1)

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}		USB operating voltage	-	3.0	-	3.6	V
LS/FS FUNCTIONALITY							
Input levels	V_{DIFS}	Differential input sensitivity(FS/LS)	-	0.2	-	-	V
	V_{CMFS}	Differential common mode range(FS/LS)	Includes V_{DI} range	0.8	-	2.5	
	V_{ILSE}	Single ended receiver low level input voltage (FS/LS)	-	-	-	0.8	
	V_{IHSE}	Single ended receiver high level input voltage (FS/LS)	-	2.0	-	-	
Output levels	V_{OLFS}	Static output level low(FS/LS)	R_L of 1.5 kΩ to V_{DD}	-	-	0.3	V
	V_{OHFS}	Static output level high(FS/LS)	R_L of 15 kΩ to V_{SS}	2.8	-	-	
R_{PD}		PA11, PA12(USBFS_DM/DP)	V_{IN} = V_{DD}	-	21	-	kΩ
R_{PU}		PA11, PA12(USBFS_DM/DP)	V_{IN} = V_{SS}	-	1.5	-	
Z_{FSDRV}(2)		Driver Output Impedance	Steady state drive	6	-	22	Ω

(1) Value guaranteed by design, not 100% tested in production.

(2) In practical implementations, 22 Ω resistors should be connected in series with the USB signal traces on the PCB.

Table 4-61. USBFS AC electrical characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
t_R	Rise time	C_L = 50 pF, 10% to 90%	4	-	20	ns
t_F	Fall time	C_L = 50 pF, 10% to 90%	4	-	20	ns
t_{RFM}	Rise / fall time matching	t_R / t_F	90	-	110	%

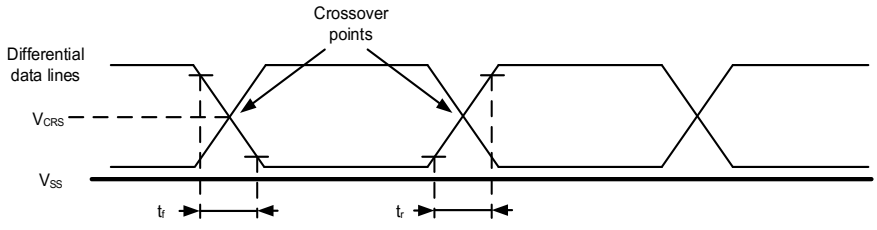
(1) Value guaranteed by design, not 100% tested in production.

Table 4-62. USBFS start up time(1)

Symbol	Description	Max	Unit
$t_{ST(USBFS)}$	USBFS startup time	1	µs

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-23. USBFS timings: definition of data signal rise and fall time



4.30. SDIO characteristics

Table 4-63. SDIO characteristics(1)(2)(3)

Symbol	Mode	Description	Conditions	Min	Typ	Max	Unit
f_{PP}	-	Clock frequency in data transfer mode	-	0.0936	-	48	MHz
$t_{W(CKL)}$		Clock low time	f_{pp} = 48 MHz	7	-	-	ns
$t_{W(CKH)}$		Clock high time		7	-	-	ns
t_{ISU}	CMD,MMC and SD HS mode	D input setup time HS(4)	f_{pp} = 48 MHz	5.8	-	-	ns
t_{IH}		D input hold time HS(4)		2.5	-	-	ns
t_{OV}		D output valid time HS(4)		-	-	9.6	ns
t_{OH}		D output hold time HS(4)		2	-	-	ns
t_{ISUD}	CMD,SD default mode	D input setup time SD(4)	f_{pp} = 24 MHz	5.8	-	-	ns
t_{IHD}		D input hold time SD(4)		2.5	-	-	ns
t_{OVD}		D output valid default time SD(4)		-		9.6	ns
t_{OHD}		D output hold default time SD(4)		2	-	-	ns

(1) CLK timing is measured at 50% of V_{DD}.
(2) Capacitive load C_L = 30 pF.
(3) Value guaranteed by design, not 100% tested in production.
(4) D Output/Input are referenced to CK.

4.31. CAN characteristics

Refer to ***Table 4-32. I/O port static characteristics*** for more details on the input/output alternate function characteristics (CAN TX and CAN RX).

4.32. TIMER characteristics

Table 4-64. TIMER characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{res}	Timer resolution time	-	1	-	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 252 MHz	3.97	-	ns
f_{EXT}	Timer external clock frequency	-	0	$f_{TIMERxCLK}$/2	MHz
		$f_{TIMERxCLK}$ = 252 MHz	0	126	MHz
RES	Timer resolution	TIMERx (except TIMER1)	-	16	bit
		TIMER1	-	32	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	-	1	65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 252 MHz	0.00397	260.06	μs

Symbol	Parameter	Conditions	Min	Max	Unit
	32-bit counter clock period when internal clock is selected	-	1	4294967296	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 252 MHz	0.00397	17043521.02	μs
t_{MAX_COUNT}	Maximum possible count (16-bit except TIMER1)	-	-	4294967296	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 252 MHz	-	17.04352102	s
	Maximum possible count (32-bit TIMER1)	-	-	2.81475E+14	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 252 MHz	-	310.2678315	h

(1) Value guaranteed by design, not 100% tested in production.

4.33. WDGT characteristics

Table 4-65. FWDGT min/max timeout period at 40 kHz (IRC40K)(1)

Prescaler divider	PSC[3:0] bits	Min timeout RLD[11:0] = 0x000	Max timeout RLD[11:0] = 0xFFF	Unit
1/4	0000	0.1	409.6	ms
1/8	0001	0.2	819.2	
1/16	0010	0.4	1638.4	
1/32	0011	0.8	3276.8	
1/64	0100	1.6	6553.6	
1/128	0101	3.2	13107.2	
1/256	0110	6.4	26214.4	
1/512	0111	12.8	52,428.8	
1/1024	1000	25.6	104,857.6	
1/2048	1001	51.2	209,715.2	
1/4096	1010	102.4	419,430.4	
1/8192	1011	204.8	838,860.8	
1/16384	1100	409.6	1,677,721.6	
1/32768	1101	819.2	3355443.2	
1/65536	1110	1638.4	6710886.4	
1/131072	1111	3276.8	13421772.8	

(1) Value guaranteed by design, not 100% tested in production.

Table 4-66. WWDGT min-max timeout value at 100 MHz (f_{PCLK1})(1)

Prescaler divider	PSC[4:0]	Min timeout value CNT[6:0] = 0x40	Unit	Max timeout value CNT[6:0] = 0x7F	Unit
1/1	00000	0.04096		2.621	
1/2	00001	0.08192		5.243	
1/4	00010	0.16384		10.486	
1/8	00011	0.32768		20.972	
1/16	00100	0.655		41.943	
1/32	00101	1.31		83.886	
1/64	00110	2.621		167.772	
1/128	00111	5.243		335.544	
1/256	01000	10.486		671.089	
1/512	01001	20.972	ms	1342.177	ms
1/1024	01010	41.943		2684.355	
1/2048	01011	83.886		5368.709	
1/4096	01100	167.772		10737.42	
1/8192	01101	335.544		21474.84	
1/16384	01110	671.089		42949.67	
1/32768	01111	1342.177		85899.35	
1/65536	10000	2684.355		171798.7	
1/131072	10001	5368.709		343597.4	
1/262144	>=10010	10737.42		687194.8	

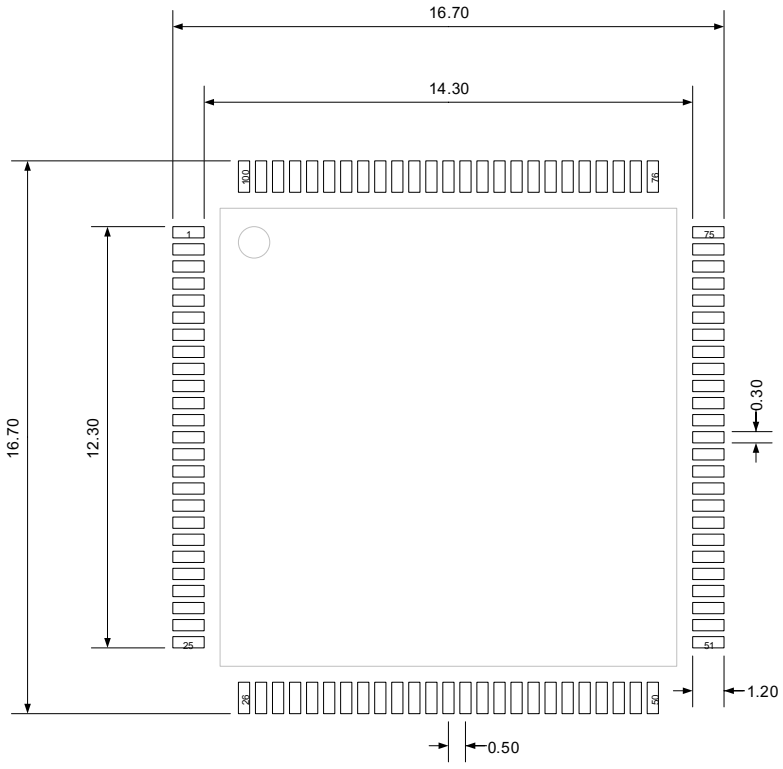
(1) Value guaranteed by design, not 100% tested in production.

5. Package information

Symbol	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
e	-	0.50	-
L	0.45	-	0.75
L1	-	1.00	-
θ	0°	-	7°

(Original dimensions are in millimeters)

Figure 5-1. LQFP100 recommended footprint



(Original dimensions are in millimeters)

5.1. LQFP64 package outline dimensions

Figure 5-2. LQFP64 package outline

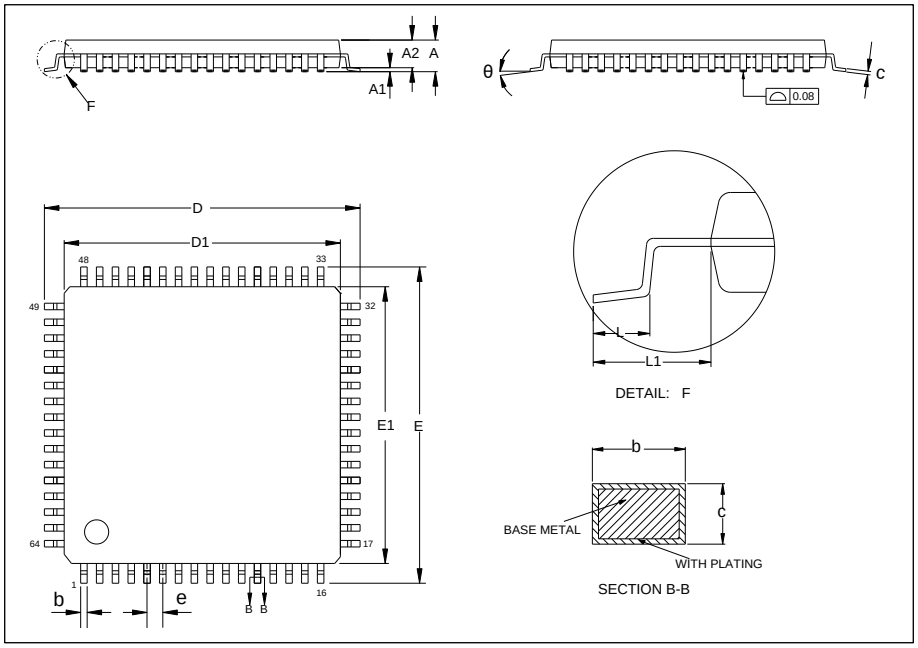
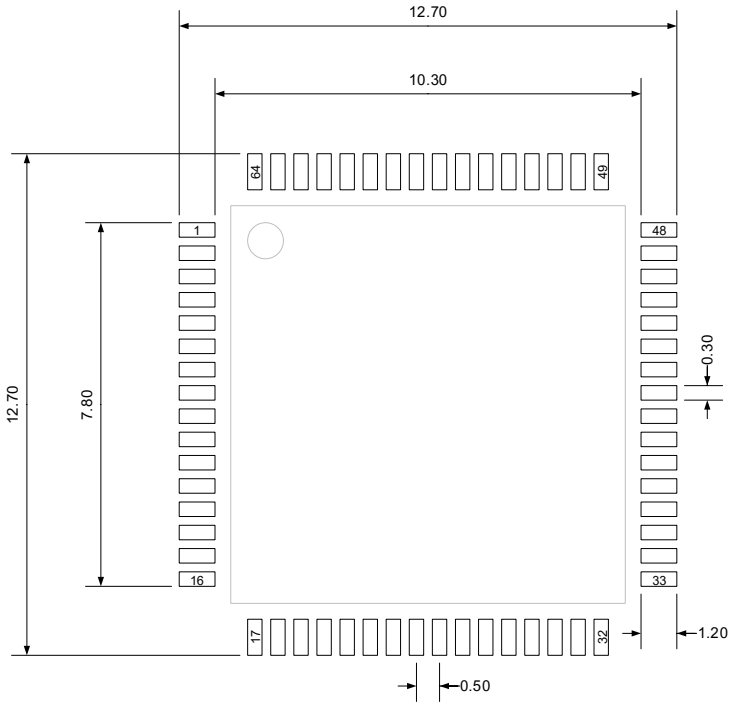


Table 5-1. LQFP64 package dimensions

Symbol	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.18	-	0.26
c	0.13	-	0.18
D	11.95	12.00	12.05
D1	9.90	10.00	10.10
E	11.95	12.00	12.05
E1	9.90	10.00	10.10
e	-	0.50	-
L	0.45	0.60	0.75
θ	0°	3.5°	7°

(Original dimensions are in millimeters)

Figure 5-3. LQFP64 recommended footprint



(Original dimensions are in millimeters)

5.2. Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter "θ". For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

θ_{JA}: Thermal resistance, junction-to-ambient.

θ_{JB}: Thermal resistance, junction-to-board.

θ_{JC}: Thermal resistance, junction-to-case.

Ψ_{JB}: Thermal characterization parameter, junction-to-board.

Ψ_{JT}: Thermal characterization parameter, junction-to-top center.

$$\theta_{JA}=(T_J-T_A)/P_D \quad (5\text{-}1)$$

$$\theta_{JB}=(T_J-T_B)/P_D \quad (5\text{-}2)$$

$$\theta_{JC}=(T_J-T_C)/P_D \quad (5\text{-}3)$$

Where, T_J = Junction temperature.

T_A = Ambient temperature

T_B = Board temperature

T_C = Case temperature which is monitoring on package surface

P_D = Total power dissipation

θ_{JA} represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower θ_{JA} can be considerate as better overall thermal performance.

θ_{JB} is used to measure the heat flow resistance between the chip surface and the PCB board.

θ_{JC} represents the thermal resistance between the chip surface and the package top case. θ_{JC} is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

Table 5-2. Package thermal characteristics(1)

Symbol	Condition	Package	Value	Unit
θ_{JA}	Natural convection, 2S2P PCB	LQFP64	48.42	°C/W
θ_{JB}	Cold plate, 2S2P PCB	LQFP64	28.17	°C/W
θ_{JC}	Cold plate, 2S2P PCB	LQFP64	17.56	°C/W
Ψ_{JB}	Natural convection, 2S2P PCB	LQFP64	27.61	°C/W
Ψ_{JT}	Natural convection, 2S2P PCB	LQFP64	1.49	°C/W

(1): Thermal characteristics are based on simulation, and meet JEDEC specification.

6. Ordering information

Table 6-1. Part ordering code for GD32E53Pxx devices

Ordering code	Flash (KB)	Package	Package type	Temperature operating range
GD32E53PRET6	512	LQFP64	Green	Industrial -40 °C to +85 °C

7. Revision history

Table 7-1. Revision history

Revision No.	Description	Date
0.9RC1	Initial Release	Nov.17, 2026

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