GigaDevice Semiconductor Inc.

GD32F10xxx
ARM® Cortex™-M3 32-bit MCU

Application Note
AN003

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1 Introduction

The GD32F10xxx family is based on the ARM Cortex-M3 core, and includes up to two 12-bit ADC modules with conversion rates up to 1 MHz. The 12-bit ADC can also be used with the DMA controller. Designing a system with a 12-bit ADC requires more attention than other lower resolution ADC systems. ADC accuracy also has an impact on the overall system quality and efficiency. You need to understand the differences associated with the ADC and the parameters affecting them.

GD32F10xxx User Manual has already provided detailed information on the ADC modules and explained how to use ADC modes and their applications. As a comparison, the purpose of this document is to highlight the differences and improve the application methods.

2 ADC power-on status

The ADC can be powered-on by setting the ADCON bit in ADC control register 2 (ADC_CTRL2), as shown in the following table. Once the ADCON bit is set for the first time, it wakes up the ADC from power down mode. **Conversion starts when ADCON bit is set by software after ADC power-on stabilization time (t_{STAB})**. You can stop conversion and put the ADC in power down mode again by resetting the ADCON bit.

ADC control register 2 (ADC_CTRL2)

Address offset: 0x08
Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								TSVRE	SWRCST	SWICST	ETERC	ETSRC[2:0]			Res.
								rw	rw	rw	rw	rw	rw	rw	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ETEIC	ETSIC[2:0]			DAL	Reserved		DMA	Reserved				RST CLB	CLB	CTN	ADCON
rw	rw	rw	rw	rw	Res.		rw					rw	rw	rw	rw

Bits	Fields	Descriptions
⋮	⋮	⋮
0	ADCON	ADC ON. The ADC will be wake up when this bit is changed from low to high and take a stabilization time. When this bit is high and “1” is written to it with other bits of this register unchanged, the conversion will start. 0: ADC disable and power down 1: ADC enable

2.1 ADCON operation regulation

- Step 1: If ADCON=0, ADC is power off.
- Step 2: Writing 1 to ADCON when ADCON=0, ADC will wake up and power on. **However, ADC needs a stabilization time t_{STAB} before ready.**
- Step 3: Writing 1 to ADCON when ADCON=1, the conversion will start. Note that in order to prevent incorrect operation, ADCON set 1 is invalid while writing other bits of ADC_CTRL2 register at the same time.
- Step 4: Writing 0 to ADCON when ADCON=1, the ADC will power down.

2.2 ADC power-on stabilization time (t_{STAB}) caculation

The ADC needs a stabilization time (t_{STAB}) before it starts converting accurately.
t_{STAB} can be calculated as following formula.

$$t_{STAB} \geq 14 \times t_{ADCClk}$$

Typical t_{STAB} value is shown as table below.

Table 1. Typical stabilization time t_{STAB} value

SysClk	ADC Prescaler	ADCClk	t_{ADCCLK}	t_{STAB}
72MHz	6	12MHz	1/12MHz	t_{STAB}>=1.17us
56MHz	6	14MHz	1/14MHz	t_{STAB}>=1us

3 ADC conversion end flag (EOC)

Once ADC Regular/Injected group channel conversion is complete, the End Of Conversion (EOC) flag in ADC status register (ADC_SR), as EOIC or EORC, is set by hardware automatically. The converted data is stored in the relevant 16-bit ADC data register. An EOIC or EORC interrupt is generated only on the end of the last channel conversion if the corresponding EOICIE or EORCIE bit of ADC control register 1 (ADC_CTRL1) is set.

The EOC flag should be cleared by software and can not be cleared by reading the 16-bit ADC data register simultaneously.

ADC status register (ADC_SR)

Address offset: 0x00

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											STRC	STIC	EOIC	EORC	AWE
											rc_w0	rc_w0	rc_w0	rc_w0	rc_w0

Bits	Fields	Descriptions
⋮	⋮	⋮
2	EOIC	End of inserted group conversion flag 0: No end of inserted group conversion 1: End of inserted group conversion
1	EORC	End of regular group conversion flag 0: No end of regular group conversion 1: End of regular group conversion
0	AWE	Analog watchdog event flag 0: No analog watchdog even 1: Analog watchdog event

4 ADC sampling time and external input impedance

The impedance of the external signal source or series resistance (R_{AIN}), between the source and pin causes a voltage drop. The charging of the capacitor is also controlled by R_{ADC}. With the addition of source resistance, the time required to fully charge the hold capacitor increases.

The following formula is used to determine the maximum external impedance allowed for an error below 1/4 of LSB to obtain the best ADC accuracy. It shows the analog signal source resistance effect.

$$R_{AIN} + R_{ADC} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})}$$

Table 2. Symbol definition of analog signal source resistance effect.

Symbol	Parameter	Value
R_{AIN}	External input impedance	
R_{ADC}	Sampling switch resistance	MAX(R_{ADC})=0.2KΩ
C_{ADC}	Internal sampling and hold capacitor	MAX(C_{ADC})=40pf
f_{ADC}	ADC clock frequency	
N	ADC resolution	12
T_S	Sampling time	

If f_{ADC} =14MHz, the typical T_S and R_{AIN} is shown as table below.

Table 3. Typical sampling cycle T_s and R_{AIN} value

T_S（cycles）	MAX（R_{AIN}）KΩ
1.5	0.08
7.5	1.18
13.5	2.28
28.5	5.04
41.5	7.44
55.5	10
71.5	13
239.5	43.9

R_{AIN} would be increased correspondingly if ADC error above 1/4 of LSB is allowed.

5 Revision history

Table 4. Revision history

Revision No.	Description	Date
1.0	Initial Release	Jun.15, 2013