GigaDevice Semiconductor Inc.

Migration from GD32F10x series to GD32F30x series

Application Note
AN011
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1. Introduction

This application note is designed to help you quickly migrate your application from the GD32F10x series microcontrollers to the GD32F30x series microcontrollers.

In order to make better use of the information in this application note, you need to download the GD32 series microcontroller data from the official website www.GD32MCU.com, such as Datasheet, user manual, official routines and various development tools.
2. **Pin compatibility**

GD32F10x and GD32F30x are Pin To Pin compatible in the same package. However, compared with GD32F10x, GD32F30x adds an internal 48MHz RC oscillator to provide a fixed frequency for the USBD module. In order to meet the accuracy requirements, GD32F30x contains a clock trim controller (CTC), so the pin definitions of the two are slightly different, as shown in *Table 2-1 Pin difference between GD32F10x series and GD32F30x series*:

<table>
<thead>
<tr>
<th>Pin name</th>
<th>Pin definition of GD32F10x series</th>
<th>Pin definition of GD32F30x series</th>
</tr>
</thead>
<tbody>
<tr>
<td>PF0</td>
<td>Default: PF0 Alternate: EXMC_A0</td>
<td>Default: PF0 Alternate: EXMC_A0</td>
</tr>
<tr>
<td></td>
<td>Remap: CTC_SYNC</td>
<td>Remap: CTC_SYNC</td>
</tr>
<tr>
<td>PD15</td>
<td>Default: PD15 Alternate: EXMC_D1</td>
<td>Default: PD15 Alternate: EXMC_D1</td>
</tr>
<tr>
<td></td>
<td>Remap: TIMER3_CH3</td>
<td>Remap: TIMER3_CH3, CTC_SYNC</td>
</tr>
<tr>
<td>PA8</td>
<td>Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT0</td>
<td>Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT0, CTC_SYNC</td>
</tr>
</tbody>
</table>
3. **Internal Resource Compatibility**

The *Table 3-1 Overview of the resource comparison between GD32F10x series and GD32F30x series* gives an overview of the resource comparison between GD32F10x and GD32F30x (take the comparison of GD32F103xE and GD32F303xE as an example):

**Table 3-1 Overview of the resource comparison between GD32F10x series and GD32F30x series**

<table>
<thead>
<tr>
<th>On-chip resources</th>
<th>GD32F103xE</th>
<th>GD32F303xE</th>
<th>Description of compatibility</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max frequency</td>
<td>108MHz</td>
<td>120MHz</td>
<td>Compatible</td>
</tr>
<tr>
<td>Core</td>
<td>Cortex® M3 core</td>
<td>Cortex® M4 core</td>
<td>M4 kernel is backward compatible</td>
</tr>
<tr>
<td>Flash</td>
<td>512K</td>
<td>512K</td>
<td>Fully compatible</td>
</tr>
<tr>
<td>RAM</td>
<td>64K</td>
<td>64K</td>
<td>Fully compatible</td>
</tr>
<tr>
<td>GPTM</td>
<td>4</td>
<td>4</td>
<td>Fully compatible</td>
</tr>
<tr>
<td>Advanced TM</td>
<td>2(RE/VE/ZE)</td>
<td>1(CE)</td>
<td>Fully compatible</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2(RE/VE/ZE)</td>
<td></td>
</tr>
<tr>
<td>Basic TM</td>
<td>2</td>
<td>2</td>
<td>Fully compatible</td>
</tr>
<tr>
<td>Systick</td>
<td>1</td>
<td>1</td>
<td>Fully compatible</td>
</tr>
<tr>
<td>Watch dog</td>
<td>2</td>
<td>2</td>
<td>Fully compatible</td>
</tr>
<tr>
<td>RTC</td>
<td>1</td>
<td>1</td>
<td>Fully compatible</td>
</tr>
<tr>
<td>USART</td>
<td>3</td>
<td>3</td>
<td>Compatible</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>F303: up to 7.5MHz(asynchronous) / 60MHz (synchronous)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>F103: up to 4.5MHz(asynchronous) / 54MHz (synchronous)</td>
</tr>
<tr>
<td>UART</td>
<td>2(RE/VE/ZE)</td>
<td>0(CE)</td>
<td>Compatible</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2(RE/VE/ZE)</td>
<td>F303: up to 7.5MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>F103: up to 4.5MHz</td>
</tr>
<tr>
<td>I2C</td>
<td>2</td>
<td>2</td>
<td>Compatible</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>F303: up to 7.1000KHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>F103: up to 400KHz</td>
</tr>
<tr>
<td>SPI/IIS</td>
<td>3/2</td>
<td>3/2</td>
<td>Compatible</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>F303: up to 30MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>F103: up to 18MHz</td>
</tr>
<tr>
<td>SDIO</td>
<td>1(RE/VE/ZE)</td>
<td>0(CE)</td>
<td>Fully compatible</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1(RE/VE/ZE)</td>
<td></td>
</tr>
<tr>
<td>CAN</td>
<td>1</td>
<td>1</td>
<td>Fully compatible</td>
</tr>
<tr>
<td>USBD</td>
<td>1</td>
<td>1</td>
<td>Fully compatible</td>
</tr>
<tr>
<td>GPIO</td>
<td>51(RE)/80(VE)/112(ZE)</td>
<td>37(CE)/51(RE)/80(VE)/112(ZE)</td>
<td>Fully compatible</td>
</tr>
<tr>
<td>EXMC</td>
<td>0(RE)/1(VE/ZE)</td>
<td>0(CE/RE)/1(VE/ZE)</td>
<td>Fully compatible</td>
</tr>
</tbody>
</table>
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<table>
<thead>
<tr>
<th>ADC(CH)</th>
<th>3(16)(RE/VE) 3(21)(ZE)</th>
<th>3(16)(CE/RE/VE) 3(21)(ZE)</th>
<th>Fully compatible</th>
</tr>
</thead>
<tbody>
<tr>
<td>DAC</td>
<td>2</td>
<td>2</td>
<td>Fully compatible</td>
</tr>
<tr>
<td>CTC</td>
<td>0</td>
<td>1</td>
<td>GD32F30x provide CTC to trim 48MHz RC oscillator</td>
</tr>
<tr>
<td>Package</td>
<td>LQFP64(RE) LQFP100(VE) LQFP144(ZE)</td>
<td>LQFP48(CE) LQFP64(RE) LQFP100(VE) LQFP144(ZE)</td>
<td>Fully compatible</td>
</tr>
</tbody>
</table>
4. Program porting

As can be seen from the previous section, the main differences between GD32F10x and GD32F30x are the main frequency (RCU system clock), kernel version and CTC, while the Cortex®-M4 is backward compatible with Cortex®-M4, so no modification is required. Then takes RCU as an example to illustrate the program porting process.

4.1. System clock configuration

The process for configuring clock for GD32F10x series and GD32F30x series is the same, but GD32F30x supports higher system clock. If the user continues to use the original clock frequency, the program does not need to be modified. If the user uses an higher clock frequency, follow the steps to modify the program (taking GD32F103 to GD32F303 and using external 8MHz high-speed crystal oscillator HXTAL as an example, the migration process of other corresponding models and using internal crystal oscillator is similar):

1. Add macro definition in system_gd32f10x.c

```c
#define __SYSTEM_CLOCK_120M_PLL_HXTAL (uint32_t)(120000000)
```

As shown in Figure 4-1 Add macro definition in system_gd32f10x.c:

![Figure 4-1 Add macro definition in system_gd32f10x.c](image)

(2) Add the declaration of using 120MHz frequency function in system_gd32f10x.c, as shown in Figure 4-2 The declaration of 120MHz function:
(3) Add the definition of using the 120MHz frequency function in the system_gd32f10x.c file:

Table 4-1. Definition of system_clock_120m_hxtal function

```c
static void system_clock_120m_hxtal(void)
{
    uint32_t timeout = 0U;
    uint32_t stab_flag = 0U;
    /* enable HXTAL */
    RCU_CTL |= RCU_CTL_HXTALEN;
    /* wait until HXTAL is stable or the startup time is longer than HXTAL_STARTUP_TIMEOUT */
    do{
        timeout++;
        stab_flag = ((RCU_CTL & RCU_CTL_HXTALSTB));
    }while((0U == stab_flag) && (HXTAL_STARTUP_TIMEOUT != timeout));
    /* if fail */
    if(0U == (RCU_CTL & RCU_CTL_HXTALSTB)){
        while(1){
            
        }
    }
    /* HXTAL is stable */
    /* AHB = SYSCLK */
    RCU_CFG0 |= RCU_AHB_CKSYS_DIV1;
}```
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/* APB2 = AHB/1 */
RCU_CFG0 |= RCU_APB2_CKAHB_DIV1;

/* APB1 = AHB/2 */
RCU_CFG0 |= RCU_APB1_CKAHB_DIV2;

#if (defined(GD32F10X_MD) || defined(GD32F10X_HD) || defined(GD32F10X_XD))
    /* select HXTAL/2 as clock source */
    RCU_CFG0 &= ~(RCU_CFG0_PLLSEL | RCU_CFG0_PREDV0);
    RCU_CFG0 |= (RCU_PLLSRC_HXTAL | RCU_CFG0_PREDV0);
    /* CK_PLL = (CK_HXTAL/2) * 30 = 120 MHz */
    RCU_CFG0 &= ~(RCU_CFG0_PLLMF | RCU_CFG0_PLLMF_4);
    RCU_CFG0 |= RCU_PLL_MUL30;
#endif

#if defined(GD32F10X_CL)
    /* CK_PLL = (CK_PREDIV0) * 30 = 120MHz */
    RCU_CFG0 &= ~(RCU_CFG0_PLLMF | RCU_CFG0_PLLMF_4);
    RCU_CFG0 |= (RCU_PLLSRC_HXTAL | RCU_PLL_MUL30);
    /* CK_PREDIV0 = (CK_HXTAL)/5 *8 /10 = 4 MHz */
    RCU_CFG1 &= ~(RCU_CFG1_PREDV0SEL | RCU_CFG1_PLL1MF | RCU_CFG1_PREDV1 | RCU_CFG1_PREDV0);
    RCU_CFG1 |= (RCU_PREDV0SRC_CKPLL1 | RCU_PLL1_MUL8 | RCU_PREDV1_DIV5 | RCU_PREDV0_DIV10);
    /* enable PLL1 */
    RCU_CTL |= RCU_CTL_PLL1EN;
    /* wait till PLL1 is ready */
    while(0U == (RCU_CTL & RCU_CTL_PLL1STB)){}
#endif /* GD32F10X_MD and GD32F10X_HD and GD32F10X_XD */

/* enable PLL */
RCU_CTL |= RCU_CTL_PLLLEN;
/* wait until PLL is stable */
while(0U == (RCU_CTL & RCU_CTL_PLLLSTB)){}
/* select PLL as system clock */
RCU_CFG0 &= ~RCU_CFG0_SCS;
RCU_CFG0 |= RCU_CKSYSSRC_PLL;
/* wait until PLL is selected as system clock */
while(0U == (RCU_CFG0 & RCU_SCSS_PLL)){}

(4) Add a call to use the 120MHz frequency function in the system_gd32f10x.c file, as shown in Figure 4-3 120MHz function call:
5. **Peripheral differences**

The peripherals of GD32F10x and GD32F30x are compatible, but GD32F30x, as a more advanced MCU, has some functions added to many peripherals compared with GD32F10x. Users can choose whether to use these functions according to the differences of peripherals listed below.

5.1. **General-purpose and alternate-function I/Os (GPIO and AFIO)**

When the I/O port is used as output, the GD32F30x can set the I/O speed to 120MHz (the maximum speed of the GD32F10x is 50MHz). When the output speed of the I/O port is greater than 50MHz, it is recommended to use the I/O compensation unit to control the slope of the I/O port to reduce the impact of I/O port noise on the power supply. For specific functions and register settings, please refer to the GD32F30x user manual.

5.2. **Analog-to-digital converter (ADC)**

The GD32F30x adds an on-chip hardware oversampling circuit compared with the GD32F10x to offload the CPU. It can handle multiple conversions and average them into a single data with increased data width, up to 16 bit. On-chip hardware oversampling circuit at the expense of lower data output rate in exchange for higher data resolution. For specific functions and register settings, please refer to the GD32F30x user manual.
5.3. **Universal synchronous/asynchronous receiver/transmitter (USART)**

Compared with GD32F10x, the GD32F30x adds block mode (GD32F10x supports character mode only), Data polarity setting and TX, RX pin level inversion, etc. Therefore, GD32F30x adds three registers: USART_CTL3, USART_RT and USART_STAT1. For specific functions and register settings, please refer to the GD32F30x user manual.

5.4. **Inter-integrated circuit interface (I2C)**

The I2C of GD32F30x and GD32F10x both support standard-mode (up to 100KHz) and fast-mode (up to 400KHz), while GD32F30x can support fast-mode-plus (up to 1MHz). Set FMPEN bit in the I2C_FMPCFG register to enable fast-mode-plus. For specific functions and register settings, please refer to the GD32F30x user manual.

5.5. **Serial peripheral interface/Inter-IC sound (SPI/I2S)**

The main difference between the SPI/I2S modules of GD32F30x and GD32F10x is that GD32F30x supports SPI TI mode, SPI NSS pulse mode and quad-SPI function (only SPI0), which the quad-SPI mode is used to control the four-wire SPI Flash peripheral. For specific functions and register settings, please refer to the GD32F30x user manual.

5.6. **Universal Serial Bus full-speed device interface (USBD)**

Compared with the GD32F10x, the GD32F30x USB 2.0 has achieved Link Power Management (LPM) level L1 in order to optimize power consumption in SUSPEND/RESUME state. LPM includes 4 states from L0 to L3. LPM L1 state (sleep state) is the new power management state. For specific functions and register settings, please refer to the GD32F30x user manual.

5.7. **Flash memory controller (FMC)**

Compared with GD32F10x, GD32F30x support bit programming, which saves some Flash space for users. Its characteristic is that the data stored in the flash memory, the bit whose value is "1" can be rewritten to "0" without affecting other bits. For example, the data stored at the address 0x0800 0400 is 0x5a5a5a5a. Using the bit programming function, the data at this address can be directly written as 0x0a0a0a0a without erasing the data at first and then writing 0x0a0a0a0a.

Please note that the bit programming function cannot write the bit with value "0" as "1", as in
the above example, writing the address of 0x08000400 as 0xfafafafa will be failed.

For specific functions and register settings, please refer to the GD32F30x user manual.
6. Revision history

<table>
<thead>
<tr>
<th>Revision No.</th>
<th>Description</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>Initial Release</td>
<td>Mar.15, 2022</td>
</tr>
</tbody>
</table>
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