GigaDevice Semiconductor Inc.

Device limitations of GD32F47x/F42x

Errata Sheet
# Table of Contents

Table of Contents.............................................................................................................. 2  
List of Figures ..................................................................................................................... 3  
List of Tables ....................................................................................................................... 4  
1. Introduction .................................................................................................................... 5  
   1.1. Revision identification ............................................................................................... 5  
   1.2. Summary of device limitations ................................................................................. 5  
2. Descriptions of device limitations .................................................................................. 7  
   2.1. GPIO ........................................................................................................................ 7  
   2.1.1. IO compensation invalidation .............................................................................. 7  
   2.2. ADC ......................................................................................................................... 7  
   2.2.1. ADC samples abnormally when using both 6-bit sampling resolution and MSB alignment... 7  
   2.2.2. ADC alignment mode is not consistent with the user manual description ............... 7  
   2.3. RTC ........................................................................................................................ 8  
   2.3.1. Calibrate abnormally when using both smooth digital calibration and FREQI calibration...... 8  
   2.4. TIMER .................................................................................................................... 8  
   2.4.1. The shadow preloaded value takes effect only on the rising edge of the counter after modification ......................................................................................................................... 8  
   2.4.2. Count error when timer works at single pulse mode ............................................ 9  
   2.5. USART .................................................................................................................... 9  
   2.5.1. Mute mode can be waked up as long as the USART_CTL0 register is operated after mute mode is enabled ............................................................................................... 9  
   2.6. I2C .......................................................................................................................... 9  
   2.6.1. I2C_FCTL register is only configurable on GD32F470xx .......................................... 9  
   2.7. SDIO ....................................................................................................................... 10  
   2.7.1. Do not support low power mode ......................................................................... 10  
   2.8. EXMC ..................................................................................................................... 10  
   2.8.1. Auto refresh function of SDRAM controller is influenced by other EXMC controller .......... 10  
   2.9. ENET ....................................................................................................................... 10  
   2.9.1. Data reception faults in MII mode ...................................................................... 10  
   2.9.2. Reception data frame is dropped when enable hardware checksum and the header checksum is 0x0000 ...................................................................................................................... 11  
3. Revision history ............................................................................................................. 12
List of Figures

Figure 1-1. Device revision code of GD32F47x/F42x.................................................. 5
List of Tables

Table 1-1. Applicable products ........................................................................................................ 5
Table 1-2. Device limitations ........................................................................................................... 5
Table 2-1. Alignment mode of routine conversion ......................................................................... 8
Table 3-1. Revision history ........................................................................................................... 12
1. **Introduction**

This document applies to GD32F47x/F42x product series, as shown in *Table 1-1. Applicable products*. It provides the technical details that need to be paid attention to in the process of using GD32 MCU, as well as solutions to related problems.

<table>
<thead>
<tr>
<th>Table 1-1. Applicable products</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Type</strong></td>
</tr>
<tr>
<td>---------</td>
</tr>
<tr>
<td>MCU</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
</tbody>
</table>

1.1. **Revision identification**

The device revision can be determined by the mark on the top of the package. The 1st code on the line 3 of the mark represents product revision code. As the picture shown in *Figure 1-1. Device revision code of GD32F47x/F42x*.

![Figure 1-1. Device revision code of GD32F47x/F42x](image)

1.2. **Summary of device limitations**

The device limitations of GD32F47x/F42x are shown in *Table 1-2. Device limitations*, please refer to section 2 for more details.

<table>
<thead>
<tr>
<th>Table 1-2. Device limitations</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Module</strong></td>
</tr>
<tr>
<td>---------</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>GPIO</td>
</tr>
<tr>
<td>ADC</td>
</tr>
<tr>
<td></td>
</tr>
</tbody>
</table>
## Device limitations of GD32F47x/F42x

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>RTC</td>
<td><em>Calibrate abnormally when using both smooth digital calibration and FREQI calibration</em></td>
<td>Y</td>
<td>Y</td>
<td></td>
</tr>
<tr>
<td></td>
<td>with the user manual description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TIMER</td>
<td><em>The shadow preloaded value takes effect only on the rising edge of the counter after modification</em></td>
<td>N</td>
<td>N</td>
<td></td>
</tr>
<tr>
<td></td>
<td><em>Count error when timer works at single pulse mode</em></td>
<td>Y</td>
<td>Y</td>
<td></td>
</tr>
<tr>
<td>USART</td>
<td><em>Mute mode can be waked up as long as the USART_CTL0 register is operated after mute mode is enabled</em></td>
<td>Y</td>
<td>Y</td>
<td></td>
</tr>
<tr>
<td>I2C</td>
<td><em>I2C_FCTL register is only configurable on GD32F470xx</em></td>
<td>N</td>
<td>N</td>
<td></td>
</tr>
<tr>
<td>SDIO</td>
<td><em>Do not support low power mode</em></td>
<td>N</td>
<td>N</td>
<td></td>
</tr>
<tr>
<td>EXMC</td>
<td><em>Auto refresh function of SDRAM controller is influenced by other EXMC controller</em></td>
<td>N</td>
<td>N</td>
<td></td>
</tr>
<tr>
<td>ENET</td>
<td><em>Data reception faults in MII mode</em></td>
<td>Y</td>
<td>Y</td>
<td></td>
</tr>
<tr>
<td></td>
<td><em>Reception data frame is dropped when enable hardware checksum and the header checksum is 0x0000</em></td>
<td>Y</td>
<td>Y</td>
<td></td>
</tr>
</tbody>
</table>

**Note:**

Y = Available  
N = Not available
2. **Descriptions of device limitations**

2.1. **GPIO**

2.1.1. **IO compensation invalidation**

*Description & impact*

IO compensation function is invalided.

*Workarounds*

Not available.

2.2. **ADC**

2.2.1. **ADC samples abnormally when using both 6-bit sampling resolution and MSB alignment**

*Description & impact*

ADC samples abnormally when using both 6-bit sampling resolution and MSB alignment mode.

*Workarounds*

Use LSB alignment mode or use 8-bit sampling resolution.

2.2.2. **ADC alignment mode is not consistent with the user manual description**

*Description & impact*

ADC alignment mode is not consistent with the user manual description.

*Workarounds*

The right alignment mode description is as follow:
## 2.3. RTC

### 2.3.1. Calibrate abnormally when using both smooth digital calibration and FREQI calibration

**Description & impact**

Using both smooth digital calibration and FREQI calibration will cause calibration result abnormal.

**Workarounds**

1) Use RTC shift function to replace smooth digital calibration, such as setting A1S bit and configuring appropriate SFS bits to satisfy the accuracy requirement.
2) Use two 16 seconds calibration window to replace one 32 seconds calibration window.

## 2.4. TIMER

### 2.4.1. The shadow preloaded value takes effect only on the rising edge of the counter after modification

**Description & impact**

The preloaded value takes effect only on the rising edge of the counter after modification which may cause problem to pwm applications with high timing requirements.

**Workarounds**

Not available.
2.4.2. **Count error when timer works at single pulse mode**

**Description & impact**

Timer works at single pulse mode and CK_APBx is CK_AHB / 4 and CK_TIMER is CK_AHB / 2, which causes count error.

**Workarounds**

1) Do not use above clock configuration.
2) Use timer update interrupt to clear error count.

2.5. **USART**

2.5.1. **Mute mode can be waked up as long as the USART_CTL0 register is operated after mute mode is enabled**

**Description & impact**

After mute mode is enabled, the operation on USART_CTL0 register will wake up USART from mute mode.

**Workarounds**

When mute mode is enabled and USART uses hardware method to detect idle frame wakeup, operation on USART_CTL0 register is not allowed. When mute mode is enabled and USART uses software method to detect idle frame wakeup, operation on USART_CTL0 register only be allowed when need to exit mute mode.

2.6. **I2C**

2.6.1. **I2C_FCTL register is only configurable on GD32F470xx**

**Description & impact**

The filter control register (I2C_FCTL) is only configurable on GD32F470xx but not on GD32F425xx or GD32F427xx.

**Workarounds**

Not available.
2.7. **SDIO**

**2.7.1. Do not support low power mode**

**Description & impact**

SDIO_CLK can not be closed automatically in bus idle state when CLKPWRSAV is set in SDIO_CLKCTL register.

**Workarounds**

Not available.

2.8. **EXMC**

**2.8.1. Auto refresh function of SDRAM controller is influenced by other EXMC controller**

**Description & impact**

Auto refresh function of SDRAM controller is influenced by other EXMC controller. When SDRAM controller execute auto refresh command, if the SDRAM bank is active, the precharge command shall be generated, which need EXMC_A10 port be 1. At that time, EXMC_A10 port is used in other EXMC controller, then the SDRAM auto refresh command execute abnormally which lead SDRAM data error.

**Workarounds**

Not available.

2.9. **ENET**

**2.9.1. Data reception faults in MII mode**

**Description & impact**

ENET_MII_COL / ENET_MII_CRS / ENET_MII_RX_ER pins are floating on MCU and external PHY has no these pins, which will cause data reception faults.

**Workarounds**

Configure ENET_MII_COL pin and ENET_MII_RX_ER pin as AF function and keep them low level. The ENET_MII_CRS pin mode and status can be ignored.
2.9.2. Reception data frame is dropped when enable hardware checksum and the header checksum is 0x0000

Description & impact

When enable hardware checksum and header checksum is 0x0000, this frame will be mistaken for error frame and dropped by hardware.

Workarounds

Use software checksum.
3. Revision history

Table 3-1. Revision history

<table>
<thead>
<tr>
<th>Revision No.</th>
<th>Description</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>Initial Release</td>
<td>Mar.16 2023</td>
</tr>
<tr>
<td>1.1</td>
<td>Update description of chapter 2.8.1</td>
<td>Apr.3 2023</td>
</tr>
</tbody>
</table>
Important Notice

This document is the property of GigaDevice Semiconductor Inc. and its subsidiaries (the "Company"). This document, including any product of the Company described in this document (the "Product"), is owned by the Company under the intellectual property laws and treaties of the People’s Republic of China and other jurisdictions worldwide. The Company reserves all rights under such laws and treaties and does not grant any license under its patents, copyrights, trademarks, or other intellectual property rights. The names and brands of third party referred thereto (if any) are the property of their respective owner and referred to for identification purposes only.

The Company makes no warranty of any kind, express or implied, with regard to this document or any Product, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. The Company does not assume any liability arising out of the application or use of any Product described in this document. Any information provided in this document is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Except for customized products which has been expressly identified in the applicable agreement, the Products are designed, developed, and/or manufactured for ordinary business, industrial, personal, and/or household applications only. The Products are not designed, intended, or authorized for use as components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, atomic energy control instruments, combustion control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or Product could cause personal injury, death, property or environmental damage ("Unintended Uses"). Customers shall take any and all actions to ensure using and selling the Products in accordance with the applicable laws and regulations. The Company is not liable, in whole or in part, and customers shall and hereby do release the Company as well as it’s suppliers and/or distributors from any claim, damage, or other liability arising from or related to all Unintended Uses of the Products. Customers shall indemnify and hold the Company as well as it’s suppliers and/or distributors harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of the Products.

Information in this document is provided solely in connection with the Products. The Company reserves the right to make changes, corrections, modifications or improvements to this document and Products and services described herein at any time, without notice.

© 2023 GigaDevice – All rights reserved