GigaDevice Semiconductor Inc.

Device limitations of GD32F45x/F40x

Errata Sheet
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Device limitations of GD32F45x/F40x

1. Introduction

This document applies to GD32F45x/F40x product series, as shown in Table 1-1. Applicable products. It provides the technical details that need to be paid attention to in the process of using GD32 MCU, as well as solutions to related problems.

Table 1-1. Applicable products

<table>
<thead>
<tr>
<th>Type</th>
<th>Part Numbers</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCU</td>
<td>GD32F405xx series</td>
</tr>
<tr>
<td></td>
<td>GD32F407xx series</td>
</tr>
<tr>
<td></td>
<td>GD32F450xx series</td>
</tr>
</tbody>
</table>

1.1. Revision identification

The device revision can be determined by the mark on the top of the package. The 1st code on the line 3 of the mark represents product revision code. As the picture shown in Figure 1-1. Device revision code of GD32F45x/F40x.

Figure 1-1. Device revision code of GD32F45x/F40x

1.2. Summary of device limitations

The device limitations of GD32F45x/F40x are shown in Table 1-2. Device limitations, please refer to section 2 for more details.

Table 1-2. Device limitations

<table>
<thead>
<tr>
<th>Module</th>
<th>Limitations</th>
<th>Workaround</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>System operation fails due to system clock switching from high clock frequency to low clock frequency</td>
<td>Y</td>
</tr>
<tr>
<td>RCU</td>
<td>Pin voltage level difference between PA11 and PA12 influences the power</td>
<td>Y</td>
</tr>
<tr>
<td>GPIO</td>
<td>DMA channel counter reconfigures</td>
<td>Y</td>
</tr>
<tr>
<td>DMA</td>
<td>DMA burst transmission faults</td>
<td>N</td>
</tr>
</tbody>
</table>
### Device limitations of GD32F45x/F40x

<table>
<thead>
<tr>
<th>Module</th>
<th>Limitations</th>
<th>Workaround</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPA</td>
<td>One extra pixel will be transferred</td>
<td>N</td>
</tr>
<tr>
<td>ADC</td>
<td>ADC samples abnormally when using both 6-bit sampling resolution and MSB alignment</td>
<td>Y</td>
</tr>
<tr>
<td></td>
<td>ADC alignment mode is not consistent with the user manual description</td>
<td>Y</td>
</tr>
<tr>
<td>RTC</td>
<td>Calibrate abnormally when using both smooth digital calibration and FREQI calibration</td>
<td>Y</td>
</tr>
<tr>
<td>TIMER</td>
<td>The shadow preloaded value takes effect only on the rising edge of the counter after modification</td>
<td>N</td>
</tr>
<tr>
<td></td>
<td>Count error when timer works at single pulse mode</td>
<td>Y</td>
</tr>
<tr>
<td>USART</td>
<td>Mute mode can be waked up as long as the USART_CTL0 register is operated after mute mode is enabled</td>
<td>Y</td>
</tr>
<tr>
<td>I2C</td>
<td>I2C_FCTL register is only configurable on GD32F450xx</td>
<td>N</td>
</tr>
<tr>
<td>EXMC</td>
<td>SDRAM controller can not be used time-shared with other EXMC controller</td>
<td>N</td>
</tr>
<tr>
<td></td>
<td>DSET bits and ASET bits configurations are invalid when NDWTEN bit is set</td>
<td>N</td>
</tr>
<tr>
<td>ENET</td>
<td>Data reception faults in MII mode</td>
<td>Y</td>
</tr>
<tr>
<td></td>
<td>Reception data frame is dropped when enable hardware checksum and the header checksum is 0x0000</td>
<td>Y</td>
</tr>
</tbody>
</table>

**Note:**

Y = Available;
N = Not available.
2. Descriptions of device limitations

2.1. RCU

2.1.1. System operation fails due to system clock switching from high clock frequency to low clock frequency

Description & impact
System operation fails when system clock switching from high clock frequency (more than 120MHz) to low clock frequency.

Workarounds
Firstly, reduce the system frequency (such as HCLK / 2 or HCLK / 4); secondly, delay more than 20 HCLK clock; finally, switch to the low clock frequency.

2.2. GPIO

2.2.1. Pin voltage level difference between PA11 and PA12 influences the power consumption in deep-sleep mode

Description & impact
Pin level difference between PA11 and PA12 influences the power consumption in deep-sleep mode.

Workarounds
Keep the same pin level on PA11 and PA12.

2.3. DMA

2.3.1. DMA channel counter reconfigures unsuccessfully

Description & impact
DMA channel counter reconfigures unsuccessfully.

Workarounds
Clear full transfer finish flag (FTIFx) and half transfer finish flag (HTIFx) before reconfiguring the DMA channel counter.
2.3.2. DMA burst transmission faults

Description & impact

The rest of data bytes that is less than fifo depth generates transmission error when using DMA burst transmission.

Workarounds

Not available.

2.4. IPA

2.4.1. One extra pixel will be transferred

Description & impact

One extra pixel will be transferred when using register value to memory direction.

Workarounds

Not available.

2.5. ADC

2.5.1. ADC samples abnormally when using both 6-bit sampling resolution and MSB alignment

Description & impact

ADC samples abnormally when using both 6-bit sampling resolution and MSB alignment mode.

Workarounds

Use LSB alignment mode or use 8-bit sampling resolution.

2.5.2. ADC alignment mode is not consistent with the user manual description

Description & impact

ADC alignment mode is not consistent with the user manual description.

Workarounds

The right alignment mode description is as follow:
Table 2-1. Alignment mode of routine conversion

<table>
<thead>
<tr>
<th>Alignment</th>
<th>Resolution</th>
<th>bit15</th>
<th>bit14</th>
<th>bit13</th>
<th>bit12</th>
<th>bit11</th>
<th>bit10</th>
<th>bit9</th>
<th>bit8</th>
<th>bit7</th>
<th>bit6</th>
<th>bit5</th>
<th>bit4</th>
<th>bit3</th>
<th>bit2</th>
<th>bit1</th>
<th>bit0</th>
</tr>
</thead>
<tbody>
<tr>
<td>LSB</td>
<td>12bit</td>
<td>0x0</td>
<td>data</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>10bit</td>
<td>0x0</td>
<td>data</td>
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<td></td>
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<tr>
<td></td>
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<td>0x0</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>MSB</td>
<td>12bit</td>
<td></td>
<td>data</td>
<td>0x0</td>
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<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>10bit</td>
<td></td>
<td>data</td>
<td>0x0</td>
<td></td>
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<tr>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>6bit</td>
<td></td>
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<td></td>
<td></td>
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<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>invalid</td>
</tr>
</tbody>
</table>

2.6. **RTC**

2.6.1. **Calibrate abnormally when using both smooth digital calibration and FREQI calibration**

**Description & impact**

Using both smooth digital calibration and FREQI calibration will cause calibration result abnormal.

**Workarounds**

1) Use RTC shift function to replace smooth digital calibration, such as setting A1S bit and configuring appropriate SFS bits to satisfy the accuracy requirement.

2) Use two 16 seconds calibration window to replace one 32 seconds calibration window.

2.7. **TIMER**

2.7.1. **The shadow preloaded value takes effect only on the rising edge of the counter after modification**

**Description & impact**

The preloaded value takes effect only on the rising edge of the counter after modification which may cause problem to pwm applications with high timing requirements.

**Workarounds**

Not available.
2.7.2. **Count error when timer works at single pulse mode**

**Description & impact**

Timer works at single pulse mode and CK_APBx is CK_AHB / 4 and CK_TIMER is CK_AHB / 2, which causes count error.

**Workarounds**

1) Do not use above clock configuration.
2) Use timer update interrupt to clear error count.

2.8. **USART**

2.8.1. **Mute mode can be waked up as long as the USART_CTL0 register is operated after mute mode is enabled**

**Description & impact**

After mute mode is enabled, the operation on USART_CTL0 register will wake up USART from mute mode.

**Workarounds**

When mute mode is enabled and USART uses hardware method to detect idle frame wakeup, operation on USART_CTL0 register is not allowed. When mute mode is enabled and USART uses software method to detect idle frame wakeup, operation on USART_CTL0 register only be allowed when need to exit mute mode.

2.9. **I2C**

2.9.1. **I2C_FCTL register is only configurable on GD32F450xx**

**Description & impact**

The filter control register (I2C_FCTL) is only configurable on GD32F450xx but not on GD32F405xx or GD32F407xx.

**Workarounds**

Not available.
2.10. EXMC

2.10.1. SDRAM controller can not be used time-shared with other EXMC controller

Description & impact
SDRAM controller can not be used time-shared with other EXMC controller.

Workarounds
Not available.

2.10.2. DSET bits and ASET bits configurations are invalid when NDWTEN bit is set

Description & impact
Data setup time (DSET) and address setup time (ASET) configurations are invalid when wait function is enabled.

Workarounds
Not available.

2.11. ENET

2.11.1. Data reception faults in MII mode

Description & impact
ENET_MII_COL / ENET_MII_CRS / ENET_MII_RX_ER pins are floating on MCU and external PHY has no these pins, which will cause data reception faults.

Workarounds
Configure ENET_MII_COL pin and ENET_MII_RX_ER pin as AF function and keep them low level. The ENET_MII_CRS pin mode and status can be ignored.

2.11.2. Reception data frame is dropped when enable hardware checksum and the header checksum is 0x0000

Description & impact
Device limitations of GD32F45x/F40x

When enable hardware checksum and header checksum is 0x0000, this frame will be mistaken for error frame and dropped by hardware.

**Workarounds**

Use software checksum.
3. Revision history

Table 3-1. Revision history

<table>
<thead>
<tr>
<th>Revision No.</th>
<th>Description</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>Initial Release</td>
<td>Jun.20 2022</td>
</tr>
</tbody>
</table>
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