GigaDevice Semiconductor Inc.

Device limitations of GD32F30x

Errata Sheet
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1. **Introduction**

This document applies to GD32F30x product series, as shown in Table 1-1. *Applicable products*. It provides the technical details that need to be paid attention to in the process of using GD32 MCU, as well as solutions to related problems.

### Table 1-1. Applicable products

<table>
<thead>
<tr>
<th>Type</th>
<th>Part Numbers</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCU</td>
<td>GD32F303xx series</td>
</tr>
<tr>
<td></td>
<td>GD32F305xx series</td>
</tr>
<tr>
<td></td>
<td>GD32F307xx series</td>
</tr>
</tbody>
</table>

1.1. **Revision identification**

The device revision can be determined by the mark on the top of the package. The 1st code on the line 3 of the mark represents product revision code. As the picture shown in Figure 1-1. *Device revision code of GD32F30x*.

![Device revision code of GD32F30x](image)

1.2. **Summary of device limitations**

The device limitations of GD32F30x are shown in Table 1-2. *Device limitations*, please refer to section 2 for more details.

### Table 1-2. Device limitations

<table>
<thead>
<tr>
<th>Module</th>
<th>Limitations</th>
<th>Workaround</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td><strong>Standby mode can not be entered normally</strong></td>
<td>Y</td>
</tr>
<tr>
<td></td>
<td><strong>Power consumption is higher in deep-sleep mode</strong></td>
<td></td>
</tr>
<tr>
<td>RCU</td>
<td><strong>MCU can not be waked up after entering deep-sleep / standby mode when DSLP_HOLD / STB_HOLD bit is set</strong></td>
<td>Y</td>
</tr>
<tr>
<td>ADC</td>
<td><strong>ADC sampling distorts during the calibration</strong></td>
<td>Y</td>
</tr>
<tr>
<td>DAC</td>
<td><strong>DAC output pin exists electric leakage to VREF+ pin when</strong></td>
<td>Y</td>
</tr>
</tbody>
</table>
## Device limitations of GD32F30x

<table>
<thead>
<tr>
<th>Device</th>
<th>Limitation</th>
<th>Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DAC</strong></td>
<td>Disabled</td>
<td>Y</td>
</tr>
<tr>
<td><strong>Timer</strong></td>
<td>Data lost when using timer capture / compare event to trigger DMA transfer and enabling the output compare shadow function</td>
<td>Y</td>
</tr>
<tr>
<td><strong>USART</strong></td>
<td>Data lost when using USART DMA transmission</td>
<td>Y</td>
</tr>
<tr>
<td><strong>Mute mode can be waked up as long as the USART_CTL0 register is operated after mute mode is enabled</strong></td>
<td>Y</td>
<td></td>
</tr>
<tr>
<td><strong>I2C</strong></td>
<td>Read one more data because the BTC flag was not cleared</td>
<td>Y</td>
</tr>
<tr>
<td><strong>EXMC</strong></td>
<td>NE timing can not satisfy the requirement when using NAND pre-waiting function</td>
<td>Y</td>
</tr>
</tbody>
</table>

**Note:**
Y = Available
N = Not available
2. Descriptions of device limitations

2.1. PMU

2.1.1. Standby mode can not be entered normally

Description & impact
When system application programme exists other interrupt code (such as systick 1us period interrupt) and needs to enter standby mode through WFI instruction, the system can not enter the standby mode normally.

Workarounds
Application programme needs to mask all interrupts except RTC wakeup source before entering standby mode.

2.1.2. Power consumption is higher in deep-sleep mode

Description & impact
Power consumption is higher in deep-sleep mode.

Workarounds
Application programme can configure I/O (not used, including internal I/O) to analog mode to reduce the power consumption.

2.2. RCU

2.2.1. MCU can not be waked up after entering deep-sleep / standby mode when DSLP_HOLD / STB_HOLD bit is set

Description & impact
When DSLP_HOLD / STB_HOLD bit is set and debug the mcu in deep-sleep / standby mode, the mcu will not be waked up.

Workarounds
The application programme need switch the system clock to IRC8M before entering the deep-sleep / standby mode.
2.3. ADC

2.3.1. ADC sampling distorts during the calibration

Description & impact
When application programme executes the adc calibration function after power up, $V_{DDA}$ voltage generates fluctuation which results in the ADC sampling value distortion.

Workarounds
1) Add 1ms delay after ADC is enabled and before calibrating.
2) Connect a 1uF (better for an extra 10nF) capacitor in parallel with $V_{DDA}$ pin.
3) Select a right bead between $V_{DDA}$ and $V_{DD}$.

2.4. DAC

2.4.1. DAC output pin exists electric leakage to $V_{REF+}$ pin when DAC is disabled

Description & impact
When DAC is disabled and $V_{REF+}$ is smaller than $V_{DD}$ exceeding 0.7V, DAC output pin exists electric leakage to $V_{REF+}$ pin.

Workarounds
Avoid $V_{REF+}$ is smaller than $V_{DD}$ exceeding 0.7V.

2.5. TIMER

2.5.1. Data lost when using timer capture / compare event to trigger DMA transfer and enabling the output compare shadow function

Description & impact
When using timer capture / compare event to trigger DMA transfer and enabling the output compare shadow function, DMA transfers data 0x00 to TIMERx_CHyCV register which will result in the second data lost after data 0x00.

Workarounds
Do not use data 0x00 in DMA transfer buffer.
2.6. **USART**

2.6.1. **Data lost when using USART DMA transmission**

**Description & impact**

Application programme configurations follow the such step:
1) Disable USART transmitter.
2) Configure the DMA channel counter.
3) Enable DMA channel.
4) Enable USART transmitter.

When using the above configuration, the transmission data is lost.

**Workarounds**

Adjust the configurations code sequence as follow:
1) Disable USART transmitter.
2) Configure the DMA channel counter.
3) Enable USART transmitter.
4) Enable DMA channel.

2.6.2. **Mute mode can be waked up as long as the USART_CTL0 register is operated after mute mode is enabled**

**Description & impact**

After mute mode is enabled, the operation on USART_CTL0 register will wake up USART from mute mode.

**Workarounds**

When mute mode is enabled and use hardware method to detect idle frame wakeup, operation on USART_CTL0 register is not allowed. When mute mode is enabled and use software method to detect idle frame wakeup, operation on USART_CTL0 register only be allowed when need to exit mute mode.

2.7. **I2C**

2.7.1. **Read one more data because the BTC flag was not cleared**

**Description & impact**

If an interrupt occurs before reading I2C_DATA register when RBNE flag is set and BTC flag is reset, I2C will read an additional data if BTC flag is set during the interrupt processing
because the read data operation can not clear the BTC flag.

**Workarounds**

1) Using interrupt method to read the I2C_DATA register.
2) Using DMA method to read the I2C_DATA register.

### 2.8. EXMC

#### 2.8.1. NE timing can not satisfy the requirement when using NAND pre-waiting function

**Description & impact**

For some EXMC_NCE-sensitive NAND Flash, NE timing can not satisfy the requirement when using NAND pre-waiting function. NE signal keeps the low level when EXMC_INTx is active.

**Workarounds**

Using general I/O port to simulate the NE timing to finish the NAND reading and writing, NE signal keeps the low level after starting reading or writing.
3. Revision history

Table 3-1. Revision history

<table>
<thead>
<tr>
<th>Revision No.</th>
<th>Description</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>Initial Release</td>
<td>Jun.20 2022</td>
</tr>
</tbody>
</table>

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