GigaDevice Semiconductor Inc.

Device limitations of GD32E50x

Errata Sheet
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1. Introduction

This document applies to GD32E50x product series, as shown in Table 1-1. Applicable products. It provides the technical details that need to be paid attention to in the process of using GD32 MCU, as well as solutions to related problems.

Table 1-1. Applicable products

<table>
<thead>
<tr>
<th>Type</th>
<th>Part Numbers</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCU</td>
<td>GD32E503xx series</td>
</tr>
<tr>
<td></td>
<td>GD32E505xx series</td>
</tr>
<tr>
<td></td>
<td>GD32E507xx series</td>
</tr>
<tr>
<td></td>
<td>GD32E508xx series</td>
</tr>
</tbody>
</table>

1.1. Revision identification

The device revision can be determined by the mark on the top of the package. The 1st code on the line 3 of the mark represents product revision code. As the picture shown in Figure 1-1. Device revision code of GD32E50x.

Figure 1-1. Device revision code of GD32E50x

1.2. Summary of device limitations

The device limitations of GD32E50x are shown in Table 1-2. Device limitations, please refer to section 2 for more details.

Table 1-2. Device limitations

<table>
<thead>
<tr>
<th>Module</th>
<th>Limitations</th>
<th>Workaround</th>
</tr>
</thead>
<tbody>
<tr>
<td>SHRTIMER</td>
<td>In certain cases, DLL calibration will lose SET/RESET</td>
<td>N</td>
</tr>
<tr>
<td></td>
<td>Unable to enter fault interrupt</td>
<td>N</td>
</tr>
<tr>
<td></td>
<td>SHRTIMER works abnormally when the update source is configured</td>
<td>N</td>
</tr>
</tbody>
</table>
## Device limitations of GD32E50x

<table>
<thead>
<tr>
<th>Module</th>
<th>Limitations</th>
<th>Workaround</th>
<th>Rev. Code</th>
<th>A</th>
</tr>
</thead>
<tbody>
<tr>
<td>SQPI</td>
<td>The power consumption in Deep-sleep/Deep-sleep 1/Deep-sleep 2 mode is high when using external PSRAM</td>
<td>Y</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>The power consumption in standby mode is high when using external PSRAM</td>
<td>Y</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Misaligned access to PSRAM causes the program to run out of track</td>
<td>Y</td>
<td></td>
<td></td>
</tr>
<tr>
<td>USB</td>
<td>When the LPM slave machine is connected to the PC host, if the previous control transaction of the LPM transaction is STALL, the LPM transaction will also be STALL</td>
<td>Y</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Failure of data transfer in high speed synchronous pressure test</td>
<td>Y</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note:**
- Y = Available
- N = Not available
2. Descriptions of device limitations

2.1. SHRTIMER

2.1.1. In certain cases, DLL calibration will lose SET/RESET

Description & impact
If the SET/RESET event occurs during DLL calibration, the SET/RESET event may be lost and has no effect on the output.

Workarounds
Not available.

2.1.2. Unable to enter fault interrupt

Description & impact
When a fault event from system fault or fault channel occurs, the corresponding interrupt cannot be generated.

Workarounds
Not available.

2.1.3. SHRTIMER works abnormally when the update source is configured

Description & impact
When SHRTIMER shadow registers are enabled, SHRTIMER works abnormally.

Workarounds
Not available.

2.2. SQPI

2.2.1. The power consumption in Deep-sleep/Deep-sleep 1/ Deep-sleep 2 mode is high when using external PSRAM

Description & impact
In Deep-sleep/Deep-sleep 1/ Deep-sleep 2 mode, the MCU does not use the GPIO configuration to shut down early to reduce power consumption.
2.2.2. The power consumption in standby mode is high when using external PSRAM

Description & impact
After MCU entered the standby mode, PF6 connected to PSRAM chip selection signal CEN also lost power, resulting in PSRAM could not enter the standby mode.

Workarounds
Switch standby mode to Deep-sleep/Deep-sleep 1/ Deep-sleep 2 mode.

2.2.3. Misaligned access to PSRAM causes the program to run out of track

Description & impact
When the PSRAM is written unaligned, the program runs out of track.

Workarounds
Read out the PSRAM contents and modify the code for alignment to achieve unaligned write operations.

2.3. USB

2.3.1. When the LPM slave machine is connected to the PC host, if the previous control transaction of the LPM transaction is STALL, the LPM transaction will also be STALL

Description & impact
In the software code, the STALL operation will STALL both the IN and OUT directions of the control endpoint. If the OUT directions of the control endpoint is STALL, the next OUT control transaction will not be properly responded and will directly return to the STALL. However, SETUP transactions can be received normally. LPM transactions do not belong to SETUP transactions. LPM transactions are a special transaction, equivalent to OUT transactions, resulting in that they cannot be ACK normally.

Workarounds
Modify the code according to the USB requirements of different PCs to solve the problem.
2.3.2. Failure of data transfer in high speed synchronous pressure test

Description & impact

During a high-speed synchronous pressure test, the device does not respond to the IN and OUT token packets of the host after a period of time. As a result, data transmission is interrupted.

Workarounds

Configure external crystal oscillator for high speed synchronous pressure test.
3. Revision history

Table 3-1. Revision history

<table>
<thead>
<tr>
<th>Revision No.</th>
<th>Description</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>Initial Release</td>
<td>Dec.12 2022</td>
</tr>
</tbody>
</table>


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