GigaDevice Semiconductor Inc.

GD32H7xx Hardware Development Guide

Application Note
AN109
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1. **Introduction**

The article is specially provided for developers of 32-bit general-purpose MCU GD32H7xx series based on Arm® Cortex®-M7 architecture. It provides an overall introduction to the hardware development of GD32H7xx series products, such as power supply, reset, clock, boot mode settings and download debugging. The purpose of this application notes is to allow developers to quickly get started and use GD32H7xx series products, and quickly develop and use product hardware, save the time of studying manuals, and speed up product development progress.

This application note is divided into seven parts to describe:

1. Power supply, mainly introduces the design of GD32H7xx series power management, power supply and reset functions.
2. Clock, mainly introduces the functional design of GD32H7xx series high and low speed clocks.
3. Boot configuration, mainly introduces the BOOT configuration and design of GD32H7xx series.
4. Typical peripheral modules, mainly introduces the hardware design of the main functional modules of the GD32H7xx series.
5. Download and debug circuit, mainly introduces the recommended typical download and debug circuit of GD32H7xx series.
6. Reference circuit and PCB Layout design, mainly introduces GD32H7xx series hardware circuit design and PCB Layout design notes.
7. Package description, mainly introduces the package forms and names included in the GD32H7xx series.

This document also satisfies the minimum system hardware resources used in application development based on GD32H7xx series products.

### Table 1-1. Applicable Products

<table>
<thead>
<tr>
<th>Type</th>
<th>Part Numbers</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCU</td>
<td>GD32H737xx series</td>
</tr>
<tr>
<td></td>
<td>GD32H757xx series</td>
</tr>
<tr>
<td></td>
<td>GD32H759xx series</td>
</tr>
</tbody>
</table>
2. Hardware design

2.1. Power supply

The \( V_{DD} / V_{DDA} \) operating voltage range of GD32H7xx series products is 1.71 V ~ 3.6 V. As shown in Figure 2-1. GD32H7xx series Power supply overview, the GD32H7xx series device has three power domains, including the \( V_{DD} / V_{DDA} \) domain, 0.9V domain and backup domain. The \( V_{DD} / V_{DDA} \) domain is directly powered by the power supply. The GD32H7xx series is embedded with LDO and low-power switching power supply voltage regulator (SMPS voltage regulator) to supply power to the 0.9V domain. There is a power switch in the backup domain. When the \( V_{DD} \) power is turned off, the power switch can switch the power of the backup domain to the \( V_{BAT} \) pin. At this time, the backup domain is powered by the \( V_{BAT} \) pin (battery). The USB part has dedicated external power supply pins and voltage regulators, which can input 5 V power supply or 3.3 V power supply.

Figure 2-1. GD32H7xx series Power supply overview
2.1.1. Backup domain

The power supply voltage range of the backup domain is 1.71 V to 3.6 V. The internal power switch selects \( V_{DD} \) power supply or \( V_{BAT} \) (battery) power supply, and then \( V_{BAK} \) powers the backup domain. The backup domain includes RTC (real-time clock), LXTAL (low-speed external crystal oscillator), BPOR (backup domain power on reset), BREG, and a total of three BKP PAD from PC13 to PC15. To ensure the contents of the registers in the backup domain and the normal operation of the RTC, the \( V_{BAK} \) pin can be connected to the battery or other backup power supply when the \( V_{DD} \) is turned off. The power switch is controlled by the \( V_{DD} / V_{DDA} \) domain power-off reset circuit. For applications without external batteries, it is recommended to connect the \( V_{BAT} \) pin to the \( V_{DD} \) pin through a 100nF capacitor to ground.

The reset source of the backup domain includes power on reset and software reset of the backup domain. Before \( V_{BAK} \) is fully powered on, the BPOR signal forces the device to be in a reset state. The application software can be configured by setting the RCU_. The BDCTL register BKPRST bit triggers a backup domain software reset.

The clock source of RTC can be a low-speed internal 32kHz RC oscillator (IRC32K) or a low-speed external crystal oscillator (LXTAL), or a high-speed external crystal oscillator (HXTAL) clock divider controlled by the RTCDIV[5:0] (located in the RCU_CFG0 register) bit domain. When \( V_{DD} \) is turned off, RTC can only select LXTAL as the clock source. Before entering power-saving mode through WFI / WFE commands, Cortex®-M7 can achieve RTC timer wake-up events by setting the expected wake-up time in the RTC register and enabling wake-up function or based on EXTI. After entering the power saving mode for a certain period of time, when the elapsed time matches the preset wake-up time, the RTC will wake up the device.

When the backup domain is powered by \( V_{DD} \) (\( V_{BAK} \) connected to \( V_{DD} \)), the following functions are available:

- PC13 can be used as a universal I/O port or RTC function pin;
- PC14 and PC15 can be used as general-purpose I/O ports or LXTAL crystal oscillator pins.

When the backup domain is powered by \( V_{BAT} \) power (\( V_{BAK} \) connected to \( V_{BAT} \)), the following functions are available:

- PC13 can only be used as an RTC function pin;
- PC14 and PC15 can only be used as LXTAL crystal oscillator pins.

**Note:** Since the PC13 to PC15 pins are powered by a power switch, the power switch can only pass small currents. Therefore, when the GPIO port of PC13 to PC15 is in output mode, its operating speed cannot exceed 2MHz (maximum load is 30pF).

\( V_{DD} \) can charge external batteries through an internal resistor. By configuring the VCRSEL bit in the PMU_CTL2 register, an internal resistance of 5K ohms or 1.5K ohms can be selected for external VBAT battery charging. Setting VCEN to 1 in the PMU_CTL2 register enables VBAT battery charging. In BKP only mode, \( V_{BAT} \) battery charging is not available.
2.1.2. **V\textsubscript{DD} / V\textsubscript{DDA} domain**

The V\textsubscript{DD} / V\textsubscript{DDA} power domain includes two parts: V\textsubscript{DD} domain and V\textsubscript{DDA} domain. If V\textsubscript{DDA} is not equal to V\textsubscript{DD}, the voltage difference between the two should not exceed 300mV (the internal V\textsubscript{DDA} and V\textsubscript{DD} of the chip are connected through a back-to-back diode). To avoid noise, V\textsubscript{DDA} can be connected to V\textsubscript{DD} through an external filter circuit, and the corresponding V\textsubscript{SSA} is connected to V\textsubscript{SS} through a specific circuit (single-point grounding, through 0Ω resistors or magnetic beads, etc.).

In order to improve the conversion accuracy of the ADC, the independent power supply for V\textsubscript{DDA} can make the analog circuit achieve better characteristics. GD32H7xx is internally integrated with V\textsubscript{REFP} pin specially designed for independent power supply of ADC (External power supply: Using 12bit ADC, 1.71 V ≤ V\textsubscript{REFP} ≤ V\textsubscript{DDA}. Using 14bit ADC, when V\textsubscript{DDA} ≥ 2.4 V, 2.4 V ≤ V\textsubscript{REFP} ≤ V\textsubscript{DDA}; when V\textsubscript{DDA} < 2.4 V, 1.8 V ≤ V\textsubscript{REFP} ≤ V\textsubscript{DDA}).

- The BGA176 package contains V\textsubscript{REFP} and V\textsubscript{REFN}, V\textsubscript{REFP} can use an external reference power supply or be directly connected to V\textsubscript{DDA}. V\textsubscript{REFN} must be connected to V\textsubscript{SSA}.
- The LQFP package contains V\textsubscript{REFP}, which can use an external reference power supply or be directly connected to V\textsubscript{DDA}.

2.1.3. **0.9V domain**

By using SMPS voltage regulator and LDO, a power supply of 0.9V power domain can be set. Different configurations can provide seven effective 0.9V power domain power supply modes.

- **Unconfigured power supply mode (default power supply mode)**

After resetting, the DVSEN bit is 0b1, the DVSCFG bit is 0b0, and the DVSCV[1:0] bit is 0b00. At this point, the SMPS voltage regulator opens and operates in normal mode with a working voltage of 1.0V. The SMPS voltage regulator can supply power to the LDO; The LDOEN bit is 0b1, the LDO is in the ON state, and supplies power to the 0.9V power domain. The power supply voltage is controlled by the LDOVS[2:0] bit domain; The BYPASS bit is 0b0, and the 0.9V power domain is not powered by V\textsubscript{CORE} (V\textsubscript{CORE} power supply is directly external).

- **LDO power supply mode**

The configuration method for entering this power supply mode is: the DVSEN bit is 0b0, and the values of the DVSCFG and DVSCV[1:0] bit fields are not affected. At this time, the SMPS voltage regulator is in the OFF state; The LDOEN bit is 0b1, and the LDO is in the ON state, supplying power to the 0.9V power domain. The power supply voltage is controlled by the LDOVS[2:0] bit domain, and the operating mode of the LDO is consistent with the low power consumption mode of the system; The BYPASS bit is 0b0, and the 0.9V power domain is not powered by V\textsubscript{CORE} (V\textsubscript{CORE} power supply is directly external). Figure 2-2. The LDO power supply 0.9V power domain shows this power supply mode.
SMPS power supply mode

The configuration method for entering this power supply mode is as follows: the DVSEN bit is 0b1, the DVSCFG bit is 0b1, and the value of the DVSC[1:0] bit field has no effect. At this time, the SMPS voltage regulator is turned on and supplies power to the 0.9V power domain. The power supply voltage is controlled by the LDOVS[2:0] bit field, and the working mode of SMPS is consistent with the low power consumption mode of the system; LDOEN bit is 0b0, and LDO is in the OFF state; The BYPASS bit is 0b0, and the 0.9V power domain is not powered by Vcore (Vcore power supply is directly external). Figure 2-3. The SMPS power supply 0.9V power domain shows this power supply mode.

SMPS supplies power to LDO, while LDO supplies power to the 0.9V power domain

The configuration method for entering this power supply mode is: DVSEN bit is 0b1, DVSCFG bit is 0b0, and the value of DVSC[1:0] bit field is 0b01 / 0b10 / 0b11. At this time, the SMPS voltage regulator is in the ON state, working in the normal mode with a working voltage of 1.8 V / 2.5 V, and supplying power to LDO. The working mode of SMPS is consistent with the low power consumption mode of the system; The LDOEN bit is 0b1, and the LDO is in the ON state, supplying power to the 0.9V power domain. The power supply voltage is controlled by the LDOVS[2:0] bit, and the operating mode of the LDO is consistent with the low power consumption mode of the system; The BYPASS bit is 0b0, and the 0.9V power domain is not powered by Vcore (Vcore power supply is directly external). Figure 2-4. SMPS supplies power to LDO, and LDO supplies 0.9V power domain shows this power supply mode.
SMPS supplies power to LDO and external power, and LDO supplies 0.9V power domain

The configuration method for entering this power supply mode is as follows: DVSEN bit is 0b1, DVSCFG bit is 0b1, and the value of DVSVC[1:0] bit field is 0b01 / 0b10 / 0b11. At this time, the SMPS voltage regulator is in the ON state, working in the main mode with a working voltage of 1.8 V / 2.5 V, and supplying LDO and external power. The working mode of SMPS is consistent with the low power consumption mode of the system; The LDOEN bit is 0b1, and the LDO is in the ON state, supplying power to the 0.9V power domain. The power supply voltage is controlled by the LDOVS[2:0] bit, and the operating mode of the LDO is consistent with the low power consumption mode of the system; The BYPASS bit is 0b0, and the 0.9V power domain is not powered by VCORE (VCORE power supply is directly external). Figure 2-5, SMPS supplies power to LDO and external power, LDO supplies 0.9V power domain shows this power supply mode.

SMPS supplies power to external power, and the external power supplies 0.9V power domain

The configuration method for entering this power supply mode is as follows: DVSEN bit is 0b1, DVSCFG bit is 0b1, and the value of DVSVC[1:0] bit field is 0b01 / 0b10 / 0b11. At this time, the SMPS voltage regulator is in the ON state, working in the main mode with a working voltage of 1.8 V / 2.5 V, and supplying external power. The external power supply lead may
be supplying power to the 0.9V power supply domain; LDOEN bit is 0b0, and LDO is in the OFF state; The BYPASS bit is 0b1, and the 0.9V power domain is powered by V\textsubscript{CORE} (V\textsubscript{CORE} power supply is directly external). \textbf{Figure 2-6. SMPS supplies power to LDO and external power, LDO supplies 0.9V power domain} shows this power supply mode.

\textbf{Figure 2-6. SMPS supplies power to LDO and external power, LDO supplies 0.9V power domain}

<table>
<thead>
<tr>
<th>SMPS (on)</th>
<th>LDO (off)</th>
</tr>
</thead>
<tbody>
<tr>
<td>V\textsubscript{DDLDO}</td>
<td>V\textsubscript{CORE}</td>
</tr>
<tr>
<td>V\textsubscript{DDLDO}</td>
<td>V\textsubscript{0.9V}</td>
</tr>
</tbody>
</table>

**Bypass mode**

The configuration method for entering this power supply mode is: the DVSEN bit is 0b0, and the values of DVSCFG and DVS\textsubscript{VC}[1:0] have no effect. At this time, the SMPS voltage regulator is in the OFF state; LDOEN bit is 0b0, and LDO is in the OFF state; The BYPASS bit is 0b1, and the 0.9V power domain is powered by V\textsubscript{CORE} (V\textsubscript{CORE} power supply is directly external). \textbf{Figure 2-7. Bypass mode} shows this power supply mode.

\textbf{Figure 2-7. Bypass mode}

<table>
<thead>
<tr>
<th>SMPS (off)</th>
<th>LDO (off)</th>
</tr>
</thead>
<tbody>
<tr>
<td>V\textsubscript{DDLDO}</td>
<td>V\textsubscript{CORE}</td>
</tr>
<tr>
<td>V\textsubscript{DDLDO}</td>
<td>V\textsubscript{0.9V}</td>
</tr>
</tbody>
</table>

**Note:** Except for the valid combinations mentioned above, all other configuration combinations of DVSEN, DVSCFG, DVS\textsubscript{VC}[1:0], LDOEN, BYPASS bits or bit values are invalid. The power state of the 0.9V power domain remains unchanged after reset (no configured power mode).

**Note:** When the SMPS voltage regulator supplies power to the 0.9V power domain and the DVS\textsubscript{VC}[1:0] is configured with an incorrect value, it will cause the SMPS voltage regulator to output high voltage to the 0.9V power domain. At this time, the 0.9V power domain will activate hardware overvoltage protection, and the hardware will be set to DVS\textsubscript{VC}[1:0] 0b00.

**Note:** The maximum operating frequency is related to the power supply voltage, please refer
2.1.4. Power supply design

The system needs a stable power supply. There are some important things to pay attention to when developing and using:

- The VDD pin must be connected with an external capacitor (N*100nF ceramic capacitor + not less than 4.7μF tantalum capacitor, at least one VDD needs to be connected to GND with a capacitor of not less than 4.7μF, and other VDD pins are connected to 100nF).
- The VDDA pin must be connected with an external capacitor (10nF + 1μF ceramic capacitor is recommended).
- The VREFP pin can be generated internally or directly connected to VDDA, and a 10nF + 1μF ceramic capacitor should be connected between the VREFP pin and ground.

Figure 2-8. GD32H7xx Recommended Power Supply Design

Note:

1. All decoupling capacitors must be placed close to the corresponding VDD, VDDA, VBAT, VREFP, VCORE pins of the chip.
2. Regardless of whether LDO is enabled or not, all VCORE of the chip should be connected...
3. When LDO is enabled, it is recommended that VCORE connect two 2.2uF ceramic capacitors to GND; When bypassing LDO, it is recommended that VCORE connect two 100nF ceramic capacitors to GND.

The recommended design of the SMPS circuit is shown in Figure 2-9. GD32H7xx Recommended SMPS circuit Design, and the typical value of the device are shown in Table 2-1. Characteristics of SMPS step-down converter external components.

![Figure 2-9. GD32H7xx Recommended SMPS circuit Design](image)

### Table 2-1. Characteristics of SMPS step-down converter external components

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>C&lt;sub&gt;c&lt;/sub&gt;</td>
<td>Capacitance of external capacitor on V&lt;sub&gt;DDSMPS&lt;/sub&gt;</td>
<td>4.7uF</td>
<td>0805</td>
</tr>
<tr>
<td></td>
<td>ESR of external capacitor</td>
<td>100mΩ</td>
<td></td>
</tr>
<tr>
<td>C&lt;sub&gt;ult&lt;/sub&gt;</td>
<td>Capacitance of external capacitor on V&lt;sub&gt;LXSMPS&lt;/sub&gt;</td>
<td>220pF</td>
<td>0603</td>
</tr>
<tr>
<td>R&lt;sub&gt;ult&lt;/sub&gt;</td>
<td>Resistor of external capacitor on V&lt;sub&gt;LXSMPS&lt;/sub&gt;</td>
<td>50Ω</td>
<td>0603</td>
</tr>
<tr>
<td>C&lt;sub&gt;OUT1&lt;/sub&gt;, C&lt;sub&gt;OUT2&lt;/sub&gt;</td>
<td>Capacitance of external capacitor on V&lt;sub&gt;FBSMPS&lt;/sub&gt;</td>
<td>10uF</td>
<td>0805</td>
</tr>
<tr>
<td></td>
<td>ESR of external capacitor</td>
<td>20mΩ</td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>Inductance of external Inductor on V&lt;sub&gt;LXSMPS&lt;/sub&gt;</td>
<td>2.2uH</td>
<td>0806</td>
</tr>
</tbody>
</table>

2.1.5. Reset and power management

GD32H7xx series reset control includes three resets: power reset, system reset and backup domain reset. A power reset is a cold reset, which resets all systems except the backup domain when the power is turned on.

The POR / PDR circuit is implemented to detect V<sub>DD</sub> / V<sub>DDA</sub> and generate the power reset.
signal which resets the whole chip except the Backup domain when the supply voltage is lower than the specified threshold. Figure 2-10. Waveform of the POR / PDR shows the relationship between the supply voltage and the power reset signal. $V_{POR}$ indicates the threshold of power on reset, while $V_{PDR}$ means the threshold of power down reset. The hysteresis voltage ($V_{hyst}$) is around 50 mV.

Figure 2-10. Waveform of the POR / PDR

The BOR circuit is used to detect $V_{DD} / V_{DDA}$ and generate the power reset signal which resets the whole chip except the Backup domain when the BOR_TH bits in option bytes is not 0b11 and the supply voltage is lower than the specified threshold which defined in the BOR_TH bits in option bytes. Notice that the POR/PDR circuit is always implemented regardless of BOR_TH bits in option bytes is 0b11 or not. Figure 2-11. Waveform of the BOR shows the relationship between the supply voltage and the BOR reset signal. $V_{BOR}$, which defined in the BOR_TH bits in option bytes, indicates the threshold of BOR on reset. The hysteresis voltage ($V_{hyst}$) is 100 mV.

Figure 2-11. Waveform of the BOR
The function of LVD is to detect whether the $V_{DD}$ / $V_{DDA}$ supply voltage is lower than the low voltage detection threshold, which is configured by the LVDT[2:0] bit in the power control register $0$ (PMU_CTL$0$). LVD is enabled by LVDEN setting. The LVDF bit in the power supply status register (PMU_CS) indicates whether a low voltage event occurs. This event is connected to the 16th line of EXTI. The user can generate a corresponding interrupt by configuring the 16th line of EXTI. Figure 2-12. Waveform of the LVD shows the relationship between $V_{DD}$ / $V_{DDA}$ supply voltage and LVD output signal. (LVD interrupt signal depends on the rising or falling edge configuration of EXTI line 16). The hysteresis voltage ($V_{hyst}$) is 100 mV.

Figure 2-12. Waveform of the LVD

GD32H7xx series internal Power monitor can be enabled or disabled through the PDR_ON pin. In general, it is recommended that users pull the PDR_ON pin up to $V_{DD}$.

When PDR_ON is connected to GND, the following functions will be disabled:

1. Internal Power On Reset(POR) / Power Down Reset(PDR) disabled.
2. Internal Brown Out Reset(BOR) disabled.
3. Internal Low Voltage Detection(LVD) disabled.
4. $V_{BAT}$ function disabled, $V_{BAT}$ pin should be connected to $V_{DD}$.

The MCU reset source can be searched by the register RCU_RSTSCK (0x40021024). This register can only clear the flag bit after power-on reset. Therefore, during use, after the reset source is obtained, the reset flag can be cleared through the RSTFC control bit, so that a watchdog reset or other reset events can be more accurately reflected in the RCU_RSTSCK register.
MCU integrates a power-up / power-down reset circuit. When designing an external reset circuit, a capacitor (typical value of 100nF) must be placed on the NRST pin to ensure that the power on the NRST pin generates a low pulse delay of at least 20us for completing effective power-on reset process.

Figure 2-13. RCU_RSTSCK Register

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
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</thead>
<tbody>
<tr>
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<td>WWDGT_RSTP</td>
<td>FWDGT_RSTP</td>
<td>SW_RSTP</td>
<td>POR_RSTP</td>
<td>EP_RSTP</td>
<td>BOR_RSTP</td>
<td>RSTFC</td>
<td>Reserved</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
</tr>
</tbody>
</table>

Figure 2-14. System Reset Circuit

Figure 2-15. Recommend External Reset Circuit

Note:

1. Internal pull-up resistance $R_{PU} = 40 \, k\Omega$. You are advised to use an external pull-up resistance of 10 kΩ to ensure that voltage interference does not cause chip abnormalities.
2. If the influence of static electricity is considered, an ESD protection diode can be placed at the NRST pin.
3. Although there is a hardware POR circuit inside the MCU, it is still recommended to add an external NRST reset resistor-capacitor circuit.
4. If the MCU starts abnormally (due to voltage fluctuations, etc.), the capacitance value of NRST to ground can be appropriately increased, and the MCU reset completion time can be extended to avoid the abnormal power-on sequence area.

2.2. Clock

GD32H7xx series has a complete clock system inside, and you can choose a suitable clock source according to different applications. The main features of the clock:

- 4 - 50 MHz external high-speed crystal oscillator (HXTAL).
- Internal 64 MHz RC oscillator (IRC64M).
- Internal 48 MHz RC oscillator (IRC48M).
- 32.768 kHz external low-speed crystal oscillator (LXTAL).
- Internal 32 kHz RC oscillator (IRC32K).
- Low power internal 4M RC oscillator (LPIRC4M).
- PLL clock source can be selected from HXTAL, LPIRC4M or IRC64M.
- PLLs support integer and decimal multiplication factors.
- The decimal frequency factor of PLLs can be modified at runtime.
- The peripheral clock supports dynamic switching.
- HXTAL clock monitor.
- LXTAL clock monitor.
Note:

1. REFSEL is the LPDTS reference clock selection bit, which can be selected as CK_PCLK4 or CK_LXTAL.
2. CK_PER is a peripheral clock, which can be a CK_LPIRC64MDIV, CK_LPIRC4M or CK_HXTAL.
3. CK_TPIU is the tracking port interface unit (TPIU) clock, which can be a CK_IRC64MDIV, CK_LPIRC4M, CK_HXTAL or CK_PLL0R.
4. CK_RSPDIF_SYMB is the RSPDIF symbol clock.
5. ADCSCK selects the bit for ADC synchronous clock.
6. USBHSx 60M is the internal PHY 60M input clock source of USBHSx.

2.2.1. External high-speed crystal oscillator clock (HXTAL)

An external high-speed crystal oscillator with a frequency range of 4 - 50MHz can provide a more accurate clock source for the system clock. Crystals with specific frequencies must be connected to the pins near the two HXTAL. The external resistance and capacitance connected to the crystal must be adjusted according to the selected oscillator.

Figure 2-17. HXTAL External Crystal Circuit

![Diagram of HXTAL External Crystal Circuit]

Figure 2-18. HXTAL External Clock Circuit

![Diagram of HXTAL External Clock Circuit]

Note:

1. When using the bypass input, the signal is input from OSCIN, and OSCOUT remains floating.
2. For the size of the external matching capacitor, please refer to the formula: $$C_1 = C_2 =$$
2*(C_{LOAD} - C_S), where C_S is the stray capacitance of the PCB and MCU pins, with a typical value of 10pF. When it is recommended to use an external high-speed crystal, try to choose a crystal load capacitance of about 20pF, so that the external matching capacitors C_1 and C_2 can be 20pF, and the PCB layout should be as close to the crystal pin as possible.

3. C_S is the parasitic capacitance on the PCB board traces and MCU pins. The closer the crystal is to the MCU, the smaller the C_S, and vice versa. Therefore, in practical applications, when the crystal is far away from the MCU, causing the crystal to work abnormally, the external matching capacitor can be appropriately reduced.

4. When using an external high-speed crystal, it is recommended to connect a 1MΩ resistor in parallel at both ends of the crystal to make the crystal easier to vibrate.

5. Accuracy: external active crystal oscillator > external passive crystal > internal crystal oscillator.

6. When the active crystal oscillator is used normally, Bypass will be turned on. At this time, the high level is required to be no less than 0.7 V_{DD}, and the low level is no more than 0.3 V_{DD}. If Bypass is not turned on, the amplitude requirements of the active crystal oscillator will be greatly reduced.

7. The traces connecting the resonator to the MCU clock pins may cause inconsistent lengths of the traces connected to the OSCOUT and OSCIN pins due to the space constraints of the PCB layout. This will make the stray capacitances introduced by the two PCB traces inconsistent, so that the load capacitances on both sides of the resonator cannot be equal in value, and there needs to be a difference to match the actual PCB board. In this case, it is recommended to contact the resonator manufacturer to calculate the actual value.

2.2.2. **External low-speed crystal oscillator clock (LXTAL)**

LXTAL is an external low-speed crystal or ceramic resonator with a frequency of 32.768kHz. It provides a low-power and high-precision clock source for real-time clock circuits. The LXTAL oscillator can be turned on and off by setting the LXTALEN bit in the backup domain control register (RCU_BDCTL). The LXTALSTB bit in the backup domain control register RCU_BDCTL is used to indicate whether the LXTAL clock is stable. If the corresponding interrupt enable bit LXTALSTBIE in the interrupt register RCU_INT is set to ‘1’, an interrupt will be generated after LXTAL stabilizes.

The external clock bypass mode can be selected by setting the LXTALBPS and LXTALEN to 1 of the backup domain control register RCU_BDCTL. CK_LXTAL is consistent with the external clock signal connected to the OSC32IN pin.
Figure 2-19. LXTAL External Crystal Circuit

Figure 2-20. LXTAL External Clock Circuit

Note:

1. When using the bypass input, the signal is input from OSC32IN, and OSC32OUT remains floating.

2. For the size of the external matching capacitor, please refer to the formula: \( C_1 = C_2 = 2(C_{LOAD} - C_S) \), where \( C_S \) is the stray capacitance of the PCB and MCU pins, the empirical value is between 2pF ~ 7pF, and 5pF is recommended as a reference value calculation. When it is recommended to use an external crystal, try to choose a crystal load capacitance of about 10pF, so that the externally connected matching capacitors \( C_1 \) and \( C_2 \) can be 10pF, and the PCB layout should be as close to the crystal pin as possible.

3. When the RTC selects IRC32K as the clock source and uses VBAT external independent power supply, if the MCU loses power at this time, the RTC will stop counting. After re powering on, the RTC will continue to accumulate timing based on the previous count value. If the application needs to use VBAT to power the RTC, and the RTC can still clock normally, the RTC must choose LXTAL as the clock source.

4. MCU can set the driving capacity of LXTAL. If during actual debugging, it is found that external low-speed crystals are difficult to vibrate, try adjusting the driving capacity of LXTAL to high.

5. The traces connecting the resonator to the MCU clock pins may cause inconsistent lengths of the traces connected to the OSCOUT and OSCIN pins due to the space constraints of the PCB layout. This will make the stray capacitances introduced by the two PCB traces inconsistent, so that the load capacitances on both sides of the resonator
cannot be equal in value, and there needs to be a difference to match the actual PCB board. In this case, it is recommended to contact the resonator manufacturer to calculate the actual value.

2.2.3. Clock Output Capability (CKOUT)

GD32H7xx series can output internal related clock signals, and different clock signals can be selected by setting the CK_OUT0 clock source selection bit field CKOUT0SEL in the clock configuration register 0 (RCU_CFG2). The corresponding GPIO pin should be configured as a backup function I/O (AFIO) mode to output the selected clock signal. The selection of CK_OUT1 clock output source is achieved by setting the CKOUT1SEL bit field in the clock configuration register RCU_CFG2.

<table>
<thead>
<tr>
<th>CKOUT0SEL[2:0]</th>
<th>Clock source</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>CK_IRC64MDIV</td>
</tr>
<tr>
<td>001</td>
<td>CK_LXTAL</td>
</tr>
<tr>
<td>010</td>
<td>CK_HXTAL</td>
</tr>
<tr>
<td>011</td>
<td>CK_PLL0P</td>
</tr>
<tr>
<td>100</td>
<td>CK_IRC48M</td>
</tr>
<tr>
<td>101</td>
<td>CK_PER</td>
</tr>
<tr>
<td>110</td>
<td>USBHS0 60M</td>
</tr>
<tr>
<td>111</td>
<td>USBHS1 60M</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CKOUT1SEL[2:0]</th>
<th>Clock source</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>CK_SYS</td>
</tr>
<tr>
<td>001</td>
<td>CK_PLL1R</td>
</tr>
<tr>
<td>010</td>
<td>CK_HXTAL</td>
</tr>
<tr>
<td>011</td>
<td>CK_PLL0P</td>
</tr>
<tr>
<td>100</td>
<td>CK_LPIRC4M</td>
</tr>
<tr>
<td>101</td>
<td>CK_IRC32K</td>
</tr>
<tr>
<td>110</td>
<td>CK_PLL2R</td>
</tr>
</tbody>
</table>

By configuring the CKOUT0DIV bit field of the RCU_CFG2 register, the frequency of the CK_OUT0 output clock can be proportionally divided, thereby reducing the output frequency of CK_OUT0.

By configuring the CKOUT1DIV bit field of the RCU_CFG0 register, the frequency of the CK_OUT1 output clock can be proportionally divided, thereby reducing the output frequency of CK_OUT1.

2.2.4. HXTAL Clock Monitor (CKM)

Set the HXTAL clock monitoring enable bit CKMEN in the control register RCU_CTL, which
enables the clock monitoring function. This function must be enabled after the delay of HXTAL start is completed, and disabled after HXTAL stop. Once an HXTAL fault is detected, HXTAL will automatically be disabled, and the HXTAL clock blocking interrupt flag bit CKMIF in the interrupt register RCU_INT will be set to ‘1’, generating an HXTAL fault event. The interrupt caused by this fault is connected to the non maskable interrupt NMI of Cortex®-M7. If HXTAL is selected as the clock source for the system or PLL0, a HXTAL fault will prompt the selection of IRC64M as the system clock source and PLL0 will be automatically disabled. If HXTAL is selected as the clock source for PLLs, a HXTAL fault will cause the PLL to be automatically disabled.

2.2.5. LXTAL Clock Monitor (LCKM)

Set the LXTAL clock monitoring enable bit LCKMEN in the clock control register RCU_BDCTL, which enables the clock monitoring function. This function must be enabled after the LXTAL start delay is completed. The clock monitor on LXTAL operates in all modes except VBAT. If a fault is detected on an external 32 kHz oscillator, an interrupt can be sent to the CPU. Then the software must disable the LCKMEN bit, stop the defective 32 kHz oscillator, and change the RTC clock source, or take any necessary measures to protect the application.

When LCKMEN is enabled, a 4-bit plus a counter will operate in the IRC32K domain. If the LXTAL clock gets stuck at 0 / 1 error or slows down by about 20KHz, the counter will overflow. LXTAL clock fault will be detected. Once an LXTAL fault is detected, the LXTAL clock blocking interrupt flag bit LCKMIF in the interrupt register RCU_INT will be set to ‘1’, generating an LXTAL fault event. This interrupt is connected to the EXTI 18 interrupt line and can be used to wake up from sleep or deep sleep mode. LXTAL fault events can also wake up the system from standby mode.

2.3. Startup Configuration

The GD32H7xx series MCU provides different boot sources, which can be selected through the boot pin and boot address 0/1 [15:0] in the Arm® Cortex®-M7 core register (FMCBTADDRMDF) boot address. Details can be found in Table 2-4, BOOT mode selection and Table 2-5, Details of BOOT mode. The level state of the BOOT pin will be latched on the rising edge of the fourth CKSYS (system clock) after reset. Users can choose the desired boot source by setting the pin level of the BOOT after power on reset and system reset.

The BOOT_ADDR[15:0] and BOOT_ADDR[15:0] addresses allow the boot memory address to be configured to any address between 0x0000 0000 and 0x9000 0000. The boot mode can be obtained from the BOOT_MODE [2:0] bit field of the SYSCFG_USERCFG0 register.
Table 2-4. BOOT mode selection

<table>
<thead>
<tr>
<th>Boot source address</th>
<th>Boot mode selection pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSB of the boot address: defined by BOOT_ADDR0[15:0]</td>
<td></td>
</tr>
<tr>
<td>LSB of the boot address: 0x0000</td>
<td>0</td>
</tr>
<tr>
<td>MSB of the boot address: defined by BOOT_ADDR1[15:0]</td>
<td></td>
</tr>
<tr>
<td>LSB of the boot address: 0x0000</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 2-5. Details of BOOT mode

<table>
<thead>
<tr>
<th>SCR</th>
<th>SPC[7:0]</th>
<th>BOOT_ADDRESS (configured in BOOT_ADDRx(x = 0,1))</th>
<th>BOOT_MODE</th>
<th>Boot from</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>x</td>
<td>XXXX</td>
<td>SECURITY BOOT</td>
<td>ROM</td>
</tr>
<tr>
<td></td>
<td>Protection level high</td>
<td>0x9000_0000</td>
<td>USER BOOT</td>
<td>OSPI0</td>
</tr>
<tr>
<td></td>
<td>Protection level high</td>
<td>0x7000_0000</td>
<td>USER BOOT</td>
<td>OSPI1</td>
</tr>
<tr>
<td></td>
<td>Protection level high</td>
<td>0x0800_0000~max user flash</td>
<td>USER BOOT</td>
<td>BOOT_ADDRESS</td>
</tr>
<tr>
<td></td>
<td>Protection level low</td>
<td>0x9000_0000</td>
<td>USER BOOT</td>
<td>OSPI0</td>
</tr>
<tr>
<td></td>
<td>Protection level low</td>
<td>0x7000_0000</td>
<td>USER BOOT</td>
<td>OSPI1</td>
</tr>
<tr>
<td></td>
<td>Protection level low</td>
<td>0x2408_0000~max RAM shared(ITCM/DTCM/AXI)</td>
<td>SRAM BOOT(RAM shared)</td>
<td>BOOT_ADDRESS</td>
</tr>
<tr>
<td></td>
<td>Protection level low</td>
<td>0x2400_0000~max AXI SRAM</td>
<td>SRAM BOOT(AXI SRAM)</td>
<td>BOOT_ADDRESS</td>
</tr>
<tr>
<td></td>
<td>Protection level low</td>
<td>0x2000_0000</td>
<td>SRAM BOOT(DTCM)</td>
<td>0x2000_0000</td>
</tr>
<tr>
<td></td>
<td>Protection level low</td>
<td>0x0800_0000~max user flash</td>
<td>USER BOOT</td>
<td>BOOT_ADDRESS</td>
</tr>
<tr>
<td></td>
<td>Protection level low</td>
<td>0x0000_0000</td>
<td>SRAM BOOT(ITCM)</td>
<td>0x0000_0000</td>
</tr>
<tr>
<td></td>
<td>Protection level low</td>
<td>0x1FF0_0000</td>
<td>SYSTEM BOOT</td>
<td>BootLoader</td>
</tr>
<tr>
<td>Other</td>
<td>Protection level low</td>
<td>Other</td>
<td>USER BOOT</td>
<td>0x0800_0000 (BOOT Pin = 0)</td>
</tr>
<tr>
<td></td>
<td>Protection level low</td>
<td>Other</td>
<td>SYSTEM BOOT</td>
<td>BootLoader (BOOT Pin = 1)</td>
</tr>
</tbody>
</table>

Figure 2-21. Recommend BOOT Circuit Design

![BOOT Circuit Design](GD32H7xx)
2.4. Typical Peripheral Modules

2.4.1. GPIO Circuit

GD32H7xx can support up to 135 universal I/O pins (GPIO), including PA0 ~ PA15, PB0 ~ PB15, PC0 ~ PC15, PD0 ~ PD15, PE0 ~ PE15, PF0 ~ PF15, PG0 ~ PG15, PH0 ~ PH15, PJ8 ~ PJ11, PK0 ~ PK2. Each on-chip device uses it to implement logical input / output functions. Each GPIO port has relevant control and configuration registers to meet the specific application requirements. The external interrupt of the GPIO pin of the on-chip device is controlled and configured by the register of the EXTI module. The basic structure of the GPIO port is shown in Figure 2-22, Basic structure of standard IO.

Figure 2-22. Basic structure of standard IO

Note:
1. The IO port is divided into 5V tolerant and non-5V tolerant. When using, pay attention to distinguish the IO port withstand voltage, refer to the datasheet for details.
2. When the 5V-tolerant IO port is configured as an open drain output or input mode, a 5V voltage can be connected. When configured as a push-pull output mode, it is prohibited to connect a 5V voltage.
3. To improve EMC performance, it is recommended to pull up or pull down the unused IO pins by hardware.
4. The three IO ports of PC13, PC14, PC15 have weak drive capability and limited output current capability (about 3mA). When configured in output mode, their working speed...
cannot exceed 2MHz (Maximum load is 30pF).

5. The same label PIN in multiple groups can only configure one port as an external interrupt. For example, PA0, PB0, and PC0 only support one of the three IO ports to generate external interrupts, and do not support three external interrupt modes.

6. Non-5V tolerance I/O, external voltage over VDD, may generate perfusion current

2.4.2. ADC Circuit

GD32H7xx integrates a 12/14 bit successive approximation analog-to-digital converter module (ADC) internally. ADC0 has 20 external channels, 1 internal channel (DAC_OUT0 channel), ADC1 has 18 external channels, 3 internal channels (battery voltage (VBAT) channel, reference voltage input channel (VREFINT), and DAC_OUT0 channel), ADC2 has 17 external channels, 4 internal channels (battery voltage (VBAT) channel, reference voltage input channel (VREFINT), internal temperature sensing channel (VSENSE), and high-precision temperature sensor channel (VSENSE2)). ADC sampling channels support multiple operation modes. After sampling conversion, conversion results can be stored in the corresponding data register in the least significant bit alignment or most significant bit alignment (ADC0/1 is a 32-bit data register, and ADC2 is a 16 bit data register). The on-chip hardware oversampling mechanism can improve performance by reducing the related computing burden from MCU.

If the ADC collects the external input voltage during use, if the sampled data fluctuates greatly, it may be due to the interference caused by power supply fluctuations. You can calibrate by sampling the internal VREFINT and then calculate the externally sampled voltage.

When designing the ADC circuit, it is recommended to place a small capacitor at the ADC input pin, as shown in Figure 2-23, ADC Acquisition Circuit Design.

Figure 2-23. ADC Acquisition Circuit Design

![ADC Acquisition Circuit Design](image)

Some pins are directly connected to PA0_C, PA1_C, PC2_C and PC3_C ADC analog input terminal (as shown in Figure 2-24, Analog configuration of ADC): The Pxy_C and Pxy pins are directly connected through analog switches.
2.4.3. Internal temperature sensor calibration

The GD32H7xx series MCU is internally integrated with a temperature sensor (ADC2_CH18), a high-precision temperature sensor (ADC2_CH20) and a low power digital temperature sensor (LPDTS), with an effective temperature measurement range of -40 °C to 105 °C. The output voltage of the temperature sensor varies linearly with temperature. To ensure the accuracy of temperature measurement, it is necessary to provide an accurate and low-temperature drift reference voltage $V_{REFP}$ for the ADC.

The output voltage of the temperature sensor varies linearly with temperature. Due to the diversity of chip production processes, the deviation of the temperature change curve may vary between chips (up to 45 °C difference). Internal temperature sensors are more suitable for detecting temperature changes than for measuring absolute temperature. If precise temperature measurement is required, an external temperature sensor should be used to calibrate this offset error.

The internal voltage reference ($V_{REFINT}$) provides a stable (bandgap reference) voltage output to the ADC and comparator. $V_{REFINT}$ internal connection to ADC1_CH17 / ADC2_CH19 input channel.

Using temperature sensors:

1. Configure the conversion sequence and sampling time of the temperature sensor channel (ADC1_CHANNEL) to $ts_{_temp}$ us;
2. Set the TSVEN1 bit in the ADC_CTL1 register to enable the temperature sensor;
3. Set the ADCON bit of the ADC_CTL1 register, or trigger ADC conversion externally;
4. Read and calculate the temperature sensor data $V_{\text{temperature}}$ from the ADC data register, and calculate the actual temperature using the following formula:

$$\text{Temperature}(\degree C) = \left\{ \left( V_{25} - V_{\text{temperature}} \right) / \text{Avg}_-\text{Slope} \right\} + 25$$

$V_{25}$: The voltage of the internal temperature sensor at 25 °C, please refer to the datasheet for typical values.

$\text{Avg}_-\text{Slope}$: The average slope of the temperature and internal temperature sensor voltage curve, please refer to the datasheet for typical values.

Using high-precision temperature sensors:

1. Configure the conversion sequence and sampling time of the temperature sensor channel (ADC2_CH20) to $ts_\text{temp}$ us;
2. Set the TSVEN2 bit in the ADC_CTL1 register to enable the temperature sensor;
3. Set the ADCON bit of the ADC_CTRL1 register, or trigger ADC conversion externally;
4. Read and calculate the temperature sensor data $V_{\text{temperature}}$ from the ADC data register, and calculate the actual temperature using the following formula:

$$\text{Temperature}(\degree C) = \left\{ (V_{\text{temperature}} - V_{25}) / \text{Avg}_-\text{Slope} \right\} + 25$$

$V_{25}$: The voltage of the internal temperature sensor at 25 °C, please refer to the datasheet for typical values.

$\text{Avg}_-\text{Slope}$: The average slope of the temperature and internal temperature sensor voltage curve, please refer to the datasheet for typical values.

**Note:**

1. When a high-precision temperature sensor is enabled, it is necessary to wait for at least 3 ADC sampling cycles, and the first three converted data should be discarded;
2. The accuracy of high-precision temperature sensor can be improved by oversampling and software averaging (50 point averaging is generally recommended).

Low power digital temperature sensor (LPDTS) is used to transmit square wave, which is converted by temperature and the frequency is proportional to the absolute temperature. The frequency measurement is based on the PCLK or the LXTAL clock.

A signal is output, which FM(T) frequency (typically 641 kHz) is related to temperature, by the analog part of temperature sensor. Two counters are embedded in the temperature sensor block, which makes the counting mode relevant to the reference clock frequency. The counting result is stored in the LPDTS_DATA register.

- When the reference clock is PCLK, the measurement method is to sample one or multiple FM(T) cycles and count at the rising edge and falling edge of PCLK.
- When the reference clock is LXTAL, the measurement method is to sample one or multiple LXTAL cycles and count at the rising edge and falling edge of FM(T).
The Temperature calculation formula When PCLK is used:
\[ T = T_0 + \left( \frac{2 \times F_{\text{PCLK}}}{\text{COVAL}} \right) \times SPT - 100 \times FREQ / RF_{\text{CF}} \]

The Temperature calculation formula When LXTAL is used:
\[ T = T_0 + \left( \frac{F_{\text{LXTAL}} \times \text{COVAL}}{2 \times SPT} \right) - \left( \frac{100 \times FREQ}{RF_{\text{CF}}} \right) \]

\( T_0 \): \( T_0 \) equal to 25 °C.
\( \text{COVAL} \): \( \text{COVAL} \) is the value of the counter output value for temperature sensor which measured and stored in the LPDTS_DATA register.
\( SPT \): \( SPT \) is Sampling time for temperature sensor.
\( FREQ \): \( FREQ \) is engineering value of the frequency measured at \( T_0 \) for temperature sensor which measured and stored in the LPDTS_SDATA register. It is expressed in hundreds of Hertz.
\( RF_{\text{CF}} \): \( RF_{\text{CF}} \) is the engineering value of the ramp coefficient for the temperature sensor.

2.4.4. **USB Circuit**

The GD32H7xx series MCU has an embedded USBHS interface, providing a USB interconnection solution for portable devices. USBHS not only supports host mode and device mode, but also supports OTG mode that follows HNP (Host Negotiation Protocol) and SRP (Session Request Protocol). The USBHS includes an internal USB PHY that can be configured to either full speed or high speed, and no longer requires an external PHY chip. USBHS can support all four transmission methods defined by the USB 2.0 protocol (control transmission, batch transmission, interrupt transmission, and synchronous transmission). In addition, there is a DMA engine operation inside the USBHS that can act as an AHB bus host to accelerate data transmission between the USBHS and the system. For the operation of full speed devices, it also supports Battery Charge Detection (BCD), Additional Detection Protocol (ADP), and Link Layer Power Management (LPM).

The USB protocol requires a clock accuracy of no less than 500ppm, and internal clocks may not be able to achieve such accuracy. Therefore, it is recommended to use external crystals.
or active crystal oscillators as the clock source for the USB module when using the USB function. When designing the circuit, in order to improve the ESD performance of USB, it is recommended to design a resistance capacitance discharge isolation circuit for the USB shell. The description of the USBHS signal line is shown in Table 2-6. USBHS signal line description.

Table 2-6. USBHS signal line description

<table>
<thead>
<tr>
<th>I/O port</th>
<th>Type</th>
<th>Description</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>VBUS</td>
<td>Input</td>
<td>Bus power port</td>
<td>For internal PHY only</td>
</tr>
<tr>
<td>DM</td>
<td>Input/Output</td>
<td>Differential data line - port</td>
<td>For internal PHY only</td>
</tr>
<tr>
<td>DP</td>
<td>Input/Output</td>
<td>Differential data line + port</td>
<td>For internal PHY only</td>
</tr>
<tr>
<td>ID</td>
<td>Input</td>
<td>USB identification: Mini connector identification port</td>
<td>For internal PHY only</td>
</tr>
<tr>
<td>ULPI_D[7:0]</td>
<td>Input/Output</td>
<td>ULPI Data line</td>
<td>For external ULPI PHY</td>
</tr>
<tr>
<td>ULPI_NXT</td>
<td>Input</td>
<td>ULPI next line</td>
<td>For external ULPI PHY</td>
</tr>
<tr>
<td>ULPI_DIR</td>
<td>Input</td>
<td>ULPI Direction</td>
<td>For external ULPI PHY</td>
</tr>
<tr>
<td>ULPI_STP</td>
<td>Output</td>
<td>ULPI Stop</td>
<td>For external ULPI PHY</td>
</tr>
<tr>
<td>ULPI_CLK</td>
<td>Input</td>
<td>ULPI Clock</td>
<td>For external ULPI PHY</td>
</tr>
</tbody>
</table>

USBHS includes an internal embedded PHY that supports high, full, and low speeds in host mode, high and full speeds in device mode, and OTG protocols with HNP and SRP. The pull-up or pull-down resistors are already integrated into the internal full speed PHY, and the USBHS can automatically control based on the current mode (host, device, or OTG mode) and connection status. Connection diagram using internal PHY is shown in Figure 2-26. Connection diagram in host or device mode. The connection diagram of OTG mode is shown in Figure 2-27. Connection diagram of using internal embedded PHY in OTG mode.

Figure 2-26. Connection diagram in host or device mode

Recommended: R=1M Ω, C=4700pF.
USBHS provides an ULPI interface for external PHYs. If a USBHS module is required to complete high-speed USB applications, then an external high-speed ULPI PHY is required. Combined with external ULPI PHY, USBHS supports high-speed hosts and devices, as well as all modes described in the previous article for internal embedded full speed PHY. The connection diagram of using external ULPI PHY is shown in Figure 2-28. Connection diagram of using external ULPI PHY.

The GD32H7xx series USB integrates a voltage regulator internally, which users can choose to enable. Connect the VDD50USB pin to a 5 V power supply to provide power for the USB module, as shown in Figure 2-29. Connection diagram of USB voltage regulator during power supply; Alternatively, bypass the voltage regulator and connect the VDD33USB pin to a 3.3 V power supply to provide power to the USB module, as shown in Figure 2-30.
Connection diagram for USB voltage regulator bypass.

Figure 2-29. Connection diagram of USB voltage regulator during power supply

![Connection diagram of USB voltage regulator during power supply](image)

Figure 2-30. Connection diagram for USB voltage regulator bypass

![Connection diagram for USB voltage regulator bypass](image)

2.5. Thermal management and low power consumption mode

GD32H7xx series has a high power consumption when using more peripherals, and users should ensure that $T_J < 125$ °C under any working condition when using it. For external circuits, refer to “AN060 Thermal management manual for GD32 MCU” and choose the appropriate heat dissipation method. There are three ways to achieve lower power consumption in internal control: slow down the system clock (HCLK, PCLK1, and PCLK2), turn off the clock of unused peripherals, or configure the output voltage of LDO through the LDOVS[2:0] bit of the PMU_CTL3 register. LDOVS[2:0] can only be configured when PLL is not enabled.

In addition, three power-saving modes can achieve lower power consumption, namely sleep mode, deep sleep mode, and standby mode. The standby mode has the lowest power consumption, and this low-power mode also requires the longest wake-up time. Wake up from Standby mode can be achieved through the rising edge of the WKUP pin, totaling 5 WKUP pins. At this time, there is no need to configure the corresponding GPIO, only the WUPENx bit in the PMU_CS register needs to be configured. The corresponding WKUP wake-up pin reference circuit design is shown in [Figure 2-31. Recommend Standby external wake-up pin circuit design](image).

Figure 2-31. Recommend Standby external wake-up pin circuit design

![Recommend Standby external wake-up pin circuit design](image)

Note: In this mode, attention should be paid to the circuit design. If there is a series resistance...
between the WKUP pin and $V_{DD}$, additional power consumption may be added.

## 2.6. Download the debug circuit

The GD32H7xx series supports both JTAG debugging interface and SWD debugging interface. By default it supports SWD interface and can be modified to JTAG mode through effuse. It also supports secure JTAG, but cannot be rolled back to SWD mode, refer to “AN111 GD32H7xx Software Development Guide” for details. The JTAG interface standard is a 20 pin interface, with 5 signal interfaces, and the SWD interface standard is a 5 pin interface, with 2 signal interfaces.

**Note:** After reset, the debug related ports are in input pull-up / pull-down mode, where:

- PA15: JTDI in pull-up mode.
- PA14: JTCK / SWCLK in pull-down mode
- PA13: JTMS / SWDIO in pull-up mode
- PB4: NJTRST in pull-up mode
- PB3: JTDO in floating mode.

### Table 2-7. JTAG download debug interface assignment

<table>
<thead>
<tr>
<th>Alternate function</th>
<th>GPIO port</th>
</tr>
</thead>
<tbody>
<tr>
<td>JTMS</td>
<td>PA13</td>
</tr>
<tr>
<td>JTCK</td>
<td>PA14</td>
</tr>
<tr>
<td>JTDI</td>
<td>PA15</td>
</tr>
<tr>
<td>JTDO</td>
<td>PB3</td>
</tr>
<tr>
<td>NJRST</td>
<td>PB4</td>
</tr>
</tbody>
</table>

### Figure 2-32. Recommend JTAG wiring reference design

![JTAG Wiring Reference Design](image-url)
Note: After reset, the debug related ports are in input pull-up / pull-down mode, where:

PA13: SWDIO in pull-up mode.
PA14: SWCLK in pull-down mode

Table 2-8. SWD download debug interface assignment

<table>
<thead>
<tr>
<th>Alternate function</th>
<th>GPIO port</th>
</tr>
</thead>
<tbody>
<tr>
<td>SWDIO</td>
<td>PA13</td>
</tr>
<tr>
<td>SWCLK</td>
<td>PA14</td>
</tr>
</tbody>
</table>

Figure 2-33. Recommend SWD Wiring Reference Design

There are several ways to improve the reliability of SWD download and debugging communication and enhance the anti-interference ability of download and debugging.

1. Shorten the length of the two SWD signal lines, preferably within 15 cm.
2. Weave the two SWD wires and the GND wire into a twist and twist them together.
3. Connect separately tens of pF small capacitors in parallel between the two signal lines of the SWD and the ground.
4. Any IO of the two signal lines of SWD is connected in series with a 100 Ω ~ 1 kΩ resistor.
2.7. Reference Schematic Design

Figure 2-34. GD32H7xx Recommend Reference Schematic Design
3. PCB Layout Design

In order to enhance the functional stability and EMC performance of the MCU, it is not only necessary to consider the performance of the supporting peripheral components, but also the PCB Layout. In addition, when conditions permit, try to choose a PCB design solution with an independent GND layer and an independent power supply layer, which can provide better EMC performance. If conditions do not allow, independent GND layer and power supply layer cannot be provided, then it is also necessary to ensure a good power supply and grounding design, such as making the GND plane under the MCU as complete as possible.

In applications with high power or strong interference, it is necessary to consider keeping the MCU away from these strong interference sources.

3.1. Power Supply Decoupling Capacitors

The GD32H7xx series power supply has VDD, VDDA, VREF and other power supply pins. Ceramic MLCC can be used for the 100nF decoupling capacitor, and the position should be as close to the power pin as possible. The power cable should be routed through the capacitor before reaching the MCU power pin. It is recommended to lay out a Layout in the form of Via near the capacitor PAD.

Figure 3-1. Recommend Power Pin Decoupling Layout Design

3.2. Clock Circuit

GD32H7xx series clocks have HXTAL and LXTAL, and the clock circuit (including crystal or crystal oscillator and capacitor, etc.) is required to be placed close to the MCU clock pin, and the clock trace should be wrapped by GND as much as possible.
Figure 3-2. Recommend Clock Pin Layout Design (passive crystal)

Note:
1. The crystal should be as close to the MCU clock pin as possible, and the matching capacitor should be as close as possible to the crystal.
2. The whole circuit should be on the same layer as the MCU, and the wiring should not go through the layer as much as possible.
3. The PCB area of the clock circuit should be kept as empty as possible, and no traces unrelated to the clock should be taken.
4. High-power, high-interference risk devices and high-speed wiring should be kept away from the clock crystal circuit as far as possible.
5. The clock line is grounded to achieve a shielding effect.

3.3. Reset Circuit

NRST trace PCB Layout reference is as follows:

Figure 3-3. Recommend NRST Trace Layout Design

Note: The resistance and capacitance of the reset circuit should be as close as possible to
the NRST pin of the MCU, and the NRST trace should be kept away from devices with strong interference risk and high-speed traces as far as possible. If conditions permit, it had better to wrap the NRST traces for better shielding effect.

3.4. USB Circuit

For the GD32H7xx series MCU USB FS module, there are two differential signal lines DM and DP. For the USB HS module, after the external high-speed PHY is connected, the PHY chip will also lead out two differential signal lines DM and DP. It is recommended that the PCB wiring requires a characteristic impedance of 90Ω. The differential wiring should be strictly in accordance with the equal length isometric gauge, and the wiring should be as short as possible. If the two differential lines are not equal in length, a serpentine wire can be used at the terminal to compensate for the short line. It is recommended to connect DM and DP directly without matching resistors in series.

DM and DP differential wiring reference is as follows:

1. Reasonably arrange the layout to shorten the differential routing distance.
2. Give priority to drawing differential lines, try not to exceed two pairs of vias on a pair of differential lines, and place them symmetrically.
3. Symmetrical parallel wiring ensures close coupling between two wires, avoiding 90°, arc or 45° wiring methods.
4. Devices such as resistors, capacitors, EMC, or test points connected to the differential wiring should also adhere to the principle of symmetry.

For the USB HS module, the data and signal control lines between the MCU and the external HS PHY should also be kept as short as possible. It is necessary to use serpentine wires for equal length processing, and the following precautions should be taken:

1. The layout should be arranged reasonably, and the USB HS-PHY chip should be as compact as possible between the MCU.
2. When wiring, take the longest signal wire as the target length and compensate for other signal wires through a serpentine routing.

3.5. BGA Circuit

For some models of the GD32H7xx series MCU with BGA100 (0.8mm Pitch) and BGA176 (0.65mm Pitch) packaging, we recommend the following wiring rules and fanout methods.

For BGA100 package with a 0.8 mm pitch, it is recommended to use a rule setting of 5 mil line width and line spacing. Use 10 / 16 mil through holes for fanout. After fanout, as shown in *Figure 3-4. Fan out method for BGA100 package*. 
For BGA176 package with a 0.65 mm pitch, it is recommended to use a rule setting of 4 mil line width and line spacing. Use 8/12 mil (if the current is large, 8/13 mil can also be used, but larger than 8/13 mil size, 4 mil line width and line spacing cannot be used) through holes for fanout. After fanout, as shown in Figure 3-5. Fan out method for BGA176 package.
4. Package Description

The GD32H7xx series comes in four packaging forms, LQFP100, LQFP144, LQFP176, BGA100 and BGA176.

Table 4-1. Package Description

<table>
<thead>
<tr>
<th>Ordering code</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>GD32H737VxT6</td>
<td>LQFP100(14x14, 0.5 pitch)</td>
</tr>
<tr>
<td>GD32H757VxT6</td>
<td>LQFP144(20x20, 0.5 pitch)</td>
</tr>
<tr>
<td>GD32H737ZxT6</td>
<td>LQFP176(24x24, 0.5 pitch)</td>
</tr>
<tr>
<td>GD32H757ZxT6</td>
<td>BGA100(8x8, 0.8 pitch)</td>
</tr>
<tr>
<td>GD32H737IxT6</td>
<td>BGA176(10x10, 0.65 pitch)</td>
</tr>
</tbody>
</table>

(Original dimensions are in millimeters)
5. Revision history

Table 5-1. Revision history

<table>
<thead>
<tr>
<th>Revision No.</th>
<th>Description</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>Initial Release</td>
<td>Apr.14, 2023</td>
</tr>
</tbody>
</table>
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