GigaDevice Semiconductor Inc.

Methods to Reduce GD32L233 MCU Power Consumption

Application Note
AN106
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1. Introduction

The GD32L233 family of devices is a 32-bit general-purpose microcontroller based on an Arm® Cortex®-M23 core with ultra-low power consumption. Its power module has a variety of power saving modes especially suitable for low power applications. This application note mainly provides a method to reduce power consumption for GD32L233 devices.
2. Reduce power consumption of GD32L233

2.1. Power supply architecture

Power consumption design is one of the most important issues of GD32L233 series products. The power management unit provides ten power saving modes that reduce power consumption and allow applications to strike the best compromise between CPU uptime requirements, speed, and power consumption. As shown in Figure 2-1. Power supply overview, Power Domain overview, the GD32L233 series device has three power domains, including the VDD / VDDA domain, 1.1V domain, and backup domain. The VDD / VDDA domain is directly powered by the power supply. The LDO is embedded in the VDD / VDDA domain to power the 1.1V domain. There is a power switch in the backup domain, and when the VDD power is off, the power switch can switch the power of the backup domain to the VBAT pin, at which point the backup domain is powered by the VBAT pin (battery).

Figure 2-1. Power supply overview
2.2. Power-saving modes

After system reset or power reset, GD32L233 MCU is in full function state and all power domains are in power supply state. At this point, there are three ways to achieve lower power consumption: Slow down the system clock (HCLK, PCLK1 and PCLK2), turn off the clock of unused peripherals, in addition, ten power saving modes can achieve lower power consumption, they are Run mode, Run mode 1, Run mode 2, Sleep mode, Sleep mode 1, Sleep mode 2, Deep sleep mode, Deep sleep mode 1, Deep sleep Mode 2 and Standby mode. The wake up time of low power mode contributes a lot to power optimization and application flexibility, so the trade-off between low power mode consumption and the corresponding wake up time must be made.

Table 2-1. Power saving mode summary

<table>
<thead>
<tr>
<th>Mode</th>
<th>Description</th>
<th>LDO</th>
<th>Entry</th>
<th>Wakeup</th>
<th>Wakeup status</th>
<th>Wakeup Latency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Run</td>
<td>no effect on all clocks, all power on</td>
<td>NPLDO on LPLDO on</td>
<td>system / power reset or wakeup from standby</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Run1</td>
<td>system clock &lt;= 16Mhz</td>
<td>NPLDO on LPLDO on</td>
<td>LDOVS set to 0.9V</td>
<td>clear LDVOS</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Run2</td>
<td>system clock &lt;= 2Mhz</td>
<td>NPLDO in low driver mode</td>
<td>LDOVS set to 0.9V and LDNP set to 1</td>
<td>clear LDVOS and LDNP</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Sleep</td>
<td>Only CPU clock is off</td>
<td>NPLDO on LPLDO on</td>
<td>SLEEPDEEP = 0,WFI or WFE from Run</td>
<td>Any interrupt for WFI Any event (or interrupt when SEVONPEND is 1) for WFE</td>
<td>Run mode</td>
<td>-</td>
</tr>
<tr>
<td>Sleep1</td>
<td>Only CPU clock is off</td>
<td>NPLDO on LPLDO on</td>
<td>SLEEPDEEP = 0,WFI or WFE from Run1</td>
<td>Any interrupt for WFI Any event (or interrupt when SEVONPEND is 1) for WFE</td>
<td>Run1 mode</td>
<td>-</td>
</tr>
<tr>
<td>Sleep2</td>
<td>Only CPU clock is off</td>
<td>NPLDO in low driver mode</td>
<td>SLEEPDEEP = 0,WFI or WFE from Run2</td>
<td>Any interrupt for WFI Any event (or interrupt when SEVONPEND is 1) for WFE</td>
<td>Run2 mode</td>
<td>-</td>
</tr>
<tr>
<td>Deep-</td>
<td>1. All clocks in the 1.1V domain are off 2. Disable IRC16M, IRC48M, HXTAL and PLLs</td>
<td>NPLDO in low driver mode or normal driver mode</td>
<td>SLEEPDEEP = 1, LPMOD = 00, WFI or WFE</td>
<td>Any interrupt from EXTI lines for WFI Any event (or interrupt when SEVONPEND is 1) from EXTI for WFE</td>
<td>Run / Run1 / Run2</td>
<td>IRC16M wakeup time, + Flash wakeup time</td>
</tr>
<tr>
<td>sleep 1</td>
<td>All clocks in the 1.1V domain are off</td>
<td>NPLDO off LPLDO on</td>
<td>SLEEPDEEP = 1, LPMOD = 01,</td>
<td>Any interrupt from EXTI lines for WFI</td>
<td>Run / Run1 / Run2</td>
<td>IRC16M wakeup time,</td>
</tr>
</tbody>
</table>
### Methods to Reduce GD32L233 MCU Power Consumption

<table>
<thead>
<tr>
<th>Mode</th>
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<th>LDO</th>
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<th>Wakeup Latency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Deep-</td>
<td>1. All clocks in the 1.1V domain are off</td>
<td>NPLDO off</td>
<td>SLEEPDEEP =</td>
<td>Any interrupt from EXTI lines for WFI</td>
<td>Run / Run1 / Run2</td>
<td>IRC16M wake-up time</td>
</tr>
<tr>
<td>sleep 2</td>
<td>2. Disable IRC16M, IRC48M, HXTAL and PLLs</td>
<td>LPLDO on</td>
<td>1, LPMOD = 10, WFI or WFE</td>
<td></td>
<td>+ NPLDO wake-up time</td>
<td></td>
</tr>
<tr>
<td></td>
<td>3. LPLDO instead of NPLDO</td>
<td></td>
<td></td>
<td>Any event (or interrupt when SEVONPEND is 1) from EXTI for WFE</td>
<td></td>
<td>+ Flash wake-up time</td>
</tr>
<tr>
<td></td>
<td>4. COREOFF0 / SRAM1 / COREOFF1 power-off.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Standby</td>
<td>1. The 1.1V domain is power off</td>
<td>NPLDO off</td>
<td>SLEEPDEEP =</td>
<td>1. NRST pin</td>
<td>Run</td>
<td>IRC16M wake-up time</td>
</tr>
<tr>
<td></td>
<td>2. Disable IRC16M, IRC48M, HXTAL and PLLs</td>
<td>LPLDO off</td>
<td>1, LPMOD = 11, WFI or WFE</td>
<td>2. WKUP pins</td>
<td>+ NPLDO wake-up time</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3. FWDGT reset</td>
<td>+ Flash wake-up time</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>4. RTC</td>
<td></td>
</tr>
<tr>
<td>BKP_ON</td>
<td>All VDD / 1.1V core domain power off</td>
<td>NPLDO off</td>
<td>VDD off</td>
<td>VDD on</td>
<td>Run</td>
<td>VDD power on sequence</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LPLDO off</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### 2.3. Methods to reduce power consumption

**System clock configuration**

Clock prescaler can be configured with clock frequencies in the AHB and APBx domains. In Run mode, the system clock value is reduced by a clock pre-divider to provide the required clock for the peripherals and to avoid power loss due to overclocking. When peripherals are not in use, power consumption is further reduced through APBx and AHB gated clock disabling.

**Peripheral clock gating**

The more peripherals are activated, the more power is consumed. By controlling the clock that does not use peripherals, energy saving is achieved.

**I/O configuration**

All unused pins should be configured as analog inputs, in which case the Schmidt trigger is disabled and each I/O consumes zero, avoiding the creation of additional current. For output,
the lowest I/O speed is recommended. Do not activate the pull-up or pull-down configuration, if it is not necessary. Users also need to disable clock output pins when they are not needed.

**Using Direct Memory Access (DMA)**

Peripherals can access data through DMA, which not only improves performance but also reduces power consumption. Before the DMA transfer ends, the CPU can enter sleep mode to achieve lower power consumption for the application.

**Use low power mode**

Entering low power mode reduces average application power consumption. In the management of power mode switching, the requirements of application power consumption, wake up source, wake up time and peripheral operation are considered. In low power mode, if the GPIO has external component input/output, you are advised to set the input to pull-up/pull-down and output push-pull to ensure that the GPIO stays stationary when it is idle.

**Use low-power functional peripherals**

Some of the GD32L233 peripherals feature low power consumption, such as LPTIMER and LPUART, which can achieve the required functions and performance while minimizing the power consumption. LPTIMER is a 32-bit timer that can operate in all power modes except Standby mode. Low power universal synchronous asynchronous receiver transmitter (LPUART) provides a low power flexible and convenient serial data exchange interface.

**Set a low core voltage**

The LDO (voltage regulator) powers the internal digital power. Setting a low core voltage is a simple and straightforward method to reduce power consumption. LDO that power the 1.1V domain and remain enabled after reset can be configured to work in different states: It includes Sleep mode (1.1V fully powered state, 0.9V fully powered state and low power state), Deep sleep mode/Deep sleep mode 1/Deep sleep mode 2 (fully powered state or low power state) and standby mode (off state). In standby mode, the 1.1V domain is directly closed to greatly reduce power consumption, but the register content in the domain is lost, including internal RAM.

**Execute code from the SRAM**

When the MCU is operating at normal or low power, code is executed from the SRAM and the flash memory can go into sleep/power down mode, further reducing power consumption.

**Shut down SRAM1**

SRAM1 (0x20004000~0x20007FFF) can be powered off independently. SRAM1 is powered on by default after the system is reset. In order to reduce the power consumption of Run mode/Run mode 1/Run mode 2, SRAM1 can be powered off. To further reduce the power consumption of low power modes (Sleep mode/Sleep Mode 1/Sleep mode 2/Deep sleep mode/Deep sleep mode 1/Deep sleep mode 2), SRAM1 can be powered off before entering low power mode.
COREOFF1 Power domain is powered off

COREOFF1 domain can be powered off separately. COREOFF1 domain is powered off by default after the system is reset. The COREOFF1 domain needs to be powered on when the COREOFF1 domain module is used. To reduce the power consumption of Run mode / Run Mode 1 / Run Mode 2, power off the COREOFF1 domain. To further reduce the power consumption of low power modes (Sleep mode / Sleep Mode 1 / Sleep mode 2 / Deep sleep mode / Deep sleep mode 1 / Deep sleep mode 2), the COREOFF1 domain can be turned off before entering low power mode. COREOFF1 power domain contains the CAU module.
3. Summary

Embedded programs need to reduce power consumption when executing programs for complex real-time applications. For a given manufacturing process and wafer area, power consumption is largely determined by two dynamically controlled factors: voltage and frequency. In GD32L233 devices, LDO provides a fixed voltage for most logic circuits to minimize power consumption, while clock sources, cascaded clock prescaler, gating techniques, and peripheral clock management allow only necessary logic gates to activate. All these methods can reduce power consumption in operating mode. At the same time, the performance and power consumption of various power saving modes are considered to provide users with flexible choices.
4. Revision history

Table 4-1. Revision history

<table>
<thead>
<tr>
<th>Revision No.</th>
<th>Description</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>Initial Release</td>
<td>Apr. 7, 2023</td>
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</table>
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