GigaDevice Semiconductor Inc.

GD32F30x&GD32F403 Hardware Development Guide

Application Note
AN053

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1. Introduction

This article is specially provided for developers of 32-bit general-purpose MCU GD32F30x/GD32F403 series based on Arm® Cortex®-M4 architecture. It provides an overall introduction to the hardware development of GD32F30x/GD32F403 series products, such as power, reset, clock, and startup mode settings and download debugging. The purpose of this application note is to allow developers to quickly get started and use GD32F30x/GD32F403 series products, and quickly develop and use product hardware, save the time of studying manuals, and speed up product development progress.

This application note is divided into seven parts to describe:

1. Power supply, mainly introduces the design of GD32F30x/GD32F403 series power management, power supply and reset functions.
2. Clock, mainly introduces the functional design of GD32F30x/GD32F403 series high and low speed clocks.
3. Boot configuration, mainly introduces the BOOT configuration and design of GD32F30x/GD32F403 series.
4. Typical peripheral modules, mainly introduces the hardware design of the main functional modules of the GD32F30x/GD32F403 series.
5. Download and debug circuit, mainly introduces the recommended typical download and debug circuit of GD32F30x/GD32F403 series.
6. Reference circuit and PCB Layout design, mainly introduces GD32F30x/GD32F403 series hardware circuit design and PCB Layout design notes.
7. Package description, mainly introduces the package forms and names included in the GD32F30x/GD32F403 series.

This document also satisfies the minimum system hardware resources used in application development based on GD32F30x/GD32F403 series products.

Table 1-1. Applicable Products

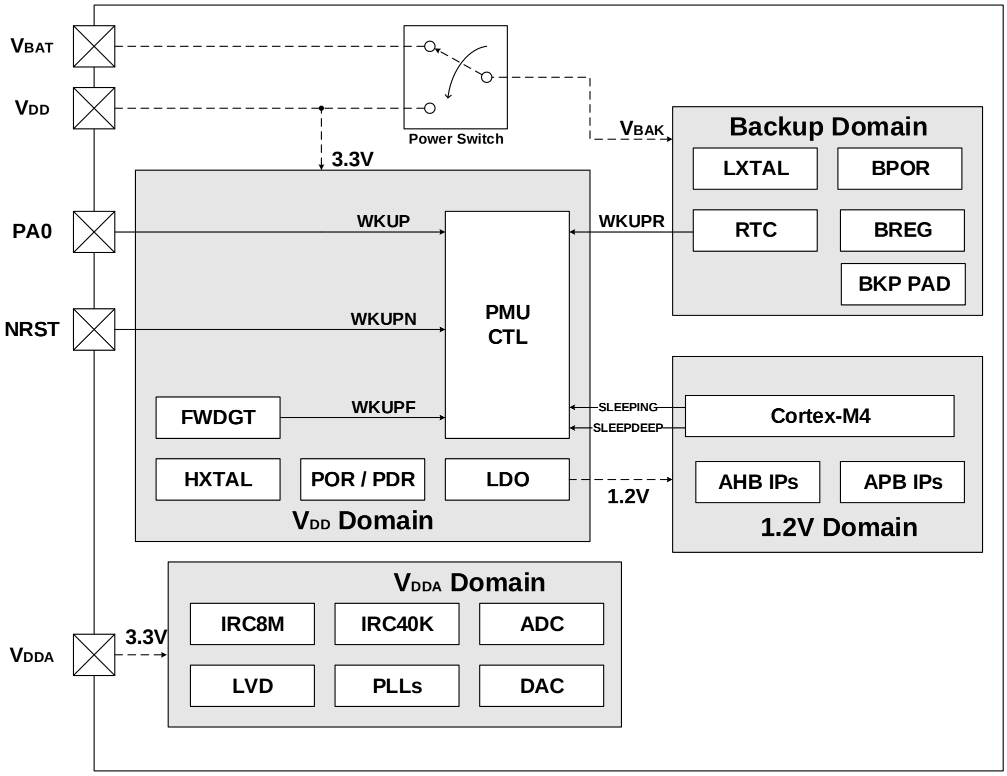
Type	Part Numbers
MCU	GD32F303xx series
	GD32F305xx series
	GD32F307xx series
	GD32F403xx series

2. Hardware design

2.1. Power supply

The V_{DD} / V_{DDA} operating voltage range of GD32F30x/GD32F403 series products is 2.6 V ~ 3.6 V. For GD32F30x/GD32F403 series, there are three power domains, including V_{DD} / V_{DDA} domain, 1.2V domain, and Backup domain, as is shown in ***Figure 2-1. GD32F30x/GD32F403 Power supply overview***. The V_{DD}/V_{DDA} domain is powered directly by the power supply, and an LDO is embedded in the V_{DD}/V_{DDA} domain to power the 1.2 V domain. The backup domain power supply V_{BAK} can be powered by V_{DD} or V_{BAT} through the power switch Power Switch. When the V_{DD} power supply is turned off, the power switch can switch the power supply of the backup domain to the V_{BAT} pin. At this time, the backup domain is powered by the V_{BAT} pin (battery).

Figure 2-1. GD32F30x/GD32F403 Power supply overview



LVD: Low Voltage Detector
POR: Power On Reset
LDO: Voltage Regulator
PDR: Power Down Reset
BPOR: V_{BAK} Power On Reset
BREG: Backup registers

2.1.1. Backup domain

The backup domain supply voltage range is 1.8V ~ 3.6V. In order to ensure the content of the Backup domain registers and the RTC supply, when V_{DD} supply is shut down, V_{BAT} pin can be connected to an optional standby voltage supplied by a battery or by another source. But when V_{DD} is connected, even if the V_{BAT} pin is powered by an external battery, etc., V_{BAK} is still powered by V_{DD}. If no external battery is used in the application, it is recommended to connect V_{BAT} pin externally to V_{DD} pin with a 100nF external ceramic decoupling capacitor.

Note: If the V_{BAT} pin is left floating, the Power Switch will switch V_{BAK} to V_{DD} after the MCU is powered on, and the internal V_{DD} will directly supply power to the Backup domain.

2.1.2. V_{DD}/V_{DDA} Power domain

V_{DD}/V_{DDA} power domain supplies power to all areas except the backup domain. If V_{DDA} is not equal to V_{DD}, the voltage difference between the two is required to be no more than 300mV (the internal V_{DDA} and V_{DD} are connected by back-to-back diodes). To avoid noise, V_{DDA} can be connected to V_{DD} through an external filter circuit, and the corresponding V_{SSA} is connected to V_{SS} through a specific circuit (single-point grounding, through 0Ω resistors or magnetic beads, etc.).

In order to improve the conversion accuracy of the ADC, the independent power supply for V_{DDA} can make the analog circuit achieve better characteristics. There is a V_{REF} pin (2.6 V≤V_{REF+}≤V_{DDA}, V_{REF-}＝V_{SSA}) for ADC independent power supply on the large package.

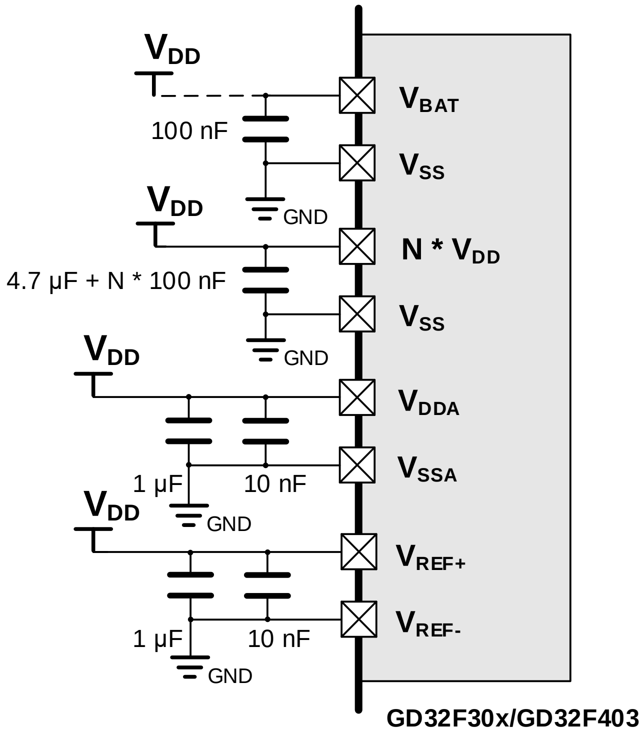
- 100 and more pin package chips contain V_{REF+} and V_{REF-}, V_{REF+} can use an external reference power supply, or can be directly connected to V_{DDA}, V_{REF-} must be connected to V_{SSA}.
- 64 and less pin package chips do not have V_{REF+} and V_{REF-}, they are directly connected to V_{DDA} and V_{SSA} internally, and all analog modules are powered by V_{DDA} (including ADC/DAC).

2.1.3. Power supply design

The system needs a stable power supply. There are some important things to pay attention to when developing and using:

- V_{DD} pin must be connected to an external capacitor (N*100nF ceramic capacitor + not less than 4.7uF tantalum capacitor, at least one V_{DD} needs to be connected to GND with a capacitor of not less than 4.7uF, and other V_{DD} pins are connected to 100nF).
- V_{DDA} pin must be connected with an external capacitor (10nF+1uF ceramic capacitor is recommended).
- V_{BAT} pin must be connected to an external battery (1.8 V ~ 3.6 V). If there is no external battery, it is recommended to connect the V_{BAT} pin to the ground through a 100nF capacitor and then connect it to the V_{DD} pin
- V_{REF+} pin can be directly connected to V_{DDA}. If a separate external reference voltage is used on V_{REF} (2.6V≤V_{REF+}≤V_{DDA}, V_{REF-}= V_{SSA}), a 10nF+1uF ceramic capacitor must also be connected to ground on the V_{REF+} pin.

Figure 2-2. GD32F30x/GD32F403 Recommend Power Supply Design



Note:

1、 All decoupling capacitors must be placed close to the corresponding V_{DD}, V_{DDA}, $V_{REF}+$, V_{BAT} pins of the chip.

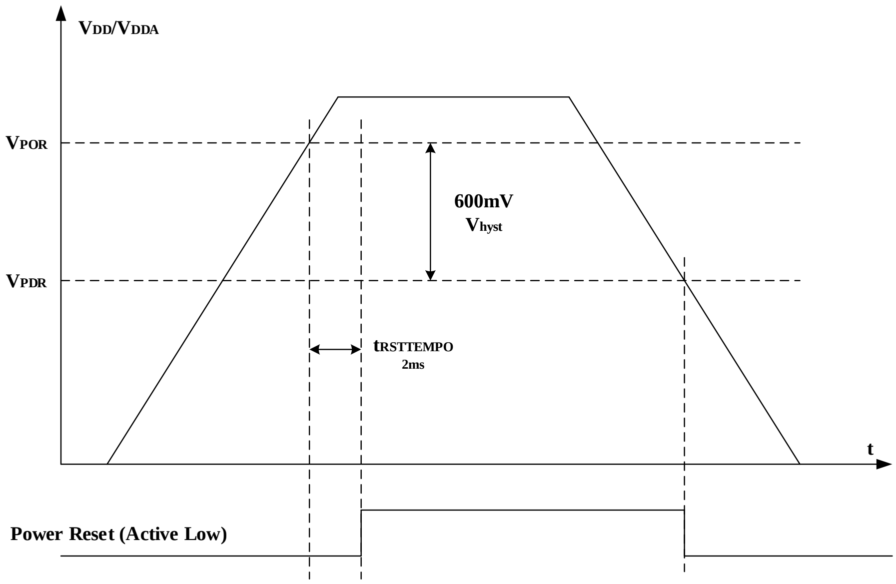
2、 V_{BAT} can be directly connected to V_{DD}, or it can be connected to an external battery according to the actual application.

2.1.4. Reset and power management

GD32F30x/GD32F403 series reset control includes three resets: power reset, system reset and backup domain reset. A power reset is a cold reset, which resets all systems except the backup domain when the power is turned on. During the power and system reset process, NRST will maintain a low level until the reset is over. When the MCU cannot be executed, the NRST pin waveform can be monitored by an oscilloscope to determine whether the chip has been reset.

The chip integrates a POR/PDR (power-on/power-down reset) circuit to detect V_{DD}/V_{DDA} and generate a power reset signal to reset the entire chip except the backup domain when the voltage is lower than a certain threshold. V_{POR} represents the threshold voltage of power-on reset, the typical value is about 2.6V, V_{PDR} represents the threshold voltage of power-down reset, and the typical value is about 1.8V. The value of the hysteresis voltage V_{hyst} is about 600mV.

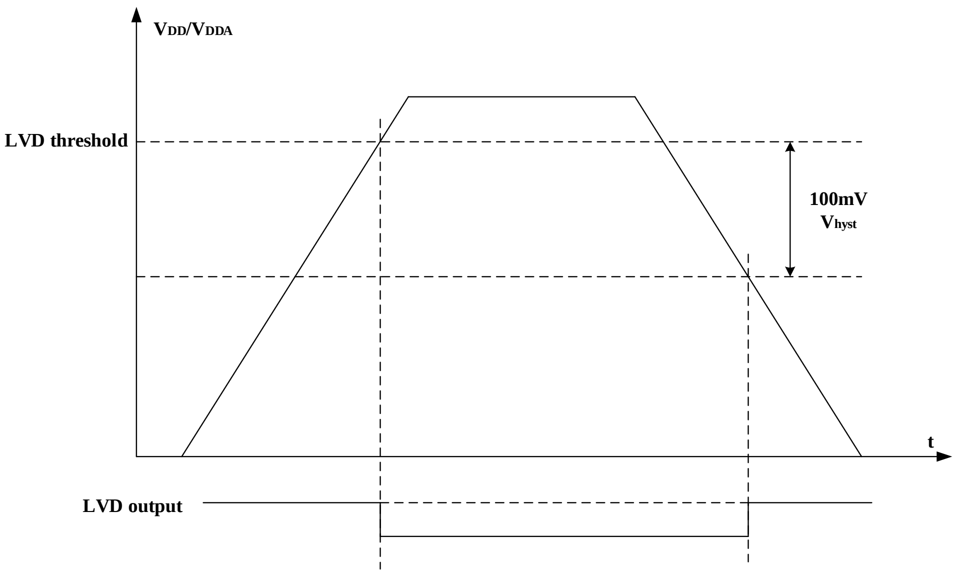
Figure 2-3. Power-on/Power-down Reset Waveforms



The function of the LVD is to detect whether the V_{DD}/V_{DDA} supply voltage is lower than the low-voltage detection threshold (2.2 V ~ 2.9 V), which is configured by the LVDT[2:0] bits in the power control register (PMU_CTL). LVD is enabled by LVDEN setting. The LVDF bit in the power status register (PMU_CS) indicates whether a low voltage event occurs. The event is connected to the 16th line of EXTI. The user can configure the 16th line of EXTI to generate a corresponding interrupt. (LVD interrupt signal depends on the rising or falling edge configuration of EXTI line 16). The value of the hysteresis voltage V_{hyst} is 100mV.

LVD application: When the MCU power supply is subject to external interference, such as a voltage drop, we can set the low voltage detection threshold (the threshold is greater than the PDR value) through LVD. Once it falls to the threshold, the LVD interrupt is turned on, which can be used in the interrupt function. Set operations such as soft reset to avoid other exceptions from the MCU.

Figure 2-4. LVD Threshold Waveform



In addition, the MCU reset source can be judged by querying the register RCU_RSTSCK (0x40021024). This register can only clear the flag bit after a power-on reset. Therefore, during use, after the reset source is obtained, the reset flag can be cleared through the RSTFC control bit. When the watchdog is reset or other reset events, it can be more accurately reflected in the RCU_RSTSCK register.

Figure 2-5. RCU_RSTSCK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LP RSTF	WWDGT RSTF	FWDGT RSTF	SW RSTF	POR RSTF	EP RSTF	Reserved	RSTFC	Reserved							
r	r	r	r	r	r		rw								
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved														IRC40K STB	IRC40KE N

MCU integrates a power-on/power-off reset circuit. When designing an external reset circuit, a capacitor (typical value of 100nF) must be placed on the NRST pin to ensure that the power on the NRST pin generates a low pulse delay of at least 20us for completing effective power-on reset process.

Figure 2-6. System Reset Circuit

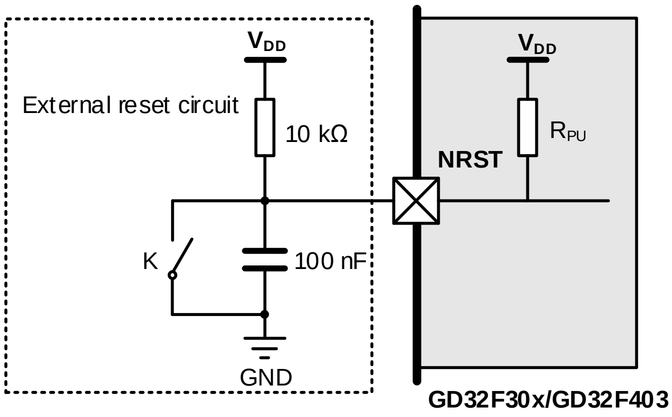
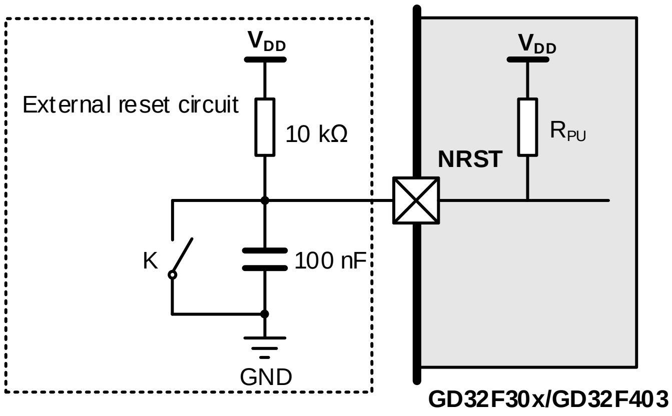


Figure 2-7. Recommend External Reset Circuit



Note:

1. The internal pull-up resistor is 40 kΩ and external pull-up resistor is recommended to be 10kΩ, so that voltage interference will not cause the chip to work abnormally.
2. If the influence of static electricity is considered, an ESD protection diode can be placed at the NRST pin.
3. Although there is a hardware POR circuit inside the MCU, it is still recommended to add an external NRST reset resistor-capacitor circuit.
4. If the MCU starts abnormally (due to voltage fluctuations, etc.), the capacitance value of NRST to ground can be appropriately increased, and the MCU reset completion time can be extended to avoid the abnormal power-on sequence area.

2.2. Clock

GD32F30x/GD32F403 series has a complete clock system inside. You can choose the appropriate clock source according to different applications. The main features of the clock are:

- 4-32MHz external high-speed crystal oscillator (HXTAL)
- 8MHz internal high-speed RC oscillator (IRC8M)
- 32.768KHz external low-speed crystal oscillator (LXTAL)
- 48 MHz internal high-speed RC oscillator (IRC48M)
- 40kHz internal low speed RC oscillator (IRC40K)
- PLL clock source can be selected from HXTAL, IRC8M or IRC48M
- HXTAL clock can be monitored

GD32F30x/GD32F403 series can be divided into GD32F303 series products, GD32F305/GD32F307 series interconnected products and GD32F403 series products. GD32F303 series products do not have USBFS module and Ethernet module. LQFP48 package products do not have SDIO and EXMC modules, LQFP64 package products do not have EXMC modules. The clock tree is shown in ***Figure 2-8. GD32F303xx Clock Tree***. The GD32F305 and GD32F307 microcontrollers are called interconnected products, and both include USBFS modules, and GD32F307 also includes Ethernet modules. LQFP64 package interconnect products do not have EXMC modules, refer to GD32_Series_of_MCUs_Selection_Guide for details. The clock tree of interconnected products is shown in ***Figure 2-9. GD32F305/F307xx Clock Tree***. GD32F403 series products include SDIO, EXMC, USBFS. The LQFP64 package product has no EXMC module, and the clock tree is shown in ***Figure 2-10. GD32F403xx Clock Tree***.

Figure 2-8. GD32F303xx Clock Tree

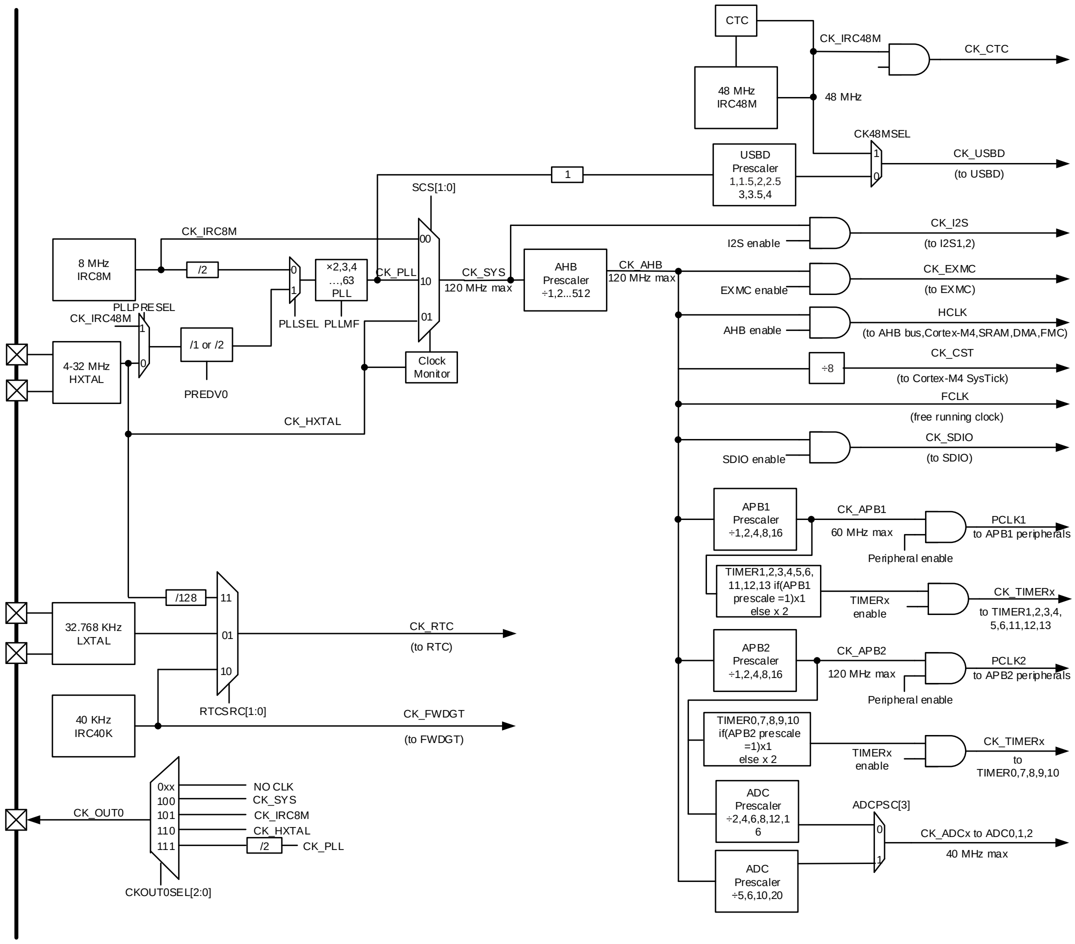


Figure 2-9. GD32F305/F307xx Clock Tree

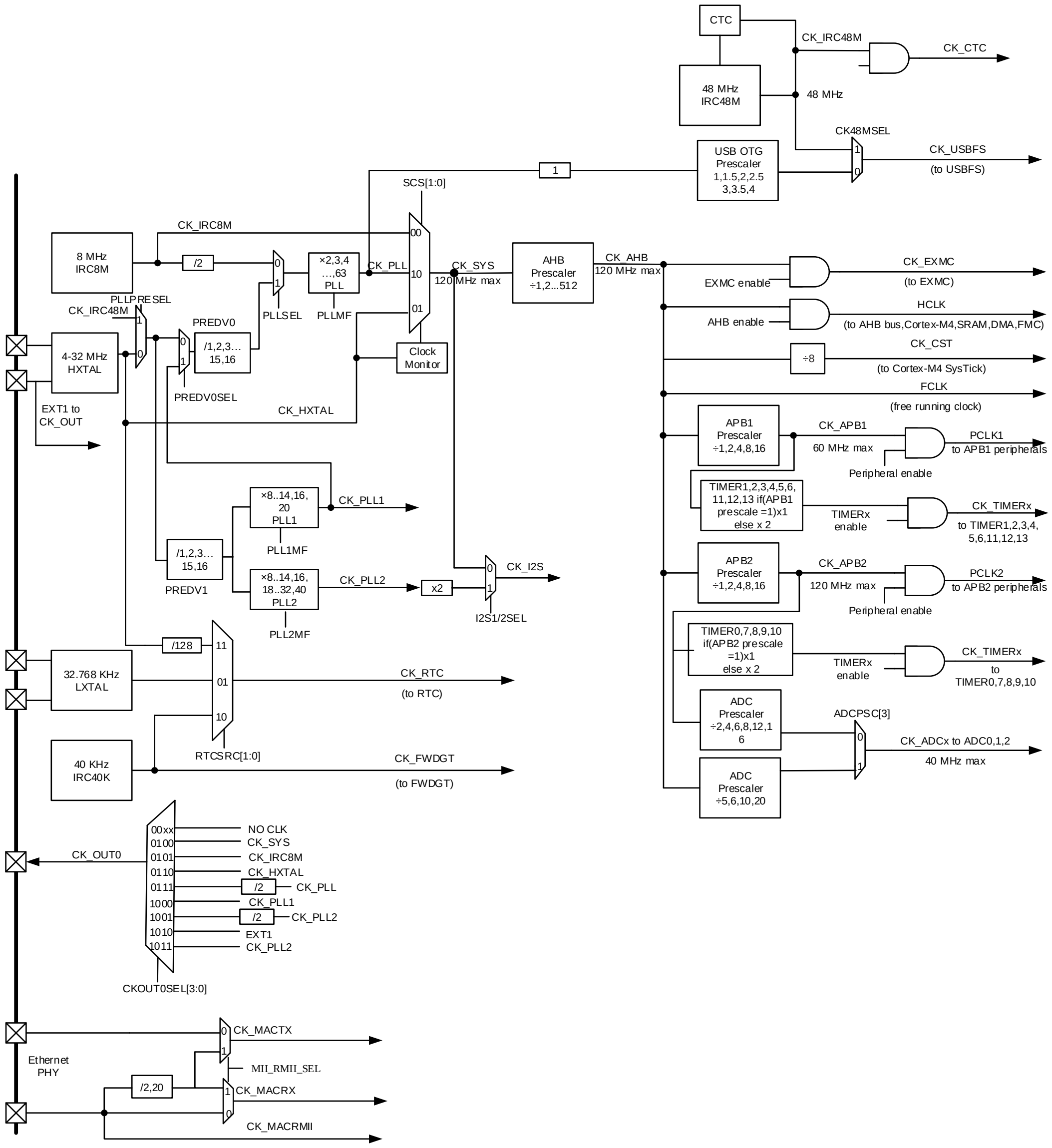
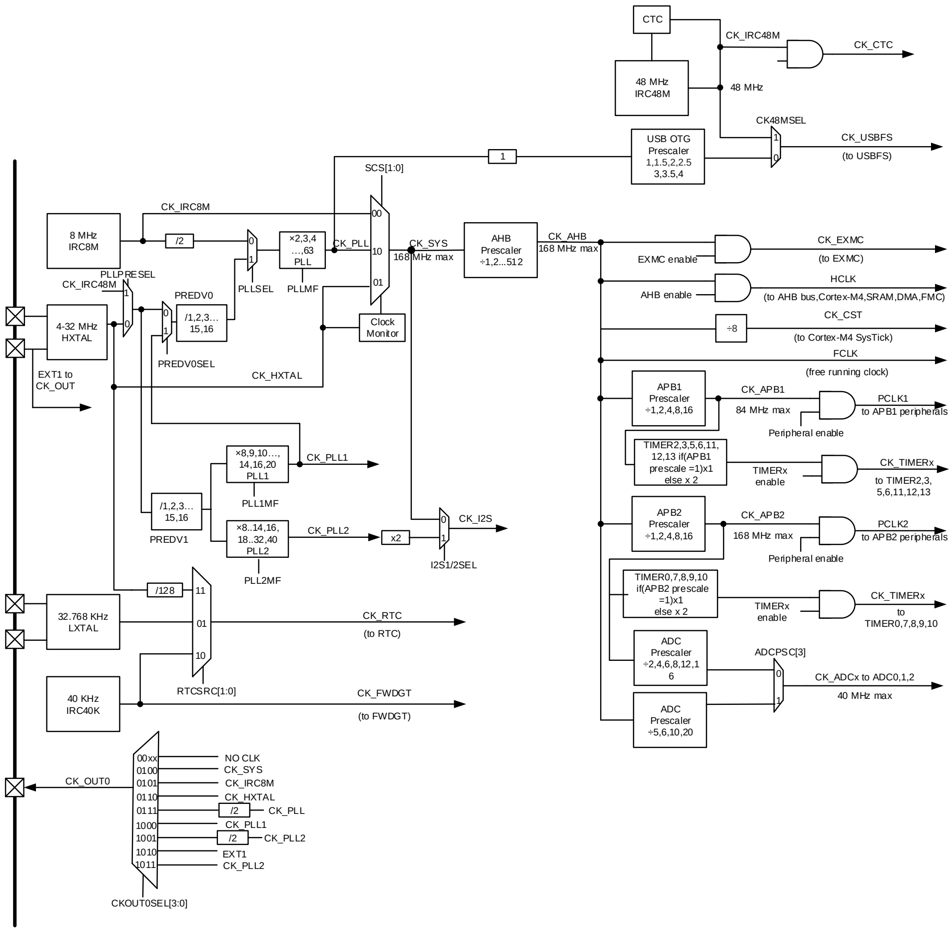


Figure 2-10. GD32F403xx Clock Tree



2.2.1. External high-speed crystal oscillator clock (HXTAL)

4-32MHz external high-speed crystal oscillator (passive crystal) can provide accurate master clock for the system. The crystal for that specific frequency must be placed close to the HXTAL pin, and the external resistors and matching capacitors connected to the crystal must be adjusted according to the chosen oscillator parameters. HXTAL can also use the bypass input mode to input the clock source (1-50MHz active crystal oscillator, etc.). When the bypass input is used, the signal is connected to OSC_IN, and OSC_OUT remains floating. The Bypass function of HXTAL needs to be turned on in software (enable the HXTALBPS bit in RCU_CTL).

Figure 2-11. HXTAL External Crystal Circuit

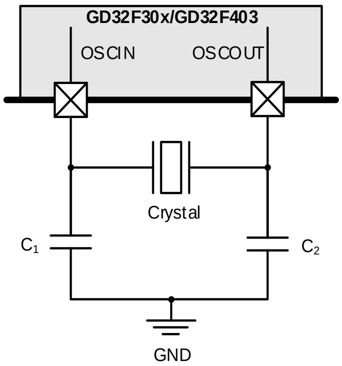
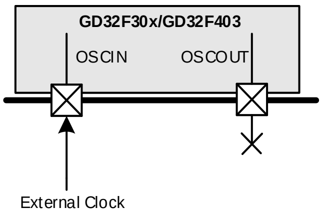


Figure 2-12. HXTAL External Clock Circuit



Note:

1. When using the bypass input, the signal is input from OSC_IN, and OSC_OUT remains floating.
2. For the size of the external matching capacitor, please refer to the formula: $C_1 = C_2 = 2*(C_{LOAD} - C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, with a typical value of 10pF. When it is recommended to use an external high-speed crystal, try to choose a crystal load capacitance of about 20pF, so that the external matching capacitors C_1 and C_2 can be 20pF, and the PCB layout should be as close as possible to the crystal pin.
3. C_S is the parasitic capacitance on the PCB board traces and IC pins. The closer the crystal is to the MCU, the smaller the C_S, and vice versa. Therefore, in practical applications, when the crystal is far away from the MCU and causes the crystal to work abnormally, the external matching capacitor can be appropriately reduced.
4. When using an external high-speed crystal, it is recommended to connect a 1MΩ resistor in parallel at both ends of the crystal to make the crystal easier to vibrate.
5. Accuracy: external active crystal > external passive crystal > internal IRC8M.
6. When the active crystal oscillator is used normally, Bypass will be turned on. At this time, the high level is required to be no less than 0.7 V_{DD}, and the low level is no more than 0.3 V_{DD}. If Bypass is not turned on, the amplitude requirements of the active crystal oscillator will be greatly reduced.

2.2.2. External low-speed crystal oscillator clock (LXTAL)

LXTAL crystal is a 32.768KHz low-speed external crystal (passive crystal), which can provide a low-power and high-precision clock source for RTC. The RTC module of the MCU is equivalent to a counter, and the accuracy will be affected by the crystal performance, matching capacitance and PCB material. If you want to obtain better accuracy, it is recommended to connect PC13 to the timer input capture pin during circuit design. TIMER to calibrate LXTAL, and set the frequency division register of RTC according to the calibration situation. LXTAL can also support bypass clock input (active crystal oscillator, etc.), which can be enabled by configuring the LXTALBPS bit in RCU_BDCTL.

Figure 2-13. LXTAL External Crystal Circuit

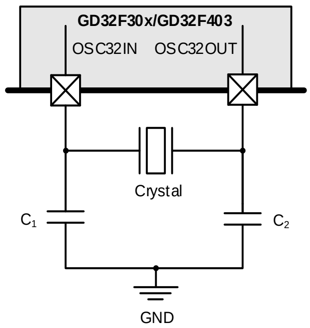
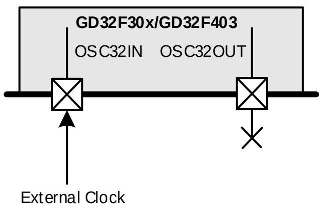


Figure 2-14. LXTAL External Clock Circuit



Note:

1. When using the bypass input, the signal is input from OSC32_IN, and OSC32_OUT remains floating.
2. For the size of the external matching capacitor, please refer to the formula: $C_1 = C_2 = 2*(C_{LOAD} - C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, the empirical value is between 2pF-7pF, and 5pF is recommended as a reference value calculation. When it is recommended to use an external crystal, try to choose a crystal load capacitance of about 10pF, so that the externally connected matching capacitors C_1 and C_2 can be 10pF, and the PCB layout should be as close to the crystal pin as possible.
3. When the RTC selects IRC40K as the clock source and uses the V_{BAT} external independent power supply, if the MCU is powered off at this time, the RTC will stop

counting. After the power is re-energized, the RTC will continue to accumulate the counting value according to the previous count value. If the application needs to use V_{BAT} to power the RTC, the RTC can still time normally, and the RTC must select LXTAL as the clock source.

2.2.3. Clock output capability (CKOUT)

For GD32F303xx series MCU, you can select different clock signal output by configuring the CKOUT0SEL[2:0] bits of the clock register RCU_CFG0, and the corresponding GPIO pin PA8 needs to be configured as a multiplexing function to output the selected signal, as shown in ***Table 2-1. CKOUT0SEL[2:0] Control Bits***.

Table 2-1. CKOUT0SEL[2:0] Control Bits

CKOUT0SEL[2:0]	Clock Source
0xx	NA
100	CK_SYS
101	CK_IRC8M
110	CK_HXTAL
111	CK_PLL/2

For GD32F305xx/GD32F307xx/GD32F403xx series interconnected MCUs, different clock signal outputs can be selected by configuring the CKOUT0SEL[3:0] bits of the clock register RCU_CFG0, and the corresponding GPIO pin PA8 needs to be configured as a multiplexing function to output the selected signal, as shown in ***Table 2-2. CKOUT0SEL[3:0] Control Bits***.

Table 2-2. CKOUT0SEL[3:0] Control Bits

CKOUT0SEL[3:0]	Clock Source
00xx	NA
0100	CK_SYS
0101	CK_IRC8M
0110	CK_HXTAL
0111	CK_PLL/2
1000	CK_PLL1
1001	CK_PLL2/2
1010	EXT1
1011	CK_PLL2

2.2.4. HXTAL Clock monitor (CKM)

Set the HXTAL clock monitoring enable bit CKMEN in the clock control register RCU_CTL, HXTAL can enable the clock monitoring function. This function needs to be enabled after HXTAL start-up delay and disabled after HXTAL is stopped. Once the HXTAL fails, the HXTAL will be automatically disabled, the HXTAL clock blocking flag CKMIF in the clock interrupt register RCU_INT is set, and the HXTAL fault event is generated. The interrupt caused by this fault is connected to the non-maskable interrupt NMI of the Cortex-M4.

Note: If HXTAL is selected as the system clock, PLL or RTC clock source, HXTAL failure will prompt the selection of IRC8M as the system clock source, the PLL will be automatically disabled, and the RTC clock source needs to be reconfigured.

2.3. Startup Configuration

GD32F30x/GD32F403 series provides three boot modes, which can be selected by the BOOT0 bit and the BOOT1 pin to determine the boot option. When designing the circuit, run the user program, the BOOT0 pin cannot be left floating, it is recommended to connect a 10kΩ resistor to GND; when running the System Memory to update the program, you need to connect the BOOT0 pin to high and the BOOT1 pin to low. After the update is completed, the user program can be run after the BOOT0 is connected to a low level; the SRAM execution program is mostly used in the debugging status.

The embedded Bootloader is stored in the system storage space for reprogramming the FLASH memory. In GD32F305xx/GD32F307xx/GD32F403xx devices, the Bootloader can interact with the outside world through USART0 (PA9 and PA10), USART1 (PD5 and PD6), USBFS (PA9, PA11 and PA12). In the GD32F303 (Flash<512kB) device, the Bootloader can interact with the outside world through USART0 (PA9 and PA10), and in the GD32F303 (Flash>512kB) device, the Bootloader can communicate with the outside world through USART0 (PA9 and PA10) USART1 (PA2 and PA3) interact. The details are shown in ***Table 2-3. Bootloader Interactive Interface***.

Table 2-3. Bootloader Interactive Interface

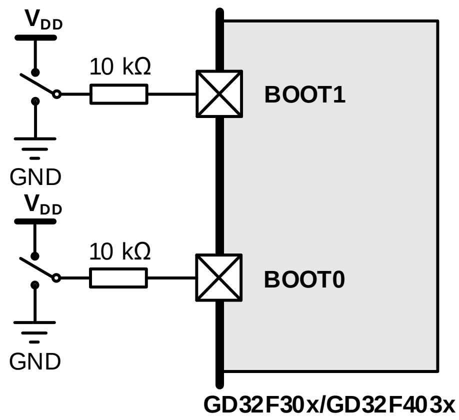
MCU Part Numbers	Bootloader Interactive Interface
GD32F305xx /GD32F307xx/GD32F403xx	USART0 (PA9 and PA10)，USART1 (PD5 and PD6)，USBFS (PA9, PA11 and PA12)
GD32F303xx（Flash<512kB）	USART0 (PA9 and PA10)
GD32F303xx（Flash>512kB）	USART0 (PA9 and PA10) USART1 (PA2 and PA3)

It should be noted that some MCU series have several interfaces of Bootloader(like USART and USB). So if we want to enter ISP mode of a specific USART, we need to make sure the potential of PA11 and PA11 is fixed and not be low at the same time. Also ensuring that the potential of RX pin of other USART interfaces of the Bootloader are fixed.

Table 2-4. BOOT Mode

BOOT Mode	BOOT1	BOOT0
Main Flash Memory	X	0
System Memory	0	1
On Chip SRAM	1	1

Figure 2-15. Recommend BOOT Circuit Design



Note:

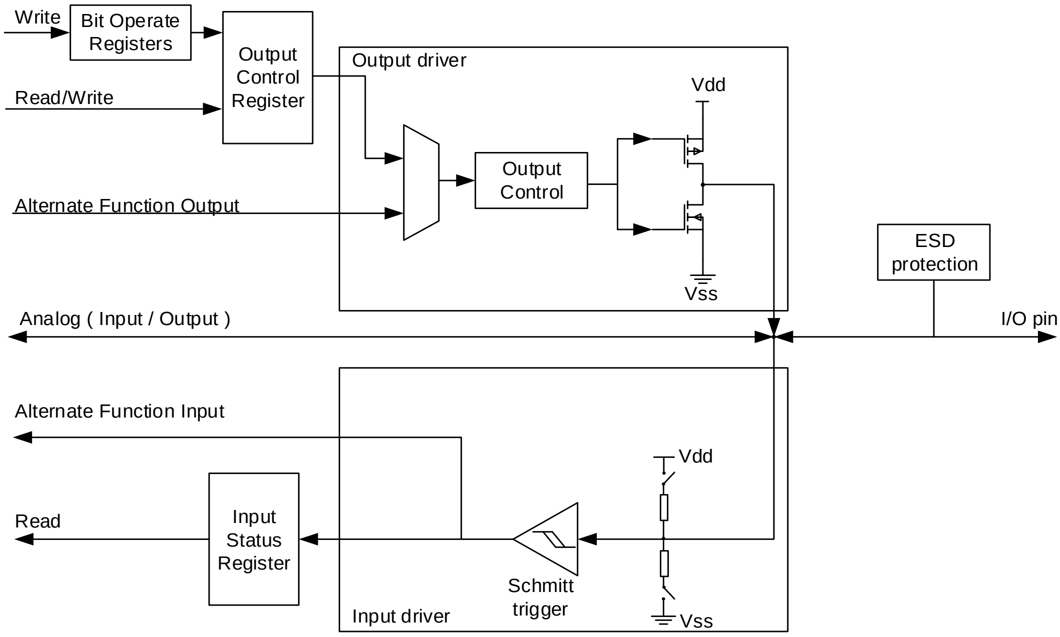
1. After the MCU is running, if the BOOT status is changed, it will take effect after the system is reset.
2. Once the BOOT1 pin state is sampled, it can be released for other purposes.

2.4. Typical Peripheral Modules

2.4.1. GPIO Circuit

The largest package GPIO interface includes 7 groups of general-purpose input/output ports, each group of ports provides up to 16 general-purpose input/output pins, which are PA0 ~ PA15, PB0 ~ PB15, PC0 ~ PC15, PD0 ~ PD15, PE0 ~ PE15, PF0 ~ PF15 and PG0 ~ PG15, each pin can be independently configured through registers, the basic structure of GPIO port is shown in *Figure 2-16. Basic Structure of Standard IO*.

Figure 2-16. Basic Structure of Standard IO



Note:

1. The IO port is divided into 5V tolerance and non-5V tolerance. When using, pay attention to distinguish the voltage tolerance of the IO port, see Datasheet for details.
2. When the 5V-tolerant IO port is directly connected to 5V, it is recommended that the IO port be configured in open-drain mode and externally pull up to work.
3. After the IO port is powered on and reset, the default mode is floating input, and the level characteristics are uncertain. In order to obtain more consistent power consumption, it is recommended that all IO ports be configured as analog inputs and then modified to the corresponding mode according to application requirements (chip Ports that are not exported internally also need to be configured).
4. To improve EMC performance, it is recommended to pull up or pull down the unused IO pins by hardware.
5. The drive capability of the three IO ports PC13, PC14, and PC15 is weak, and the output current capability is limited (about 3mA). When configured in output mode, the operating speed cannot exceed 2MHz (the maximum load is 30pF).
6. The same label PIN in multiple groups can only configure one port as an external interrupt. For example, PA0, PB0, and PC0 only support one of the three IO ports to generate external interrupts, and do not support three external interrupt modes.
7. For 5VT IO, it may introduce sink current when the voltage of the IO is beyong V_{DD}.

2.4.2. USART Circuit

Universal Synchronous Asynchronous Receiver Transmitter (USART) provides a flexible and convenient serial data exchange interface, and data frames can be transmitted in full-duplex or half-duplex, synchronous or asynchronous mode. The USART provides a programmable baud rate generator that divides the system clock to generate the specific frequency required for USART transmission and reception.

USART not only supports the standard asynchronous transceiver mode, but also implements some other types of serial data exchange modes, such as infrared coding specification, SIR, smart card protocol, LIN, and synchronous single-duplex mode. It also supports multiprocessor communication and Modem flow control operation (CTS/RTS). Data frames support transmission from the LSB or MSB. Both the polarity of the data bits and the TX/RX pins can be flexibly configured.

USART supports DMA function to realize high-speed data communication.

Table 2-5. USART Important Pin Description

Pin	Type	Description
RX	Input	Receive data
TX	Output I/O (Single-Wire Mode/Smart Card Mode)	Send data, when USART is enabled, if no data is sent, the default is high level.
CK	Output	Serial clock signal for synchronous communication
nCTS	Input	Hardware flow control mode send enable signal
nRTS	Output	Hardware flow control mode send request signal

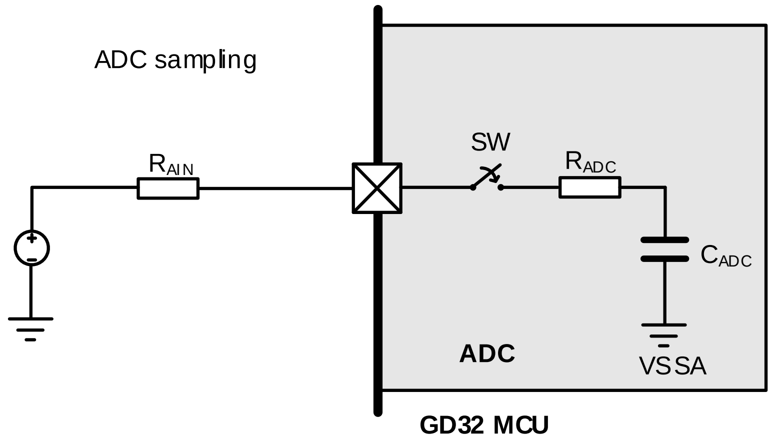
2.4.3. ADC Circuit

The GD32F30x/GD32F403 series integrates a 12-bit SAR ADC, which has up to 18 channels and can measure 16 external and 2 internal signal sources. The internal signal is the temperature sensor channel (ADC0_CH16) and the internal reference voltage input channel (ADC0_CH17). The temperature sensor reflects the change in temperature and is not suitable for measuring absolute temperature. If accurate temperature measurement is required, an external temperature sensor must be used. The internal reference voltage V_{REFINT} provides a regulated voltage output (1.2V) to the ADC and is internally connected to ADC0_IN17.

If the ADC collects the external input voltage during use, if the sampled data fluctuates greatly, it may be due to the interference caused by power supply fluctuations. You can calibrate by sampling the internal V_{REFINT} and then calculate the externally sampled voltage.

When designing the ADC circuit, it is recommended to place a small capacitor at the ADC input pin. It is recommended to place a small capacitor of 500pF.

Figure 2-17. ADC Acquisition Circuit Design



When f_{ADC} = 40MHz, the relationship between Input impedance and Sampling period is shown in ***Table 2-6. fADC=40MHz Relationship between Sampling period and External input impedance***. In order to obtain better conversion results, it is recommended to reduce the frequency of f_{ADC} as much as possible during use, select a larger value for the sampling period, and minimize the input impedance when designing the external circuit. If necessary, use the op amp to follow to reduce the input impedance.

Table 2-6. fADC=40MHz Relationship between Sampling period and External input impedance

T_s (cycles)	t_s (μs)	$R_{AIN\ max}$ (kΩ)
1.5	0.0375	0.15
7.5	0.1875	2.96
13.5	0.3375	5.77
28.5	0.7125	12.8
41.5	1.0375	18.9
55.5	1.3875	25.4
71.5	1.7875	32.9
239.5	5.9875	N/A

2.4.4. DAC Circuit

The digital/analog converter of GD32F30x/GD32F403 can convert 12-bit digital data to voltage output on external pins. Data can be in 8-bit or 12-bit mode, left-justified or right-justified. When external triggering is enabled, DMA can be used to update digital data on the input. At the output voltage, the DAC output buffer can be used to obtain higher drive capability. The two DACs can work independently or concurrently.

Table 2-7. DAC Related Pin Description

Name	Description	Signal type
V_{DDA}	Analog power	Input, Analog power
V_{SSA}	Analog power ground	Input, Analog power ground
V_{REF+}	DAC positive reference voltage	Input, Analog positive

Name	Description	Signal type
	2.6V ≤ V_{REF+} ≤ V_{DDA}	reference voltage
DAC_OUTx	DACx analog output	Analog output signal

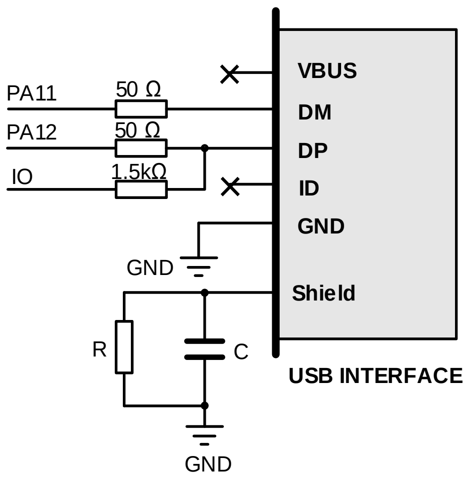
Before enabling the DAC module, the GPIO port (PA4 corresponds to DAC0, PA5 corresponds to DAC1) should be configured in analog mode.

2.4.5. USB Circuit

The GD32F305/GD32F307xx interconnected MCU has a built-in USB interface, which is a USBFS module. The USB protocol requires a clock accuracy of not less than 500ppm, and the internal clock may not be able to achieve such accuracy, so it is recommended to use an external crystal or an active crystal oscillator as the USB module clock source when using the USB function.

GD32F303x can only be designed as a USB device. When designing the circuit, a controllable 1.5K pull-up resistor needs to be designed for the DP data line. The recommended USB-Device reference circuit is shown in ***Figure 2-18. Recommend USB-Device Reference Circuit***. In order to improve the ESD performance of USB, it is recommended to design a resistance-capacitance discharge isolation circuit for the USB case.

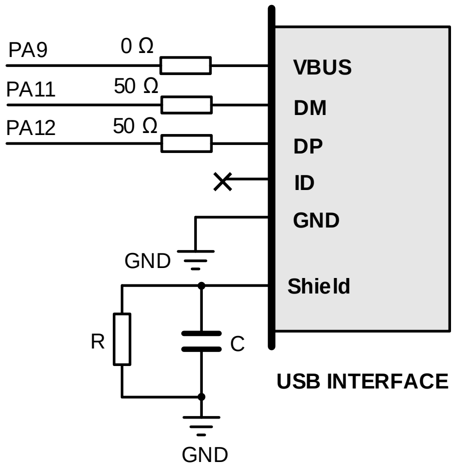
Figure 2-18. Recommend USB-Device Reference Circuit



Recommendation: R = 1MΩ, C = 4700pF

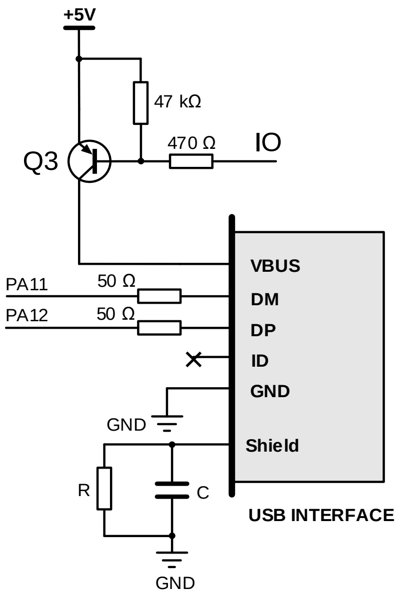
The USB module of GD32F305xx/GD32F307xx interconnected MCU/GD32F403xx can be designed as both USB device and USB host. The recommended circuit when designed as Device is shown in ***Figure 2-19. Recommend USB-Device (USBFS) Reference Circuit***; when designed as Device, if PA9 is connected to VBUS, the DP line does not need an external 1.5K pull-up resistor; if PA9 is not connected To VBUS, if the VBUSIG control bit in the USBFS_GCCFG register has been configured, the USB_DP data line can not be connected with a 1.5K pull-up resistor. If this register is not configured, the USB_DP data line needs to be connected with a 1.5K pull-up resistor. In order to improve the ESD performance of USB, it is recommended to design a resistance-capacitance discharge isolation circuit for the USB case. When designing in host mode, the recommended circuit is shown in ***Figure 2-20. Recommend USB-Host Reference Circuit***.

Figure 2-19. Recommend USB-Device (USBFS) Reference Circuit



Recommendation: R = 1MΩ, C = 4700pF

Figure 2-20. Recommend USB-Host Reference Circuit

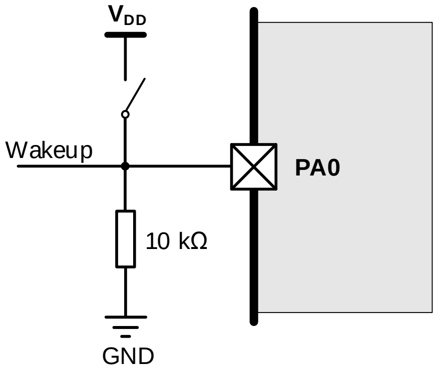


Recommendation: R = 1MΩ, C = 4700pF

2.4.6. Standby mode wake-up circuit

The GD32F30x/GD32F403 series supports three low-power modes, namely sleep mode, deep-sleep mode and standby mode. The standby mode with the lowest power consumption is the standby mode, which requires the longest wake-up time. Wake-up from Standby mode can be woken up by the rising edge of the WKUP pin. At this time, there is no need to configure the corresponding GPIO, just configure the WUPEN bit in the PMU_CS register. The WKUP wake-up pin reference circuit is designed as follows:

Figure 2-21. Recommend Standby External Wake-up Pin Circuit Design



Note: In this mode, attention should be paid to the circuit design. If there is a series resistance between PA0 and VDD, additional power consumption may be added.

2.5. Download the debug circuit

GD32F30x/GD32F403 series cores support JTAG debug interface and SWD interface. The JTAG interface standard is a 20-pin interface, including 5 signal interfaces, and the SWD interface standard is a 5-pin interface, including 2 signal interfaces.

Note: After reset, the debug related ports are in input PU/PD mode, where:
PA15: JTDI is in pull-up mode.
PA14: JTCK/SWCLK in pull-down mode.
PA13: JTMS/SWDIO in pull-up mode.
PB4: NJTRST is in pull-up mode.
PB3: JTDO is floating mode.

Table 2-8. JTAG Download Debug Interface Assignment

Alternate function	GPIO Port
JTMS	PA13
JTCK	PA14
JTDI	PA15
JTDO	PB3
NJTRST	PB4

Figure 2-22. Recommend JTAG Wiring Reference Design

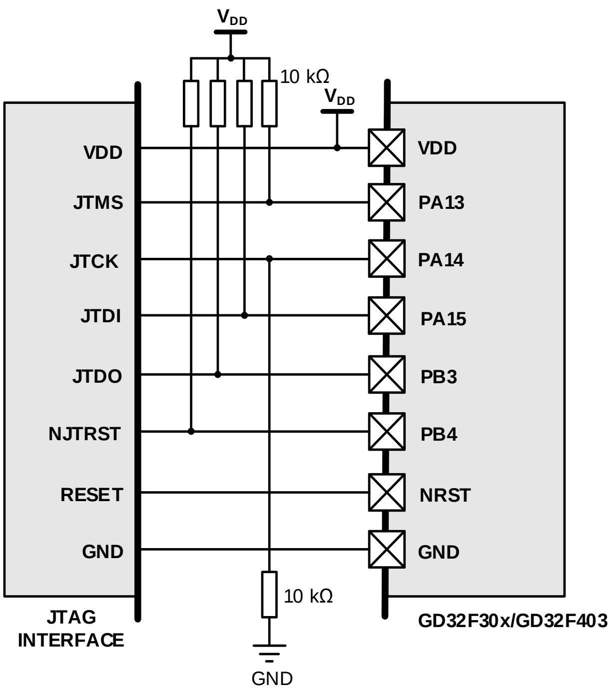
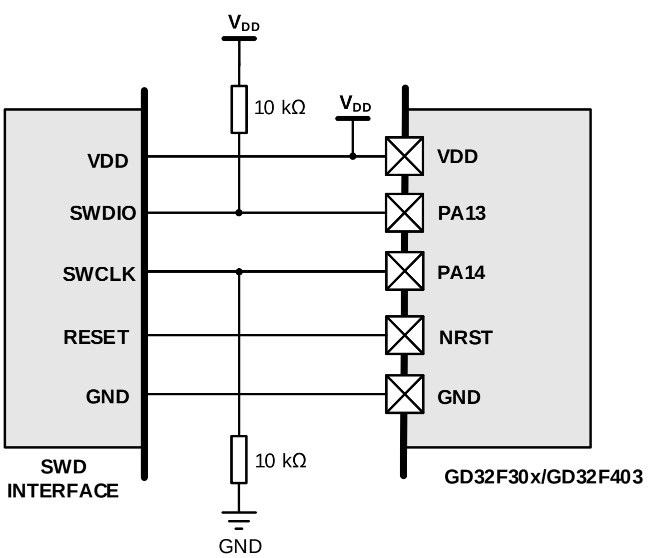


Table 2-9. SWD Download Debug Interface Assignment

Alternate function	GPIO Port
SWDIO	PA13
SWCLK	PA14

Figure 2-23. Recommend SWD Wiring Reference Design



There are several ways to improve the reliability of SWD download and debugging communication and enhance the anti-interference ability of download and debugging.

（1） Shorten the length of the two SWD signal lines, preferably within 15cm.

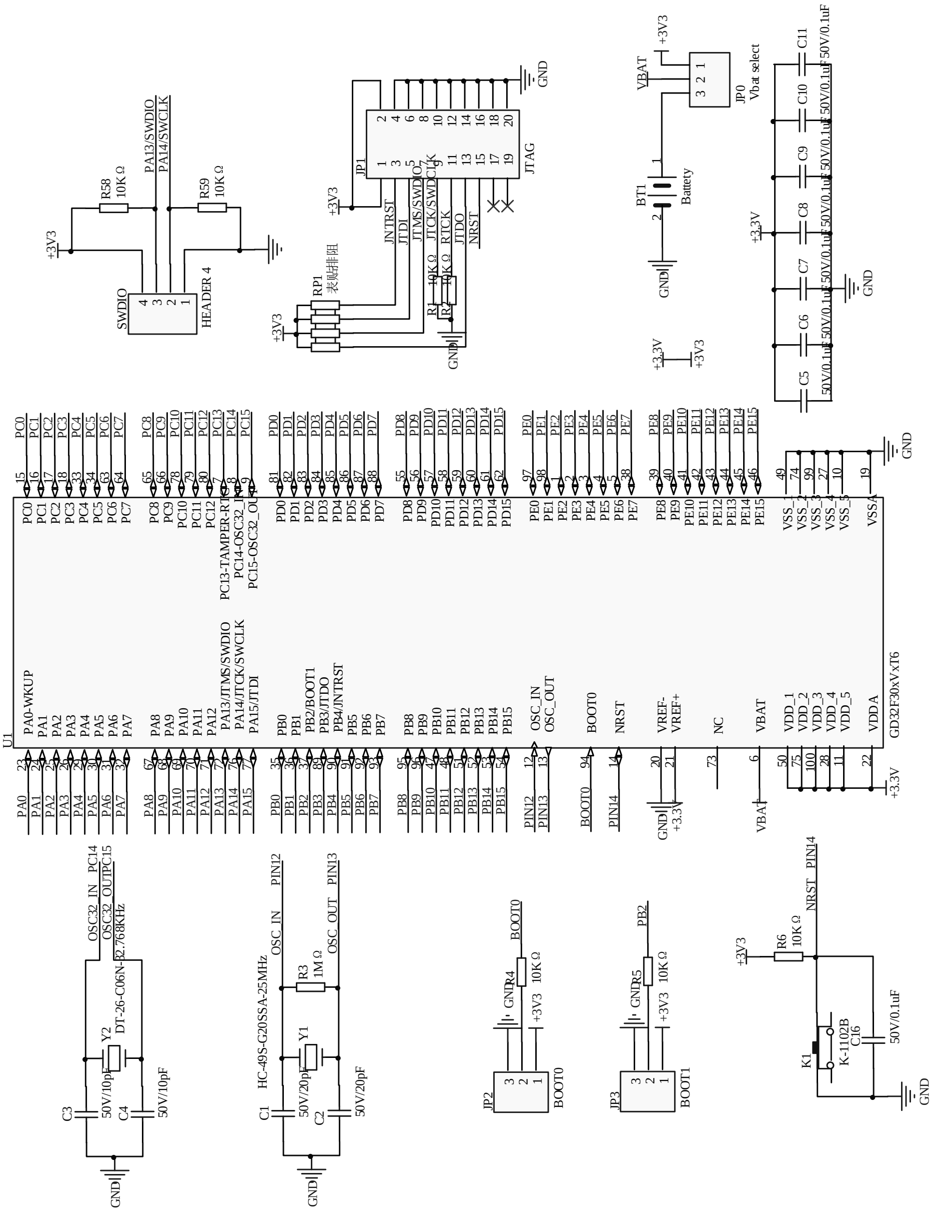
（2） Weave the two SWD wires and the GND wire into a twist and twist them together.

（3） Connect separately tens of pF small capacitors in parallel between the two signal lines of the SWD and the ground.

（4） Any IO of the two signal lines of SWD is connected in series with a 100Ω~1KΩ resistor.

2.6. Reference Schematic Design

Figure 2-24. GD32F30x/GD32F403 Recommend Reference Schematic Design



3. PCB Layout Design

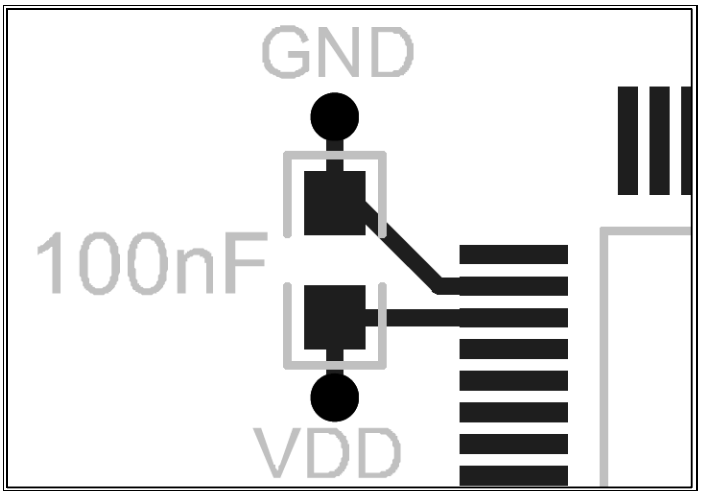
In order to enhance the functional stability and EMC performance of the MCU, it is not only necessary to consider the performance of the supporting peripheral components, but also the PCB Layout. In addition, when conditions permit, try to choose a PCB design scheme with an independent GND layer and an independent power supply layer, which can provide better EMC performance. If conditions do not allow, independent GND layer and power supply layer cannot be provided, then it is also necessary to ensure a good power supply and grounding design, such as making the GND plane under the MCU as complete as possible.

In applications with high power or strong interference, it is necessary to consider keeping the MCU away from these strong interference sources.

3.1. Power Supply Decoupling Capacitors

The GD32F30x/GD32F403 series power supply has three power supply pins: V_{DD}, V_{DDA} and V_{BAT}. The 100nF decoupling capacitor can be made of ceramic, and it is necessary to ensure that the position is as close to the power supply pin as possible. The power trace should try to make it pass through the capacitor first and then reach the MCU power pin, It is recommended to punch holes near the capacitor pad to connect with GND.

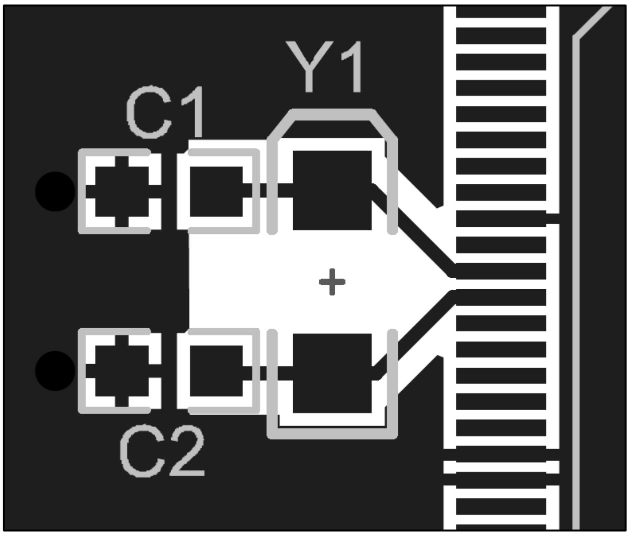
Figure 3-1. Recommend Power Pin Decoupling Layout Design



3.2. Clock Circuit

GD32F30x/GD32F403 series clocks have HXTAL and LXTAL, and the clock circuit (including crystal or crystal oscillator and capacitor, etc.) is required to be placed close to the MCU clock pin, and the clock trace should be wrapped by GND as much as possible.

Figure 3-2. Recommend Clock Pin Layout Design (passive crystal)



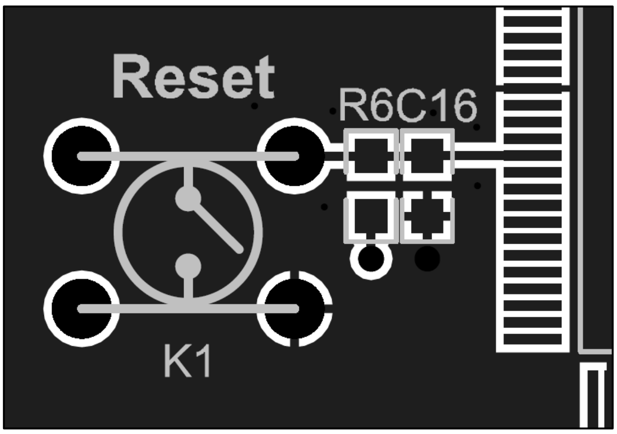
Note:

1. The crystal should be as close to the MCU clock pin as possible, and the matching capacitor should be as close as possible to the crystal.
2. The whole circuit should be on the same layer as the MCU, and the wiring should not go through the layer as much as possible.
3. The PCB area of the clock circuit should be kept as empty as possible, and no traces unrelated to the clock should be taken.
4. High-power, high-interference risk devices and high-speed wiring should be kept away from the clock crystal circuit as far as possible.
5. The clock line is grounded to achieve a shielding effect.

3.3. Reset Circuit

NRST trace PCB Layout reference is as follows:

Figure 3-3. Recommend NRST Trace Layout Design



Note: The resistance and capacitance of the reset circuit should be as close as possible to the NRST pin of the MCU, and the NRST trace should be kept away from devices with strong interference risk and high-speed traces as far as possible. If conditions permit, it had better to wrap the NRST traces for better shielding effect.

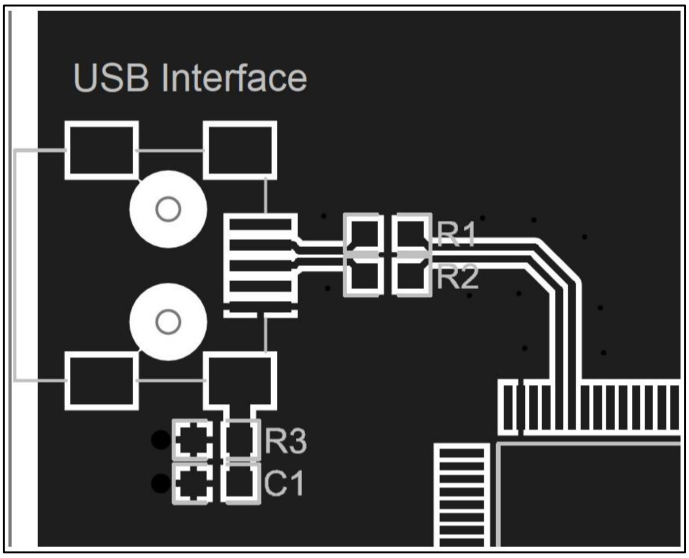
3.4. USB Circuit

The USB module has two differential signal lines, DM and DP. It is recommended that the PCB traces require a characteristic impedance of 90ohm. The differential traces should be run in strict accordance with the rule of equal length and equal distance, and the traces should be kept as short as possible. If the two differential lines are not equal in length , the short line can be compensated with a serpentine line at the terminal.

Due to impedance matching considerations, the series matching resistance is recommended to be about 50Ω. When the USB terminal interface is far away from the MCU, the series resistance value needs to be appropriately increased.

The USB differential trace reference is as follows:

Figure 3-4. Recommend USB Differential Trace Layout Design



Recommendation: R1 = R2 = 50Ω, R3 = 1MΩ, C = 4700pF

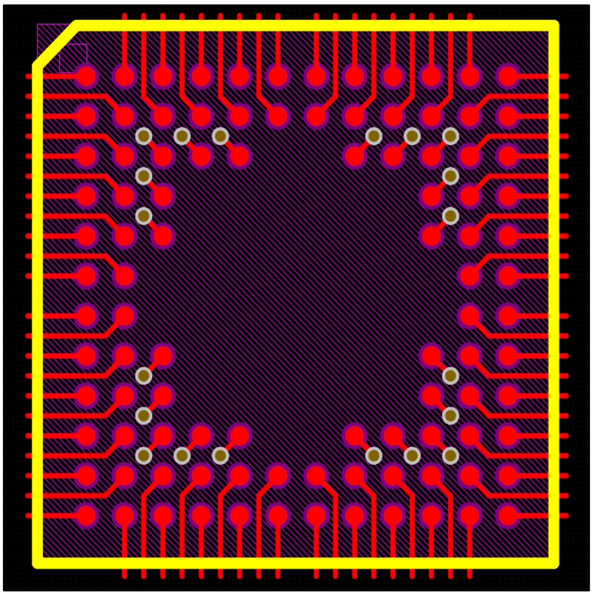
Note:

1. Reasonable placement during layout to shorten the differential trace distance.
2. Draw differential lines first, try not to exceed two pairs of vias for a pair of differential lines, and place them symmetrically.
3. Symmetrical parallel wiring to ensure that the two lines are tightly coupled, avoiding 90°, arc or 45° wiring.
4. Devices such as resistance-capacitor, EMC connected to the differential traces, or test points should also be symmetrical.

3.5. BGA Trace

The GD32F403 series includes the BGA100 package, and the corresponding model is GD32F403VxH6. The wiring of this chip is similar to other BGA chips, and each ball pad is fanned out first, and then the wiring operation is performed. For the BGA package with 0.5 mm pitch, if the BGA pad size is set to 0.25/0.35, and the distance between the vias and the pad and the line width and line spacing is 3 mil, the dog bone type fan-out can be used, and the fan-out is shown in ***Figure 3-5. Fan-Out Method of BGA100 Package***. The distance between the via and the pad is 4.5mil; however, this kind of wiring has high requirements on the PCB manufacturer's process, so it is necessary to communicate with the PCB manufacturer before wiring. To the requirements, the BGA package can be punched through holes and blind buried holes.

Figure 3-5. Fan-Out Method of BGA100 Package



4. Package Description

The GD32F30x/GD32F403 series has a total of 5 package types, namely LQFP48, LQFP64, LQFP100, BGA100, and LQFP144.

Table 4-1. Package Description

Ordering code	Package
GD32F303CxT6	LQFP48(7x7, 0.5 pitch)
GD32F30xRxT6/GD32F403RxT6	LQFP64(10x10, 0.5 pitch)
GD32F30xVxT6/GD32F403VxT6	LQFP100(14x14, 0.5 pitch)
GD32F30xZxT6/GD32F403ZxT6	LQFP144(20x20, 0.5pitch)
GD32F403VxH6	BGA100(7x7, 0.5pitch)

(Original dimensions are in millimeters)

5. Revision history

Table 5-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Apr.20 2022
1.1	Add some notes of bootloader and some minor updates	Dec.14.2022

Important Notice