GigaDevice Semiconductor Inc.

Arm® Cortex®- M3/M4/M23/M33 32-bit MCU

Application Note
AN035
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**1. Introduction**

The GD32F10x devices provide three kinds of boot sources which can be selected by the BOOT0 and BOOT1 pins. The details are shown in Table 1-1. Boot modes. The value on the two pins is latched on the 4th rising edge of CK_SYS after a reset. It is up to the user to set the BOOT0 and BOOT1 pins after a power-on reset or a system reset to select the required boot source. Once the two pins have been sampled, they are free and can be used for other purposes.

<table>
<thead>
<tr>
<th>Selected boot source</th>
<th>Boot mode selection pins</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Boot1</td>
</tr>
<tr>
<td>Main Flash Memory</td>
<td>x</td>
</tr>
<tr>
<td>Boot loader</td>
<td>0</td>
</tr>
<tr>
<td>On-chip SRAM</td>
<td>1</td>
</tr>
</tbody>
</table>

**Note:** When the boot source is hoped to be set as “Main Flash Memory”, the Boot0 pin has to be connected with GND definitely and can not be floating.

After power-on sequence or a system reset, the Arm® Cortex®-M3/M4/M23/M33 processor fetches the top-of-stack value from address 0x0000 0000 and the base address of boot code from 0x0000 0004 in sequence. Then, it starts executing code from the base address of boot code.

Due to the selected boot source, either the main flash memory (original memory space beginning at 0x0800 0000) or the system memory (original memory space beginning at 0x1FFF F000) is aliased in the boot memory space which begins at the address 0x0000 0000. When the on-chip SRAM whose memory space is beginning at 0x2000 0000 is selected as the boot source, in the application initialization code, you have to relocate the vector table in SRAM using the NVIC exception table and offset register.

The embedded boot loader is located in the System memory, which is used to reprogram the Flash memory.
2. **Boot from SRAM**

2.1. **Hardware configuration**

When boot from SRAM, the level of BOOT0 and BOOT1 must be configured as high, as is shown in Table 1-1. *Boot modes*. When designing the circuit, a jumper cap is usually used to switch the high and low levels of boot pins, as is shown in *Figure 2-1. Schematic of BOOT pins*.

![Figure 2-1. Schematic of BOOT pins](image)

2.2. **Configuration steps in Keil**

1. Configure IROM1 and IRAM1 as SRAM address in “Option for Target -> Target”, as is shown in *Figure 2-2. Configuration of IROM1 and IRAM1 address*.

![Figure 2-2. Configuration of IROM1 and IRAM1 address](image)

2. Use the NVIC exception table and offset register to reallocate the vector table to SRAM. Add the global macro “VECT_TAB_SRAM” to “Option for Target -> c/c++ -> Define”, as is shown in *Figure 2-3. Add the global macro “VECT_TAB_SRAM”*. 

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AN035
Boot from SRAM
Add the code related to the macro "VECT_TAB_SRAM" in the SystemInit() function, as is shown in Table 2-1. Add the code related to the macro "VECT_TAB_SRAM".

Table 2-1. Add the code related to the macro "VECT_TAB_SRAM"

```c
/*! 
  \brief setup the microcontroller system, initialize the system 
  \param[in] none 
  \param[out] none 
  \retval none */

void SystemInit(void)
{
  /* reset the RCU clock configuration to the default reset state */
  /* enable IRC8M */
  RCU_CTL |= RCU_CTL_IRC8MEN;
  /* reset SCS, AHBPSC, APB1PSC, APB2PSC, ADCPSC, CKOUT0SEL bits */
  RCU_CFG0 &= ~((RCU_CFG0_SCS | RCU_CFG0_AHBPSC | RCU_CFG0_APB1PSC | RCU_CFG0_APB2PSC | RCU_CFG0_ADCPSC | RCU_CFG0_ADCPSC_2 | RCU_CFG0_CKOUT0SEL);
  /* reset HXTALEN, CKMEN, PLLLEN bits */
  RCU_CTL &= ~(RCU_CTL_HXTALEN | RCU_CTL_CKMEN | RCU_CTL_PLLLEN);
  /* Reset HXTALBPS bit */
  RCU_CTL &= ~(RCU_CTL_HXTALBPS);
  /* reset PLLSEL, PREDV0_LSB, PLLMF, USBFSPSC bits */
  #ifdef GD32F10X_CL
  RCU_CFG0 &= ~((RCU_CFG0_PLLSEL | RCU_CFG0_PREDV0_LSB | RCU_CFG0_PLLMF | RCU_CFG0_USBFSPSC | RCU_CFG0_PLLMF_4);
```
RCU_CFG1 = 0x00000000U;
#else
    RCU_CFG0 &= ~(RCU_CFG0_PLLSEL | RCU_CFG0_PREDV0 | RCU_CFG0_PLLMF | RCU_CFG0_USBDPSC | RCU_CFG0_PLLMF_4);
#endif /* GD32F10X_CL */

#if (defined(GD32F10X_MD) || defined(GD32F10X_HD) || defined(GD32F10X_XD))
    /* reset HXTALEN, CKMEN and PLLEN bits */
    RCU_CTL &= ~(RCU_CTL_PLLEN | RCU_CTL_CKMEN | RCU_CTL_HXTALEN);
    /* disable all interrupts */
    RCU_INT = 0x009F0000U;
#else defined(GD32F10X_CL)
    /* Reset HXTALEN, CKMEN, PLLEN, PLL1EN and PLL2EN bits */
    RCU_CTL &= ~(RCU_CTL_PLLEN | RCU_CTL_PLL1EN | RCU_CTL_PLL2EN | RCU_CTL_CKMEN | RCU_CTL_HXTALEN);
    /* disable all interrupts */
    RCU_INT = 0x00FF0000U;
#endif

/* Configure the System clock source, PLL Multiplier, AHB/APBx prescalers and Flash settings */
system_clock_config();
#ifndef VECT_TAB_SRAM
    nvic_vector_table_set(NVIC_VECTTAB_RAM,VECT_TAB_OFFSET);
#else
    nvic_vector_table_set(NVIC_VECTTAB_FLASH,VECT_TAB_OFFSET);
#endif

3. Configure the erase mode as “Do not Erase” in “Option for Target -> Debug -> Setting -> Flash Download”, as is shown in Figure 2-4. Select the erase mode.
4. Configure the algorithm address as SRAM address in “Option for Target -> Debug -> Setting -> Flash Download”, as is shown in Figure 2-5. Configure the algorithm address.

Figure 2-5. Configure the algorithm address

5. Before Reset_Handler in the startup file (such as startup_gd32f10x_cl.s), use SPACE to apply for a section of empty memory, as is shown in Figure 2-6. Use SPACE to apply empty memory. So as to locate the Reset_Handler at address 0x20001E0, as is shown in Figure 2-7. Realocate the address of Reset_Handler.
Figure 2-6. Use SPACE to apply empty memory

```assembly
Skip_Mem
SPACE 0x7C
__Vectors_End
__Vectors_Size EQU __Vectors_End - __Vectors
AREA |.text|, CODE, READONLY

; /* reset_Handler */
Reset_Handler PROC
EXPORT Reset_Handler [WEAK]
IMPORT __main
IMPORT SystemInit
LDR R0, =SystemInit
BLX R0
LDR R0, =__main
BX R0
ENDE
```

Figure 2-7. Realocate the address of Reset_Handler

```
__rt_final_cpp 0x200001dd Thumb Code 0
__rt_final_exit 0x200001dd Thumb Code 0
Reset_Handler 0x200001e1 Thumb Code 8
```

```
ADC1_IRQHandler 0x200001f2 Thumb Code 0
CANG_TX_IRQHandler 0x200001f6 Thumb Code 0
CANG_RX1_IRQHandler 0x200001f6 Thumb Code 0
CANG_RX0_IRQHandler 0x200001f6 Thumb Code 0
CANG_RX1_IRQHandler 0x200001f6 Thumb Code 0
```
3. Demonstration in debug mode

Remove “Run to main()” in “Option for Target -> Debug”, as is shown in Figure 3-1. Remove “Run to main()”.

Figure 3-1. Remove “Run to main()”

Enter the debug mode, the program starts running at the address 0x200001E0.

Figure 3-2. Debug the program

So far, boot from SRAM is successfully. As long as the power is not cut off, the program can run after reset.
4. **Revision history**

Table 4-1. Revision history

<table>
<thead>
<tr>
<th>Revision No.</th>
<th>Description</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>Initial Release</td>
<td>Nov.01, 2021</td>
</tr>
</tbody>
</table>
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