GigaDevice Semiconductor Inc.

Arm® Cortex®-M3/4 32-bit MCU

Application Note
AN024
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1. **Introduction to scatter loading in KEIL**

In the project generated by KEIL's default configuration, MDK will get the FLASH and RAM size information of the chip according to the chip model we configured in the option, and will automatically generate a scatter-loading named after the project name with the suffix *.sct File (Linker Control File, scatter loading), the linker determines the allocation address of each section on the memory according to the configuration of the generated scatter-loading file. Therefore, we can modify the file to store the specified code section in different locations.

This application note is based on the GD32F4xx series, using the GD32F450i-EVAL board, the keil version is 4.74.0.22, and the compiler version is V5.03.0.76, which describes how to implement the following functions:

- Load global variables to the specified location.
- Load function to the specified location.
- Load array to the specified position.
- Load .c file to the specified location.
- The above function is loaded to the designated location of SDRAM.
2. Implementation of scatter-loading in KEIL

2.1. Use manually written sct files

This project directly uses the manually-written sct file. Uncheck the “Options for Target->Linker-> Use Memory Layout from Target Dialog” option in MDK. After unchecking, you can directly click the “Edit” button to edit the sct file of the project. The related configuration is shown in **Figure 2-1. Use manually written sct file**.

**Figure 2-1. Use manually written sct file**

Similarly, you can also go to the project directory "GD32F4xx_ScatterLoading_v1.0.0 \ Project \ Keil_project \ MDK-ARM \ GD32F450.sct" to edit it, the file opening code is shown in **Table 2-1. GD32F450.sct code**.

**Table 2-1. GD32F450.sct code**

```
; ************************************************************
; *** Scatter-Loading Description File generated by uVision ***
; ************************************************************

LR_IROM1 0x08000000 0x0001ffff  { ; load region size_region
ER_IROM1 0x08000000 0x0001ffff  { ; load address = execution address
*.o (RESET, +First)
*(InRoot$$Sections)
}
RW_IRAM1 0x20000000 0x00001000  { ; RW data
.Any (+RW +ZI)
}
ER_ISDRAM_FUNC 0xc0000000 0x00001000  {
```
/** Array scatter loading **/ LR_IROM2 0x08020000 0x0001ffff {
    RW_IRAM_Array 0x20001000 0x00000020 {
        main.o(RAM_Array)
    }
}

**** File scatter loading ****/
LR_IROM3 0x08040000 0x0001ffff {
    ER_IROM_Object 0x08040000 0x0001ffff {
        gd32f4xx_it.o (+RO)
    }
    RW_IRAM_Object 0x20001100 0x00000100 {
        hw_config.o (+RO)
    }
}

**** Function scatter loading ****/
LR_IROM4 0x08060000 0x0001ffff {
    ER_IROM_FUNC 0x08060000 0x0001ffff {
        main.o(ROM_FUNC)
    }
    ER_IRAM_FUNC 0x20001200 0x00000100 {
        main.o(SRAM_FUCN)
    }
}

**** Variable scatter loading ****/
LR_IROM5 0x08080000 0x0001ffff {
    ER_IROM_VARIABLE 0x08080000 0x0001ffff {
        main.o(ROM_VARIABLE)
    }
}
The red part is the main part of the code added to achieve the scattered loading function, which will be analyzed in detail below.

2.2. Load global variables to the specified location

Method 1: Add the following code to the GD32F450.sct file, as shown in Table 2-2. 

<table>
<thead>
<tr>
<th>Table 2-2. GD32F450.sct loads the global variable to the specified location code</th>
</tr>
</thead>
<tbody>
<tr>
<td>**** Variable scatter loading ****/</td>
</tr>
<tr>
<td>LR_IROM5 0x08080000 0x0001ffff {</td>
</tr>
<tr>
<td>ER_IROM_VARIABLE 0x08080000 0x0001ffff {</td>
</tr>
<tr>
<td>main.o(ROM_VARIABLE)</td>
</tr>
<tr>
<td>}</td>
</tr>
</tbody>
</table>

The above code loads the ROM_VARIABLE section in the main.o module to the starting position of 0x08080000. The global variables defined in the main.c file are shown in Table 2-3. Load the global variable to the specified location code in main.c 1.

<table>
<thead>
<tr>
<th>Table 2-3. Load the global variable to the specified location code in main.c 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>/* load the variable testValue_ROM to flash address 0x08080000 */</td>
</tr>
<tr>
<td>uint32_t testValue_ROM <strong>attribute</strong>((section(&quot;ROM_VARIABLE&quot;)))=5;</td>
</tr>
</tbody>
</table>

Method 2: Add __attribute__((at(xxx))) after the global variable. This routine defines the variable uint32_t testValue_RAM in main.c.

<table>
<thead>
<tr>
<th>Table 2-4. Main.c loads the global variable to the specified location code 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>/* load the variable testValue_RAM to ram address 0x20003000 */</td>
</tr>
<tr>
<td>uint32_t testValue_RAM <strong>attribute</strong>((at(0x20003000)))=6;</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Table 2-5. Load the global variable to the specified location and print the result</th>
</tr>
</thead>
<tbody>
<tr>
<td>variable testValue_ROM address is 0x8080000</td>
</tr>
<tr>
<td>variable testValue_RAM address is 0x20003000</td>
</tr>
</tbody>
</table>

/* load the variable testValue_RAM to ram address 0x20003000 */
2.3. Load the function to the specified location

Add the following code to the GD32F450.sct file, as shown in Table 2-6. Load the function to the specified location code in GD32F450.sct.

Table 2-6. Load the function to the specified location code in GD32F450.sct

```
**** Function scatter loading ***/
LR_IROM4 0x08060000 0x0001ffff {
    ER_IROM_FUNC 0x08060000 0x0001ffff {
        main.o(ROM_FUNC)
    }
    ER_IRAM_FUNC 0x20001200 0x00000100 {
        main.o(SRAM_FUCN)
    }
}
```

The above code will load the ROM_FUNC section and SRAM_FUCN section in the main.o module to the starting position of 0x08060000 and 0x20001200, respectively. In the main.c file, allocate the delay function and the fill_TX_Data function to ROM_FUNC and SRAM_FUCN respectively, and the code is shown in Table 2-7. Load the function to the specified location code in main.c.

Table 2-7. Load the function to the specified location code in main.c

```
/* load the function delay() to flash address 0x08060000 */
/*
 \brief delay program
 param[in] none
 param[out] none
 retval none
*/
void delay(void) __attribute__((section("ROM_FUNC")))
{
    uint32_t i;
    for(i=0;i<0x2fffff;i++);
}

/* load the function fill_TX_Data() to sram address 0x20001200 */
/*
 \brief fill_TX_Data program
 param[in] none
 param[out] none
 retval none
*/
void fill_TX_Data(void) __attribute__((section("SRAM_FUCN")))
;
void fill_TX_Data()
{
    uint32_t i;
    for(i = 0;i<5;i++)
    {
        TX_Data[i] = i;
    }
}

The program debugging results are shown in **Figure 2-2. Use manually written sct file**.

**Figure 2-2. Use manually written sct file**

2.4. **Load the array to the specified location**

**Method 1**: Add the following code to the GD32F450.sct file, as shown in **Table 2-8. Load the function to the specified location code in GD32F450.sct**.

**Table 2-8. Load the function to the specified location code in GD32F450.sct**

```c
/*** Array scatter loading **/
LR_IROM2 0x08020000 0x0001ffff {
    RW_IRAM_Array 0x20001000 0x00000020 {
        main.o(RAM_Array)
    }
}
```

The above code loads the RAM_Array section in the main.o module to the starting position of 0x20001000, and defines the array TX_Data[] in main.c. The codes are shown in **Table 2-9. Code to load the array to the specified location in main.c** 1.

**Table 2-9. Code to load the array to the specified location in main.c** 1

```c
/* load the array TX_Data[5] to sram address 0x20001000 */
uint32_t TX_Data[5] __attribute__((section(".bss.RAM_Array")))={0};
```
**Method 2:** Add `__attribute__((at(xxx)))` after the array. This routine defines the array `test` in `main.c` and the `const char constdata[]` code in the `const-data.c` file as shown in **Table 2-10. Code to load the array to the specified position in data.c.** As shown, define `test_sram[]` in `main.c`, the code is shown in **Table 2-11. Code to load the array to the specified location in main.c.**

**Table 2-10. Code to load the array to the specified position in data.c**

```c
/* Load const array constdata to address 0x08001000 */
const char constdata[] __attribute__((at(0x08001000))) = {
  0x52, 0x49, 0x46, 0x46, 0xB4, 0x5C, 0x03, 0x00,
  0x57, 0x41, 0x56, 0x45, 0x6D, 0x74, 0x20,
  0x10, 0x00, 0x00, 0x00, 0x01, 0x00, 0x02, 0x00,
  0x80, 0x3E, 0x00, 0x00, 0x00, 0xFA, 0x00, 0x00,
  0x04, 0x00, 0x10, 0x00, 0x64, 0x61, 0x74, 0x61,
  0x90, 0x5C, 0x03, 0x00, 0x00, 0x00, 0x00, 0x00,
  0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00,
  ...
};
```

**Table 2-11. Code to load the array to the specified location in main.c.**

```c
/* load the array test_sram[5] to sram address 0x20007000*/
uint32_t test_sram[5] __attribute__((at(0x20007000)))={1,2,3,4,5};
```

Print the array address through the `printf` function, the results are shown in **Table 2-12. Load the array to the specified position and print the result.**

**Table 2-12. Load the array to the specified position and print the result**

- `constdata` address is 0x8001000
- `TX_Data` address is 0x20001000
- `test_sram` address is 0x20007000

The program debugging results are shown in **Figure 2-3. Debugging result of the array loaded to the specified position.**

**Figure 2-3. Debugging result of the array loaded to the specified position**
2.5. Load the .c file to the specified location

Add the following code to the GD32F450.sct file, as shown in Table 2-13. Code to load the file to the specified location in GD32F450.sct.

Table 2-13. Code to load the file to the specified location in GD32F450.sct

```
***** File scatter loading  ****/
LR_IROM3 0x08040000 0x0001ffff {
  ER_IROM_Object  0x08040000 0x0001ffff {
    gd32f4xx_it.o (+RO)
  }
  RW_IRAM_Object 0x20001100 0x00000100 {
    hw_config.o (+RO)
  }
}
```

The above code will load the gd32e230_it.o file to the starting position of 0x08040000 and the hw_config.o file to the starting position of 0x20001100. The debugging results of the program as shown in Figure 2-4. Debugging result of the .c file load to the specified location.

Figure 2-4. Debugging result of the .c file load to the specified location
3. Scattered loading of SDRAM

3.1. The basic principle of scatter loading of SDRAM

In Cortex-M4 core, we can access the addresses above 0x2000 0000 and read data and instructions through the system bus, but in the default configuration of the kernel, some addresses are in the address segment that prohibits execution of instructions, so the code is loaded onto this segment, and an error occurs during execution. The address allocation of SDRAM in EXMC of GD32F450 is 0xC0000000-0xDFFFFFF located in this address segment.

In response to the above problems, there are two solutions to achieve scatter loading in SDRAM:

1. Configure the MPU (Memory Protect Unit) register to make the 0xC0000000 address segment executable (this example will use this implementation).

2. Adopt memory mapping method (map SDRAM address segment to executable area by configuring SYSCFG register).

3.2. Implementation of SDRAM distributed loading

Add the following red font codes to the GD32F450.sct file. The codes are shown in Table 3-1.

Table 3-1. SDRAM scatter-loading implementation code in GD32F450.sct

```plaintext
LR_IROM1 0x08000000 0x0001ffff {      ; load region size_region
ER_IROM1 0x08000000 0x0000ffff {    ; load address = execution address
    *.o (RESET, +First)
    *(InRoot$$Sections)
}
RW_IRAM1 0x20000000 0x00010000 {  ; RW data
    .ANY (+RW +ZI)
}
ER_ISDRAM_FUNC 0xc0000000 0x00001000 {
    *(SDRAM_FUNC)
}
ER_ISDRAM_ARRAY 0xc0001000 0x00001000 {
    *(SDRAM_ARRAY)
}
ER_ISDRAM_OBJ 0xc0002000 0x00001000 {
    test.o (+RO)
}
```
The above code will load the SDRAM_FUNC segment, SDRAM_ARRAY segment and test.o file to the starting addresses of 0xc0001000, 0xc0000000 and 0xc0002000 respectively. Add the following code to startup_gd32f450.s, as shown in Figure 3-1. Add code to startup_gd32f450.s.

Figure 3-1. Add code to startup_gd32f450.s

```
:int reset_Handler PROC
PROC Reset_Handler
   IMPORT SystemInit
   IMPORT DoInit
   IMPORT __main
   BLX Ro, SystemInit
   LDR Ro, =DoInit
   BLX Ro, __main
   LDR Ro, =__main
   BX Ro
ENDP
```

The DoInit function is defined in main.c, which mainly implements EXMC initialization and MPU related configuration. The function codes are shown in Table 3-2. DoInit function implementation code.

Table 3-2. DoInit function implementation code

```
/*!
 * brief initialize the sdram, setup the MPU
 * param[in] none
 * param[out] none
 * retval none
 */
void DoInit(void)
{
    /* sdram peripheral initialize */
    exmc_synchronous_dynamic_ram_init(EXMC_SDRAM_DEVICE0);
    /* Configures the MPU regions */
    mpu_setup();
}
```

Define the variable uint32_t testValue_SDRAM in main.c, the array int test_sdram[5], the function testFuncInSDRAM, and add the file test.c. The main codes are shown in Table 3-3. Scatter-loading into the specified location code of SDRAM.

Table 3-3. Scatter-loading into the specified location code of SDRAM

```
/* load the variable testValue_RAM to sdram address 0xC00003000 */
uint32_t testValue_SDRAM __attribute__((at(0xC00003000)));
/* load the array test_sdram[5] to sdram address 0xc0001000 */
uint32_t test_sdram[5] __attribute__((section("SDRAM_ARRAY")))={0};
/* load the function testFuncInSDRAM to sdram address 0xc0000000 */
```
void testFuncInSDRAM(void) __attribute__((section("SDRAMFUNC"))); /* test.c */
void test_in_s dram()
{
    gd_eval_led_on(LED3);
}

Table 3-4. Load variables and arrays to the specified location of SDRAM and the result
and Figure 3-2. Debugging result of loading the function and .c file to the designated
location of SDRAM show the results of program operation and debugging:

<table>
<thead>
<tr>
<th>Variable</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>testValue_SDRAM</td>
<td>0xc0003000</td>
</tr>
<tr>
<td>test_sDRAM</td>
<td>0xc0001000</td>
</tr>
</tbody>
</table>

Figure 3-2. Debugging result of loading the function and .c file to the designated
location of SDRAM
4. Results

View the "GD32F4XX_ScatterLoading_v1.0.0\Project\Keil\MDK-ARM\Listings \ Project.map" file and open it as shown in Figure 4-1. Scatter loading project to compile Project.map file.

From the map file, it can be seen that the load address and execution address of each segment conform to the specified scattered load area.
5. **Revision history**

Table 5-1. Revision history

<table>
<thead>
<tr>
<th>Revision No.</th>
<th>Description</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>Initial Release</td>
<td>Apr.30, 2021</td>
</tr>
</tbody>
</table>
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