GigaDevice Semiconductor Inc.

Arm® Cortex®-M3/4 32-bit MCU

Application Note
AN008
A solution to the existing limitations of deep-sleep mode

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1. **Introduction**

There is a limitation when using deep-sleep mode with GD32 series MCUs. If user enable some interrupts which are not the target wake-up source, when using deep-sleep mode, regardless of the use of WFI or WFE instruction, there will be a serious risk, that after entering deep-sleep mode, MCU may never be awakened by the target signal.
2. **Workarounds**

In order to avoid this risk, the user should replace the font-weight part of the function `pmu_to_deepsleepmode` in the **Table 2-1. original function of GD standard lib**. The function could be found in the file named similar as “gd32fxxx_pmu.c” in our standard library.

The user needs to select the corresponding new codes according to MCU product type.

**Table 2-1. original function of GD standard lib**

```c
/*! 
\brief PMU work at deep sleep mode 
\param[in] ldo 
\param[in] deepsleepmodecmd: 
\param[out] none 
\retval none */
void pmu_to_deepsleepmode(uint32_t ldo,uint8_t deepsleepmodecmd)
{
  /* clear stbmod and ldolp bits */
  PMU_CTL &= ~((uint32_t)(PMU_CTL_STBMOD | PMU_CTL_LDOLP));

  /* set ldolp bit according to pmu_ldo */
  PMU_CTL |= ldo;

  /* set sleepdeep bit of Cortex-M4 system control register */
  SCB->SCR |= SCB_SCR_SLEEPDEEP_Msk;

  /* select WFI or WFE command to enter deepsleep mode */
  if(WFI_CMD == deepsleepmodecmd){
    _WFI();
  }else{
    _SEV();
    _WFE();
  }

  /* reset sleep deep bit of Cortex-M4 system control register */
  SCB->SCR &= ~(uint32_t)SCB_SCR_SLEEPDEEP_Msk;
}
```
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2.1. The corresponding replacement codes for GD32F10x / F20x / F30x / F403 series lib

Table 2.2. Replacement codes for GD32F10x / F20x / F30x / F403

```c
{
    static uint32_t reg_snap[4];

    reg_snap[0] = REG32(0xE000E010);
    reg_snap[1] = REG32(0xE000E100);
    reg_snap[2] = REG32(0xE000E104);
    reg_snap[3] = REG32(0xE000E108);

    REG32(0xE000E010) &= 0x00010004;
    REG32(0xE000E180) = 0xFF7FF83D;
    REG32(0xE000E184) = 0xBFFFF8FF;
    REG32(0xE000E188) = 0xFFFFFFFF;

    /* select WFI or WFE command to enter deepsleep mode */
    if(WFI_CMD == deepsleepmodecmd){
        __WFI();
    }else{
        __SEV();
        __WFE();
        __WFE();
    }

    REG32(0xE000E010) = reg_snap[0];
    REG32(0xE000E100) = reg_snap[1];
    REG32(0xE000E104) = reg_snap[2];
    REG32(0xE000E108) = reg_snap[3];
}
```
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2.2. The corresponding replacement codes for GD32F1x0 / F3x0 series lib

Table 2-3. Replacement codes for GD32F1x0 / F3x0

```c
{
    static uint32_t reg_snap[4];

    reg_snap[0] = REG32(0xE000E010);
    reg_snap[1] = REG32(0xE000E100);
    reg_snap[2] = REG32(0xE000E104);
    reg_snap[3] = REG32(0xE000E108);

    REG32(0xE000E010) &= 0x00010004;
    REG32(0xE000E180) = 0XB7FFEF19;
    REG32(0xE000E184) = 0XFFFFFBFF;
    REG32(0xE000E188) = 0xFFFFFFFF;

    /* select WFI or WFE command to enter deepsleep mode */
    if(WFI_CMD == deepsleepmodecmd){
        __WFI();
    }else{
        __SEV();
        __WFE();
        __WFE();
    }

    REG32(0xE000E010) = reg_snap[0];
    REG32(0xE000E100) = reg_snap[1];
    REG32(0xE000E104) = reg_snap[2];
    REG32(0xE000E108) = reg_snap[3];
}
```
2.3. The corresponding replacement codes for GD32F40x series

lib

Table 2-4. Replacement codes for GD32F40x

```c
{
    static uint32_t reg_snap[4];

    reg_snap[0] = REG32(0xE000E010);
    reg_snap[1] = REG32(0xE000E010);
    reg_snap[2] = REG32(0xE000E104);
    reg_snap[3] = REG32(0xE000E108);

    REG32(0xE000E010) &= 0x00010004;
    REG32(0xE000E180) = 0xFFF7FF83D;
    REG32(0xE000E184) = 0xBFFFF8FF;
    REG32(0xE000E188) = 0xFFFFFFFF;

    /* select WFI or WFE command to enter deep sleep mode */
    if(WFI_CMD == deepsleepmodecmd){
        __WFI();
    }else{
        __SEV();
        __WFE();
        __WFE();
    }

    REG32(0xE000E010) = reg_snap[0];
    REG32(0xE000E100) = reg_snap[1];
    REG32(0xE000E104) = reg_snap[2];
    REG32(0xE000E108) = reg_snap[3];
}
```
3. Revision history

Table 3-1. Revision history

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<tr>
<th>Revision No.</th>
<th>Description</th>
<th>Date</th>
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<tr>
<td>1.0</td>
<td>Initial Release</td>
<td>Nov.30 2021</td>
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