GigaDevice Semiconductor Inc.

GD32F450xx
Arm® Cortex®-M4 32-bit MCU

Datasheet
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1. General description

The GD32F450xx device belongs to the stretch performance line of GD32 MCU family. It is a new 32-bit general-purpose microcontroller based on the Arm® Cortex®-M4 RISC core with best cost-performance ratio in terms of enhanced processing capacity, reduced power consumption and peripheral set. The Cortex®-M4 core features a Floating Point Unit (FPU) that accelerates single precision floating point math operations and supports all Arm® single precision instructions and data types. It implements a full set of DSP instructions to address digital signal control markets that demand an efficient, easy-to-use blend of control and signal processing capabilities. It also provides a Memory Protection Unit (MPU) and powerful trace technology for enhanced application security and advanced debug support.

The GD32F450xx device incorporates the Arm® Cortex®-M4 32-bit processor core operating at 200 MHz frequency with Flash accesses zero wait states to obtain maximum efficiency. It provides up to 3072 KB on-chip Flash memory and 512 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer up to three 12-bit 2.6 MSPS ADCs, two 12-bit DACs, up to eight general 16-bit timers, two 16-bit PWM advanced timers, two 32-bit general timers, and two 16-bit basic timers, as well as standard and advanced communication interfaces: up to six SPIs, three I2Cs, four USARTs and four UARTs, two I2Ss, two CANs, a SDIO, USBFS and USBHS, and an ENET. Additional peripherals as Digital camera interface (DCI), EXMC interface with SDRAM extension support, TFT-LCD Interface (TLI) and Image Processing Accelerator (IPA) are included.

The device operates from a 2.6 to 3.6V power supply and available in –40 to +85 °C temperature range. Three power saving modes provide the flexibility for maximum optimization of power consumption, an especially important consideration in low power applications.

The above features make GD32F450xx devices suitable for a wide range of interconnection and advanced applications, especially in areas such as industrial control, consumer and handheld equipment, embedded modules, human machine interface, security and alarm systems, graphic display, automotive navigation, drone, IoT and so on.
## 2. Device overview

### 2.1. Device information

#### Table 2-1. GD32F450xx devices features and peripheral list

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2.2. Block diagram

Figure 2-1. GD32F450xx block diagram
2.3. Pinouts and pin assignment

Figure 2.2. GD32F450lx BGA176 pinouts

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Figure 2-3. GD32F450Zx LQFP144 pinouts

GigaDevice GD32F450Zx
LQFP144
2.4. Memory map

Table 2-2. GD32F450xx memory map

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<td>EXMC - SWREG</td>
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<td>EXMC - PC CARD</td>
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**Note:**
(1) ADC_SSTAT, ADC_SYNCCTL, ADC_SYNCDATA based on base address of ADC0.
2.5. Clock tree

**Figure 2.5. GD32F450xx clock tree**

**Legend:**
- HXTAL: High speed crystal oscillator
- LXTAL: Low speed crystal oscillator
- IRC16M: Internal 16M RC oscillators
- IRC32K: Internal 32K RC oscillator
- IRC48M: Internal 48M RC oscillators
## 2.6. Pin definitions

### 2.6.1. GD32F450lx BGA176 pin definitions

Table 2-3. GD32F450lx BGA176 pin definitions

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<th>Level(2)</th>
<th>Functions description</th>
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(1) Pin Type: I/O, P = Pull up, N = Pull down

(2) I/O Level: 5V, 3.3V, 2.5V, 1.8V, 1.35V, 1.0V, 0.6V, 0.3V, 0.18V

(3) Function: Alternate, Default, Alternate and Default, Alternate, Default and Alternate, Default and Alternate
## 2.6.2. GD32F450Zx LQFP144 pin definitions

### Table 2-4. GD32F450Zx LQFP144 pin definitions

<table>
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<tr>
<th>Pin Name</th>
<th>PINS</th>
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<th>I/O Level(2)</th>
<th>Functions description</th>
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| PE6      | 5    | I/O        | 5VT          | Default: PE6  
Alternate: TRACED2, TIMER8_CH0, SPI3_MISO, EXMC_A21, DCI_D6, TLI_G0, EVENTOUT |
| VBAT     | 6    | P          | -            | Default: VBAT |
| PC13-TAMPER-RTC | 7 | I/O  | 5VT  | Default: PC13  
Alternate: EVENTOUT  
Additional:RTC_TIMPO, RTC_OUT, RTC_TS |
| PC14-OSC32IN | 8 | I/O  | 5VT  | Default: PC14  
Alternate: EVENTOUT  
Additional:OSC32IN |
| PC15-OSC32OUT | 9 | I/O  | 5VT  | Default: PF0  
Alternate: I2C1_SDA, EXMC_A0, EVENTOUT, CTC_SYNC |
| PF0      | 10   | I/O       | 5VT          | Default: PF1  
Alternate: I2C1_SCL, EXMC_A1, EVENTOUT |
| PF1      | 11   | I/O       | 5VT          | Default: PF2  
Alternate: I2C1_SMB, EXMC_A2, EVENTOUT |
| PF2      | 12   | I/O       | 5VT          | Default: PF3  
Alternate: EXMC_A3, EVENTOUT, I2C1_TXFRAME  
Additional:ADC2_IN9 |
| PF3      | 13   | I/O       | 5VT          | Default: PF4  
Alternate: EXMC_A4, EVENTOUT  
Additional:ADC2_IN14 |
| PF4      | 14   | I/O       | 5VT          | Default: PF5  
Alternate: EXMC_A5, EVENTOUT  
Additional:ADC2_IN15 |
| VSS      | 16   | P         | -            | Default: VSS |
| VDD      | 17   | P         | -            | Default: VDD |
| PF6      | 18   | I/O       | 5VT          | Default: PF6  
Alternate: TIMER9_CH0, SPI4_NSS, UART6_RX, EXMC_NIORD, EVENTOUT  
Additional:ADC2_IN4 |
| PF7      | 19   | I/O       | 5VT          | Default: PF7  
Alternate: TIMER10_CH0, SPI4_SCK, UART6_TX, EXMC_NREG, EVENTOUT  
Additional:ADC2_IN5 |
| PF8      | 20   | I/O       | 5VT          | Default: PF8  
Alternate: SPI4_MISO, TIMER12_CH0, EXMC_NIOWR, EVENTOUT  
Additional:ADC2_IN6 |
<p>| PF9      | 21   | I/O       | 5VT          | Default: PF9 |</p>
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<td>I/O Level(2)</td>
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<td>I/O Level(2)</td>
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<td>I/O Level(2)</td>
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Notes:

(1) Type: I = input, O = output, P = power.
(2) I/O Level: 5VT = 5 V tolerant.

### 2.6.3. GD32F450Vx LQFP100 pin definitions

Table 2-5. GD32F450Vx LQFP100 pin definitions

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pins</th>
<th>Pin Type(1)</th>
<th>I/O Level(2)</th>
<th>Functions description</th>
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<td>Default: PD8 Alternate: USART2_TX, EXMC_D13, EVENTOUT</td>
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<td>Default: PD9 Alternate: USART2_RX, EXMC_D14, EVENTOUT</td>
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<td>Pin Type(1)</td>
<td>I/O Level(2)</td>
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**Notes:**
(1) Type: I = input, O = output, P = power.
(2) I/O Level: 5VT = 5 V tolerant.
### 2.6.4. GD32F450xx pin alternate functions

#### Table 2-6. Port A alternate functions summary

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>AF0</th>
<th>AF1</th>
<th>AF2</th>
<th>AF3</th>
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<th>AF14</th>
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Note: AF0, AF1, AF2, etc., refer to the alternate functions assigned to each pin. The table lists the functions associated with each pin as per the datasheet specifications.
### Table 2-10. Port E alternate functions summary

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**Notes:**
- **Timer3_CH1**: Timer3 Channel 1
- **Timer3_CH2**: Timer3 Channel 2
- **CTC_SYN**: CTC Synchronization
- **EXMC_A18**: External Memory Controller A18
- **EXMC_D0**: External Memory Controller D0
- **EXMC_D1**: External Memory Controller D1
- **EVENTOUT**: Event Output
- **UART7_RX**: UART7 Receive
- **UART7_TX**: UART7 Transmit
- **ENET_MII_TXD3**: Ethernet MII TXD3
- **EXMC_D4**: External Memory Controller D4
- **DCI_D2**: DCI D2
- **DCI_D3**: DCI D3
- **DCI_D4**: DCI D4
- **DCI_D6**: DCI D6
- **DCI_D7**: DCI D7
- **TLI_B0**: TLI B0
- **TLI_B1**: TLI B1
- **TLI_G0**: TLI G0
- **TLI_G1**: TLI G1
- **TLI_B4**: TLI B4
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3. **Functional description**

3.1. **Arm® Cortex®-M4 core**

The Arm® Cortex®-M4 processor is a high performance embedded processor with DSP instructions which allow efficient signal processing and complex algorithm execution. It brings an efficient, easy-to-use blend of control and signal processing capabilities to meet the digital signal control markets demand. The processor is highly configurable enabling a wide range of implementations from those requiring floating point operations, memory protection and powerful trace technology to cost sensitive devices requiring minimal area, while delivering outstanding computational performance and an advanced system response to interrupts.

- 32-bit Arm® Cortex®-M4 processor core
  - Up to 200 MHz operation frequency
  - Single-cycle multiplication and hardware divider
  - Floating Point Unit (FPU)
  - Integrated DSP instructions
  - Integrated Nested Vectored Interrupt Controller (NVIC)
  - 24-bit SysTick timer

The Cortex®-M4 processor is based on the Armv7-M architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M4:

- Internal Bus Matrix connected with ICode bus, DCode bus, system bus, Private Peripheral Bus (PPB) and debug accesses (AHB-AP)
- Nested Vectored Interrupt Controller (NVIC)
- Flash Patch and Breakpoint (FPB)
- Data Watchpoint and Trace (DWT)
- Instrument Trace Macrocell (ITM)
- Memory Protection Unit (MPU)
- Serial Wire JTAG Debug Port (SWJ-DP)
- Trace Port Interface Unit (TPIU)

3.2. **On-chip memory**

- Up to 3072 Kbytes of Flash memory, including code Flash and data Flash
- 256 KB to 512 KB of SRAM

The Arm® Cortex®-M4 processor is structured in Harvard architecture which can use separate buses to fetch instructions and load/store data. 3072 Kbytes of inner Flash at most, which includes code Flash and data Flash is available for storing programs and data, and accessed (R/W) at CPU clock speed with zero wait states. Up to 512 Kbytes of inner SRAM is composed of SRAM0 (112KB), SRAM1 (16KB), and SRAM2 (64KB) and ADDSRAM (256KB) that can
be accessed at the same time, and including 64 KB of TCM (tightly-coupled memory) data RAM that can be accessed only by the data bus of the Cortex®-M4 core. The additional 4KB of backup SRAM (BKP SRAM) is implemented in the backup domain, which can keep its content even when the $V_{DD}$ power supply is down. Table 2-2. GD32F450xx memory map shows the memory map of the GD32F450xx series of devices, including Flash, SRAM, peripheral, and other pre-defined regions.

3.3. Clock, reset and supply management

- Internal 16 MHz factory-trimmed RC and external 4 to 32 MHz crystal oscillator
- Internal 48 MHz RC oscillator
- Internal 32 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator
- Integrated system clock PLL
- 2.6 to 3.6 V application supply and I/Os
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD)

The Clock Control Unit (CCU) provides a range of oscillator and clock functions. These include internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and two APB domains. The maximum frequency of the two AHB domains are 200 MHz. The maximum frequency of the two APB domains including APB1 is 50 MHz and APB2 is 100 MHz. See Figure 2-5. GD32F450xx clock tree for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from 2.4 V and down to 1.8V. The device remains in reset mode when $V_{DD}$ is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:
- $V_{DD}$ range: 2.6 to 3.6 V, external power supply for I/Os and the internal regulator. Provided externally through $V_{DD}$ pins.
- $V_{SSA}, V_{DDA}$ range: 2.6 to 3.6 V, external analog power supplies for ADC, reset blocks, RCs and PLL. $V_{DDA}$ and $V_{SSA}$ must be connected to $V_{DD}$ and $V_{SS}$, respectively.
- $V_{BAT}$ range: 1.8 to 3.6 V, power supply for RTC, external clock 32 KHz oscillator and backup registers (through power switch) when $V_{DD}$ is not present.

3.4. Boot modes

At startup, boot pins are used to select one of three boot options:
- Boot from main Flash memory (default)
- Boot from system memory
3.5. Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are sleep mode, deep-sleep mode, and standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep mode**
  In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt/event can wake up the system.

- **Deep-sleep mode**
  In deep-sleep mode, all clocks in the 1.2V domain are off, and all of the high speed crystal oscillator (IRC16M, HXTAL) and PLL are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the 16 external lines, the RTC alarm, RTC Tamper and TimeStamp event, the LVD output, ENET wakeup, RTC wakeup and USB wakeup. When exiting the deep-sleep mode, the IRC16M is selected as the system clock.

- **Standby mode**
  In standby mode, the whole 1.2V domain is power off, the LDO is shut down, and all of IRC16M, HXTAL and PLL are disabled. The contents of SRAM and registers (except backup registers) are lost. There are four wakeup sources for the standby mode, including the external reset from NRST pin, the RTC, the FWDGT reset, and the rising edge on WKUP pin.

3.6. Analog to digital converter (ADC)

- 12-bit SARADC’s conversion rate is up to 2.6 MSPS
- 12-bit, 10-bit, 8-bit or 6-bit configurable resolution
- Hardware oversampling ratio adjustable from 2 to 256x improves resolution to 16-bit
- Input voltage range: $V_{SSA} \text{ to } V_{DDA}$ (2.6 V ≤ $V_{DDA}$ ≤ 3.6 V)
- Temperature sensor

Up to three 12-bit 2.6 MSPS multi-channel ADCs are integrated in the device. It has a total of
19 multiplexed channels: 16 external channels, 1 channel for internal temperature sensor (V\textsubscript{SENSE}), 1 channel for internal reference voltage (V\textsubscript{REFINT}) and 1 channel for external battery power supply (V\textsubscript{BAT}). The input voltage range is between 2.6 V and 3.6 V. An on-chip hardware oversampling scheme improves performance while off-loading the related computational burden from the CPU. An analog watchdog block can be used to detect the channels, which are required to remain within a specific threshold window. A configurable channel management block can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced use.

The ADC can be triggered from the events generated by the general level 0 timers (TIMERx) and the advanced timers (TIMER0 and TIMER7) with internal connection. The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally connected to the ADC\_IN16 input channel which is used to convert the sensor output voltage in a digital value.

### 3.7. Digital to analog converter (DAC)

- Two 12-bit DAC converter of independent output channel
- 8-bit or 12-bit mode in conjunction with the DMA controller

The 12-bit buffered DAC channel is used to generate variable analog outputs. The DACs are designed with integrated resistor strings structure. The DAC channels can be triggered by the timer update outputs or EXTI with DMA support. The maximum output value of the DAC is V\textsubscript{REF+}.

### 3.8. DMA

- 16 channels DMA controller and each channel are configurable (8 for DMA0 and 8 for DMA1)
- Support independent 8, 16, 32-bit memory and peripheral transfer
- Peripherals supported: Timers, ADC, SPIs, I2Cs, USARTs, UARTs, DAC, I2S, SDIO and DCI

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory.

Each channel is connected to fixed hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.
3.9. General-purpose inputs/outputs (GPIOs)

- Up to 140 fast GPIOs, all mappable on 16 external interrupt lines
- Analog input/output configurable
- Alternate function input/output configurable

There are up to 140 general purpose I/O pins (GPIO) in GD32F450xx, named PA0 ~ PA15, PB0 ~ PB15, PC0 ~ PC15, PD0 ~ PD15, PE0 ~ PE15, PF0 ~ PF15, PG0 ~ PG15, PH0 ~ PH15 and PI0 ~ PI11 to implement logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt/event controller (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current capable except for analog inputs.

3.10. Timers and PWM generation

- Two 16-bit advanced timer (TIMER0 & TIMER7), eight 16-bit general timers (TIMER2, TIMER3, TIMER8 ~ TIMER13), two 32-bit general timers (TIMER1 & TIMER4) and two 16-bit basic timer (TIMER5 & TIMER6)
- Up to 4 independent channels of PWM, output compare or input capture for each general timer and external trigger input
- 16-bit, motor control PWM advanced timer with programmable dead-time generation for output match
- Encoder interface controller with two inputs using quadrature decoder
- 24-bit SysTick timer down counter
- 2 watchdog timers (free watchdog timer and window watchdog timer)

The advanced timer (TIMER0 & TIMER7) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general timer. The 4 independent channels can be used for input capture, output compare, PWM generation (edge-aligned or center-aligned counting modes) and single pulse mode output. If configured as a general 16-bit timer, it has the same functions as the TIMERx timer. It can be synchronized with external signals or to interconnect with other general timers together which have the same architecture and features.

The general timer, can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TIMER1 & TIMER4 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TIMER2 & TIMER3 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. TIMER8 ~
TIMER13 is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. The general timer also supports an encoder interface with two inputs using quadrature decoder.

The basic timer, known as TIMER5 & TIMER6, are mainly used for DAC trigger generation. They can also be used as a simple 16-bit time base.

The GD32F450xx have two watchdog peripherals, free watchdog timer and window watchdog timer. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-bit prescaler. It is clocked from an independent 32 KHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog timer is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wakeup interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. It features:
- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

### 3.11. Real time clock (RTC) and backup registers

- Independent binary-coded decimal (BCD) format timer/counter with twenty 32-bit backup registers.
- Calendar with sub-second, seconds, minutes, hours, week day, date, year and month automatically correction
- Alarm function with wake up from deep-sleep and standby mode capability
- On-the-fly correction for synchronization with master clock. Digital calibration with 1 ppm resolution for compensation of quartz crystal inaccuracy.

The real time clock is an independent timer which provides a set of continuously running counters in backup registers to provide a real calendar function, and provides an alarm interrupt or an expected interrupt. It is not reset by a system or power reset, or when the device wakes up from standby mode. A prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 KHz from external crystal oscillator.
3.12. **Inter-integrated circuit (I2C)**

- Up to three I2C bus interfaces can support both master and slave mode with a frequency up to 400 KHertz (Fast mode)
- Provide arbitration function, optional PEC (packet error checking) generation and checking
- Supports 7-bit and 10-bit addressing mode and general call addressing mode

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides transfer rate of up to 100 KHz in standard mode and up to 400 KHz in fast mode. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

3.13. **Serial peripheral interface (SPI)**

- Up to six SPI interfaces with a frequency of up to 30 MHz
- Support both master and slave mode
- Hardware CRC calculation and transmit automatic CRC error checking
- Quad wire configuration available in master mode (only in SPI5)

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). Both SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking. Quad-SPI master mode is also supported in SPI5 (SPI5 is not available in GD32F450Vx series).


- Up to four USARTs and four UARTs with operating frequency up to 12.5 MHz
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- ISO 7816-3 compliant smart card interface

The USART (USART0, USART1, USART2, USART5) and UART (UART3, UART4, UART6, UART7) are used to transfer data between parallel and serial interfaces, provides a flexible
full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART/UART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART/UART transmitter and receiver. The USART/UART also supports DMA function for high speed data communication.

3.15. **Inter-IC sound (I2S)**

- Two I2S bus Interfaces with sampling frequency from 8 KHz to 192 KHz, multiplexed with SPI1 and SPI2
- Support either master or slave mode Audio
- Sampling frequencies from 8 KHz up to 192 KHz are supported

The Inter-IC sound (I2S) bus provides a standard communication interface for digital audio applications by 4-wire serial lines. GD32F450xx contain an I2S-bus interface that can be operated with 16/32 bit resolution in master or slave mode, pin multiplexed with SPI1 and SPI2. The audio sampling frequencies from 8 KHz to 192 KHz is supported.

3.16. **Universal serial bus full-speed interface (USBFS)**

- One USB device/host/OTG full-speed Interface with frequency up to 12 Mbit/s
- Internal 48 MHz oscillator support crystal-less operation
- Internal main PLL for USB CLK compliantly
- Internal USBFS PHY support

The Universal Serial Bus (USB) is a 4-wire bus with 4 bidirectional endpoints. The device controller enables 12 Mbit/s data exchange with integrated transceivers. Transaction formatting is performed by the hardware, including CRC generation and checking. It supports both host and device modes, as well as OTG mode with Host Negotiation Protocol (HNP) and Session Request Protocol (SRP). The controller contains a full-speed USB PHY internal. For full-speed or low-speed operation, no more external PHY chip is needed. It supports all the four types of transfer (control, bulk, Interrupt and isochronous) defined in USB 2.0 protocol. The required precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use an HXTAL crystal oscillator) or by the internal 48 MHz oscillator in automatic trimming mode that allows crystal-less operation.

3.17. **Universal serial bus high-speed interface (USBHS)**

- One USB device/host/OTG high-speed Interface with frequency up to 480 Mbit/s
- An external PHY device connected to the ULPI is required when using in HS mode

USBHS supports both host and device modes, as well as OTG mode with Host Negotiation Protocol (HNP) and Session Request Protocol (SRP). The controller provides ULPI interface.
for external USB PHY integration and it also contains a full-speed USB PHY internal. For full-speed or low-speed operation, no more external PHY chip is needed. It supports all the four types of transfer (control, bulk, Interrupt and isochronous) defined in USB 2.0 protocol. HUB connection is supported when USBHS operates at high-speed in host mode. There is also a DMA engine operating as an AHB bus master in USBHS to speed up the data transfer between USBHS and system.

3.18. Controller area network (CAN)

- Two CAN2.0B interface with communication frequency up to 1 Mbit/s
- Internal main PLL for CAN CLK compliantly

Controller area network (CAN) is a method for enabling serial communication in field bus. The CAN protocol has been used extensively in industrial automation and automotive applications. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three mailboxes for transmission and two FIFOs of three message deep for reception. It also provides 28 scalable/configurable identifier filter banks for selecting the incoming messages needed and discarding the others.

3.19. Ethernet (ENET)

- IEEE 802.3 compliant media access controller (MAC) for Ethernet LAN
- 10/100 Mbit/s rates with dedicated DMA controller and SRAM
- Support hardware precision time protocol (PTP) with conformity to IEEE 1588

The Ethernet media access controller (MAC) conforms to IEEE 802.3 specifications and fully supports IEEE 1588 standards. The embedded MAC provides the interface to the required external network physical interface (PHY) for LAN bus connection via an internal media independent interface (MII) or a reduced media independent interface (RMII). The number of MII signals provided up to 16 with 25 MHz output and RMII up to 7 with 50 MHz output. The function of 32-bit CRC checking is also available.

3.20. External memory controller (EXMC)

- Supported external memory: SRAM, PSRAM, ROM and NOR-Flash, NAND Flash and CF card, SDRAM with up to 32-bit data bus
- Provide ECC calculating hardware module for NAND Flash memory block
- Two SDRAM banks with independent configuration, up to 13-bits Row Address, 11-bits Column Address, 2-bits internal banks address
- SDRAM Memory size: 4x16Mx32bit (256 MB), 4x16Mx16bit (128 MB), 4x16Mx8bit (64 MB)

External memory controller (EXMC) is an abbreviation of external memory controller. It is
divided into several sub-banks for external device support, each sub-bank has its own chip selection signal but at one time, only one bank can be accessed. The EXMC supports code execution from external memory except NAND Flash and CF card. The EXMC also can be configured to interface with the most common LCD module of Motorola 6800 and Intel 8080 series and reduce the system cost and complexity.

The EXMC of GD32F450xx in LQFP144 & BGA176 package also supports synchronous dynamic random access memory (SDRAM). It translates AHB transactions into the appropriate SDRAM protocol, and meanwhile, makes sure the access time requirements of the external SDRAM devices are satisfied.

3.21. Secure digital input and output card interface (SDIO)

- Support SD2.0/SDIO2.0/MMC4.2 host interface

The Secure Digital Input and Output Card Interface (SDIO) provides access to external SD memory cards specifications version 2.0, SDIO card specification version 2.0 and multi-media card system specification version 4.2 with DMA supported. In addition, this interface is also compliant with CE-ATA digital protocol rev1.1.

3.22. TFT LCD interface (TLI)

- 24-bit RGB Parallel Pixel Output; 8 bits-per-pixel (RGB888)
- Supports up to XVGA (1024x768) resolution
- 2 display layers with dedicated FIFO (64x32-bit)

The TFT LCD interface provides a parallel digital RGB (Red, Green and Blue) and signals for horizontal, vertical synchronization, Pixel Clock and Data Enable as output to interface directly to a variety of LCD (Liquid Crystal Display) and TFT (Thin Film Transistor) panels. A built-in DMA engine continuously move data from system memory to TLI and then, output to an external LCD display. Two separate layers are supported in TLI, as well as layer window and blending function.

3.23. Image processing accelerator (IPA)

- Copy one source image to the destination image
- Convert one source image to the destination image with specific pixel format
- Convert and blend two source images to the destination image with specific pixel format
- Fill up the destination image with a specific color

The Image processing accelerator (IPA) provides a configurable and flexible image format conversion from one or two source image to the destination image. Eleven pixel formats from 4-bit up to 32-bit per pixel independently for the two source images and five pixel formats from 16-bit up to 32-bit per pixel for the destination image are supported. Two 256*32 bits Look-
Up Tables (LUT) separately for the two source images are implemented for the indirect pixel formats.

3.24. Digital camera interface (DCI)

- Digital video/picture capture
- 8/10/12/14 data width supported
- High transfer efficiency with DMA interface
- Video/picture crop supported
- Various pixel formats supported including JPEG/YCrCb/RGB
- Hard/embedded synchronous signals supported

DCI is an 8-bit to 14-bit parallel interface that able to capture video or picture from a camera via Digital Camera Interface. It supports 8/10/12/14 bits data width through DMA operation.

3.25. Debug mode

- Serial wire JTAG debug port (SWJ-DP)

The Arm® SWJ-DP Interface is embedded and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

3.26. Package and operation temperature

- BGA176 (GD32F450Ix), LQFP144 (GD32F450Zx) and LQFP100 (GD32F450Vx)
- Operation temperature range: -40°C to +85°C (industrial level)
4. Electrical characteristics

4.1. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1. Absolute maximum ratings\(^{(1)}\) \(^{(4)}\)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V(_{DD})</td>
<td>External voltage range(^{(2)})</td>
<td>(V_{SS} - 0.3)</td>
<td>(V_{SS} + 3.6)</td>
<td>V</td>
</tr>
<tr>
<td>V(_{DDA})</td>
<td>External analog supply voltage</td>
<td>(V_{SSA} - 0.3)</td>
<td>(V_{SSA} + 3.6)</td>
<td>V</td>
</tr>
<tr>
<td>V(_{BAT})</td>
<td>External battery supply voltage</td>
<td>(V_{SS} - 0.3)</td>
<td>(V_{SS} + 3.6)</td>
<td>V</td>
</tr>
<tr>
<td>V(_{IN})</td>
<td>Input voltage on 5V tolerant pin(^{(3)})</td>
<td>(V_{SS} - 0.3)</td>
<td>(V_{DD} + 3.6)</td>
<td>V</td>
</tr>
<tr>
<td>(</td>
<td>\Delta V_{DDX}</td>
<td>)</td>
<td>Variations between different V(_{DD}) power pins</td>
<td>—</td>
</tr>
<tr>
<td>(</td>
<td>V_{SSX} - V_{SS}</td>
<td>)</td>
<td>Variations between different ground pins</td>
<td>—</td>
</tr>
<tr>
<td>I(_{IO})</td>
<td>Maximum current for GPIO pins</td>
<td>—</td>
<td>(\pm 25)</td>
<td>mA</td>
</tr>
<tr>
<td>T(_{A})</td>
<td>Operating temperature range</td>
<td>-40</td>
<td>+85</td>
<td>(^{\circ})C</td>
</tr>
<tr>
<td>P(_{D})</td>
<td>Power dissipation at T(_{A}) = 85(^{\circ})C of BGA176</td>
<td>—</td>
<td>888</td>
<td>mW</td>
</tr>
<tr>
<td></td>
<td>Power dissipation at T(_{A}) = 85(^{\circ})C of LQFP144</td>
<td>—</td>
<td>820</td>
<td>mW</td>
</tr>
<tr>
<td></td>
<td>Power dissipation at T(_{A}) = 85(^{\circ})C of LQFP100</td>
<td>—</td>
<td>697</td>
<td>mW</td>
</tr>
<tr>
<td>T(_{STG})</td>
<td>Storage temperature range</td>
<td>-65</td>
<td>+150</td>
<td>(^{\circ})C</td>
</tr>
<tr>
<td>T(_{J})</td>
<td>Maximum junction temperature</td>
<td>—</td>
<td>125</td>
<td>(^{\circ})C</td>
</tr>
</tbody>
</table>

(1) Guaranteed by design, not tested in production.
(2) All main power and ground pins should be connected to an external power source within the allowable range.
(3) V\(_{IN}\) maximum value cannot exceed 6.5 V.
(4) It is recommended that V\(_{DD}\) and V\(_{DDA}\) are powered by the same source. The maximum difference between V\(_{DD}\) and V\(_{DDA}\) does not exceed 300 mV during power-up and operation.

4.2. Recommended DC characteristics

Table 4-2. DC operating conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min(^{(1)})</th>
<th>Typ</th>
<th>Max(^{(1)})</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V(_{DD})</td>
<td>Supply voltage</td>
<td>—</td>
<td>2.6</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>V(_{DDA})</td>
<td>Analog supply voltage</td>
<td>Same as V(_{DD})</td>
<td>2.6</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>V(_{BAT})</td>
<td>Battery supply voltage</td>
<td>—</td>
<td>1.8</td>
<td>—</td>
<td>3.6</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) Based on characterization, not tested in production.
Figure 4-1. Recommended power supply decoupling capacitors

(1) The \( V_{\text{REF}+} \) and \( V_{\text{REF}-} \) pins are only available on no less than 100-pin packages, or else the \( V_{\text{REF}+} \) and \( V_{\text{REF}-} \) pins are not available and internally connected to \( V_{\text{DDA}} \) and \( V_{\text{SSA}} \) pins.

(2) All decoupling capacitors need to be as close as possible to the pins on the PCB board.

Table 4-3. Clock frequency

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_{\text{HCLK}} )</td>
<td>AHB clock frequency</td>
<td>—</td>
<td>—</td>
<td>200</td>
<td>MHz</td>
</tr>
<tr>
<td>( f_{\text{APB1}} )</td>
<td>APB1 clock frequency</td>
<td>—</td>
<td>—</td>
<td>50</td>
<td>MHz</td>
</tr>
<tr>
<td>( f_{\text{APB2}} )</td>
<td>APB2 clock frequency</td>
<td>—</td>
<td>—</td>
<td>100</td>
<td>MHz</td>
</tr>
</tbody>
</table>

(1) Guaranteed by design, not tested in production.

Table 4-4. Operating conditions at Power up / Power down

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{\text{VDD}} )</td>
<td>( V_{\text{DD}} ) rise time rate</td>
<td>—</td>
<td>0</td>
<td>∞</td>
<td>µs/V</td>
</tr>
<tr>
<td></td>
<td>( V_{\text{DD}} ) fall time rate</td>
<td>—</td>
<td>20</td>
<td>∞</td>
<td>µs/V</td>
</tr>
</tbody>
</table>

(1) Guaranteed by design, not tested in production.

Table 4-5. Start-up timings of Operating conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typ</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{\text{start-up}} )</td>
<td>Start-up time</td>
<td>Clock source from HXTAL</td>
<td>143</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Clock source from IRC16M</td>
<td>143</td>
<td></td>
</tr>
</tbody>
</table>

(1) Based on characterization, not tested in production.
(2) After power-up, the start-up time is the time between the rising edge of NRST high and the main function.
(3) PLL is off.

Table 4-6. Power saving mode wakeup timings characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Typ</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{\text{Sleep}} )</td>
<td>Wakeup from Sleep mode</td>
<td>1.5</td>
<td>µs</td>
</tr>
<tr>
<td>( t_{\text{Deep-sleep}} )</td>
<td>Wakeup from Deep-sleep mode (LDO On)</td>
<td>3.3</td>
<td></td>
</tr>
</tbody>
</table>
4.3. Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

Table 4-7. Power consumption characteristics (2)(3)(4)(5)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ(1)</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>I&lt;sub&gt;DD&lt;/sub&gt;+I&lt;sub&gt;DDA&lt;/sub&gt;</td>
<td>Supply current (Run mode)</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = V&lt;sub&gt;DDA&lt;/sub&gt; = 3.3 V, HXTAL = 25 MHz, System clock = 200 MHz, All peripherals enabled</td>
<td>—</td>
<td>98.12</td>
<td>—</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = V&lt;sub&gt;DDA&lt;/sub&gt; = 3.3 V, HXTAL = 25 MHz, System clock = 200 MHz, All peripherals disabled</td>
<td>—</td>
<td>59.74</td>
<td>—</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = V&lt;sub&gt;DDA&lt;/sub&gt; = 3.3 V, HXTAL = 25 MHz, System clock = 180 MHz, All peripherals enabled</td>
<td>—</td>
<td>88.74</td>
<td>—</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = V&lt;sub&gt;DDA&lt;/sub&gt; = 3.3 V, HXTAL = 25 MHz, System clock = 180 MHz, All peripherals disabled</td>
<td>—</td>
<td>54.12</td>
<td>—</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = V&lt;sub&gt;DDA&lt;/sub&gt; = 3.3 V, HXTAL = 25 MHz, System clock = 120 MHz, All peripherals enabled</td>
<td>—</td>
<td>60.74</td>
<td>—</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = V&lt;sub&gt;DDA&lt;/sub&gt; = 3.3 V, HXTAL = 25 MHz, System clock = 120 MHz, All peripherals disabled</td>
<td>—</td>
<td>37.34</td>
<td>—</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = V&lt;sub&gt;DDA&lt;/sub&gt; = 3.3 V, HXTAL = 25 MHz, System clock = 108 MHz, All peripherals enabled</td>
<td>—</td>
<td>55.36</td>
<td>—</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = V&lt;sub&gt;DDA&lt;/sub&gt; = 3.3 V, HXTAL = 25 MHz, System clock = 108 MHz, All peripherals disabled</td>
<td>—</td>
<td>34.76</td>
<td>—</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = V&lt;sub&gt;DDA&lt;/sub&gt; = 3.3 V, HXTAL = 25 MHz, System clock = 90 MHz, All peripherals enabled</td>
<td>—</td>
<td>46.22</td>
<td>—</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = V&lt;sub&gt;DDA&lt;/sub&gt; = 3.3 V, HXTAL = 25 MHz, System clock = 90 MHz, All peripherals disabled</td>
<td>—</td>
<td>29.52</td>
<td>—</td>
<td>mA</td>
</tr>
</tbody>
</table>

(1) Based on characterization, not tested in production.
(2) The wakeup time is measured from the wakeup event to the point at which the application code reads the first instruction under the below conditions: V<sub>CC</sub> = V<sub>DDA</sub> = 3.3 V, IRC16M = System clock = 16 MHz.

(3)(4)(5) Based on characterization, not tested in production.
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ&lt;sup&gt;(1)&lt;/sup&gt;</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD} = V_{DDA} = 3.3$ V, HXTAL = 25 MHz, System clock = 60 MHz, All peripherals enabled</td>
<td></td>
<td></td>
<td>31.98</td>
<td></td>
<td>31.98</td>
<td>mA</td>
</tr>
<tr>
<td>$V_{DD} = V_{DDA} = 3.3$ V, HXTAL = 25 MHz, System clock = 60 MHz, All peripherals disabled</td>
<td></td>
<td></td>
<td>20.64</td>
<td></td>
<td>20.64</td>
<td>mA</td>
</tr>
<tr>
<td>$V_{DD} = V_{DDA} = 3.3$ V, HXTAL = 25 MHz, System clock = 30 MHz, All peripherals enabled</td>
<td></td>
<td></td>
<td>18.06</td>
<td></td>
<td>18.06</td>
<td>mA</td>
</tr>
<tr>
<td>$V_{DD} = V_{DDA} = 3.3$ V, HXTAL = 25 MHz, System clock = 30 MHz, All peripherals disabled</td>
<td></td>
<td></td>
<td>12.16</td>
<td></td>
<td>12.16</td>
<td>mA</td>
</tr>
<tr>
<td>$V_{DD} = V_{DDA} = 3.3$ V, IRC16M = 16 MHz, System clock = 25 MHz, All peripherals enabled</td>
<td></td>
<td></td>
<td>14.40</td>
<td></td>
<td>14.40</td>
<td>mA</td>
</tr>
<tr>
<td>$V_{DD} = V_{DDA} = 3.3$ V, IRC16M = 16 MHz, System clock = 25 MHz, All peripherals disabled</td>
<td></td>
<td></td>
<td>9.48</td>
<td></td>
<td>9.48</td>
<td>mA</td>
</tr>
<tr>
<td>$V_{DD} = V_{DDA} = 3.3$ V, IRC16M = 16 MHz, System clock = 16 MHz, All peripherals enabled</td>
<td></td>
<td></td>
<td>10.10</td>
<td></td>
<td>10.10</td>
<td>mA</td>
</tr>
<tr>
<td>$V_{DD} = V_{DDA} = 3.3$ V, IRC16M = 16 MHz, System clock = 16 MHz, All peripherals disabled</td>
<td></td>
<td></td>
<td>6.96</td>
<td></td>
<td>6.96</td>
<td>mA</td>
</tr>
<tr>
<td>$V_{DD} = V_{DDA} = 3.3$ V, IRC16M = 16 MHz, System clock = 8 MHz, All peripherals enabled</td>
<td></td>
<td></td>
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<td>6.38</td>
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<td>Conditions</td>
<td>Min</td>
<td>Typ$^{(1)}$</td>
<td>Max</td>
<td>Unit</td>
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<td>66.50</td>
<td>— mA</td>
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<td>$V_{DD} = V_{DDA} = 3.3 , V$, HXTAL = 25 MHz, System clock = 200 MHz, CPU clock off, All peripherals disabled</td>
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<td>28.96</td>
<td>— mA</td>
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<td>60.26</td>
<td>— mA</td>
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<td>— mA</td>
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<tr>
<td>$V_{DD} = V_{DDA} = 3.3 , V$, HXTAL = 25 MHz, System clock = 108 MHz, CPU clock off, All peripherals enabled</td>
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<td>— mA</td>
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<td>17.96</td>
<td>— mA</td>
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<td>$V_{DD} = V_{DDA} = 3.3 , V$, HXTAL = 25 MHz, System clock = 90 MHz, CPU clock off, All peripherals enabled</td>
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<td>31.94</td>
<td>— mA</td>
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<td>$V_{DD} = V_{DDA} = 3.3 , V$, HXTAL = 25 MHz, System clock = 90 MHz, CPU clock off, All peripherals disabled</td>
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<td>14.94</td>
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<td>— mA</td>
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<td>13.34</td>
<td>— mA</td>
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<td>$V_{DD} = V_{DDA} = 3.3 , V$, HXTAL = 25 MHz, System clock = 30 MHz, CPU clock off, All peripherals disabled</td>
<td>—</td>
<td>7.58</td>
<td>— mA</td>
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**Supply current (Sleep mode)**
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<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ&lt;sup&gt;(1)&lt;/sup&gt;</th>
<th>Max</th>
<th>Unit</th>
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<tbody>
<tr>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = V&lt;sub&gt;DDA&lt;/sub&gt; = 3.3 V, IRC16M = 16 MHz, System clock = 25 MHz, CPU clock off, All peripherals enabled</td>
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<td>10.52</td>
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<td>—</td>
<td>mA</td>
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<td>5.70</td>
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<td>mA</td>
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<td>—</td>
<td>—</td>
<td>mA</td>
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<td>V&lt;sub&gt;DD&lt;/sub&gt; = V&lt;sub&gt;DDA&lt;/sub&gt; = 3.3 V, IRC16M = 16 MHz, System clock = 8 MHz, CPU clock off, All peripherals enabled</td>
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<td>5.18</td>
<td>—</td>
<td>—</td>
<td>mA</td>
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</tr>
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<td>V&lt;sub&gt;DD&lt;/sub&gt; = V&lt;sub&gt;DDA&lt;/sub&gt; = 3.3 V, IRC16M = 16 MHz, System clock = 8 MHz, CPU clock off, All peripherals disabled</td>
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<td>3.58</td>
<td>—</td>
<td>—</td>
<td>mA</td>
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<td>3.78</td>
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<td>—</td>
<td>mA</td>
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<td>—</td>
<td>3.00</td>
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<td>—</td>
<td>mA</td>
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<td>V&lt;sub&gt;DD&lt;/sub&gt; = V&lt;sub&gt;DDA&lt;/sub&gt; = 3.3 V, IRC16M = 16 MHz, System clock = 2 MHz, CPU clock off, All peripherals enabled</td>
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<td>3.14</td>
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<td>mA</td>
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<td>2.74</td>
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<td>mA</td>
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<td>V&lt;sub&gt;DD&lt;/sub&gt; = V&lt;sub&gt;DDA&lt;/sub&gt; = 3.3 V, LDO in normal power and normal driver mode, IRC32K off, RTC off, All GPIOs analog mode</td>
<td>—</td>
<td>1.21</td>
<td>11</td>
<td>11</td>
<td>mA</td>
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<td>V&lt;sub&gt;DD&lt;/sub&gt; = V&lt;sub&gt;DDA&lt;/sub&gt; = 3.3 V, LDO in normal power and low driver mode, IRC32K off, RTC off, All GPIOs analog mode</td>
<td>—</td>
<td>1.18</td>
<td>11</td>
<td>11</td>
<td>mA</td>
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<tr>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = V&lt;sub&gt;DDA&lt;/sub&gt; = 3.3 V, LDO in low power and normal driver mode, IRC32K off, RTC off, All GPIOs analog mode</td>
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<td>0.83</td>
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<td>11</td>
<td>mA</td>
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<td>V&lt;sub&gt;DD&lt;/sub&gt; = V&lt;sub&gt;DDA&lt;/sub&gt; = 3.3 V, LDO in low power and low driver mode, IRC32K off, RTC off, All GPIOs analog mode</td>
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<td>Conditions</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
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<td>-------</td>
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<tr>
<td></td>
<td>Supply current (Standby mode)</td>
<td>$V_{DD} = V_{DDA} = 3.3, \text{V}, \text{LXTAL} \text{ off, IRC32K on, RTC on SRAM ON}$</td>
<td>$-$</td>
<td>$6.84$</td>
<td>$16.5$</td>
<td>$\mu\text{A}$</td>
</tr>
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<td>$V_{DD} = V_{DDA} = 3.3, \text{V}, \text{LXTAL} \text{ off, IRC32K on, RTC off SRAM ON}$</td>
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<td>$6.50$</td>
<td>$16.5$</td>
<td>$\mu\text{A}$</td>
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<tr>
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<td>$V_{DD} = V_{DDA} = 3.3, \text{V}, \text{LXTAL} \text{ off, IRC32K off, RTC off SRAM ON}$</td>
<td>$-$</td>
<td>$5.92$</td>
<td>$16.5$</td>
<td>$\mu\text{A}$</td>
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<td>$V_{DD} = V_{DDA} = 3.3, \text{V}, \text{LXTAL} \text{ off, IRC32K on, RTC off SRAM OFF}$</td>
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<td>$5.22$</td>
<td>$16.5$</td>
<td>$\mu\text{A}$</td>
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<td>$V_{DD} = V_{DDA} = 3.3, \text{V}, \text{LXTAL} \text{ off, IRC32K on, RTC off SRAM OFF}$</td>
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<td>$4.87$</td>
<td>$16.5$</td>
<td>$\mu\text{A}$</td>
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<td>$V_{DD} = V_{DDA} = 3.3, \text{V}, \text{LXTAL} \text{ off, IRC32K off, RTC off SRAM OFF}$</td>
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<td>$4.30$</td>
<td>$16.5$</td>
<td>$\mu\text{A}$</td>
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<td></td>
<td>Battery supply current (Backup mode)</td>
<td>$V_{DD} \text{ off, } V_{DDA} \text{ off, } V_{BAT} = 3.6, \text{V}, \text{LXTAL on with external crystal, RTC on, LXTAL High driving SRAM ON}$</td>
<td>$-$</td>
<td>$3.84$</td>
<td>$-$</td>
<td>$\mu\text{A}$</td>
</tr>
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<td>$V_{DD} \text{ off, } V_{DDA} \text{ off, } V_{BAT} = 3.3, \text{V}, \text{LXTAL on with external crystal, RTC on, LXTAL High driving SRAM ON}$</td>
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<td>$3.46$</td>
<td>$-$</td>
<td>$\mu\text{A}$</td>
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<td>$V_{DD} \text{ off, } V_{DDA} \text{ off, } V_{BAT} = 2.6, \text{V}, \text{LXTAL on with external crystal, RTC on, LXTAL High driving SRAM ON}$</td>
<td>$-$</td>
<td>$3.26$</td>
<td>$-$</td>
<td>$\mu\text{A}$</td>
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<td>$V_{DD} \text{ off, } V_{DDA} \text{ off, } V_{BAT} = 3.6, \text{V}, \text{LXTAL on with external crystal, RTC on, LXTAL High driving SRAM OFF}$</td>
<td>$-$</td>
<td>$1.99$</td>
<td>$-$</td>
<td>$\mu\text{A}$</td>
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<td>$V_{DD} \text{ off, } V_{DDA} \text{ off, } V_{BAT} = 3.3, \text{V}, \text{LXTAL on with external crystal, RTC on, LXTAL High driving SRAM OFF}$</td>
<td>$-$</td>
<td>$1.82$</td>
<td>$-$</td>
<td>$\mu\text{A}$</td>
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<td>$V_{DD} \text{ off, } V_{DDA} \text{ off, } V_{BAT} = 2.6, \text{V}, \text{LXTAL on with external crystal, RTC on, LXTAL High driving, SRAM OFF}$</td>
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<td>$1.52$</td>
<td>$-$</td>
<td>$\mu\text{A}$</td>
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<td>$V_{DD} \text{ off, } V_{DDA} \text{ off, } V_{BAT} = 3.6, \text{V}, \text{LXTAL on with external crystal, RTC on, LXTAL Low driving, SRAM ON}$</td>
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<td>$3.20$</td>
<td>$-$</td>
<td>$\mu\text{A}$</td>
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<td>$V_{DD} \text{ off, } V_{DDA} \text{ off, } V_{BAT} = 2.6, \text{V}, \text{LXTAL on with external crystal, RTC on, LXTAL Low driving, SRAM ON}$</td>
<td>$-$</td>
<td>$2.90$</td>
<td>$-$</td>
<td>$\mu\text{A}$</td>
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<td>$V_{DD} \text{ off, } V_{DDA} \text{ off, } V_{BAT} = 2.6, \text{V}, \text{LXTAL on with external crystal, RTC on, LXTAL Low driving, SRAM ON}$</td>
<td>$-$</td>
<td>$2.65$</td>
<td>$-$</td>
<td>$\mu\text{A}$</td>
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<td>Symbol</td>
<td>Parameter</td>
<td>Conditions</td>
<td>Conditions</td>
<td>Min</td>
<td>Typ(1)</td>
<td>Max</td>
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<td>------------</td>
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<tr>
<td>VDD off, VDDA off, VBAT = 3.6 V, LXTAL on with external crystal, RTC on, LXTAL Low driving, SRAM OFF</td>
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<td>1.36</td>
<td>—</td>
<td>μA</td>
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<td>VDD off, VDDA off, VBAT = 3.3 V, LXTAL on with external crystal, RTC on, LXTAL Low driving, SRAM OFF</td>
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<td>1.25</td>
<td>—</td>
<td>μA</td>
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<tr>
<td>VDD off, VDDA off, VBAT = 2.6 V, LXTAL on with external crystal, RTC on, LXTAL Low driving, SRAM OFF</td>
<td>—</td>
<td>0.91</td>
<td>—</td>
<td>μA</td>
<td></td>
<td></td>
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<tr>
<td>VDD off, VDDA off, VBAT = 3.6 V, LXTAL off with external crystal, RTC on, SRAM ON</td>
<td>—</td>
<td>1.98</td>
<td>—</td>
<td>μA</td>
<td></td>
<td></td>
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<tr>
<td>VDD off, VDDA off, VBAT = 3.3 V, LXTAL off with external crystal, RTC on, SRAM ON</td>
<td>—</td>
<td>1.82</td>
<td>—</td>
<td>μA</td>
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<td>VDD off, VDDA off, VBAT = 2.6 V, LXTAL off with external crystal, RTC on, SRAM ON</td>
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<td>1.75</td>
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<td>μA</td>
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<td>VDD off, VDDA off, VBAT = 3.6 V, LXTAL off with external crystal, RTC on, SRAM OFF</td>
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<td>0.13</td>
<td>—</td>
<td>μA</td>
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<tr>
<td>VDD off, VDDA off, VBAT = 3.3 V, LXTAL off with external crystal, RTC on, SRAM OFF</td>
<td>—</td>
<td>0.04</td>
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<td>μA</td>
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<td>—</td>
<td>0</td>
<td>—</td>
<td>μA</td>
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</table>

(1) Based on characterization, not tested in production.
(2) Unless otherwise specified, all values given for T_A = 25 °C and test result is mean value.
(3) When System Clock is less than 4 MHz, an external source is used, and the HXTAL bypass function is needed, no PLL.
(4) When System Clock is greater than 8 MHz, a crystal 8 MHz is used, and the HXTAL bypass function is closed, using PLL.
(5) When analog peripheral blocks such as ADCs, DACs, HXTAL, LXTAL, IRC16M, or IRC32K are ON, an additional power consumption should be considered.
Figure 4-2. Typical supply current consumption in Run mode

Figure 4-3. Typical supply current consumption in Sleep mode

Table 4-8. Peripheral current consumption characteristics(1)
## Peripherals

### Typical consumption at $T_A = 25\ ^\circ\text{C}$ (TYP)

<table>
<thead>
<tr>
<th>Peripherals</th>
<th>Unit</th>
</tr>
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<tbody>
<tr>
<td>USB_ULPI + USB_HS</td>
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<td>ETH_MAC + ETH_MAC_TX + ETH_MAC_RX + ETH_MAC_PTP</td>
<td>6.66</td>
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<td>IPA</td>
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<td>DMA1</td>
<td>3.32</td>
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<td>DMA0</td>
<td>3.36</td>
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<td>TCMSRAM</td>
<td>1.04</td>
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<tr>
<td>BKPSRAM</td>
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<td>CRC</td>
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<td>GPIOA</td>
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<td>GPIOB</td>
<td>0.59</td>
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<td>GPIOC</td>
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<td>GPIOD</td>
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<tr>
<td>GPIOE</td>
<td>0.61</td>
</tr>
<tr>
<td>GPIOF</td>
<td>0.59</td>
</tr>
<tr>
<td>GPIOG</td>
<td>0.60</td>
</tr>
<tr>
<td>GPIOH</td>
<td>0.60</td>
</tr>
<tr>
<td>GPIOI</td>
<td>0.57</td>
</tr>
<tr>
<td>USB_FS</td>
<td>3.33</td>
</tr>
<tr>
<td>TRNG</td>
<td>1.01</td>
</tr>
<tr>
<td>DCI</td>
<td>1.25</td>
</tr>
<tr>
<td>EXMC</td>
<td>4.29</td>
</tr>
<tr>
<td>UART7</td>
<td>0.87</td>
</tr>
<tr>
<td>UART6</td>
<td>0.06</td>
</tr>
<tr>
<td>DAC1+DAC2(2)</td>
<td>5.35</td>
</tr>
<tr>
<td>PMU</td>
<td>0.3</td>
</tr>
<tr>
<td>CAN1</td>
<td>0.26</td>
</tr>
<tr>
<td>CAN0</td>
<td>0.3</td>
</tr>
<tr>
<td>I2C2</td>
<td>0.16</td>
</tr>
<tr>
<td>I2C1</td>
<td>0.17</td>
</tr>
<tr>
<td>I2C0</td>
<td>0.18</td>
</tr>
<tr>
<td>UART4</td>
<td>0.13</td>
</tr>
<tr>
<td>UART3</td>
<td>0.1</td>
</tr>
<tr>
<td>USART2</td>
<td>0.19</td>
</tr>
<tr>
<td>USART1</td>
<td>0.17</td>
</tr>
<tr>
<td>SPI2/I2S2(3)</td>
<td>0.06/0.12</td>
</tr>
<tr>
<td>SPI1/I2S1(3)</td>
<td>0.06/0.16</td>
</tr>
<tr>
<td>WWDG</td>
<td>0.92</td>
</tr>
<tr>
<td>TIMER13</td>
<td>0.92</td>
</tr>
<tr>
<td>TIMER12</td>
<td>1.01</td>
</tr>
</tbody>
</table>
### 4.4. EMC characteristics

EMS (electromagnetic susceptibility) includes ESD (Electrostatic discharge, positive and negative) and FTB (Burst of Fast Transient voltage, positive and negative) testing result is given in Table 4-9, EMS characteristics(1), based on the EMS levels and classes compliant with IEC 61000 series standard.

(1) Based on characterization, not tested in production.
(2) DEN0 and DEN1 bits in the DAC_CTL register are set to 1, and the converted value set to 0x800.
(3) Enable SPIx CLKEN, I2SSSEL bit and I2SEN bit set to 1 in SPI_I2SCTL.
(4) System clock = f_HCLK = 200 MHz, f_APB1 = f_HCLK/4, f_APB2 = f_HCLK/2, f_ADCCLK = f_APB1/4, ADON bit is set to 1.
(5) If there is no other description, then VDD = VDDA = 3.3 V, HXTAL = 25 MHz, system clock = f_HCLK = 200 MHz, f_APB1 = f_HCLK/4, f_APB2 = f_HCLK/2.
Table 4-9. EMS characteristics(1)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Level/Class</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{ESD}</td>
<td>Voltage applied to all device pins to induce a functional disturbance</td>
<td>V_{DD} = 3.3 V, T_{A} = 25 °C LQFP144, f_{HCLK} = 168 MHz conforms to IEC 61000-4-2</td>
<td>3A</td>
</tr>
<tr>
<td>V_{FTB}</td>
<td>Fast transient voltage burst applied to induce a functional disturbance through 100 pF on V_{DD} and V_{SS} pins</td>
<td>V_{DD} = 3.3 V, T_{A} = 25 °C LQFP144, f_{HCLK} = 168 MHz conforms to IEC 61000-4-4</td>
<td>3A</td>
</tr>
</tbody>
</table>

(1) Based on characterization, not tested in production.

4.5. Power supply supervisor characteristics

Table 4-10. Power supply supervisor characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{LVD}(1)</td>
<td>Low voltage Detector level selection</td>
<td>LVDT&lt;2:0&gt; = 000(rising edge)</td>
<td>—</td>
<td>2.15</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVDT&lt;2:0&gt; = 000(falling edge)</td>
<td>—</td>
<td>2.04</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVDT&lt;2:0&gt; = 001(rising edge)</td>
<td>—</td>
<td>2.28</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVDT&lt;2:0&gt; = 001(falling edge)</td>
<td>—</td>
<td>2.17</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVDT&lt;2:0&gt; = 010(rising edge)</td>
<td>—</td>
<td>2.43</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVDT&lt;2:0&gt; = 010(falling edge)</td>
<td>—</td>
<td>2.31</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVDT&lt;2:0&gt; = 011(rising edge)</td>
<td>—</td>
<td>2.56</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVDT&lt;2:0&gt; = 011(falling edge)</td>
<td>—</td>
<td>2.45</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVDT&lt;2:0&gt; = 100(rising edge)</td>
<td>—</td>
<td>2.7</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVDT&lt;2:0&gt; = 100(falling edge)</td>
<td>—</td>
<td>2.59</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVDT&lt;2:0&gt; = 101(rising edge)</td>
<td>—</td>
<td>2.84</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVDT&lt;2:0&gt; = 101(falling edge)</td>
<td>—</td>
<td>2.73</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVDT&lt;2:0&gt; = 110(rising edge)</td>
<td>—</td>
<td>2.98</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVDT&lt;2:0&gt; = 110(falling edge)</td>
<td>—</td>
<td>2.87</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVDT&lt;2:0&gt; = 111(rising edge)</td>
<td>—</td>
<td>3.12</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVDT&lt;2:0&gt; = 111(falling edge)</td>
<td>—</td>
<td>3.01</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>V_{LVDhyst}(2)</td>
<td>LVD hysteresis</td>
<td>—</td>
<td>—</td>
<td>100</td>
<td>—</td>
<td>mV</td>
</tr>
<tr>
<td>V_{POR}(1)</td>
<td>Power on reset threshold</td>
<td>—</td>
<td>2.30</td>
<td>2.40</td>
<td>2.48</td>
<td>V</td>
</tr>
<tr>
<td>V_{PDR}(1)</td>
<td>Power down reset threshold</td>
<td>—</td>
<td>1.72</td>
<td>1.80</td>
<td>1.88</td>
<td>V</td>
</tr>
</tbody>
</table>
4.6. Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up (LU) test is based on the two measurement methods.

Table 4-11. ESD characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;ESD(HBM)&lt;/sub&gt;</td>
<td>Electrostatic discharge voltage (human body model)</td>
<td>T&lt;sub&gt;A&lt;/sub&gt; = 25 °C; JESD22-A114</td>
<td>—</td>
<td>—</td>
<td>7000</td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;ESD(CDM)&lt;/sub&gt;</td>
<td>Electrostatic discharge voltage (charge device model)</td>
<td>T&lt;sub&gt;A&lt;/sub&gt; = 25 °C; JESD22-C101</td>
<td>—</td>
<td>—</td>
<td>800</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) Based on characterization, not tested in production.

Table 4-12. Static latch-up characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>LU</td>
<td>I-test</td>
<td>T&lt;sub&gt;A&lt;/sub&gt; = 25 °C; JESD78</td>
<td>—</td>
<td>—</td>
<td>±200</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;supply&lt;/sub&gt; over voltage</td>
<td></td>
<td>—</td>
<td>—</td>
<td>5.4</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) Based on characterization, not tested in production.

4.7. External clock characteristics

Table 4-13. High speed external clock (HXTAL) generated from a crystal/ceramic
### Table 4-14. High speed external clock characteristics (HXTAL in bypass mode)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_{\text{HXTAL}} )(^{(1)} )</td>
<td>Crystal or ceramic frequency</td>
<td>2.6 V ( \leq V_{\text{DD}} \leq 3.6 ) V</td>
<td>1</td>
<td>—</td>
<td>50</td>
<td>MHz</td>
</tr>
<tr>
<td>( R_s )(^{(2)} )</td>
<td>Feedback resistor</td>
<td>( V_{\text{DD}} = 3.3 ) V</td>
<td>—</td>
<td>400</td>
<td>—</td>
<td>kΩ</td>
</tr>
<tr>
<td>( C_{\text{HXTAL}} )(^{(2)}(^{(3)} )</td>
<td>Recommended matching capacitance on OSCIN and OSCOUT</td>
<td>—</td>
<td>—</td>
<td>20</td>
<td>30</td>
<td>pF</td>
</tr>
<tr>
<td>( \text{Ducy}_{\text{HXTAL}} )(^{(2)} )</td>
<td>Crystal or ceramic duty cycle</td>
<td>—</td>
<td>30</td>
<td>50</td>
<td>70</td>
<td>%</td>
</tr>
<tr>
<td>( g_m )(^{(2)} )</td>
<td>Oscillator transconductance</td>
<td>Startup</td>
<td>—</td>
<td>25</td>
<td>—</td>
<td>mA/V</td>
</tr>
<tr>
<td>( I_{\text{DDHXTAL}} )(^{(1)} )</td>
<td>Crystal or ceramic operating current</td>
<td>( V_{\text{DD}} = 3.3 ) V, ( f_{\text{HCLK}} = f_{\text{IRC16M}} = 16 ) MHz</td>
<td>—</td>
<td>1</td>
<td>—</td>
<td>mA</td>
</tr>
<tr>
<td>( t_{\text{SUHXTAL}} )(^{(1)} )</td>
<td>Crystal or ceramic startup time</td>
<td>( V_{\text{DD}} = 3.3 ) V, ( f_{\text{HCLK}} = f_{\text{IRC16M}} = 16 ) MHz</td>
<td>—</td>
<td>1.8</td>
<td>—</td>
<td>ms</td>
</tr>
</tbody>
</table>

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) \( C_{\text{HXTAL}} = C_{\text{HXTAL2}} = 2*(C_{\text{LOAD}} - C_s) \). For \( C_{\text{HXTAL1}} \) and \( C_{\text{HXTAL2}} \), it is recommended matching capacitance on OSCIN and OSCOUT. For \( C_{\text{LOAD}} \), it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For \( C_s \), it is PCB and MCU pin stray capacitance.

### Table 4-15. Low speed external clock (LXTAL) generated from a crystal/ceramic

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_{\text{HXTAL}_{\text{ext}}} )(^{(1)} )</td>
<td>External clock source or oscillator frequency</td>
<td>2.6 V ( \leq V_{\text{DD}} \leq 3.6 ) V</td>
<td>1</td>
<td>—</td>
<td>50</td>
<td>MHz</td>
</tr>
<tr>
<td>( V_{\text{HXTALH}} )(^{(2)} )</td>
<td>OSCIN input pin high level voltage</td>
<td>( V_{\text{DD}} = 3.3 ) V</td>
<td>0.7</td>
<td>—</td>
<td>( V_{\text{DD}} ) V</td>
<td>V</td>
</tr>
<tr>
<td>( V_{\text{HXTALL}} )(^{(2)} )</td>
<td>OSCIN input pin low level voltage</td>
<td>( V_{\text{SS}} )</td>
<td>—</td>
<td>0.3</td>
<td>( V_{\text{DD}} ) V</td>
<td>V</td>
</tr>
<tr>
<td>( t_{\text{HL(HXTAL)}} )(^{(2)} )</td>
<td>OSCIN high or low time</td>
<td>—</td>
<td>5</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{\text{DF(HXTAL)}} )(^{(2)} )</td>
<td>OSCIN rise or fall time</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>( C_{\text{IN}} )(^{(2)} )</td>
<td>OSCIN input capacitance</td>
<td>—</td>
<td>—</td>
<td>5</td>
<td>—</td>
<td>pF</td>
</tr>
<tr>
<td>( \text{Ducy}_{\text{HXTAL}} )(^{(2)} )</td>
<td>Duty cycle</td>
<td>—</td>
<td>40</td>
<td>—</td>
<td>60</td>
<td>%</td>
</tr>
</tbody>
</table>

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
Table 4-16. Low speed external user clock characteristics (LXTAL in bypass mode)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>f_LXTAL_ext(1)</td>
<td>External clock source or oscillator frequency</td>
<td>V_DD = 3.3 V</td>
<td>—</td>
<td>32.768</td>
<td>—</td>
<td>kHz</td>
</tr>
<tr>
<td>V_LXTALH(2)</td>
<td>OSC32IN input pin high level voltage</td>
<td>—</td>
<td>0.7 V_DD</td>
<td>—</td>
<td>V_DD</td>
<td>V</td>
</tr>
<tr>
<td>V_LXTALL(2)</td>
<td>OSC32IN input pin low level voltage</td>
<td>—</td>
<td>V_SS</td>
<td>—</td>
<td>0.3 V_DD</td>
<td></td>
</tr>
<tr>
<td>t_H/LXTA(2)</td>
<td>OSC32IN high or low time</td>
<td>—</td>
<td>450 ns</td>
<td>—</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>t_R/F(LXTAL)(2)</td>
<td>OSC32IN rise or fall time</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>50 ns</td>
<td></td>
</tr>
<tr>
<td>C_IN(2)</td>
<td>OSC32IN input capacitance</td>
<td>—</td>
<td>—</td>
<td>5 pF</td>
<td>—</td>
<td>pF</td>
</tr>
<tr>
<td>DQ(y(LXTAL)(2)</td>
<td>Duty cycle</td>
<td>—</td>
<td>30</td>
<td>50</td>
<td>70</td>
<td>%</td>
</tr>
</tbody>
</table>

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) C_LXTAL = C_LXTAL2 = 2*(C_LOAD - C_S). For C_LXTAL and C_LXTAL2, it is recommended matching capacitance on OSC32IN and OSC32OUT. For C LOAD, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.
(4) t_SULXTAL is the startup time measured from the moment it is enabled (by software) to the 32.768 kHz oscillator stabilization flags is SET. This value varies significantly with the crystal manufacturer.
## 4.8. Internal clock characteristics

### Table 4-17. High speed internal clock (IRC16M) characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{IRC16M}$</td>
<td>High Speed Internal Oscillator (IRC16M) frequency</td>
<td>$V_{DD} = V_{DDA} = 3.3,\text{V}$</td>
<td>—</td>
<td>16</td>
<td>—</td>
<td>MHz</td>
</tr>
<tr>
<td>ACCIRC16M</td>
<td>IRC16M oscillator Frequency accuracy, Factory-trimmed</td>
<td>$V_{DD} = V_{DDA} = 3.3,\text{V}$, $T_A = -40,^\circ\text{C} \sim +85,^\circ\text{C}$&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>-4.0</td>
<td>—</td>
<td>+5.0</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td>IRC16M oscillator Frequency accuracy, Factory-trimmed</td>
<td>$V_{DD} = V_{DDA} = 3.3,\text{V}$, $T_A = 0,^\circ\text{C} \sim +85,^\circ\text{C}$&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>-2.0</td>
<td>—</td>
<td>+2.0</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td>IRC16M oscillator Frequency accuracy, Factory-trimmed</td>
<td>$V_{DD} = V_{DDA} = 3.3,\text{V}$, $T_A = 25,^\circ\text{C}$&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>-1.0</td>
<td>—</td>
<td>+1.0</td>
<td>%</td>
</tr>
<tr>
<td>DucyIRC16M&lt;sup&gt;(2)&lt;/sup&gt;</td>
<td>IRC16M oscillator duty cycle</td>
<td>$V_{DD} = V_{DDA} = 3.3,\text{V}$</td>
<td>45</td>
<td>50</td>
<td>55</td>
<td>%</td>
</tr>
<tr>
<td>IODARIRC16M&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>IRC16M oscillator operating current</td>
<td>$V_{DD} = V_{DDA} = 3.3,\text{V}$, $f_{HCLK} = f_{HXTAL_PLL} = 200,\text{MHz}$</td>
<td>—</td>
<td>66</td>
<td>80</td>
<td>μA</td>
</tr>
<tr>
<td>fSUIRC16M&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>IRC16M oscillator startup time</td>
<td>$V_{DD} = V_{DDA} = 3.3,\text{V}$, $f_{HCLK} = f_{HXTAL_PLL} = 200,\text{MHz}$</td>
<td>—</td>
<td>2.5</td>
<td>4</td>
<td>μs</td>
</tr>
</tbody>
</table>

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
Table 4-18. High speed internal clock (IRC48M) characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>fIRC48M</td>
<td>High Speed Internal Oscillator (IRC48M) frequency</td>
<td>( V_{DD} = 3.3 , \text{V} )</td>
<td>—</td>
<td>48</td>
<td>—</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td>IRC48M oscillator Frequency accuracy, Factory-trimmed</td>
<td>( V_{DD} = V_{DDA} = 3.3 , \text{V} ), ( T_A = -40 , ^\circ \text{C} \sim +85 , ^\circ \text{C} )(^{(1)})</td>
<td>-4.0</td>
<td>—</td>
<td>+5.0</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td>IRC48M oscillator Frequency accuracy, User trimming step(^{(1)})</td>
<td></td>
<td>—</td>
<td>—</td>
<td>0.12</td>
<td>—%</td>
</tr>
<tr>
<td>DIRC48M(^{(2)})</td>
<td>IRC48M oscillator duty cycle</td>
<td>( V_{DD} = V_{DDA} = 3.3 , \text{V} )</td>
<td>45</td>
<td>50</td>
<td>55</td>
<td>%</td>
</tr>
<tr>
<td>IDDARC48M(^{(3)})</td>
<td>IRC48M oscillator operating current</td>
<td>( V_{DD} = V_{DDA} = 3.3 , \text{V} ), ( f_{HCLK} = f_{HXTAL_PLL} = 200 , \text{MHz} )</td>
<td>—</td>
<td>240</td>
<td>300</td>
<td>μA</td>
</tr>
<tr>
<td>tSUIRC48M(^{(1)})</td>
<td>IRC48M oscillator startup time</td>
<td>( V_{DD} = V_{DDA} = 3.3 , \text{V} ), ( f_{HCLK} = f_{HXTAL_PLL} = 200 , \text{MHz} )</td>
<td>—</td>
<td>2.5</td>
<td>4</td>
<td>μs</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Based on characterization, not tested in production.

\(^{(2)}\) Guaranteed by design, not tested in production.

Table 4-19. Low speed internal clock (IRC32K) characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>fIRC32K(^{(1)})</td>
<td>Low Speed Internal oscillator (IRC32K) frequency</td>
<td>( V_{DD} = V_{DDA} = 3.3 , \text{V} ), ( T_A = -40 , ^\circ \text{C} \sim +85 , ^\circ \text{C} )</td>
<td>20</td>
<td>32</td>
<td>45</td>
<td>kHz</td>
</tr>
<tr>
<td>IDDARC32K(^{(2)})</td>
<td>IRC32K oscillator operating current</td>
<td>( V_{DD} = V_{DDA} = 3.3 , \text{V} ), ( f_{HCLK} = f_{HXTAL_PLL} = 200 , \text{MHz} )</td>
<td>—</td>
<td>0.4</td>
<td>0.6</td>
<td>μA</td>
</tr>
<tr>
<td>tSUIRC32K(^{(2)})</td>
<td>IRC32K oscillator startup time</td>
<td>( V_{DD} = V_{DDA} = 3.3 , \text{V} ), ( f_{HCLK} = f_{HXTAL_PLL} = 200 , \text{MHz} )</td>
<td>—</td>
<td>110</td>
<td>150</td>
<td>μs</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Guaranteed by design, not tested in production.

\(^{(2)}\) Based on characterization, not tested in production.

4.9. PLL characteristics

Table 4-20. PLL characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>fPLLIN(^{(1)})</td>
<td>PLL input clock frequency</td>
<td>—</td>
<td>1</td>
<td>—</td>
<td>4</td>
<td>MHz</td>
</tr>
<tr>
<td>fPLLOUT(^{(2)})</td>
<td>PLL output clock frequency</td>
<td>—</td>
<td>100</td>
<td>500</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>fVCO(^{(2)})</td>
<td>PLL VCO output clock frequency</td>
<td>—</td>
<td>32</td>
<td>344</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>tLOCK(^{(2)})</td>
<td>PLL lock time</td>
<td>VCO freq = 100 MHz</td>
<td>80</td>
<td>168</td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>VCO freq = 500 MHz</td>
<td>100</td>
<td>300</td>
<td>μs</td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) Based on characterization, not tested in production.

\(^{(2)}\) Guaranteed by design, not tested in production.
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>fPLLIN(1)</td>
<td>PLL2S input clock frequency</td>
<td>—</td>
<td>1</td>
<td>—</td>
<td>4</td>
<td>MHz</td>
</tr>
<tr>
<td>fPLLOUT(2)</td>
<td>PLL2S output clock frequency</td>
<td>—</td>
<td>100</td>
<td>—</td>
<td>500</td>
<td>MHz</td>
</tr>
<tr>
<td>fVCO(2)</td>
<td>PLL2S VCO output clock frequency</td>
<td>—</td>
<td>32</td>
<td>—</td>
<td>344</td>
<td>MHz</td>
</tr>
<tr>
<td>tLOCK(2)</td>
<td>PLL2S lock time</td>
<td>VCO freq = 100 MHz</td>
<td>—</td>
<td>80</td>
<td>168</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VCO freq = 500 MHz</td>
<td>—</td>
<td>100</td>
<td>300</td>
<td>μs</td>
</tr>
<tr>
<td>fDDA(1)(3)</td>
<td>Current consumption on VDDA</td>
<td>VCO freq = 500 MHz</td>
<td>—</td>
<td>1100</td>
<td>—</td>
<td>μA</td>
</tr>
<tr>
<td>JitterPLL</td>
<td>Cycle to cycle Jitter (rms)</td>
<td>System clock</td>
<td>—</td>
<td>40</td>
<td>—</td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td>Cycle to cycle Jitter (peak to peak)</td>
<td>System clock</td>
<td>—</td>
<td>400</td>
<td>—</td>
<td>ps</td>
</tr>
</tbody>
</table>

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) System clock = IRC16M = 16 MHz, PLL clock source = IRC16M/2 = 8 MHz, fPLLOUT = 200 MHz.
(4) Value given with main PLL running.

### Table 4-22. PLLSAI characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>fPLLIN(1)</td>
<td>PLLSAI input clock frequency</td>
<td>—</td>
<td>1</td>
<td>—</td>
<td>4</td>
<td>MHz</td>
</tr>
<tr>
<td>fPLLOUT(2)</td>
<td>PLLSAI output clock frequency</td>
<td>—</td>
<td>100</td>
<td>—</td>
<td>500</td>
<td>MHz</td>
</tr>
<tr>
<td>fVCO(2)</td>
<td>PLLSAI VCO output clock frequency</td>
<td>—</td>
<td>32</td>
<td>—</td>
<td>344</td>
<td>MHz</td>
</tr>
<tr>
<td>tLOCK(2)</td>
<td>PLLSAI lock time</td>
<td>VCO freq = 100 MHz</td>
<td>—</td>
<td>80</td>
<td>168</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VCO freq = 500 MHz</td>
<td>—</td>
<td>100</td>
<td>300</td>
<td>μs</td>
</tr>
<tr>
<td>fDDA(1)(3)</td>
<td>Current consumption on VDDA</td>
<td>VCO freq = 500 MHz</td>
<td>—</td>
<td>1100</td>
<td>—</td>
<td>μA</td>
</tr>
<tr>
<td>JitterPLL</td>
<td>Cycle to cycle Jitter (rms)</td>
<td>System clock</td>
<td>—</td>
<td>40</td>
<td>—</td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td>Cycle to cycle Jitter (peak to peak)</td>
<td>System clock</td>
<td>—</td>
<td>400</td>
<td>—</td>
<td>ps</td>
</tr>
</tbody>
</table>

(1) Based on characterization, not tested in production.
Table 4-23. PLL spread spectrum clock generation (SSCG) characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>FMOD</td>
<td>Modulation frequency</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>KHz</td>
</tr>
<tr>
<td>Mdamp</td>
<td>Peak modulation amplitude</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>2</td>
<td>%</td>
</tr>
<tr>
<td>MODCNT*</td>
<td></td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>2^15.1</td>
<td></td>
</tr>
<tr>
<td>MODSTEP</td>
<td></td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td></td>
</tr>
</tbody>
</table>

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

**Equation 1**: SSCG configuration equation:

MODCNT = \( \text{round}\left(\frac{f_{PLLIN}}{4}\right)\)

MODSTEP = \( \text{round}\left(\text{mdamp} \times \frac{f_{PLLIN}}{2^{14}} / 100\right)\)

The formula above (Equation 1) is SSCG configuration equation.

### 4.10. Memory characteristics

Table 4-24. Flash memory characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min(^{(1)})</th>
<th>Typ(^{(1)})</th>
<th>Max(^{(2)})</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>PE(_{CYC})</td>
<td>Number of guaranteed program / erase cycles before failure (Endurance)</td>
<td>(T_A = -40 ^\circ C \sim +85 ^\circ C)</td>
<td>100</td>
<td>—</td>
<td>—</td>
<td>kcycles</td>
</tr>
<tr>
<td>t(_{RET})</td>
<td>Data retention time</td>
<td>—</td>
<td>—</td>
<td>20</td>
<td>—</td>
<td>years</td>
</tr>
<tr>
<td>t(_{PROG})</td>
<td>Word programming time</td>
<td>(T_A = -40 ^\circ C \sim +85 ^\circ C)</td>
<td>—</td>
<td>37.5</td>
<td>180</td>
<td>μs</td>
</tr>
<tr>
<td>t(_{ERASE16kB})</td>
<td>Sector(16kB) erase time</td>
<td>(T_A = -40 ^\circ C \sim +85 ^\circ C)</td>
<td>—</td>
<td>200</td>
<td>2000</td>
<td>ms</td>
</tr>
<tr>
<td>t(_{ERASE64kB})</td>
<td>Sector(64kB) erase time</td>
<td>(T_A = -40 ^\circ C \sim +85 ^\circ C)</td>
<td>—</td>
<td>300</td>
<td>4000</td>
<td>ms</td>
</tr>
<tr>
<td>t(_{ERASE128kB})</td>
<td>Sector(128kB) erase time</td>
<td>—</td>
<td>600</td>
<td>8000</td>
<td></td>
<td></td>
</tr>
<tr>
<td>t(_{ERASE512kB})</td>
<td>Mass erase time</td>
<td>(T_A = -40 ^\circ C \sim +85 ^\circ C)</td>
<td>—</td>
<td>2.4</td>
<td>32</td>
<td>s</td>
</tr>
<tr>
<td>t(_{ERASE1MB})</td>
<td>Mass erase time</td>
<td>(T_A = -40 ^\circ C \sim +85 ^\circ C)</td>
<td>—</td>
<td>4.8</td>
<td>64</td>
<td>s</td>
</tr>
<tr>
<td>t(_{ERASE2MB})</td>
<td>Mass erase time</td>
<td>(T_A = -40 ^\circ C \sim +85 ^\circ C)</td>
<td>—</td>
<td>9.6</td>
<td>128</td>
<td>s</td>
</tr>
<tr>
<td>t(_{ERASE3MB})</td>
<td>Mass erase time</td>
<td>(T_A = -40 ^\circ C \sim +85 ^\circ C)</td>
<td>—</td>
<td>14.4</td>
<td>192</td>
<td>s</td>
</tr>
</tbody>
</table>

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

### 4.11. NRST pin characteristics

Table 4-25. NRST pin characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{IL_NRST})(^{(1)})</td>
<td>NRST Input low level voltage</td>
<td>(V_{DD} = V_{DDA} = 2.6 \text{ V})</td>
<td>0.5</td>
<td>—</td>
<td>60</td>
<td>ηV</td>
</tr>
<tr>
<td>(V_{IH_NRST})(^{(1)})</td>
<td>NRST Input high level voltage</td>
<td>(0.7 \text{ V}<em>{DD} \sim V</em>{DD} + 0.5)</td>
<td>—</td>
<td>60</td>
<td>—</td>
<td>ηV</td>
</tr>
<tr>
<td>(V_{hyst})(^{(1)})</td>
<td>Schmidt trigger Voltage hysteresis</td>
<td>—</td>
<td>360</td>
<td>—</td>
<td>—</td>
<td>mV</td>
</tr>
<tr>
<td>(V_{IL_NRST})(^{(1)})</td>
<td>NRST Input low level voltage</td>
<td>(V_{DD} = V_{DDA} = 3.3 \text{ V})</td>
<td>0.5</td>
<td>—</td>
<td>60</td>
<td>ηV</td>
</tr>
</tbody>
</table>
### Table 4-26. I/O port DC characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IL}$</td>
<td>Standard IO Low level input voltage</td>
<td>$2.6 \text{ V} \leq V_{DD} = V_{DDA} \leq 3.6 \text{ V}$</td>
<td>—</td>
<td>—</td>
<td>0.3 $V_{DD}$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>5V-tolerant IO Low level input voltage</td>
<td>$2.6 \text{ V} \leq V_{DD} = V_{DDA} \leq 3.6 \text{ V}$</td>
<td>—</td>
<td>—</td>
<td>0.3 $V_{DD}$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Standard IO Low level input voltage</td>
<td>$2.6 \text{ V} \leq V_{DD} = V_{DDA} \leq 3.6 \text{ V}$</td>
<td>0.7 $V_{DD}$</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>5V-tolerant IO Low level input voltage</td>
<td>$2.6 \text{ V} \leq V_{DD} = V_{DDA} \leq 3.6 \text{ V}$</td>
<td>0.7 $V_{DD}$</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low level output voltage for an IO Pin ($I_O = +8 \text{ mA}$)</td>
<td>$V_{DD} = 2.6 \text{ V}$</td>
<td>—</td>
<td>—</td>
<td>0.17</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 3.3 \text{ V}$</td>
<td>—</td>
<td>—</td>
<td>0.16</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 3.6 \text{ V}$</td>
<td>—</td>
<td>—</td>
<td>0.16</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Low level output voltage for an IO Pin ($I_O = +20 \text{ mA}$)</td>
<td>$V_{DD} = 2.6 \text{ V}$</td>
<td>—</td>
<td>—</td>
<td>0.46</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 3.3 \text{ V}$</td>
<td>—</td>
<td>—</td>
<td>0.40</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 3.6 \text{ V}$</td>
<td>—</td>
<td>—</td>
<td>0.40</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>High level output voltage for an IO Pin ($I_O = +8 \text{ mA}$)</td>
<td>$V_{DD} = 2.6 \text{ V}$</td>
<td>2.39</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 3.3 \text{ V}$</td>
<td>3.12</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 3.6 \text{ V}$</td>
<td>3.41</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
</tbody>
</table>
If \((t_r + t_f) \leq 2/3 \, T\), then maximum frequency is achieved. The duty cycle is \((45\%-55\%)\) when loaded by 50 pF.

**Table 4-27. I/O port AC characteristics**

<table>
<thead>
<tr>
<th>GPIOx_OSPD[1:0] bit value (^{(3)})</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIOx_OSPD0-&gt;OSPDy[1:0] = 00 (IO_Speed = 2 MHz)</td>
<td>Maximum frequency (^{(4)})</td>
<td>(V_{DD} = 3.3 , V, , C_L = 10 , pF)</td>
<td>30</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_{DD} = 3.3 , V, , C_L = 30 , pF)</td>
<td>25</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_{DD} = 3.3 , V, , C_L = 50 , pF)</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>GPIOx_OSPD0-&gt;OSPDy[1:0] = 01 (IO_Speed = 25 MHz)</td>
<td>Maximum frequency (^{(4)})</td>
<td>(V_{DD} = 3.3 , V, , C_L = 10 , pF)</td>
<td>95</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_{DD} = 3.3 , V, , C_L = 30 , pF)</td>
<td>80</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_{DD} = 3.3 , V, , C_L = 50 , pF)</td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>GPIOx_OSPD0-&gt;OSPDy[1:0] = 10 (IO_Speed = 50 MHz)</td>
<td>Maximum frequency (^{(4)})</td>
<td>(V_{DD} = 3.3 , V, , C_L = 10 , pF)</td>
<td>160</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_{DD} = 3.3 , V, , C_L = 30 , pF)</td>
<td>125</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_{DD} = 3.3 , V, , C_L = 50 , pF)</td>
<td>90</td>
<td></td>
</tr>
<tr>
<td>GPIOx_OSPD0-&gt;OSPDy[1:0] = 11 (IO_Speed = 200 MHz)</td>
<td>Maximum frequency (^{(4)})</td>
<td>(V_{DD} = 3.3 , V, , C_L = 10 , pF)</td>
<td>200</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_{DD} = 3.3 , V, , C_L = 30 , pF)</td>
<td>170</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_{DD} = 3.3 , V, , C_L = 50 , pF)</td>
<td>130</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 4-5. I/O port AC characteristics definition**

- Based on characterization, not tested in production. 
- Guaranteed by design, not tested in production. 
- All pins except PC13 / PC14 / PC15 / P18. Since PC13 to PC15 and P18 are supplied through the Power Switch, which can only be obtained by a small current, the speed of GPIOs PC13 to PC15 and P18 should not exceed 2 MHz when they are in output mode (maximum load: 30 pF).
### 4.13. ADC characteristics

#### Table 4-28. ADC characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDDA(1)</td>
<td>Operating voltage</td>
<td>—</td>
<td>2.6</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>VIN(1)</td>
<td>ADC input voltage range</td>
<td>—</td>
<td>0</td>
<td>—</td>
<td>VREF+</td>
<td>V</td>
</tr>
<tr>
<td>VREF+,(2)</td>
<td>Positive Reference Voltage</td>
<td>—</td>
<td>2.6</td>
<td>—</td>
<td>VDDA</td>
<td>V</td>
</tr>
<tr>
<td>VREF-,(2)</td>
<td>Negative Reference Voltage</td>
<td>—</td>
<td>VSSA</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>fADC(1)</td>
<td>ADC clock</td>
<td>12-bit</td>
<td>0.007</td>
<td>—</td>
<td>2.6</td>
<td>MSP</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10-bit</td>
<td>0.008</td>
<td>—</td>
<td>3.1</td>
<td>S</td>
</tr>
<tr>
<td></td>
<td></td>
<td>8-bit</td>
<td>0.01</td>
<td>—</td>
<td>3.6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>6-bit</td>
<td>0.011</td>
<td>—</td>
<td>4.4</td>
<td></td>
</tr>
<tr>
<td>fS(1)</td>
<td>Sampling rate</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>12-bit</td>
<td>0.007</td>
<td>—</td>
<td>2.6</td>
<td>MSP</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10-bit</td>
<td>0.008</td>
<td>—</td>
<td>3.1</td>
<td>S</td>
</tr>
<tr>
<td></td>
<td></td>
<td>8-bit</td>
<td>0.01</td>
<td>—</td>
<td>3.6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>6-bit</td>
<td>0.011</td>
<td>—</td>
<td>4.4</td>
<td></td>
</tr>
<tr>
<td>VAIN(1)</td>
<td>Analog input voltage</td>
<td>16 external; 3 internal</td>
<td>0</td>
<td>—</td>
<td>VDDA</td>
<td>V</td>
</tr>
<tr>
<td>RAIN(2)</td>
<td>External input impedance</td>
<td>See Equation 2</td>
<td>—</td>
<td>—</td>
<td>52.1</td>
<td>kΩ</td>
</tr>
<tr>
<td>RADC(2)</td>
<td>Input sampling switch resistance</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>0.55</td>
<td>kΩ</td>
</tr>
<tr>
<td>CADC(2)</td>
<td>Input sampling capacitance</td>
<td>No pin/pad capacitance included</td>
<td>—</td>
<td>—</td>
<td>5.5</td>
<td>pF</td>
</tr>
<tr>
<td>tCAL(2)</td>
<td>Calibration time</td>
<td>fADC = 40 MHz</td>
<td>3.275</td>
<td>—</td>
<td>12</td>
<td>μs</td>
</tr>
<tr>
<td>tS(2)</td>
<td>Sampling time</td>
<td>fADC = 40 MHz</td>
<td>0.075</td>
<td>—</td>
<td>12</td>
<td>μs</td>
</tr>
<tr>
<td>tCONV(2)</td>
<td>Total conversion time (including sampling time)</td>
<td>12-bit</td>
<td>—</td>
<td>15</td>
<td>—</td>
<td>1/fADC</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10-bit</td>
<td>—</td>
<td>13</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>8-bit</td>
<td>—</td>
<td>11</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>6-bit</td>
<td>—</td>
<td>9</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>tSU(2)</td>
<td>Startup time</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>1</td>
<td>μs</td>
</tr>
</tbody>
</table>

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.

**Equation 2:** $R_{\text{AIN max}}$ formula

$$R_{\text{AIN max}} < \frac{T_s}{f_{\text{ADC}}C_{\text{ADC}}\ln(2^{N+2})} - R_{\text{ADC}}$$

The formula above (Equation 2) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here $N = 12$ (from 12-bit resolution).

#### Table 4-29. ADC RAIN max for $f_{\text{ADC}} = 40$ MHz(2)

<table>
<thead>
<tr>
<th>$T_s$ (cycles)</th>
<th>$T_s$ (μs)</th>
<th>$R_{\text{AIN max}}$ (KΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>0.075</td>
<td>0.85</td>
</tr>
<tr>
<td>15</td>
<td>0.375</td>
<td>6.5</td>
</tr>
<tr>
<td>28</td>
<td>0.7</td>
<td>12.6</td>
</tr>
<tr>
<td>55</td>
<td>1.375</td>
<td>25.2</td>
</tr>
<tr>
<td>84</td>
<td>2.1</td>
<td>38.8</td>
</tr>
<tr>
<td>112</td>
<td>2.8</td>
<td>51.9</td>
</tr>
<tr>
<td>144</td>
<td>3.6</td>
<td>N/A</td>
</tr>
<tr>
<td>480</td>
<td>12</td>
<td>N/A</td>
</tr>
</tbody>
</table>
Table 4-30. ADC dynamic accuracy at $f_{\text{ADC}} = 30 \, \text{MHz}^{(1)}$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>ENOB</td>
<td>Effective number of bits</td>
<td>$f_{\text{ADC}} = 30 , \text{MHz}$</td>
<td>10.5</td>
<td>10.6</td>
<td>—</td>
<td>bits</td>
</tr>
<tr>
<td>SNDR</td>
<td>Signal-to-noise and distortion ratio</td>
<td>$V_{\text{DDA}} = V_{\text{REF}+} = 2.6 , \text{V}$</td>
<td>65</td>
<td>65.6</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>SNR</td>
<td>Signal-to-noise ratio</td>
<td>Input Frequency = 110 kHz</td>
<td>65.5</td>
<td>66</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>THD</td>
<td>Total harmonic distortion</td>
<td>Temperature = 25 ℃</td>
<td>-74</td>
<td>-76</td>
<td>—</td>
<td></td>
</tr>
</tbody>
</table>

(1) Based on characterization, not tested in production.  
(2) Guaranteed by design, not tested in production.

Table 4-31. ADC dynamic accuracy at $f_{\text{ADC}} = 30 \, \text{MHz}^{(1)}$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>ENOB</td>
<td>Effective number of bits</td>
<td>$f_{\text{ADC}} = 30 , \text{MHz}$</td>
<td>10.7</td>
<td>10.8</td>
<td>—</td>
<td>bits</td>
</tr>
<tr>
<td>SNDR</td>
<td>Signal-to-noise and distortion ratio</td>
<td>$V_{\text{DDA}} = V_{\text{REF}+} = 3.3 , \text{V}$</td>
<td>66.2</td>
<td>65.8</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>SNR</td>
<td>Signal-to-noise ratio</td>
<td>Input Frequency = 110 kHz</td>
<td>66.8</td>
<td>67.4</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>THD</td>
<td>Total harmonic distortion</td>
<td>Temperature = 25 ℃</td>
<td>-71</td>
<td>-75</td>
<td>—</td>
<td></td>
</tr>
</tbody>
</table>

(1) Based on characterization, not tested in production.  
(2) Guaranteed by design, not tested in production.

Table 4-32. ADC dynamic accuracy at $f_{\text{ADC}} = 36 \, \text{MHz}^{(1)}$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>ENOB</td>
<td>Effective number of bits</td>
<td>$f_{\text{ADC}} = 36 , \text{MHz}$</td>
<td>10.3</td>
<td>10.4</td>
<td>—</td>
<td>bits</td>
</tr>
<tr>
<td>SNDR</td>
<td>Signal-to-noise and distortion ratio</td>
<td>$V_{\text{DDA}} = V_{\text{REF}+} = 3.3 , \text{V}$</td>
<td>63.8</td>
<td>64.4</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>SNR</td>
<td>Signal-to-noise ratio</td>
<td>Input Frequency = 110 kHz</td>
<td>64.2</td>
<td>65</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>THD</td>
<td>Total harmonic distortion</td>
<td>Temperature = 25 ℃</td>
<td>-70</td>
<td>-72</td>
<td>—</td>
<td></td>
</tr>
</tbody>
</table>

(1) Based on characterization, not tested in production.  
(2) Guaranteed by design, not tested in production.

Table 4-33. ADC dynamic accuracy at $f_{\text{ADC}} = 40 \, \text{MHz}^{(1)}$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>ENOB</td>
<td>Effective number of bits</td>
<td>$f_{\text{ADC}} = 40 , \text{MHz}$</td>
<td>9.9</td>
<td>10.0</td>
<td>—</td>
<td>bits</td>
</tr>
<tr>
<td>SNDR</td>
<td>Signal-to-noise and distortion ratio</td>
<td>$V_{\text{DDA}} = V_{\text{REF}+} = 3.3 , \text{V}$</td>
<td>61.4</td>
<td>62</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>SNR</td>
<td>Signal-to-noise ratio</td>
<td>Input Frequency = 110 kHz</td>
<td>62</td>
<td>62.4</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>THD</td>
<td>Total harmonic distortion</td>
<td>Temperature = 25 ℃</td>
<td>-68</td>
<td>-70</td>
<td>—</td>
<td></td>
</tr>
</tbody>
</table>

(1) Based on characterization, not tested in production.  
(2) Guaranteed by design, not tested in production.

Table 4-34. ADC static accuracy at $f_{\text{ADC}} = 15 \, \text{MHz}^{(1)}$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test conditions</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Offset</td>
<td>Offset error</td>
<td>$f_{\text{ADC}} = 15 , \text{MHz}$</td>
<td>±2</td>
<td>±3</td>
<td>LSB</td>
</tr>
<tr>
<td>DNL</td>
<td>Differential linearity error</td>
<td>$V_{\text{DDA}} = V_{\text{REF}+} = 3.3 , \text{V}$</td>
<td>±0.9</td>
<td>±1.2</td>
<td>LSB</td>
</tr>
<tr>
<td>INL</td>
<td>Integral linearity error</td>
<td></td>
<td>±1.1</td>
<td>±1.5</td>
<td>LSB</td>
</tr>
</tbody>
</table>
4.14. Temperature sensor characteristics

Table 4-35. Temperature sensor characteristics\(^{(1)}\)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>VSENSE linearity with temperature</td>
<td>—</td>
<td>±1.5</td>
<td>—</td>
<td>°C</td>
</tr>
<tr>
<td>Avg. Slope</td>
<td>Average slope</td>
<td>—</td>
<td>4.1</td>
<td>—</td>
<td>mV/°C</td>
</tr>
<tr>
<td>V(_{25})</td>
<td>Voltage at 25 °C</td>
<td>—</td>
<td>1.45</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>t(<em>{S</em>{\text{temp}}})(^{(2)})</td>
<td>ADC sampling time when reading the temperature</td>
<td>—</td>
<td>17.1</td>
<td>—</td>
<td>µs</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Based on characterization, not tested in production.
\(^{(2)}\) Guaranteed by design, not tested in production.

4.15. DAC characteristics

Table 4-36. DAC characteristics

<table>
<thead>
<tr>
<th>Symbol (^{(1)})</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V(_{DDA})</td>
<td>Operating voltage</td>
<td></td>
<td>2.6</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>V(_{REF+})</td>
<td>Positive Reference Voltage</td>
<td></td>
<td>—</td>
<td>2.6</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>V(_{REF-})</td>
<td>Negative Reference Voltage</td>
<td></td>
<td>—</td>
<td>—</td>
<td>V(_{SSA})</td>
<td>—</td>
</tr>
<tr>
<td>R(_{LOAD})</td>
<td>Resistive load</td>
<td>Resistive load with buffer ON</td>
<td>5</td>
<td>—</td>
<td>—</td>
<td>kΩ</td>
</tr>
<tr>
<td>R(_{O})</td>
<td>Impedance output</td>
<td>Impedance output with buffer OFF</td>
<td>—</td>
<td>—</td>
<td>15</td>
<td>kΩ</td>
</tr>
<tr>
<td>C(_{LOAD})</td>
<td>Capacitive load</td>
<td>Capacitive load with buffer ON</td>
<td>—</td>
<td>—</td>
<td>50</td>
<td>pF</td>
</tr>
<tr>
<td>DAC(_{OUT}) min(^{(2)})</td>
<td>Lower DAC(_{OUT}) voltage</td>
<td>Lower DAC(_{OUT}) voltage with buffer ON</td>
<td>0.2</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>DAC(_{OUT}) max(^{(2)})</td>
<td>Higher DAC(_{OUT}) voltage</td>
<td>Higher DAC(_{OUT}) voltage with buffer ON</td>
<td>—</td>
<td>—</td>
<td>V(_{DDA})-0.2</td>
<td>V</td>
</tr>
<tr>
<td>I(_{DDA})</td>
<td>DAC current consumption in quiescent mode</td>
<td>With no load, middle code(0x800) on the input,</td>
<td>—</td>
<td>—</td>
<td>500</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_{REF+} = 3.6) V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I(_{DDVREF+}) (^{(1)})</td>
<td>DAC current consumption in quiescent mode</td>
<td>With no load, worst code(0xF1C) on the input,</td>
<td>—</td>
<td>—</td>
<td>560</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_{REF+} = 3.6) V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>With no load, middle code(0x800) on the input,</td>
<td>—</td>
<td>—</td>
<td>86</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_{REF+} = 3.6) V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Symbol</td>
<td>Parameter</td>
<td>Conditions</td>
<td>Standard mode</td>
<td>Fast mode</td>
<td>Unit</td>
<td></td>
</tr>
<tr>
<td>--------</td>
<td>----------------------------------</td>
<td>-----------------------------</td>
<td>---------------</td>
<td>-----------</td>
<td>------</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td>t_{SCL(H)}</td>
<td>SCL clock high time</td>
<td>—</td>
<td>4.0</td>
<td>—</td>
<td>0.6</td>
<td>—</td>
</tr>
<tr>
<td>t_{SCL(L)}</td>
<td>SCL clock low time</td>
<td>—</td>
<td>4.7</td>
<td>—</td>
<td>1.3</td>
<td>—</td>
</tr>
<tr>
<td>t_{SDA}</td>
<td>SDA setup time</td>
<td>—</td>
<td>2</td>
<td>—</td>
<td>0.8</td>
<td>—</td>
</tr>
<tr>
<td>t_{H(SDA)}</td>
<td>SDA data hold time</td>
<td>—</td>
<td>250</td>
<td>—</td>
<td>250</td>
<td>—</td>
</tr>
<tr>
<td>t_{H(SDA/SCL)}</td>
<td>SDA and SCL rise time</td>
<td>—</td>
<td>1000</td>
<td>20</td>
<td>300</td>
<td>—</td>
</tr>
<tr>
<td>t_{H(SDA/SCL)}</td>
<td>SDA and SCL fall time</td>
<td>—</td>
<td>4</td>
<td>300</td>
<td>4</td>
<td>300</td>
</tr>
<tr>
<td>t_{H(STA)}</td>
<td>Start condition hold time</td>
<td>—</td>
<td>4.0</td>
<td>—</td>
<td>0.6</td>
<td>—</td>
</tr>
<tr>
<td>t_{H(STA)}</td>
<td>Repeated Start condition setup time</td>
<td>—</td>
<td>4.7</td>
<td>—</td>
<td>0.6</td>
<td>—</td>
</tr>
<tr>
<td>t_{H(STO)}</td>
<td>Stop condition setup time</td>
<td>—</td>
<td>4.0</td>
<td>—</td>
<td>0.6</td>
<td>—</td>
</tr>
<tr>
<td>t_{buff}</td>
<td>Stop to Start condition time (bus free)</td>
<td>—</td>
<td>4.7</td>
<td>—</td>
<td>1.3</td>
<td>—</td>
</tr>
</tbody>
</table>

(1) Guaranteed by design, not tested in production.
(2) Test condition: GPIO_SPEED set 2 MHz and external pull-up resistor value is 1 kΩ when operate EEPROM with I2C.

4.16. I2C characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Standard mode</th>
<th>Fast mode</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
<td>Min</td>
</tr>
<tr>
<td>DNL(1)</td>
<td>Differential non linearity</td>
<td>10-bit configuration</td>
<td>—</td>
<td>—</td>
<td>±0.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>12-bit configuration</td>
<td>—</td>
<td>—</td>
<td>±2</td>
</tr>
<tr>
<td>INL(1)</td>
<td>Integral non linearity</td>
<td>10-bit configuration</td>
<td>—</td>
<td>—</td>
<td>±1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>12-bit configuration</td>
<td>—</td>
<td>—</td>
<td>±4</td>
</tr>
<tr>
<td>Offset(1)</td>
<td>Offset error</td>
<td>DAC in 12-bit mode</td>
<td>—</td>
<td>—</td>
<td>±12</td>
</tr>
<tr>
<td>GE(1)</td>
<td>Gain error</td>
<td>DAC in 12-bit mode</td>
<td>—</td>
<td>—</td>
<td>±0.5</td>
</tr>
<tr>
<td>T_{setting}(1)</td>
<td>Setting time</td>
<td>C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 5 kΩ</td>
<td>—</td>
<td>0.5</td>
<td>1</td>
</tr>
<tr>
<td>T_{wakeup}(2)</td>
<td>Wakeup from off state</td>
<td></td>
<td>—</td>
<td>5</td>
<td>10</td>
</tr>
<tr>
<td>Update rate(2)</td>
<td>Max frequency for a correct</td>
<td>C_{LOAD} ≤ 50 pF, R_{LOAD} ≥ 5 kΩ</td>
<td>—</td>
<td>—</td>
<td>4</td>
</tr>
<tr>
<td>PSRR(2)</td>
<td>Power supply rejection ratio</td>
<td>No R_{Load}, C_{LOAD}=50 pF</td>
<td>—</td>
<td>-90</td>
<td>-75</td>
</tr>
</tbody>
</table>

(1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.


4.17. SPI characteristics

Table 4-38. Standard SPI characteristics *(1)*

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>f_{SCK}</td>
<td>SCK clock frequency</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>30</td>
<td>MHz</td>
</tr>
<tr>
<td>t_{SCK(H)}</td>
<td>SCK clock high time</td>
<td>Master mode, f_{CLK} = 100 MHz,</td>
<td>18</td>
<td>20</td>
<td>22</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>presc = 8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_{SCK(L)}</td>
<td>SCK clock low time</td>
<td>Master mode, f_{CLK} = 100 MHz,</td>
<td>18</td>
<td>20</td>
<td>22</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>presc = 8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td><strong>SPI master mode</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_{V(MO)}</td>
<td>Data output valid time</td>
<td>—</td>
<td>—</td>
<td>7</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>t_{H(MO)}</td>
<td>Data output hold time</td>
<td>—</td>
<td>—</td>
<td>4</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>t_{SU(MI)}</td>
<td>Data input setup time</td>
<td>—</td>
<td>1</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>t_{H(MI)}</td>
<td>Data input hold time</td>
<td>—</td>
<td>0</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td><strong>SPI slave mode</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_{SU(NSS)}</td>
<td>NSS enable setup time</td>
<td>—</td>
<td>0</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>t_{H(NSS)}</td>
<td>NSS enable hold time</td>
<td>—</td>
<td>1</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>t_{A(SO)}</td>
<td>Data output access time</td>
<td>—</td>
<td>—</td>
<td>9</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>t_{DIS(SO)}</td>
<td>Data output disable time</td>
<td>—</td>
<td>—</td>
<td>8</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>t_{V(SO)}</td>
<td>Data output valid time</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>t_{H(SO)}</td>
<td>Data output hold time</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>t_{SU(SI)}</td>
<td>Data input setup time</td>
<td>—</td>
<td>0</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>t_{H(SI)}</td>
<td>Data input hold time</td>
<td>—</td>
<td>2</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
</tbody>
</table>

*(1) Based on characterization, not tested in production.*
Figure 4-7. SPI timing diagram - master mode

**Figure 4-8. SPI timing diagram - slave mode**
### 4.18. I2S characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>f_CK</td>
<td>Clock frequency</td>
<td>Master mode (data: 16 bits, Audio frequency = 96 kHz)</td>
<td>—</td>
<td>3.078</td>
<td>—</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Slave mode</td>
<td></td>
<td></td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>t_H</td>
<td>Clock high time</td>
<td></td>
<td>—</td>
<td>162</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>t_L</td>
<td>Clock low time</td>
<td></td>
<td>—</td>
<td>163</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>t_V(WS)</td>
<td>WS valid time</td>
<td>Master mode</td>
<td>—</td>
<td>2</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_H(WS)</td>
<td>WS hold time</td>
<td>Master mode</td>
<td>—</td>
<td>2</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>t_SU(WS)</td>
<td>WS setup time</td>
<td>Slave mode</td>
<td>0</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>t_H(WS)</td>
<td>WS hold time</td>
<td>Slave mode</td>
<td>3</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>Du_Cy(SCK)</td>
<td>I2S slave input clock  cycle</td>
<td>Slave mode</td>
<td></td>
<td>50</td>
<td>—</td>
<td>%</td>
</tr>
<tr>
<td>t_SU(SD_MR)</td>
<td>Data input setup time</td>
<td>Master mode</td>
<td>0</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>t_SU(SD_SR)</td>
<td>Data input setup time</td>
<td>Slave mode</td>
<td>0</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>t_H(SD_MR)</td>
<td>Data input hold time</td>
<td>Master receiver</td>
<td>1</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>t_H(SD_SR)</td>
<td>Data input hold time</td>
<td>Slave receiver</td>
<td>3</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>t_V(SD_ST)</td>
<td>Data output valid time</td>
<td>Slave transmitter (after enable edge)</td>
<td>—</td>
<td>12</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>t_H(SD_ST)</td>
<td>Data output hold time</td>
<td>Slave transmitter (after enable edge)</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>t_V(SD_MT)</td>
<td>Data output valid time</td>
<td>Slave transmitter (after enable edge)</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>t_H(SD_MT)</td>
<td>Data output hold time</td>
<td>Master transmitter (after enable edge)</td>
<td>—</td>
<td>7</td>
<td>—</td>
<td>ns</td>
</tr>
</tbody>
</table>

(1) Guaranteed by design, not tested in production.
(2) Based on characterization, not tested in production.
Figure 4-9. I2S timing diagram - master mode

Figure 4-10. I2S timing diagram - slave mode
4.19. USART characteristics

Table 4-41. USART characteristics\(^{(1)}\)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>f(_{SCK})</td>
<td>SCK clock frequency</td>
<td>f(_{PCLKx}) = 100 MHz</td>
<td>—</td>
<td>—</td>
<td>50</td>
<td>MHz</td>
</tr>
<tr>
<td>t(_{SCK(H)})</td>
<td>SCK clock high time</td>
<td>f(_{PCLKx}) = 100 MHz</td>
<td>5.8</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>t(_{SCK(L)})</td>
<td>SCK clock low time</td>
<td>f(_{PCLKx}) = 100 MHz</td>
<td>5.8</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
</tbody>
</table>

(1) Guaranteed by design, not tested in production.

4.20. SDIO characteristics

Table 4-41. SDIO characteristics\(^{(1)}\)\(^{(2)}\)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>f(_{PP})</td>
<td>Clock frequency in data transfer mode</td>
<td>—</td>
<td>0</td>
<td>—</td>
<td>48</td>
<td>MHz</td>
</tr>
<tr>
<td>t(_{W(CKL)})</td>
<td>Clock low time</td>
<td>f(_{pp}) = 48 MHz</td>
<td>10.5</td>
<td>11</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>t(_{W(CKH)})</td>
<td>Clock high time</td>
<td>f(_{pp}) = 48 MHz</td>
<td>9.5</td>
<td>10</td>
<td>—</td>
<td>ns</td>
</tr>
</tbody>
</table>

CMD, D inputs (referenced to CK) in MMC and SD HS mode

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>t(_{ISU})</td>
<td>Input setup time HS</td>
<td>f(_{pp}) = 48 MHz</td>
<td>4</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>t(_{IH})</td>
<td>Input hold time HS</td>
<td>f(_{pp}) = 48 MHz</td>
<td>3</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
</tbody>
</table>

CMD, D outputs (referenced to CK) in MMC and SD HS mode

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>t(_{OV})</td>
<td>Output valid time HS</td>
<td>f(_{pp}) = 48 MHz</td>
<td>—</td>
<td>—</td>
<td>13.8</td>
<td>ns</td>
</tr>
<tr>
<td>t(_{OH})</td>
<td>Output hold time HS</td>
<td>f(_{pp}) = 48 MHz</td>
<td>12</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
</tbody>
</table>

CMD, D inputs (referenced to CK) in SD default mode

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>t(_{ISUD})</td>
<td>Input setup SD</td>
<td>f(_{pp}) = 24 MHz</td>
<td>3</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>t(_{IHD})</td>
<td>Input hold time SD</td>
<td>f(_{pp}) = 24 MHz</td>
<td>3</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
</tbody>
</table>

CMD, D outputs (referenced to CK) in SD default mode

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>t(_{OVD})</td>
<td>Output valid default time SD</td>
<td>f(_{pp}) = 24 MHz</td>
<td>—</td>
<td>2.4</td>
<td>2.8</td>
<td>ns</td>
</tr>
<tr>
<td>t(_{OHD})</td>
<td>Output hold default time SD</td>
<td>f(_{pp}) = 24 MHz</td>
<td>0.8</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
</tbody>
</table>

(1) CLK timing is measured at 50% of V\(_{DD}\).
(2) Capacitive load C\(_{L}\) = 30 pF.
(3) Based on characterization, not tested in production.
(4) Guaranteed by design, not tested in production.

4.21. CAN characteristics

Refer to Table 4-26, I/O port DC characteristics\(^{(1)}\) for more details on the input/output alternate function characteristics (CANTX and CANRX).
4.22. **USBFS characteristics**

**Table 4-42. USBFS start up time**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>tSTARTUP(1)</td>
<td>USBFS startup time</td>
<td>1</td>
<td></td>
<td>1</td>
<td>μs</td>
</tr>
</tbody>
</table>

(1) Guaranteed by design, not tested in production.

**Table 4-43. USBFS DC electrical characteristics**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input levels(1)</td>
<td>VDD</td>
<td>USBFS operating voltage</td>
<td>—</td>
<td>3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>VDI</td>
<td>Differential input sensitivity</td>
<td>—</td>
<td>0.2</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>VCM</td>
<td>Differential common mode range</td>
<td>Includes VDI range</td>
<td>0.8</td>
<td>—</td>
<td>2.5</td>
</tr>
<tr>
<td></td>
<td>VSE</td>
<td>Single ended receiver threshold</td>
<td>—</td>
<td>1.3</td>
<td>—</td>
<td>2.0</td>
</tr>
<tr>
<td>Output levels (2)</td>
<td>VOL</td>
<td>Static output level low</td>
<td>RL of 1.0 kΩ to 3.6 V</td>
<td>—</td>
<td>0.06</td>
<td>0.3</td>
</tr>
<tr>
<td></td>
<td>VOH</td>
<td>Static output level high</td>
<td>RL of 15 kΩ to VSS</td>
<td>2.8</td>
<td>3.3</td>
<td>3.6</td>
</tr>
<tr>
<td></td>
<td>RPD(2)</td>
<td>PA11, PA12(USBFS_DM/DP)</td>
<td>VIN = VDD</td>
<td>17</td>
<td>21</td>
<td>25</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PB14, PB15(USBHS_DM/DP)</td>
<td>VSE(USBFS_VBUS)</td>
<td>0.72</td>
<td>0.9</td>
<td>1.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PA9(USBFS_VBUS)</td>
<td>PB13(USBHS_VBUS)</td>
<td>VIN = VSS</td>
<td>1.2</td>
<td>1.5</td>
</tr>
<tr>
<td></td>
<td>RPU(2)</td>
<td>PA11, PA12(USBFS_DM/DP)</td>
<td>VIN = VDD</td>
<td>0.24</td>
<td>0.3</td>
<td>0.33</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PB14, PB15(USBHS_DM/DP)</td>
<td>VSE(USBFS_VBUS)</td>
<td>PA9(USBFS_VBUS)</td>
<td>PB13(USBHS_VBUS)</td>
<td></td>
</tr>
</tbody>
</table>

(1) Guaranteed by design, not tested in production.
(2) Based on characterization, not tested in production.

**Table 4-44. USBFS full speed-electrical characteristics(1)**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>tR</td>
<td>Rise time</td>
<td>CL = 50 pF</td>
<td>4</td>
<td>—</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>tf</td>
<td>Fall time</td>
<td>CL = 50 pF</td>
<td>4</td>
<td>—</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>tRFM</td>
<td>Rise/ fall time matching</td>
<td>tR / tf</td>
<td>90</td>
<td>—</td>
<td>110</td>
<td>%</td>
</tr>
<tr>
<td>VCRS</td>
<td>Output signal crossover voltage</td>
<td>—</td>
<td>1.3</td>
<td>—</td>
<td>2.0</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) Guaranteed by design, not tested in production.

**Figure 4-11. USBFS timings: definition of data signal rise and fall time**
### 4.23. USBHS characteristics

#### Table 4-45. USBHS clock timing parameters

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>USBHS operating voltage</td>
<td>3.0</td>
<td>—</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>fHCLK</td>
<td>fHCLK value to guarantee proper</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>operation of USBHS interface</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FSTART_8BIT</td>
<td>Frequency (first transition) 8-bit ±10%</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FSTEADY</td>
<td>Frequency (steady state) ±500 ppm</td>
<td>59.97</td>
<td>60</td>
<td>60.63</td>
<td>MHz</td>
</tr>
<tr>
<td>DSTART_8BIT</td>
<td>Duty cycle (first transition) 8-bit ±10%</td>
<td>40</td>
<td>50</td>
<td>60</td>
<td>%</td>
</tr>
<tr>
<td>DSTEADY</td>
<td>Duty cycle (steady state) ±500 ppm</td>
<td>49.975</td>
<td>50</td>
<td>50.025</td>
<td>%</td>
</tr>
</tbody>
</table>

(1) Guaranteed by design, not tested in production.

#### Table 4-46. USB-ULPI Dynamic characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>tSC</td>
<td>Control in (ULPI_DIR, ULPI_NXT) setup time</td>
<td>—</td>
<td>—</td>
<td>2</td>
<td>ns</td>
</tr>
<tr>
<td>tHC</td>
<td>Control in (ULPI_DIR, ULPI_NXT) hold time</td>
<td>0.5</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tSD</td>
<td>Data in setup time</td>
<td>—</td>
<td>—</td>
<td>2</td>
<td>ns</td>
</tr>
<tr>
<td>tHD</td>
<td>Data in hold time</td>
<td>0</td>
<td>—</td>
<td>—</td>
<td>ns</td>
</tr>
</tbody>
</table>

(1) Guaranteed by design, not tested in production.

### 4.24. EXMC characteristics

#### Table 4-47. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>t(NE)</td>
<td>EXMC_NE low time</td>
<td>24</td>
<td>26</td>
<td>ns</td>
</tr>
<tr>
<td>t(NOEX,NE)</td>
<td>EXMC_NEx low to EXMC_NOE low</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>t(NOEX)</td>
<td>EXMC_NOE low time</td>
<td>24</td>
<td>26</td>
<td>ns</td>
</tr>
<tr>
<td>t(NOEX,NOE)</td>
<td>EXMC_NOE high to EXMC_NE high hold time</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>t(A,NE)</td>
<td>EXMC_NEx low to EXMC_A valid</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>t(BL,NE)</td>
<td>EXMC_NEx low to EXMC_BL valid</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>t(DATA,NE)</td>
<td>Data to EXMC_NEx high setup time</td>
<td>19</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>t(DATA,NOE)</td>
<td>Data to EXMC_NOEx high setup time</td>
<td>19</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>t(NOEX,NOE)</td>
<td>Data hold time after EXMC_NOE high</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>t(NOEX,NE)</td>
<td>Data hold time after EXMC_NEx high</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>t(NOADV,NE)</td>
<td>EXMC_NEx low to EXMC_NADV low</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>t(NOADV)</td>
<td>EXMC_NADV low time</td>
<td>4</td>
<td>6</td>
<td>ns</td>
</tr>
</tbody>
</table>

(1) C_L = 30 pF.
(2) Guaranteed by design, not tested in production.
(3) Based on configure: fHCLK = 200 MHz, AddressSetupTime = 0, AddressHoldTime = 1, DataSetupTime = 1.
### Table 4-48. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{\text{w(NE)}} )</td>
<td>EXMC_NE low time</td>
<td>14</td>
<td>16</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{\text{V(NWE,NE)}} )</td>
<td>EXMC_NEx low to EXMC_NWE low</td>
<td>4</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{\text{w(NWE)}} )</td>
<td>EXMC_NWE low time</td>
<td>4</td>
<td>6</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{\text{h(NE, NWE)}} )</td>
<td>EXMC_NWE high to EXMC_NE high hold time</td>
<td>4</td>
<td>6</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{\text{V(A,NE)}} )</td>
<td>EXMC_NEx low to EXMC_A valid</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{\text{V(NADV,NE)}} )</td>
<td>EXMC_NEx low to EXMC_NADV low</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{\text{w(NADV)}} )</td>
<td>EXMC_NADV low time</td>
<td>4</td>
<td>6</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{\text{h(AD, NADV)}} )</td>
<td>EXMC_AD(address) valid hold time after EXMC_NADV high</td>
<td>9</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{\text{h(A, NWE)}} )</td>
<td>Address hold time after EXMC_NWE high</td>
<td>4</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{\text{w(BL, NWE)}} )</td>
<td>EXMC_BL hold time after EXMC_NWE high</td>
<td>4</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{\text{w(BL, NE)}} )</td>
<td>EXMC_NEx low to EXMC_BL valid</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{\text{w(DATA, NADV)}} )</td>
<td>EXMC_NADV high to DATA valid</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{\text{h(DATA, NWE)}} )</td>
<td>Data hold time after EXMC_NWE high</td>
<td>4</td>
<td>—</td>
<td>ns</td>
</tr>
</tbody>
</table>

(1) \( C_L = 30 \text{ pF} \).
(2) Guaranteed by design, not tested in production.
(3) Based on configure: \( f_{\text{CLK}} = 200 \text{ MHz} \), AddressSetupTime = 0, AddressHoldTime = 1, DataSetupTime = 1.

### Table 4-49. Asynchronous multiplexed PSRAM/NOR read timings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{\text{w(NE)}} )</td>
<td>EXMC_NE low time</td>
<td>34</td>
<td>36</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{\text{V(NOEX,NE)}} )</td>
<td>EXMC_NEx low to EXMC_NOE low</td>
<td>14</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{\text{w(NOEX)}} )</td>
<td>EXMC_NOE low time</td>
<td>19</td>
<td>21</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{\text{h(NOE, NOE)}} )</td>
<td>EXMC_NOE high to EXMC_NE high hold time</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{\text{V(A,NE)}} )</td>
<td>EXMC_NEx low to EXMC_A valid</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{\text{h(A, NOE)}} )</td>
<td>Address hold time after EXMC_NOE high</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{\text{w(BL, NE)}} )</td>
<td>EXMC_NEx low to EXMC_BL valid</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{\text{w(BL, NOE)}} )</td>
<td>EXMC_BL hold time after EXMC_NOE high</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{\text{su(DATA, NOE)}} )</td>
<td>Data to EXMC_NEx high setup time</td>
<td>19</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{\text{su(DATA, NOE)}} )</td>
<td>Data to EXMC_NOEx high setup time</td>
<td>19</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{\text{h(DATA, NOE)}} )</td>
<td>Data hold time after EXMC_NOE high</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{\text{h(DATA, NE)}} )</td>
<td>Data hold time after EXMC_NEx high</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{\text{V(NADV, NE)}} )</td>
<td>EXMC_NEx low to EXMC_NADV low</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{\text{w(NADV)}} )</td>
<td>EXMC_NADV low time</td>
<td>4</td>
<td>6</td>
<td>ns</td>
</tr>
<tr>
<td>( T_{\text{h(AD, NADV)}} )</td>
<td>EXMC_AD(address) valid hold time after EXMC_NADV high</td>
<td>4</td>
<td>6</td>
<td>ns</td>
</tr>
</tbody>
</table>

(1) \( C_L = 30 \text{ pF} \).
(2) Guaranteed by design, not tested in production.
(3) Based on configure: \( f_{\text{CLK}} = 200 \text{ MHz} \), AddressSetupTime = 0, AddressHoldTime = 1, DataSetupTime = 1.

### Table 4-50. Asynchronous multiplexed PSRAM/NOR write timings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{\text{w(NE)}} )</td>
<td>EXMC_NE low time</td>
<td>24</td>
<td>26</td>
<td>ns</td>
</tr>
<tr>
<td>Symbol</td>
<td>Parameter</td>
<td>Min</td>
<td>Max</td>
<td>Unit</td>
</tr>
<tr>
<td>---------------</td>
<td>-----------------------------------------------</td>
<td>-----</td>
<td>-----</td>
<td>------</td>
</tr>
<tr>
<td>tV(NWE_NE)</td>
<td>EXMC_NEx low to EXMC_NWE low</td>
<td>4</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tV(NWE)</td>
<td>EXMC_NWE low time</td>
<td>14</td>
<td>16</td>
<td>ns</td>
</tr>
<tr>
<td>tV(NWE_NWE)</td>
<td>EXMC_NWE high to EXMC_NE high hold time</td>
<td>4</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tV(NE_NE)</td>
<td>EXMC_NEx low to EXMC_A valid</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tV(NADV_NE)</td>
<td>EXMC_NEx low to EXMC_NADV low</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tV(NADV)</td>
<td>EXMC_NADV low time</td>
<td>4</td>
<td>6</td>
<td>ns</td>
</tr>
<tr>
<td>tH(AD_NADV)</td>
<td>EXMC_AD(address) valid hold time after</td>
<td>4</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>EXMC_NADV high</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tH(A_NWE)</td>
<td>Address hold time after EXMC_NWE high</td>
<td>4</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tH(BL_NWE)</td>
<td>EXMC_BL hold time after EXMC_NWE high</td>
<td>4</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tV(DATA_NADV)</td>
<td>EXMC_NADV high to DATA valid</td>
<td>4</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tV(DATA_NWE)</td>
<td>Data hold time after EXMC_NWE high</td>
<td>4</td>
<td>—</td>
<td>ns</td>
</tr>
</tbody>
</table>

(1) C\text{L} = 30 \text{pF}.
(2) Guaranteed by design, not tested in production.
(3) Based on configure: \(f_{\text{HCLK}} = 200 \text{MHz}\), AddressSetupTime = 0, AddressHoldTime = 1, DataSetupTime = 1.

**Table 4-51. Synchronous multiplexed PSRAM/NOR read timings\(^{(1)(2)(3)}\)**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>tV(CLK)</td>
<td>EXMC_CLK period</td>
<td>20</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tV(CLKL-NEXL)</td>
<td>EXMC_CLK low to EXMC_NEx low</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tV(CLKH-NEXL)</td>
<td>EXMC_CLK high to EXMC_NEx high</td>
<td>9</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tV(CLKL-NADVL)</td>
<td>EXMC_CLK low to EXMC_NADV low</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tV(CLKL-NADVH)</td>
<td>EXMC_CLK low to EXMC_NADV high</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tV(CLKL-AL)</td>
<td>EXMC_CLK low to EXMC_Ax valid</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tV(CLKH-AL)</td>
<td>EXMC_CLK high to EXMC_Ax invalid</td>
<td>9</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tV(CLKL-NOEL)</td>
<td>EXMC_CLK low to EXMC_NOE low</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tV(CLKH-NOEH)</td>
<td>EXMC_CLK high to EXMC_NOE high</td>
<td>9</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tV(CLKL-ADV)</td>
<td>EXMC_CLK low to EXMC_AD valid</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tV(CLKL-NWEL)</td>
<td>EXMC_CLK low to EXMC_NWE low</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
</tbody>
</table>

(1) C\text{L} = 30 \text{pF}.
(2) Guaranteed by design, not tested in production.
(3) Based on configure: \(f_{\text{HCLK}} = 200 \text{MHz}\), BurstAccessMode = Enable; Memory Type = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); Data Latency = 1.

**Table 4-52. Synchronous multiplexed PSRAM write timings\(^{(1)(2)(3)}\)**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>tV(CLK)</td>
<td>EXMC_CLK period</td>
<td>20</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tV(CLKL-NEXL)</td>
<td>EXMC_CLK low to EXMC_NEx low</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tV(CLKH-NEXL)</td>
<td>EXMC_CLK high to EXMC_NEx high</td>
<td>9</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tV(CLKL-NADVL)</td>
<td>EXMC_CLK low to EXMC_NADV low</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tV(CLKL-NADVH)</td>
<td>EXMC_CLK low to EXMC_NADV high</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tV(CLKL-AL)</td>
<td>EXMC_CLK low to EXMC_Ax valid</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tV(CLKH-AL)</td>
<td>EXMC_CLK high to EXMC_Ax invalid</td>
<td>9</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tV(CLKL-NOEL)</td>
<td>EXMC_CLK low to EXMC_NOE low</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tV(CLKH-NOEH)</td>
<td>EXMC_CLK high to EXMC_NOE high</td>
<td>9</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tV(CLKL-ADV)</td>
<td>EXMC_CLK low to EXMC_AD valid</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tV(CLKL-NWEL)</td>
<td>EXMC_CLK low to EXMC_NWE low</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
</tbody>
</table>
Table 4-53. Synchronous non-multiplexed PSRAM/NOR read timings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_w(\text{CLK}) )</td>
<td>EXMC_CLK period</td>
<td>20</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_d(\text{CLKL-NExL}) )</td>
<td>EXMC_CLK low to EXMC_NEx low</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_d(\text{CLKH-NExH}) )</td>
<td>EXMC_CLK high to EXMC_NEx high</td>
<td>9</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_d(\text{CLKL-NADVL}) )</td>
<td>EXMC_CLK low to EXMC_NADV low</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_d(\text{CLKL-NADVH}) )</td>
<td>EXMC_CLK low to EXMC_NADV high</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_d(\text{CLKL-AV}) )</td>
<td>EXMC_CLK low to EXMC_Ax valid</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_d(\text{CLKH-AV}) )</td>
<td>EXMC_CLK high to EXMC_Ax invalid</td>
<td>9</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_d(\text{CLKL-NOEL}) )</td>
<td>EXMC_CLK low to EXMC_NOE low</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_d(\text{CLKH-NOEH}) )</td>
<td>EXMC_CLK high to EXMC_NOE high</td>
<td>9</td>
<td>—</td>
<td>ns</td>
</tr>
</tbody>
</table>

(1) \( C_L = 30 \) pF.
(2) Guaranteed by design, not tested in production.
(3) Based on configure: \( f_{\text{HCLK}} = 200 \) MHz, BurstAccessMode = Enable; MemoryType = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); DataLatency = 1.

Table 4-54. Synchronous non-multiplexed PSRAM write timings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_w(\text{CLK}) )</td>
<td>EXMC_CLK period</td>
<td>20</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_d(\text{CLKL-NExL}) )</td>
<td>EXMC_CLK low to EXMC_NEx low</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_d(\text{CLKH-NExH}) )</td>
<td>EXMC_CLK high to EXMC_NEx high</td>
<td>9</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_d(\text{CLKL-NADVL}) )</td>
<td>EXMC_CLK low to EXMC_NADV low</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_d(\text{CLKL-NADVH}) )</td>
<td>EXMC_CLK low to EXMC_NADV high</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_d(\text{CLKL-AV}) )</td>
<td>EXMC_CLK low to EXMC_Ax valid</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_d(\text{CLKH-AV}) )</td>
<td>EXMC_CLK high to EXMC_Ax invalid</td>
<td>9</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_d(\text{CLKL-NWEL}) )</td>
<td>EXMC_CLK low to EXMC_NWE low</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_d(\text{CLKH-NWEH}) )</td>
<td>EXMC_CLK high to EXMC_NWE high</td>
<td>9</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_d(\text{CLKL-DATA}) )</td>
<td>EXMC_A/D valid data after EXMC_CLK low</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_d(\text{CLKL-NBLH}) )</td>
<td>EXMC_CLK low to EXMC_NBL high</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
</tbody>
</table>

(1) \( C_L = 30 \) pF.
(2) Guaranteed by design, not tested in production.
(3) Based on configure: \( f_{\text{HCLK}} = 200 \) MHz, BurstAccessMode = Enable; MemoryType = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); DataLatency = 1.
4.25. **TIMER characteristics**

**Table 4-55. TIMER characteristics**(1)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{res}$</td>
<td>Timer resolution time</td>
<td>$f_{\text{TIMERxCLK}} = 200$ MHz</td>
<td>5</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>$f_{\text{EXT}}$</td>
<td>Timer external clock frequency</td>
<td>$f_{\text{TIMERxCLK}} = 200$ MHz</td>
<td>0</td>
<td>100 MHz</td>
<td></td>
</tr>
<tr>
<td>RES</td>
<td>Timer resolution</td>
<td>TIMERx (except TIMER1 &amp; TIMER4)</td>
<td>—</td>
<td>16</td>
<td>bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TIMER1 &amp; TIMER4</td>
<td>—</td>
<td>32</td>
<td>bit</td>
</tr>
<tr>
<td>$t_{\text{COUNTER}}$</td>
<td>16-bit counter clock period when internal clock is selected</td>
<td>$f_{\text{TIMERxCLK}} = 200$ MHz</td>
<td>0.005</td>
<td>327.68</td>
<td>μs</td>
</tr>
<tr>
<td>$t_{\text{MAX_COUNT}}$</td>
<td>Maximum possible count</td>
<td>$f_{\text{TIMERxCLK}} = 200$ MHz</td>
<td>65536x65536</td>
<td>21.47</td>
<td>s</td>
</tr>
</tbody>
</table>

(1) Guaranteed by design, not tested in production.

4.26. **DCI characteristics**

**Table 4-56. DCI characteristics**(1)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency ratio</td>
<td>DCI_PIXCLK / fHCLK</td>
<td>—</td>
<td>0.4</td>
<td></td>
</tr>
<tr>
<td>DCI_PIXCLK</td>
<td>Pixel clock input</td>
<td>—</td>
<td>80 MHz</td>
<td></td>
</tr>
<tr>
<td>$D_{\text{Pixel}}$</td>
<td>Pixel clock input duty cycle</td>
<td>30</td>
<td>70</td>
<td>%</td>
</tr>
<tr>
<td>$t_{\text{su(DATA)}}$</td>
<td>Data input setup time</td>
<td>2.5</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{th(DATA)}}$</td>
<td>Data output valid time</td>
<td>1</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{su(HSYNC)}}$</td>
<td>DCI_HS input setup time</td>
<td>2</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{su(VSYNC)}}$</td>
<td>DCI_VS input setup time</td>
<td>2</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{th(HSYNC)}}$</td>
<td>DCI_HS input hold time</td>
<td>0.5</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{th(VSYNC)}}$</td>
<td>DCI_VS input hold time</td>
<td>0.5</td>
<td>—</td>
<td>ns</td>
</tr>
</tbody>
</table>

(1) Guaranteed by design, not tested in production.
4.27.  WDGT characteristics

Table 4-57. FWDGT min/max timeout period at 32 kHz (IRC32K) \(^{(1)}\)

<table>
<thead>
<tr>
<th>Prescaler divider</th>
<th>PR[2:0] bits</th>
<th>Min timeout RLD[11:0] = 0x000</th>
<th>Max timeout RLD[11:0] = 0xFFF</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/4</td>
<td>000</td>
<td>0.125</td>
<td>512</td>
<td>ms</td>
</tr>
<tr>
<td>1/8</td>
<td>001</td>
<td>0.25</td>
<td>1024</td>
<td></td>
</tr>
<tr>
<td>1/16</td>
<td>010</td>
<td>0.5</td>
<td>2048</td>
<td></td>
</tr>
<tr>
<td>1/32</td>
<td>011</td>
<td>1.0</td>
<td>4096</td>
<td></td>
</tr>
<tr>
<td>1/64</td>
<td>100</td>
<td>2.0</td>
<td>8192</td>
<td></td>
</tr>
<tr>
<td>1/128</td>
<td>101</td>
<td>4.0</td>
<td>16384</td>
<td></td>
</tr>
<tr>
<td>1/256</td>
<td>110 or 111</td>
<td>8.0</td>
<td>32768</td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) Guaranteed by design, not tested in production.

Table 4-58. WWDGT min-max timeout value at 50 MHz (f_PCLK1) \(^{(1)}\)

<table>
<thead>
<tr>
<th>Prescaler divider</th>
<th>PSC[2:0]</th>
<th>Min timeout value CNT[6:0] = 0x40</th>
<th>Unit</th>
<th>Max timeout value CNT[6:0] = 0x7F</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/1</td>
<td>00</td>
<td>81.92</td>
<td>μs</td>
<td>5.24</td>
<td>ms</td>
</tr>
<tr>
<td>1/2</td>
<td>01</td>
<td>163.84</td>
<td></td>
<td>10.49</td>
<td></td>
</tr>
<tr>
<td>1/4</td>
<td>10</td>
<td>327.68</td>
<td></td>
<td>20.97</td>
<td></td>
</tr>
<tr>
<td>1/8</td>
<td>11</td>
<td>655.36</td>
<td></td>
<td>41.94</td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) Guaranteed by design, not tested in production.

4.28.  Parameter conditions

Unless otherwise specified, all values given for V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C.
5. Package information

5.1. BGA176 package outline dimensions

Figure 5-1. BGA176 package outline
### Table 5-1. BGA176 package dimensions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>—</td>
<td>—</td>
<td>0.89</td>
</tr>
<tr>
<td>A1</td>
<td>0.13</td>
<td>0.18</td>
<td>0.23</td>
</tr>
<tr>
<td>A2</td>
<td>0.53</td>
<td>0.58</td>
<td>0.63</td>
</tr>
<tr>
<td>A3</td>
<td>0.45 BASIC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>c</td>
<td>0.10</td>
<td>0.13</td>
<td>0.16</td>
</tr>
<tr>
<td>D</td>
<td>9.90</td>
<td>10.00</td>
<td>10.10</td>
</tr>
<tr>
<td>D1</td>
<td>9.10 BASIC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>E</td>
<td>9.90</td>
<td>10.00</td>
<td>10.10</td>
</tr>
<tr>
<td>E1</td>
<td>9.10 BASIC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>e</td>
<td>0.65 BASIC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>0.325 REF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>b</td>
<td>0.20</td>
<td>0.25</td>
<td>0.30</td>
</tr>
<tr>
<td>aaa</td>
<td>0.10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ccc</td>
<td>0.20</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ddd</td>
<td>0.08</td>
<td></td>
<td></td>
</tr>
<tr>
<td>eee</td>
<td>0.15</td>
<td></td>
<td></td>
</tr>
<tr>
<td>fff</td>
<td>0.08</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### 5.2. LQFP144 package outline dimensions

**Figure 5-2. LQFP144 package outline**
Table 5-2. LQFP144 package dimensions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>—</td>
<td>—</td>
<td>1.60</td>
</tr>
<tr>
<td>A1</td>
<td>0.05</td>
<td>—</td>
<td>0.15</td>
</tr>
<tr>
<td>A2</td>
<td>1.35</td>
<td>1.40</td>
<td>1.45</td>
</tr>
<tr>
<td>A3</td>
<td>0.59</td>
<td>0.64</td>
<td>0.69</td>
</tr>
<tr>
<td>D</td>
<td>21.80</td>
<td>22.0</td>
<td>22.20</td>
</tr>
<tr>
<td>D1</td>
<td>19.90</td>
<td>20.0</td>
<td>20.10</td>
</tr>
<tr>
<td>E</td>
<td>21.80</td>
<td>22.0</td>
<td>22.20</td>
</tr>
<tr>
<td>E1</td>
<td>19.90</td>
<td>20.0</td>
<td>20.10</td>
</tr>
<tr>
<td>θ</td>
<td>0°</td>
<td>3.5°</td>
<td>7°</td>
</tr>
<tr>
<td>c</td>
<td>0.13</td>
<td>—</td>
<td>0.17</td>
</tr>
<tr>
<td>c1</td>
<td>0.12</td>
<td>0.13</td>
<td>0.14</td>
</tr>
<tr>
<td>L</td>
<td>0.45</td>
<td>—</td>
<td>0.75</td>
</tr>
<tr>
<td>L1</td>
<td>—</td>
<td>1.0 REF</td>
<td>—</td>
</tr>
<tr>
<td>b</td>
<td>0.18</td>
<td>—</td>
<td>0.26</td>
</tr>
<tr>
<td>b1</td>
<td>0.17</td>
<td>0.20</td>
<td>0.23</td>
</tr>
<tr>
<td>e</td>
<td>—</td>
<td>0.50 BSC</td>
<td>—</td>
</tr>
</tbody>
</table>

(Original dimensions are in millimeters)
5.3. LQFP100 package outline dimensions

Figure 5-3. LQFP100 package outline

Table 5-3. LQFP100 package dimensions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>—</td>
<td>—</td>
<td>1.60</td>
</tr>
<tr>
<td>A1</td>
<td>0.05</td>
<td>—</td>
<td>0.15</td>
</tr>
<tr>
<td>A2</td>
<td>1.35</td>
<td>1.40</td>
<td>1.45</td>
</tr>
<tr>
<td>A3</td>
<td>0.59</td>
<td>0.64</td>
<td>0.69</td>
</tr>
<tr>
<td>D</td>
<td>15.80</td>
<td>16.0</td>
<td>16.20</td>
</tr>
<tr>
<td>D1</td>
<td>13.90</td>
<td>14.0</td>
<td>14.10</td>
</tr>
<tr>
<td>E</td>
<td>15.80</td>
<td>16.0</td>
<td>16.20</td>
</tr>
<tr>
<td>E1</td>
<td>13.90</td>
<td>14.0</td>
<td>14.10</td>
</tr>
<tr>
<td>θ</td>
<td>0°</td>
<td>3.5°</td>
<td>7°</td>
</tr>
<tr>
<td>c</td>
<td>0.13</td>
<td>—</td>
<td>0.17</td>
</tr>
<tr>
<td>c1</td>
<td>0.12</td>
<td>0.13</td>
<td>0.14</td>
</tr>
<tr>
<td>L</td>
<td>0.45</td>
<td>0.6</td>
<td>0.75</td>
</tr>
<tr>
<td>L1</td>
<td>—</td>
<td>1.0 REF</td>
<td>—</td>
</tr>
<tr>
<td>b</td>
<td>0.18</td>
<td>0.20</td>
<td>0.26</td>
</tr>
<tr>
<td>b1</td>
<td>0.17</td>
<td>0.20</td>
<td>0.23</td>
</tr>
<tr>
<td>eB</td>
<td>15.05</td>
<td>—</td>
<td>15.35</td>
</tr>
</tbody>
</table>
5.4. Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter “Θ”. For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

Θ_{JA}: Thermal resistance, junction-to-ambient.
Θ_{JB}: Thermal resistance, junction-to-board.
Θ_{JC}: Thermal resistance, junction-to-case.
Ψ_{JB}: Thermal characterization parameter, junction-to-board.
Ψ_{JT}: Thermal characterization parameter, junction-to-top center.

\[ Θ_{JA} = \frac{(T_J - T_A)}{P_D} \]
\[ Θ_{JB} = \frac{(T_J - T_B)}{P_D} \]
\[ Θ_{JC} = \frac{(T_J - T_C)}{P_D} \]

Where, \( T_J \) = Junction temperature.
\( T_A \) = Ambient temperature
\( T_B \) = Board temperature
\( T_C \) = Case temperature which is monitoring on package surface
\( P_D \) = Total power dissipation

Θ_{JA} represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower Θ_{JA} can be considerate as better overall thermal performance. Θ_{JA} is generally used to estimate junction temperature.

Θ_{JB} is used to measure the heat flow resistance between the chip surface and the PCB board.
Θ_{JC} represents the thermal resistance between the chip surface and the package top case.
Θ_{JC} is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

Table 5-4. Package thermal characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Condition</th>
<th>Package</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Θ_{JA}</td>
<td>( T_A = 85°C ), Natural convection, 2S2P PCB</td>
<td>BGA176</td>
<td>45.02</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LQFP144</td>
<td>48.76</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LQFP100</td>
<td>57.42</td>
<td>°C/W</td>
</tr>
<tr>
<td>Θ_{JB}</td>
<td>( T_A = 25°C ), Cold plate, 2S2P PCB</td>
<td>BGA176</td>
<td>26.55</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LQFP144</td>
<td>35.00</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LQFP100</td>
<td>31.68</td>
<td>°C/W</td>
</tr>
<tr>
<td>Θ_{JC}</td>
<td>( T_A = 25°C ), Cold plate, 2S2P PCB</td>
<td>BGA176</td>
<td>9.93</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LQFP144</td>
<td>12.03</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LQFP100</td>
<td>13.85</td>
<td>°C/W</td>
</tr>
<tr>
<td>Ψ_{JB}</td>
<td>( T_A = 85°C ), Natural convection, 2S2P</td>
<td>BGA176</td>
<td>28.31</td>
<td>°C/W</td>
</tr>
<tr>
<td>Symbol</td>
<td>Condition</td>
<td>Package</td>
<td>Value</td>
<td>Unit</td>
</tr>
<tr>
<td>--------</td>
<td>-----------</td>
<td>---------</td>
<td>-------</td>
<td>------</td>
</tr>
<tr>
<td></td>
<td>PCB</td>
<td>LQFP144</td>
<td>35.32</td>
<td></td>
</tr>
<tr>
<td></td>
<td>LQFP100</td>
<td>41.28</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\Psi_{JT}$</td>
<td>$T_A = 85^\circ C$, Natural convection, 2S2P PCB</td>
<td>BGA176</td>
<td>0.69</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td>LQFP144</td>
<td>1.86</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>LQFP100</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) Thermal characteristics are based on simulation, and meet JEDEC specification.
6. Ordering information

Table 6-1. Part ordering code for GD32F450xx devices

<table>
<thead>
<tr>
<th>Ordering code</th>
<th>Flash (KB)</th>
<th>Package</th>
<th>Package type</th>
<th>Temperature operating range</th>
</tr>
</thead>
<tbody>
<tr>
<td>GD32F450VET6</td>
<td>512</td>
<td>LQFP100</td>
<td>Green</td>
<td>Industrial</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>GD32F450VG6</td>
<td>1024</td>
<td>LQFP100</td>
<td>Green</td>
<td>Industrial</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>GD32F450VIT6</td>
<td>2048</td>
<td>LQFP100</td>
<td>Green</td>
<td>Industrial</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>GD32F450VK6</td>
<td>3072</td>
<td>LQFP100</td>
<td>Green</td>
<td>Industrial</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>GD32F450ZET6</td>
<td>512</td>
<td>LQFP144</td>
<td>Green</td>
<td>Industrial</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>GD32F450ZGT6</td>
<td>1024</td>
<td>LQFP144</td>
<td>Green</td>
<td>Industrial</td>
</tr>
<tr>
<td></td>
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<td></td>
<td></td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>GD32F450ZIT6</td>
<td>2048</td>
<td>LQFP144</td>
<td>Green</td>
<td>Industrial</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>GD32F450ZKT6</td>
<td>3072</td>
<td>LQFP144</td>
<td>Green</td>
<td>Industrial</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>GD32F450IGH6</td>
<td>1024</td>
<td>BGA176</td>
<td>Green</td>
<td>Industrial</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>GD32F450IIH6</td>
<td>2048</td>
<td>BGA176</td>
<td>Green</td>
<td>Industrial</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>GD32F450IKH6</td>
<td>3072</td>
<td>BGA176</td>
<td>Green</td>
<td>Industrial</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-40°C to +85°C</td>
</tr>
</tbody>
</table>
7. Revision history

Table 7-1. Revision history

<table>
<thead>
<tr>
<th>Revision No.</th>
<th>Description</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>Initial Release</td>
<td>Oct. 25, 2016</td>
</tr>
<tr>
<td>1.1</td>
<td>Pin alternate functions summary updated</td>
<td>Oct. 29, 2016</td>
</tr>
<tr>
<td>1.2</td>
<td>Repair history accumulation error</td>
<td>Jan.24, 2018</td>
</tr>
<tr>
<td>2.0</td>
<td>Repair history accumulation error and electrical characteristics updated</td>
<td>May.19, 2020</td>
</tr>
</tbody>
</table>

- 1. Update BGA176 parameter A max in Table 5-1. **BGA176 package dimensions**, the value changes from 0.84mm to 0.89mm
- 2. Update Memory characteristics in Table 4-24. **Flash memory characteristics**.
- 3. Modify the DCMI to DCI in chapter **DCI characteristics**.
- 4. Modify LDO in run mode to LDO in normal power and normal driver mode, LDO in low power mode to LDO in normal power and low driver mode, Main LDO in under drive mode to LDO in low power and normal drive mode, Low Power LDO in under drive mode to LDO in low power and low drive mode in Table 4-7. **Power consumption characteristics**.
- 5. Modify the second DAC_OUT min to DAC_OUT max in Table 4-36. **DAC characteristics**.
- 6. Changed the range of TSTG from -55-+150°C to -65-150°C in Table 4-1. **Absolute maximum ratings**.
- 7. Delete Fast mode Plus and add parameter t_{st}(sta), t_{st}(sto) and t_{st}, update I2C Timing diagram in I2C characteristics.
- 8. Update the SPI Timing diagram in chapter **SPI characteristics**.

<table>
<thead>
<tr>
<th>Revision No.</th>
<th>Description</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.1</td>
<td></td>
<td>May.31, 2021</td>
</tr>
</tbody>
</table>

2.2 Correct the value of VREF+ in Table 4-28. **ADC characteristics** Oct.18, 2021
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